

# Q1 3-Phase TNPC Module

## NXH40T120L3Q1

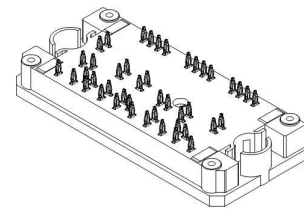
The NXH40T120L2Q1 is a power module containing a three channel T-type neutral-point clamped (TNPC) circuit. Each channel has two 1200 V, 40 A IGBTs with inverse diodes and two 650 V, 25 A IGBTs with inverse diodes. The module contains an NTC thermistor.

### Features

- Low Package Height
- Compact 82.5 mm x 37.4 mm x 12 mm Package
- Options with Press-fit Pins and Solder Pins
- Options with Pre-applied Thermal Interface Material (TIM) and without Pre-applied TIM
- Thermistor
- This Device is Pb-Free and is RoHS Compliant

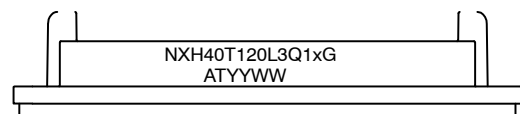
### Applications

- Solar Inverters
- UPS
- Energy Storage Systems



**Q1 3-TNPC  
CASE 180AS**  
Solder pins follow similar pattern

### MARKING DIAGRAM



NXH40T120L3Q1x = Device Code  
A = Assembly Site Code  
T = Test Site Code  
YYWW = Year and Work Week Code  
G = Pb-Free Package

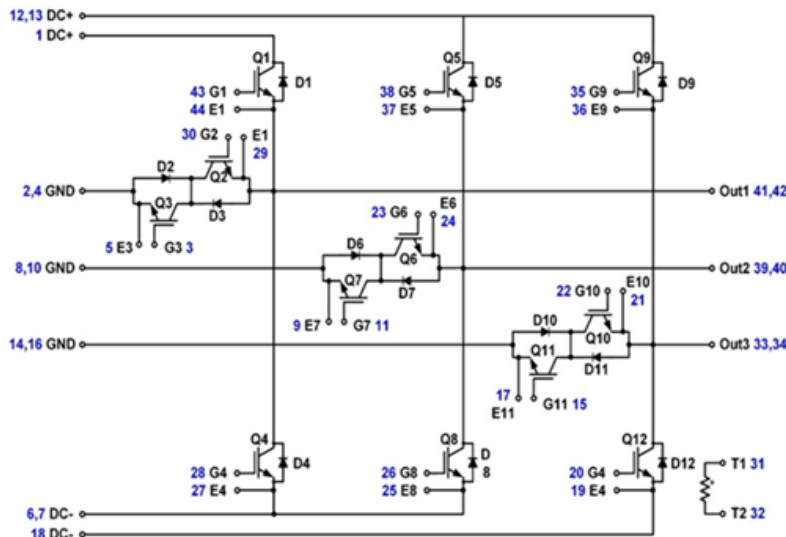
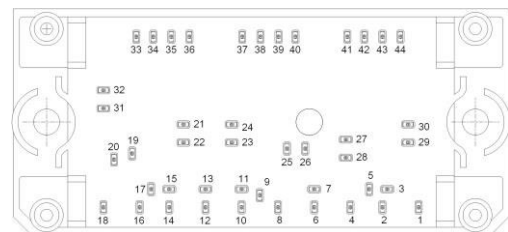


Figure 1. NXH40T120L3Q1 Schematic Diagram

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# NXH40T120L3Q1

## MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
<b>IGBT (Q1, Q4, Q5, Q8, Q9, Q12)</b>			
Collector – Emitter Voltage	V <sub>CES</sub>	1200	V
Gate – Emitter Voltage	V <sub>GE</sub>	±20	V
Continuous Collector Current @ T <sub>C</sub> = 80°C (T <sub>J</sub> = 175°C)	I <sub>C</sub>	40	A
Pulsed Collector Current (T <sub>J</sub> = 175°C)	I <sub>Cpulse</sub>	120	A
Maximum Power Dissipation (T <sub>J</sub> = 175°C)	P <sub>tot</sub>	145	W
Minimum Operating Junction Temperature	T <sub>JMIN</sub>	-40	°C
Maximum Operating Junction Temperature	T <sub>JMAX</sub>	175	°C

## DIODE (D1, D4, D5, D8, D9, D12)

Peak Repetitive Reverse Voltage	V <sub>RRM</sub>	1200	V
Continuous Forward Current @ T <sub>C</sub> = 80°C (T <sub>J</sub> = 175°C)	I <sub>F</sub>	25	A
Repetitive Peak Forward Current (T <sub>J</sub> = 175°C)	I <sub>FRM</sub>	75	A
Maximum Power Dissipation (T <sub>J</sub> = 175°C)	P <sub>tot</sub>	55	W
Minimum Operating Junction Temperature	T <sub>JMIN</sub>	-40	°C
Maximum Operating Junction Temperature	T <sub>JMAX</sub>	175	°C

## IGBT+DIODE (Q2+D2, Q3+D3, Q6+D6, Q7+D7, Q10+D10, Q11+D11)

Collector – Emitter Voltage	V <sub>CES</sub>	650	V
Gate – Emitter Voltage	V <sub>GE</sub>	±20	V
Continuous Collector Current @ T <sub>C</sub> = 80°C (T <sub>J</sub> = 175°C)	I <sub>C</sub>	42	A
Pulsed Collector Current (T <sub>J</sub> = 175°C)	I <sub>Cpulse</sub>	126	A
Maximum Power Dissipation (T <sub>J</sub> = 175°C)	P <sub>tot</sub>	146	W
Minimum Operating Junction Temperature	T <sub>JMIN</sub>	-40	°C
Maximum Operating Junction Temperature	T <sub>JMAX</sub>	175	°C

## THERMAL PROPERTIES

Storage Temperature range	T <sub>stg</sub>	-40 to 150	°C
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## INSULATION PROPERTIES

Isolation Test Voltage, t = 1 sec, 60 Hz	V <sub>is</sub>	3000	V <sub>RMS</sub>
Creepage Distance		12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

## RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T <sub>J</sub>	-40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless Otherwise Noted)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	
<b>IGBT CHARACTERISTICS (Q1, Q4, Q5, Q8, Q9, Q12)</b>							
Collector–Emitter Cutoff Current	V <sub>GE</sub> = 0 V, V <sub>CE</sub> = 1200 V	ICES	–	–	400	μA	
Collector–Emitter Saturation Voltage	V <sub>GE</sub> = 15 V, I <sub>C</sub> = 40 A, T <sub>J</sub> = 25°C	VCE(sat)	–	1.85	2.20	V	
	V <sub>GE</sub> = 15 V, I <sub>C</sub> = 40 A, T <sub>J</sub> = 150°C		–	2.25	–		
Gate–Emitter Threshold Voltage	V <sub>GE</sub> = V <sub>CE</sub> , I <sub>C</sub> = 1.5 mA	VGE(TH)	4.50	–	6.50	V	
Gate Leakage Current	V <sub>GE</sub> = 20 V, V <sub>CE</sub> = 0 V	IGES	–	–	800	nA	
Turn–on Delay Time	T <sub>J</sub> = 25°C V <sub>CE</sub> = 350 V, I <sub>C</sub> = 28 A, V <sub>GE</sub> = ±15 V, R <sub>G</sub> = 8 Ω	td(on)	–	63	–	ns	
Rise Time		t <sub>r</sub>	–	22	–		
Turn–off Delay Time		td(off)	–	199	–		
Fall Time		t <sub>f</sub>	–	23	–		
Turn–on Switching Loss per Pulse		E <sub>on</sub>	–	560	–		μJ
Turn off Switching Loss per Pulse		E <sub>off</sub>	–	338	–		
Turn–on Delay Time	T <sub>J</sub> = 125°C V <sub>CE</sub> = 350 V, I <sub>C</sub> = 28 A, V <sub>GE</sub> = ±15 V, R <sub>G</sub> = 8 Ω	td(on)	–	59	–	ns	
Rise Time		t <sub>r</sub>	–	24	–		
Turn–off Delay Time		td(off)	–	225	–		
Fall Time		t <sub>f</sub>	–	80	–		
Turn – on Switching Loss per Pulse		E <sub>on</sub>	–	757	–		μJ
Turn off Switching Loss per Pulse		E <sub>off</sub>	–	910	–		
Input Capacitance	V <sub>CE</sub> = 20 V V <sub>GE</sub> = 0 V, f = 1 MHz	Cies	–	7753	–	pF	
Output Capacitance		Co <sub>es</sub>	–	227	–		
Reverse Transfer Capacitance		Cres	–	127	–		
Total Gate Charge	V <sub>CE</sub> = 350 V, I <sub>C</sub> = 40 A, V <sub>GE</sub> = ±15 V	Q <sub>g</sub>	–	536	–	nC	
Thermal Resistance – chip–to–heatsink	Thermal grease, Thickness ≤ 2.25 Mil, λ = 2.9 W/mK	RthJH	–	1.01	–	°C/W	

## DIODE CHARACTERISTICS (D1, D4, D5, D8, D9, D12)

Diode Forward Voltage	I <sub>F</sub> = 20 A, T <sub>J</sub> = 25°C	V <sub>F</sub>	–	2.4	2.7	V
	I <sub>F</sub> = 20 A, T <sub>J</sub> = 150°C		–	1.7	–	
Reverse Recovery Time	T <sub>J</sub> = 25°C V <sub>CE</sub> = 350 V, I <sub>C</sub> = 28 A, V <sub>GE</sub> = ±15 V, R <sub>G</sub> = 16 Ω	t <sub>rr</sub>	–	43	–	ns
Reverse Recovery Charge		Q <sub>rr</sub>	–	756	–	μC
Peak Reverse Recovery Current		I <sub>RRM</sub>	–	35	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	750	–	A/μs
Reverse Recovery Energy		E <sub>rr</sub>	–	104	–	μJ
Reverse Recovery Time	T <sub>J</sub> = 125°C V <sub>CE</sub> = 350 V, I <sub>C</sub> = 28 A, V <sub>GE</sub> = ±15 V, R <sub>G</sub> = 16 Ω	t <sub>rr</sub>	–	129	–	ns
Reverse Recovery Charge		Q <sub>rr</sub>	–	2702	–	μC
Peak Reverse Recovery Current		I <sub>RRM</sub>	–	45	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	407	–	A/μs
Reverse Recovery Energy		E <sub>rr</sub>	–	428	–	μJ
Thermal Resistance – chip–to–heatsink	Thermal grease, Thickness ≤ 2.25 Mil, λ = 2.9 W/mK	RthJH	–	1.63	–	°C/W

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless Otherwise Noted) (continued)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	
<b>IGBT CHARACTERISTICS (Q2, Q3, Q6, Q7, Q10, Q11)</b>							
Collector-Emitter Cutoff Current	V <sub>GE</sub> = 0 V, V <sub>CE</sub> = 650 V	ICES	–	–	250	μA	
Collector-Emitter Saturation Voltage	V <sub>GE</sub> = 15 V, I <sub>C</sub> = 50 A, T <sub>J</sub> = 25°C	VCE(sat)	–	1.50	–	V	
	V <sub>GE</sub> = 15 V, I <sub>C</sub> = 50 A, T <sub>J</sub> = 150°C		–	1.53	–		
Gate-Emitter Threshold Voltage	V <sub>GE</sub> = V <sub>CE</sub> , I <sub>C</sub> = 1.65 mA	V <sub>GE</sub> (TH)	2.60	4.40	6.40	V	
Gate Leakage Current	V <sub>GE</sub> = 20 V, V <sub>CE</sub> = 0 V	IGES	–	–	400	nA	
Turn-on Delay Time	T <sub>J</sub> = 25°C V <sub>CE</sub> = 350 V, I <sub>C</sub> = 28 A, V <sub>GE</sub> = ±15 V, R <sub>G</sub> = 16 Ω	td(on)	–	54	–	ns	
Rise Time		t <sub>r</sub>	–	15	–		
Turn-off Delay Time		td(off)	–	157	–		
Fall Time		t <sub>f</sub>	–	12	–		
Turn-on Switching Loss per Pulse		E <sub>on</sub>	–	416	–		μJ
Turn off Switching Loss per Pulse		E <sub>off</sub>	–	321	–		
Turn-on Delay Time	T <sub>J</sub> = 125°C V <sub>CE</sub> = 350 V, I <sub>C</sub> = 28 A, V <sub>GE</sub> = ±15 V, R <sub>G</sub> = 16 Ω	td(on)	–	52	–	ns	
Rise Time		t <sub>r</sub>	–	16	–		
Turn-off Delay Time		td(off)	–	178	–		
Fall Time		t <sub>f</sub>	–	18	–		
Turn – on Switching Loss per Pulse		E <sub>on</sub>	–	671	–		μJ
Turn off Switching Loss per Pulse		E <sub>off</sub>	–	444	–		
Input Capacitance	V <sub>CE</sub> = 20 V V <sub>GE</sub> = 0 V, f = 1 MHz	C <sub>ies</sub>	–	3137	–	pF	
Output Capacitance		C <sub>oes</sub>	–	146	–		
Reverse Transfer Capacitance		C <sub>res</sub>	–	17	–		
Total Gate Charge	V <sub>CE</sub> = 350 V, I <sub>C</sub> = 40 A, V <sub>GE</sub> = ±15 V	Q <sub>g</sub>	–	180	–	nC	
Thermal Resistance – chip-to-heatsink	Thermal grease, Thickness ≤ 2.25 Mil, λ = 2.9 W/mK	R <sub>thJH</sub>	–	0.995	–	°C/W	

## DIODE CHARACTERISTICS (D2, D3, D6, D7, D10, D11)

Diode Forward Voltage	I <sub>F</sub> = 20 A, T <sub>J</sub> = 25°C	V <sub>F</sub>	–	1.28	–	V
	I <sub>F</sub> = 20 A, T <sub>J</sub> = 150°C		–	1.18	–	
Combined IGBT + Diode Voltage Drop	I <sub>F</sub> = 20 A, T <sub>J</sub> = 25°C	V <sub>F</sub>	–	3.05	3.4	V
Reverse Recovery Time	T <sub>J</sub> = 25°C V <sub>CE</sub> = 350 V, I <sub>C</sub> = 28 A, V <sub>GE</sub> = ±15 V, R <sub>G</sub> = 8 Ω	t <sub>rr</sub>	–	69	–	ns
Reverse Recovery Charge		Q <sub>rr</sub>	–	1267	–	μC
Peak Reverse Recovery Current		I <sub>RRM</sub>	–	41	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	1599	–	A/μs
Reverse Recovery Energy		E <sub>rr</sub>	–	244	–	μJ
Reverse Recovery Time	T <sub>J</sub> = 125°C V <sub>CE</sub> = 350 V, I <sub>C</sub> = 28 A, V <sub>GE</sub> = ±15 V, R <sub>G</sub> = 8 Ω	t <sub>rr</sub>	–	111	–	ns
Reverse Recovery Charge		Q <sub>rr</sub>	–	2323	–	μC
Peak Reverse Recovery Current		I <sub>RRM</sub>	–	40	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	470	–	A/μs
Reverse Recovery Energy		E <sub>rr</sub>	–	510	–	μJ

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless Otherwise Noted) (continued)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>THERMISTOR CHARACTERISTICS</b>						
Nominal resistance	T = 25°C	R <sub>25</sub>		22		kΩ
Nominal resistance	T = 100°C	R <sub>100</sub>		1468		Ω
Deviation of R <sub>25</sub>		R/R	-5		5	%
Power dissipation		P <sub>D</sub>		200		mW
Power dissipation constant				2		mW/K
B-value	B(25/50), tolerance ±3%			3950		K
B-value	B(25/100), tolerance ±3%			3998		K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH40T120L3Q1PG	NXH40T120L3Q1PG	Q1 3-Phase TNPC – Case 180AS Press-fit Pins (Pb-Free)	21 Units / Blister Tray
NXH40T120L3Q1SG	NXH40T120L3Q1SG	Q1 3-Phase TNPC – Case 180BN Solder Pins (Pb-Free)	21 Units / Blister Tray
NXH40T120L3Q1PTG	NXH40T120L3Q1PTG	Q1 3-Phase TNPC – Case 180AS Press-fit Pins (Pb-Free)	21 Units / Blister Tray

# NXH40T120L3Q1

## TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT (Q1, Q4, Q5, Q8, Q9, Q12) AND DIODE (D1, D4, D5, D8, D9, D12)

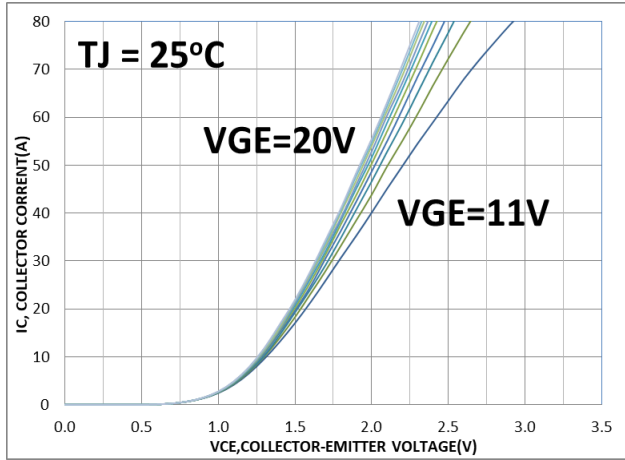


Figure 2. Typical Output Characteristics

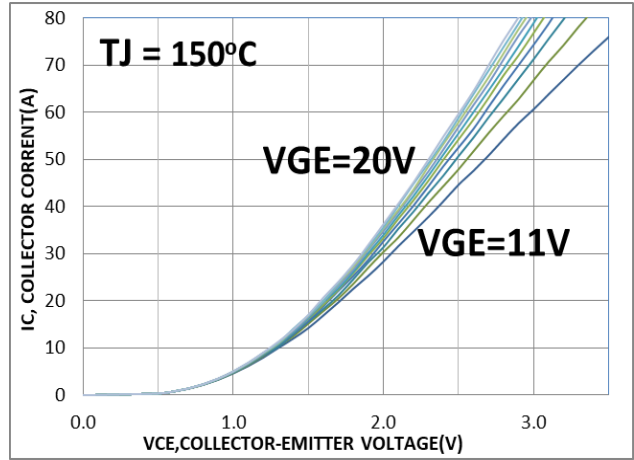


Figure 3. Typical Output Characteristics

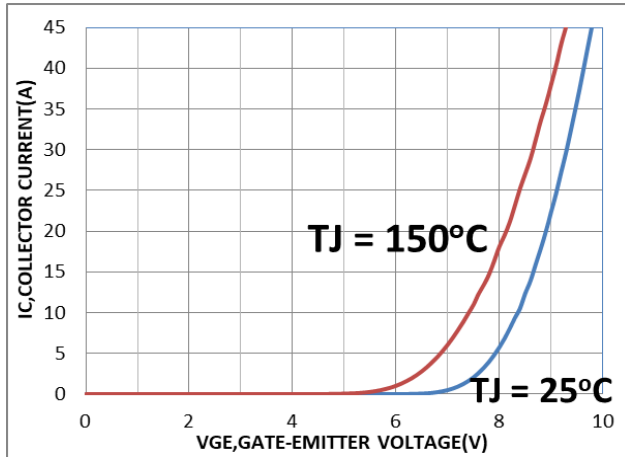


Figure 4. Typical Transfer Characteristics

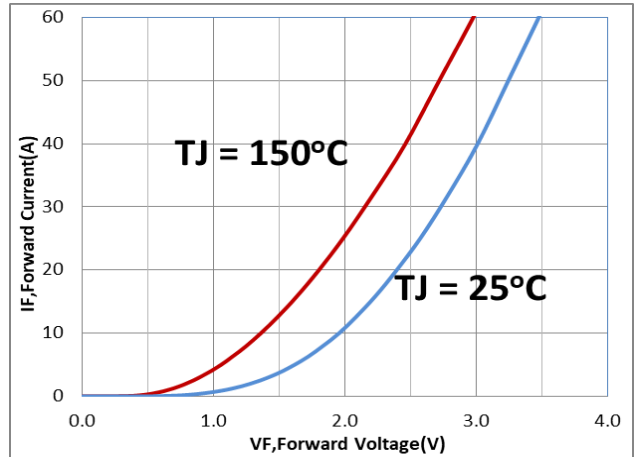


Figure 5. Diode Forward Characteristics

# NXH40T120L3Q1

## TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT (Q1, Q4, Q5, Q8, Q9, Q12) AND DIODE (D1, D4, D5, D8, D9, D12)

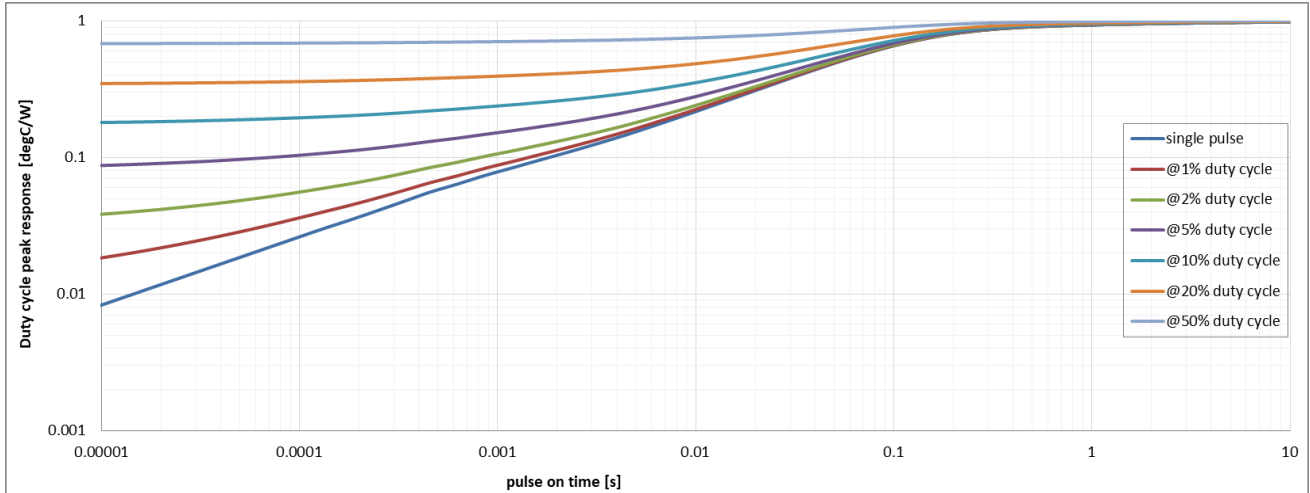


Figure 6. Transient Thermal Impedance (Half Bridge IGBT)

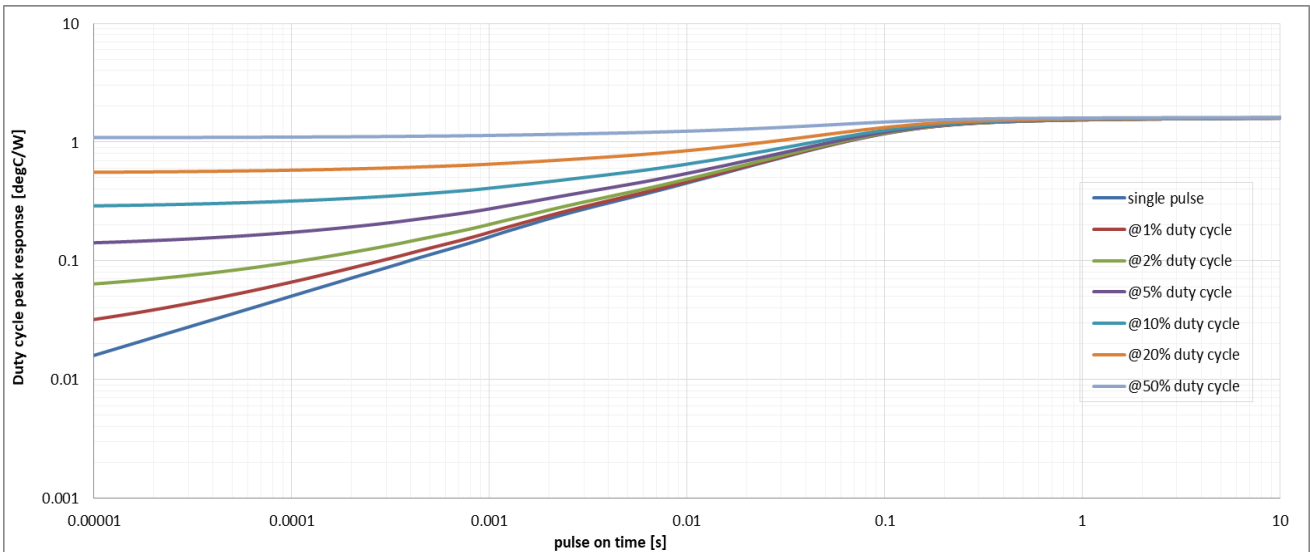


Figure 7. Transient Thermal Impedance (Half Bridge Diode)

# NXH40T120L3Q1

## TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT (Q1, Q4, Q5, Q8, Q9, Q12) AND DIODE (D1, D4, D5, D8, D9, D12)

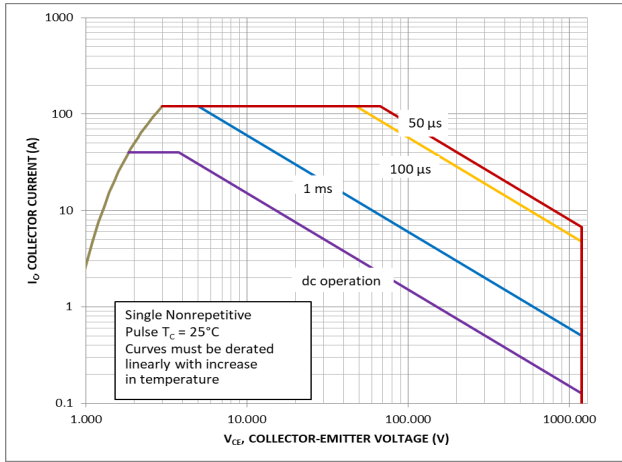


Figure 8. FBSOA

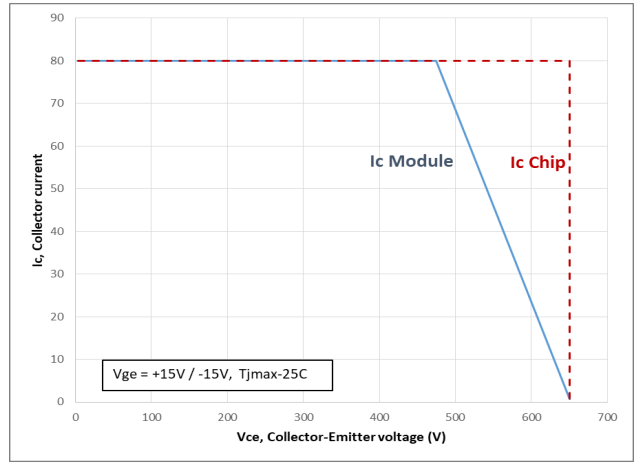


Figure 9. RBSOA

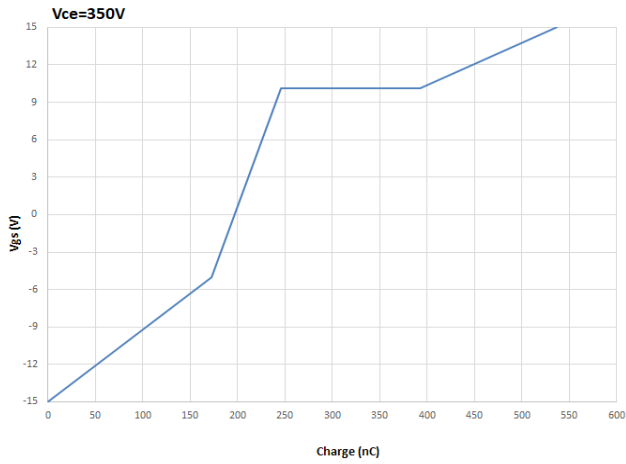


Figure 10. Gate Voltage vs. Gate Charge



# NXH40T120L3Q1

## TYPICAL CHARACTERISTICS – NP IGBT + DIODE (Q2+D2, Q3+D3, Q6+D6, Q7+D7, Q10+D10, Q11+D11)

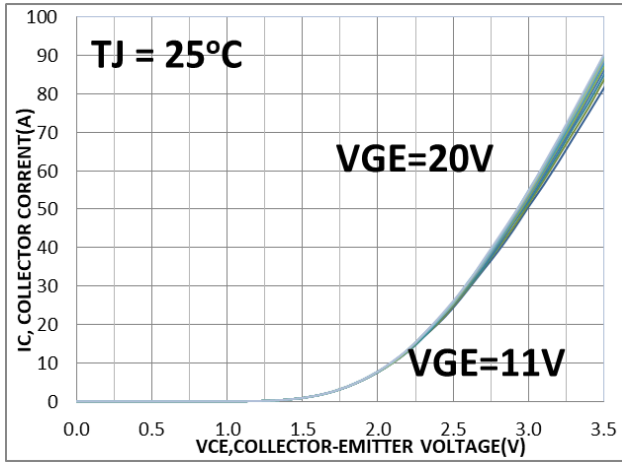


Figure 11. Typical Output Characteristics  
( $I_C$  versus  $V_{DT}$ )

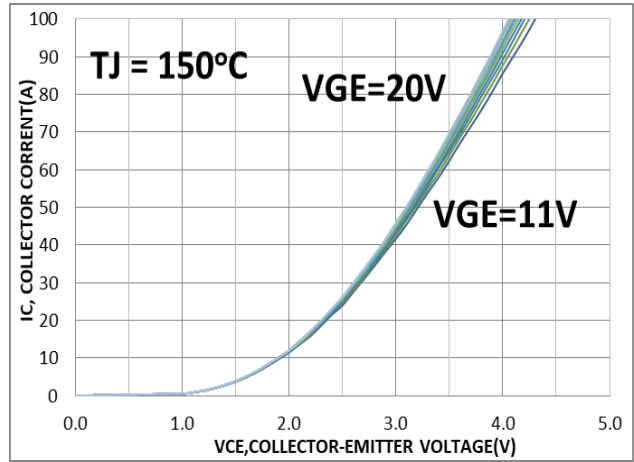


Figure 12. Typical Output Characteristics  
( $I_C$  versus  $V_{DT}$ )

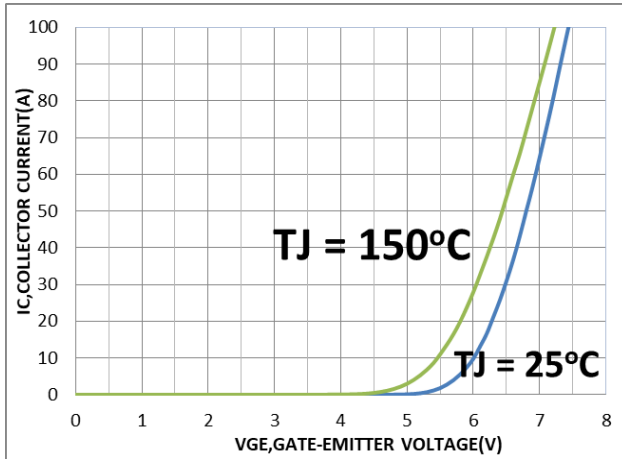


Figure 13. Typical Transfer Characteristics

# NXH40T120L3Q1

## TYPICAL CHARACTERISTICS – NP IGBT + DIODE (Q2+D2, Q3+D3, Q6+D6, Q7+D7, Q10+D10, Q11+D11)

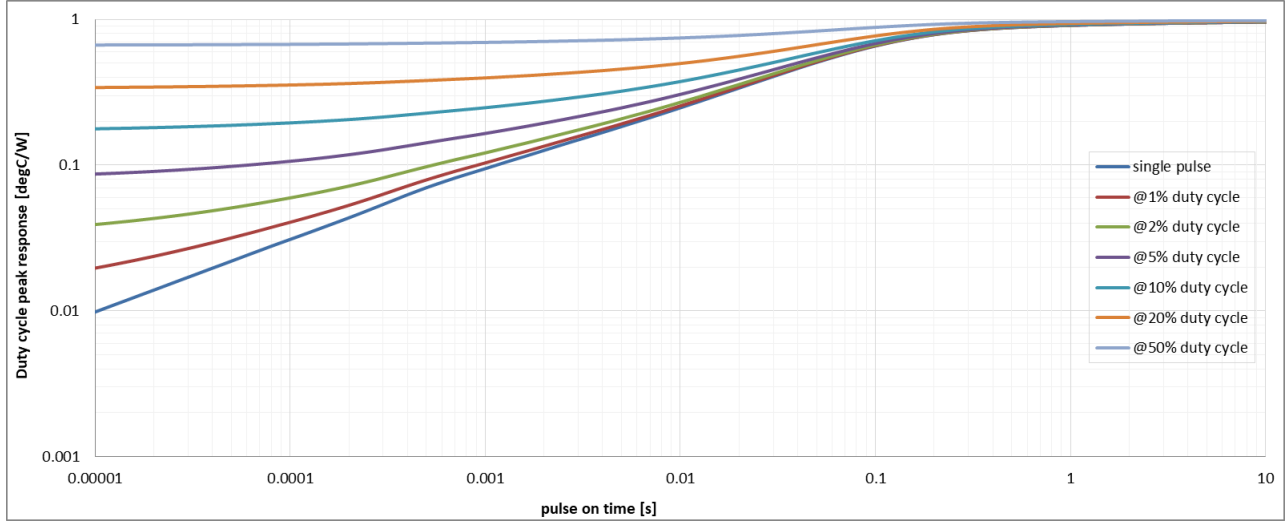


Figure 14. Transient Thermal Impedance (Neutral Point IGBT + Diode)

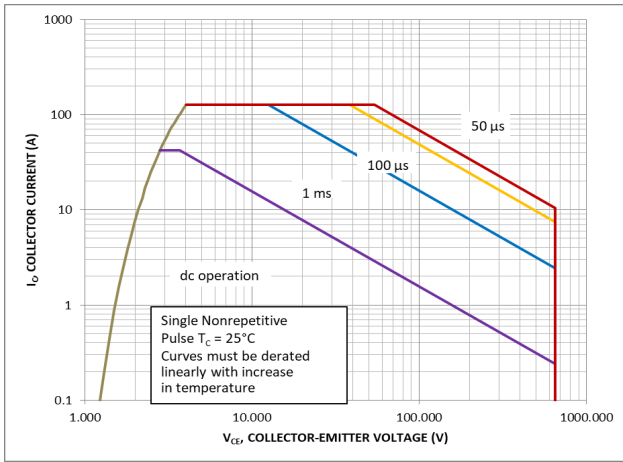


Figure 15. FBSOA (NP IGBT + Diode)

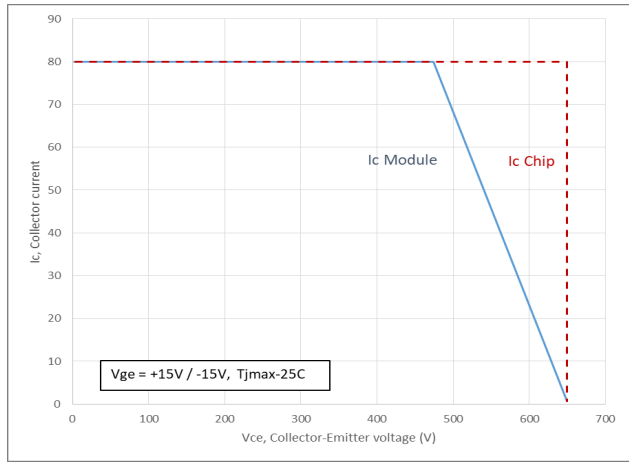


Figure 16. RBSOA (NP IGBT + Diode)

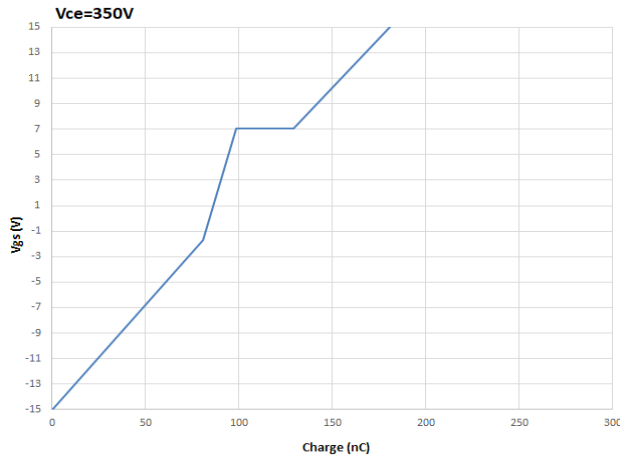


Figure 17. Gate Voltage vs. Gate Charge

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## TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT COMMUTATES NEUTRAL POINT DIODE

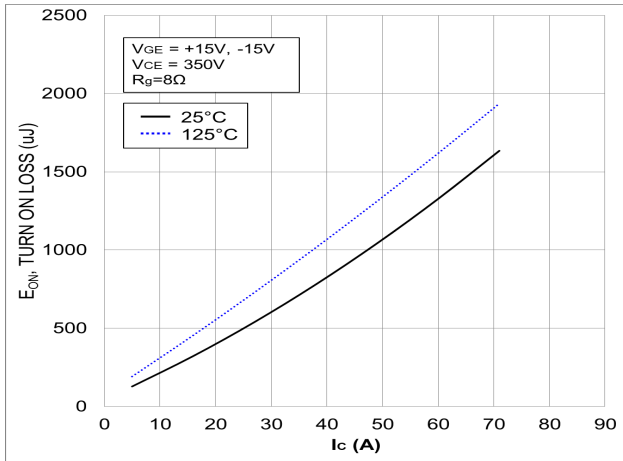


Figure 18. Typical Switching Loss  $E_{ON}$  vs.  $I_C$

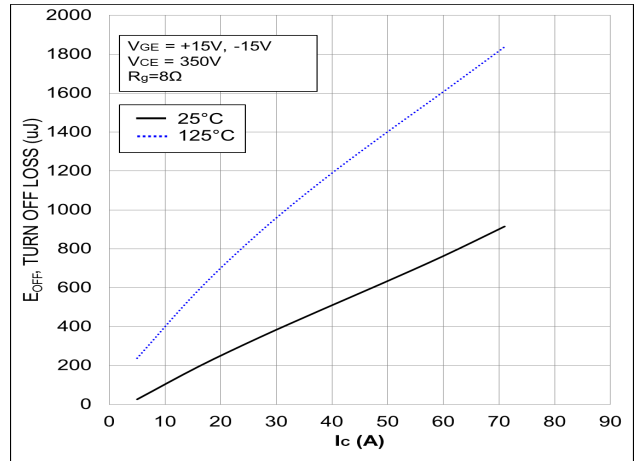


Figure 19. Typical Switching Loss  $E_{OFF}$  vs.  $I_C$

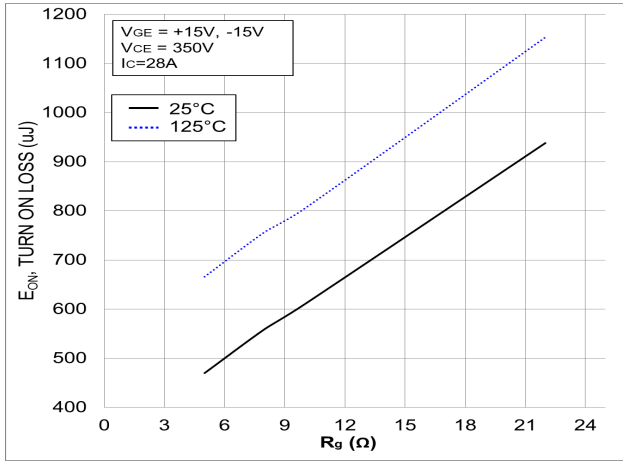


Figure 20. Typical Switching Loss  $E_{ON}$  vs.  $R_g$

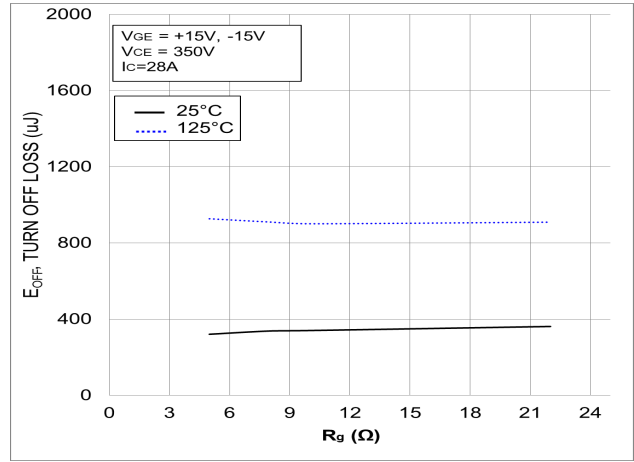


Figure 21. Typical Switching Loss  $E_{OFF}$  vs.  $R_g$

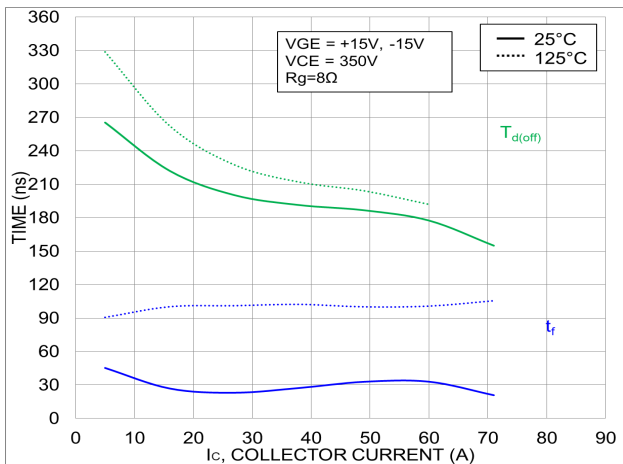


Figure 22. Typical Switching Time  $T_{DOFF}$  vs.  $I_C$

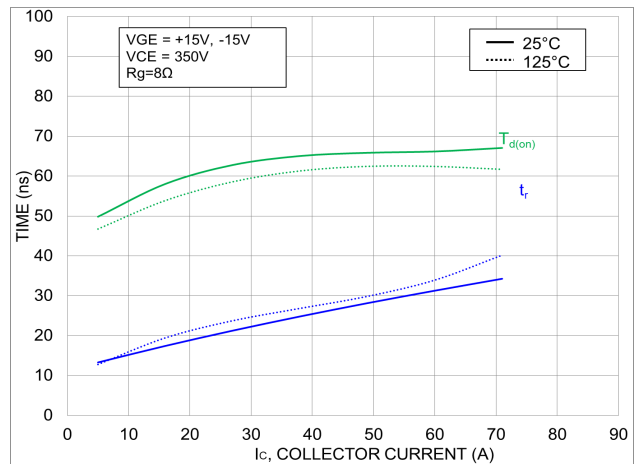


Figure 23. Typical Switching Time  $T_{DON}$  vs.  $I_C$

# NXH40T120L3Q1

## TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT COMMUTATES NEUTRAL POINT DIODE

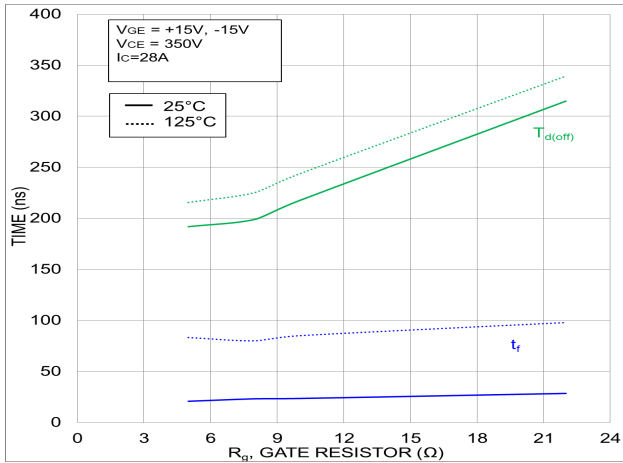


Figure 24. Typical Switching Time  $T_{DOFF}$  vs.  $R_G$

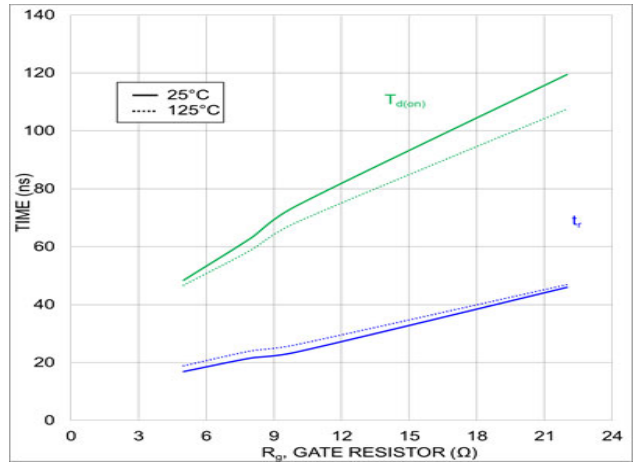


Figure 25. Typical Switching Time  $T_{DON}$  vs.  $R_G$

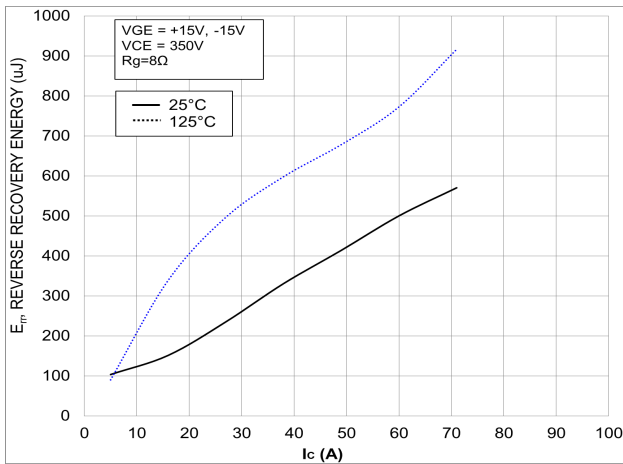


Figure 26. Typical Reverse Recovery Energy Loss vs.  $I_C$

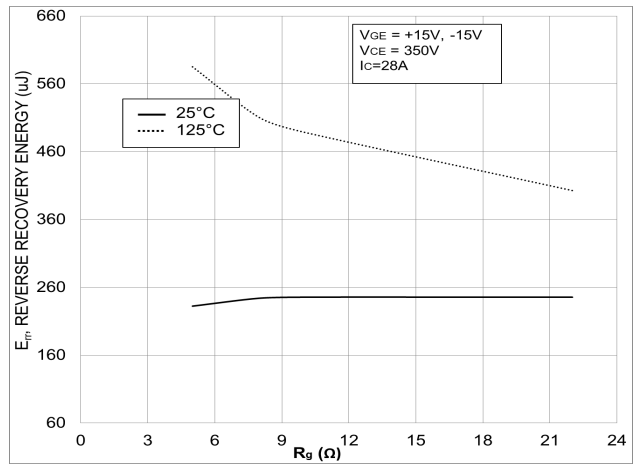


Figure 27. Typical Reverse Recovery Energy Loss vs.  $R_G$

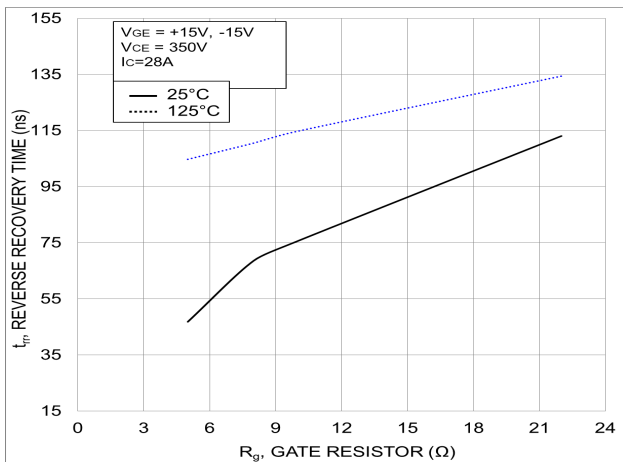


Figure 28. Typical Reverse Recovery Time vs.  $R_G$

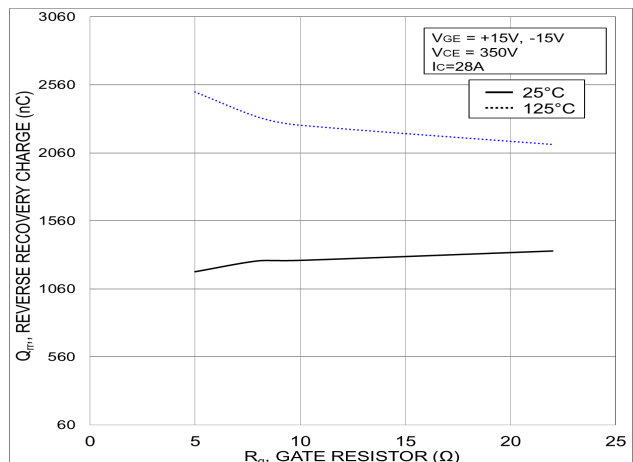


Figure 29. Typical Reverse Recovery Charge vs.  $R_G$

TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT COMMUTATES NEUTRAL POINT DIODE

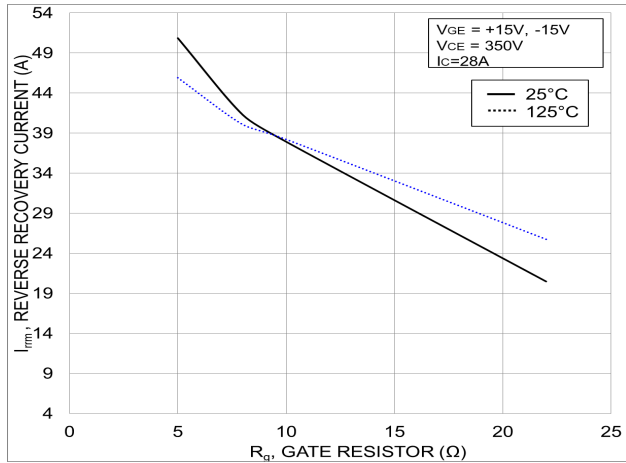


Figure 30. Typical Reverse Recovery Peak Current vs.  $R_G$

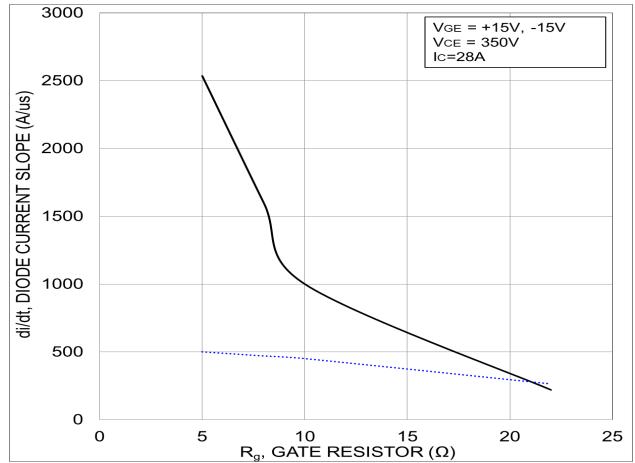


Figure 31. Typical di/dt vs.  $R_G$

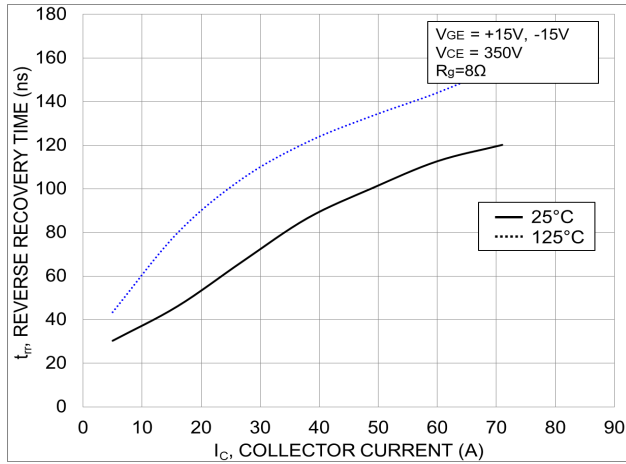


Figure 32. Typical Reverse Recovery Time vs.  $I_C$

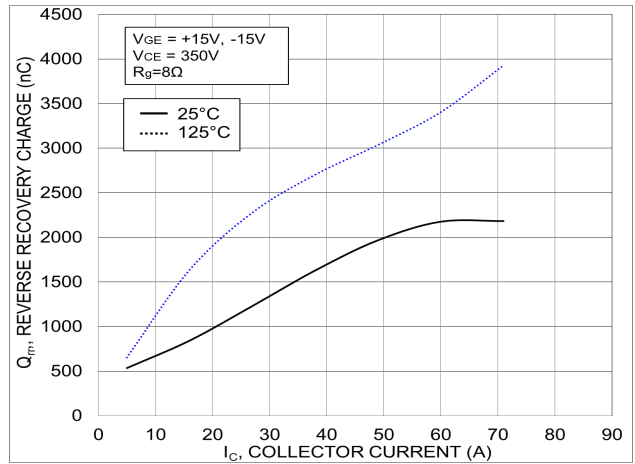


Figure 33. Typical Reverse Recovery Charge vs.  $I_C$

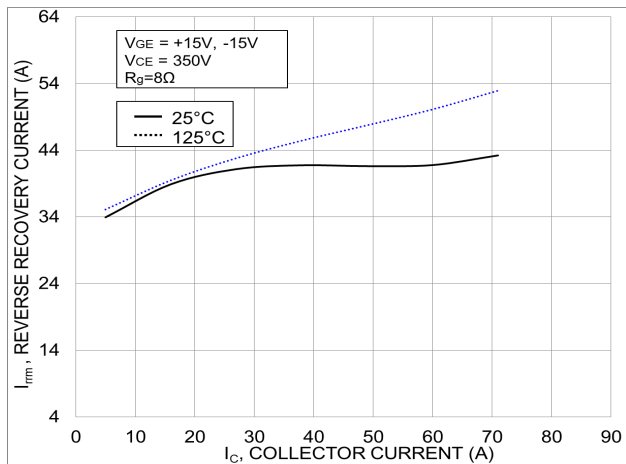


Figure 34. Typical Reverse Recovery Current vs.  $I_C$

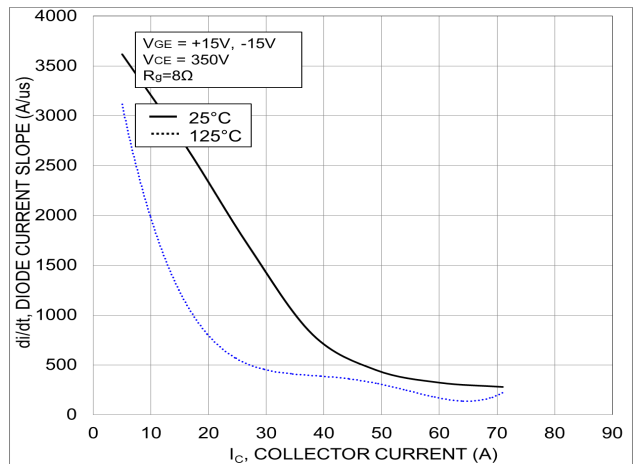


Figure 35. Typical di/dt Current Slope vs.  $I_C$

# NXH40T120L3Q1

## TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT COMMUTATES HALF BRIDGE DIODE

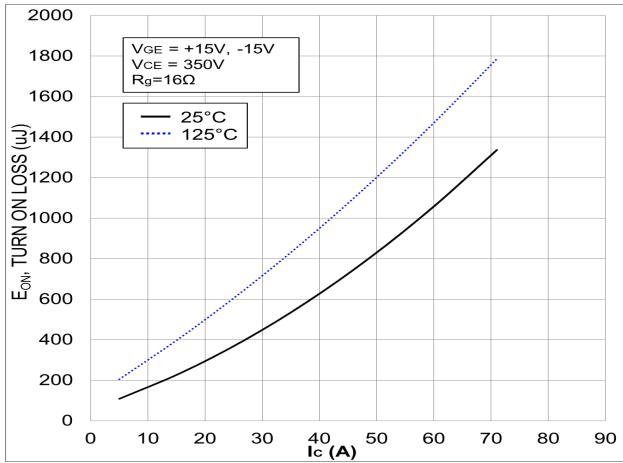


Figure 36. Typical Turn ON Loss vs.  $I_c$

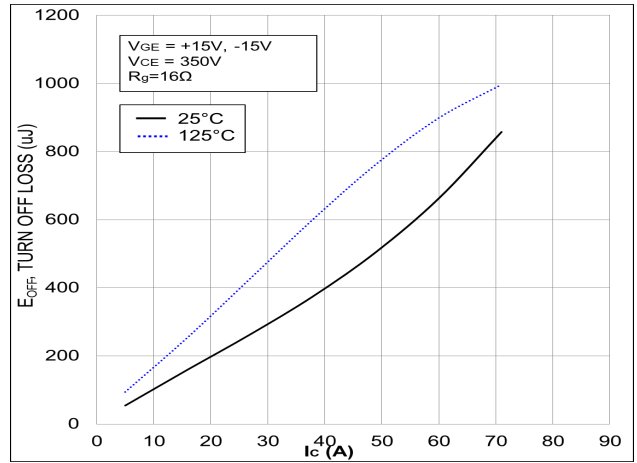


Figure 37. Typical Turn OFF Loss vs.  $I_c$

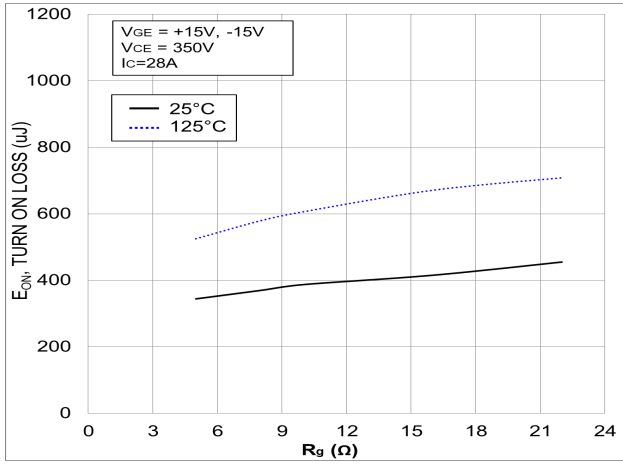


Figure 38. Typical Turn ON Loss vs.  $R_g$

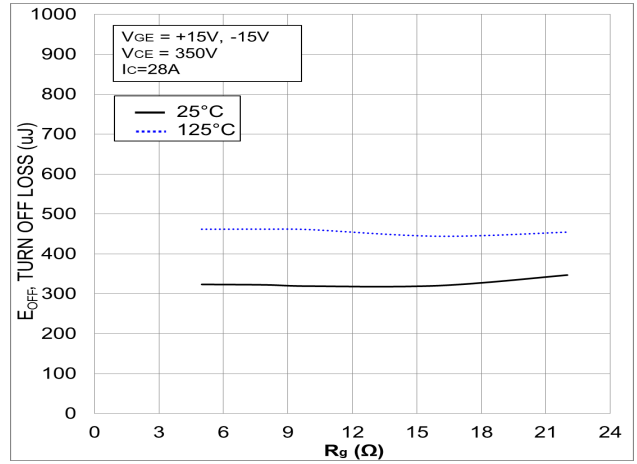


Figure 39. Typical Turn OFF Loss vs.  $R_g$

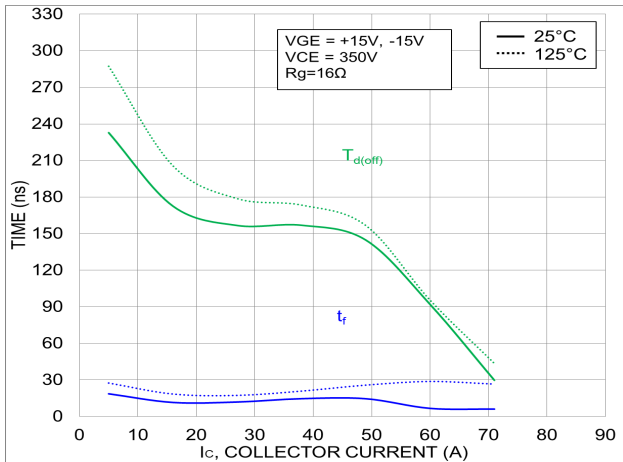


Figure 40. Typical Turn-Off Switching Time vs.  $I_c$

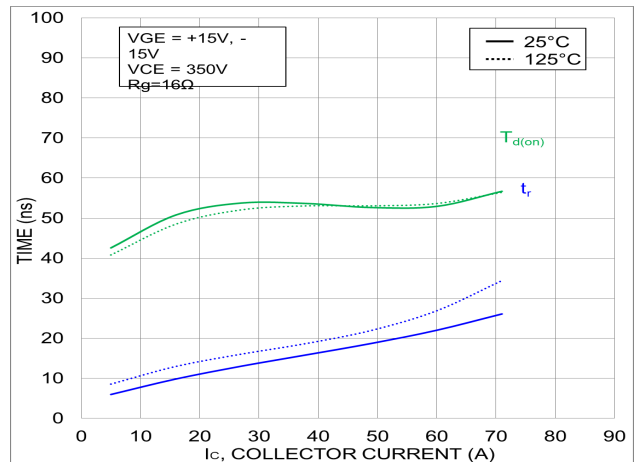


Figure 41. Typical Turn-On Switching Time vs.  $I_c$

# NXH40T120L3Q1

## TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT COMMUTATES HALF BRIDGE DIODE

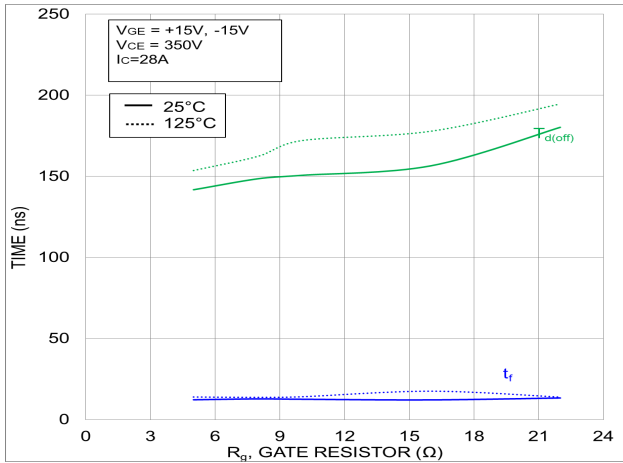


Figure 42. Typical Turn-Off Switching Time vs.  $R_G$

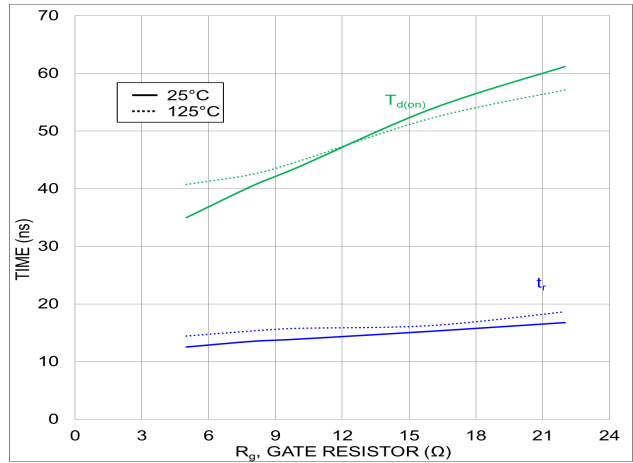


Figure 43. Typical Turn-On Switching Time vs.  $R_G$

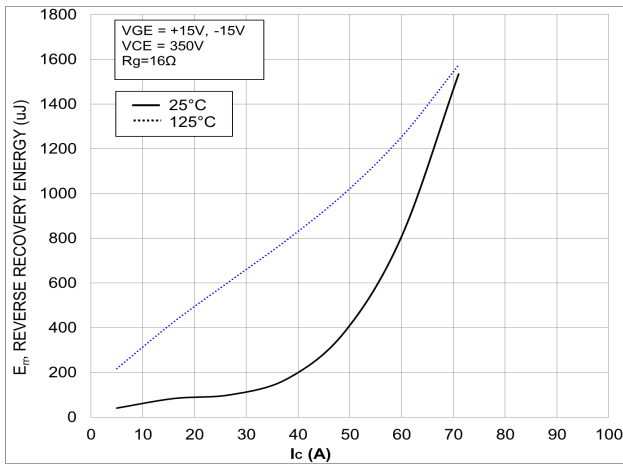


Figure 44. Typical Reverse Recovery Energy Loss vs.  $I_C$

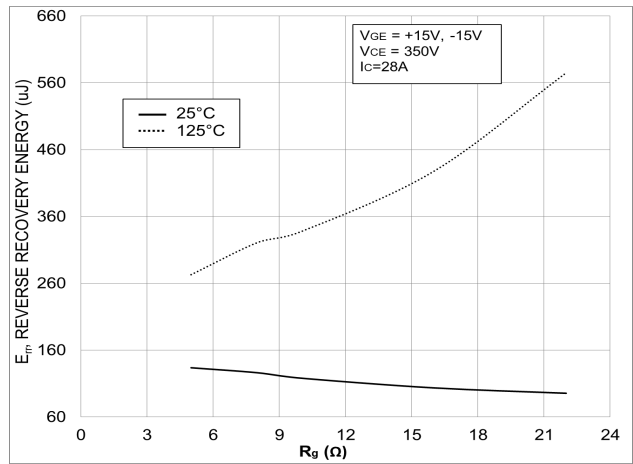


Figure 45. Typical Reverse Recovery Energy Loss vs.  $R_G$

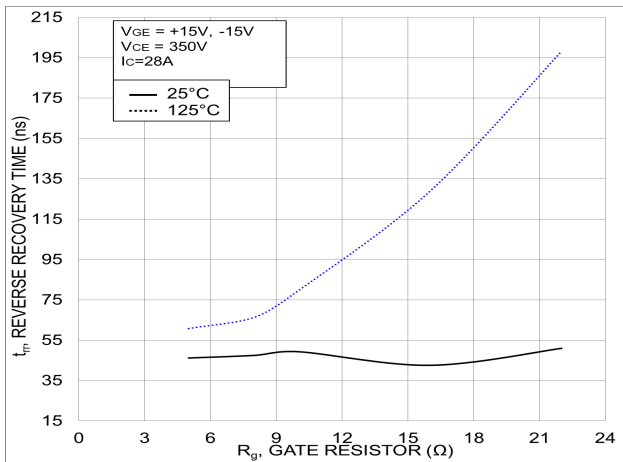


Figure 46. Typical Reverse Recovery Time vs.  $R_G$

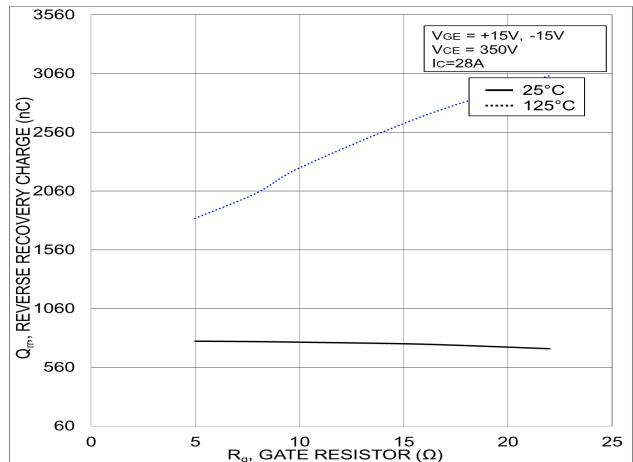
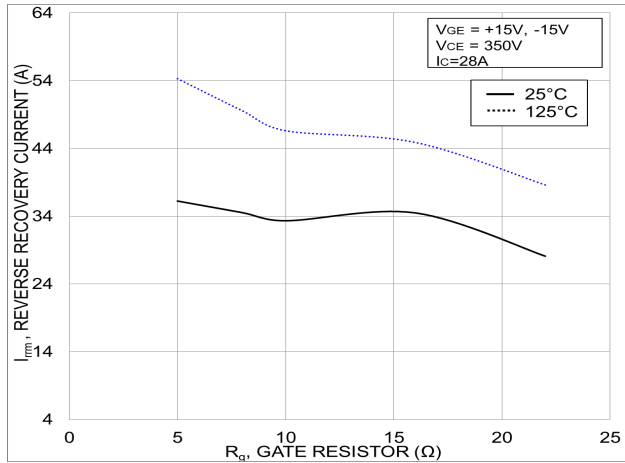


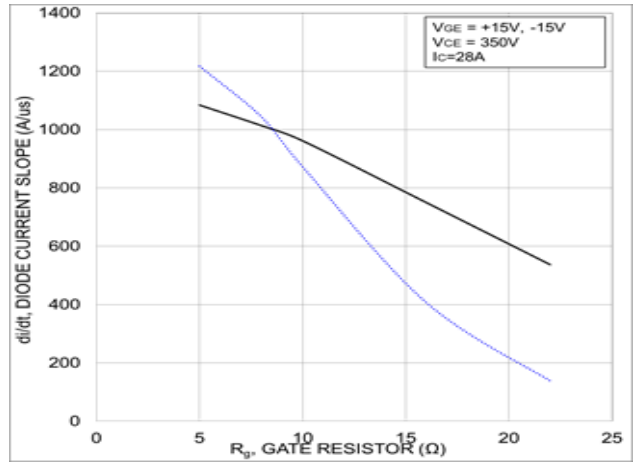
Figure 47. Typical Reverse Recovery Charge vs.  $R_G$

# NXH40T120L3Q1

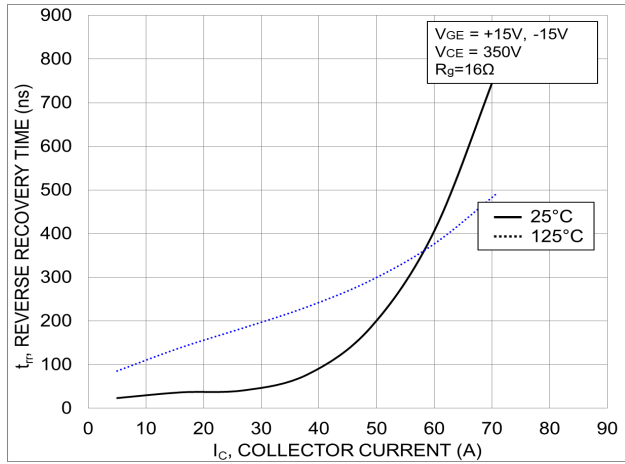
## TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT COMMUTATES HALF BRIDGE DIODE



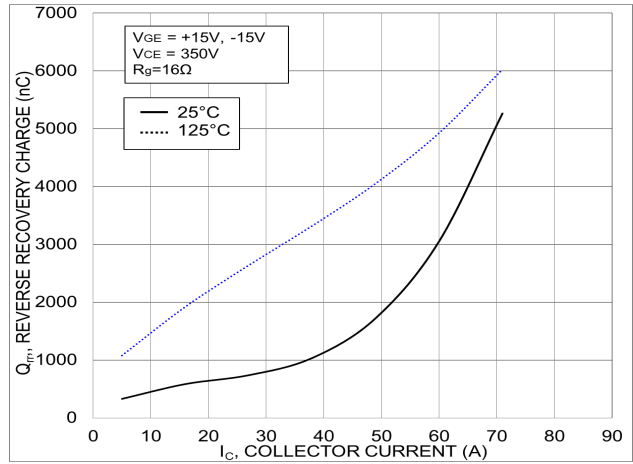
**Figure 48. Typical Reverse Recovery Peak Current vs.  $R_G$**



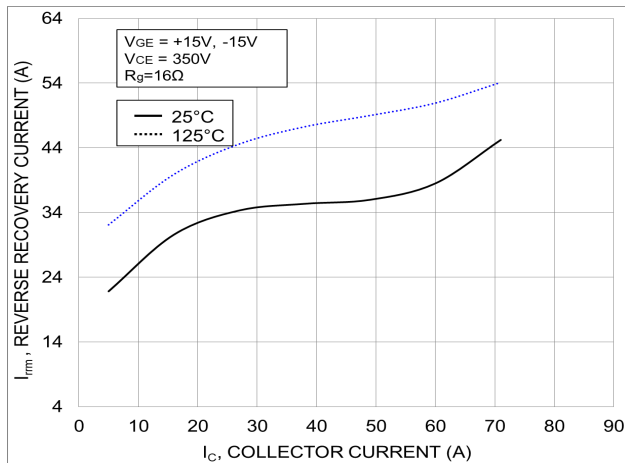
**Figure 49. Typical di/dt vs.  $R_G$**



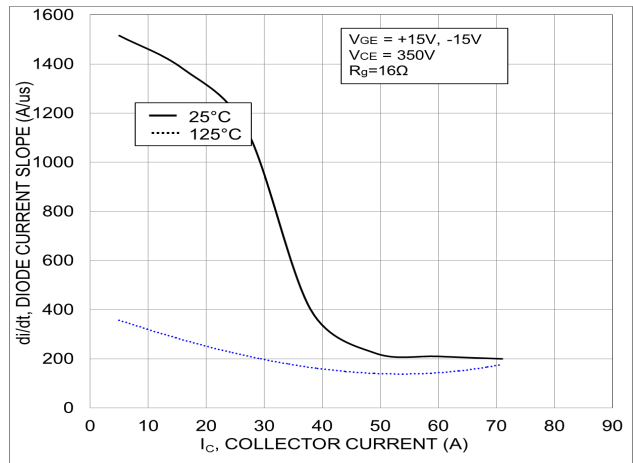
**Figure 50. Typical Reverse Recovery Time vs.  $I_C$**



**Figure 51. Typical Reverse Recovery Charge vs.  $I_C$**



**Figure 52. Typical Reverse Recovery Current vs.  $I_C$**



**Figure 53. Typical di/dt Current Slope vs.  $I_C$**



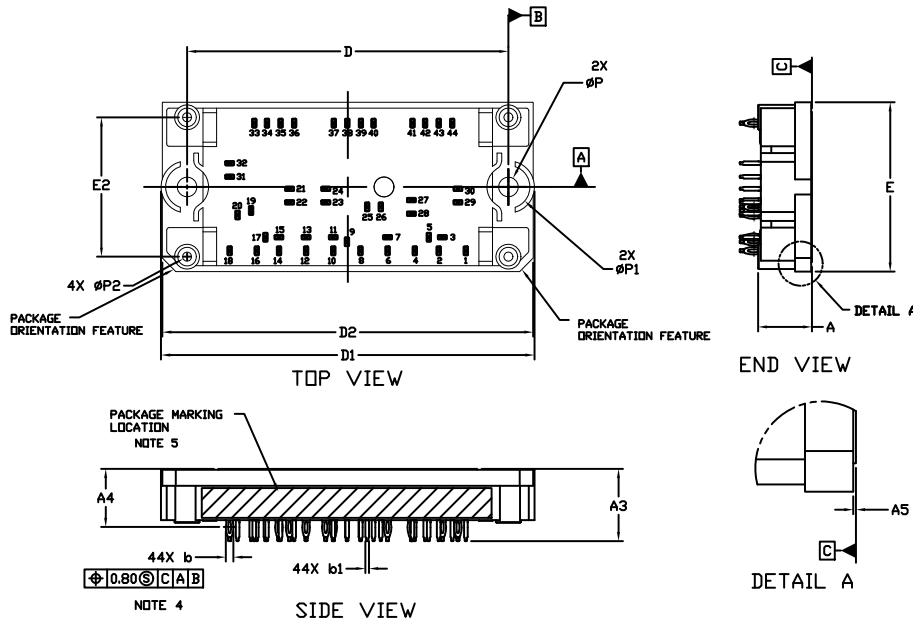
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



PIM44, 71x37.4  
CASE 180AS  
ISSUE O

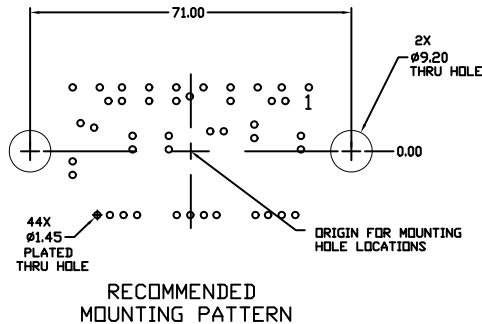
DATE 25 JUN 2018



PIN	PIN POSITION		PIN	PIN POSITION	
	X	Y		X	Y
1	26.10	14.10	23	-4.85	3.40
2	20.10	14.10	24	-4.85	0.40
3	20.90	11.10	25	4.30	4.40
4	14.80	14.10	26	7.30	4.40
5	17.90	11.10	27	14.05	2.90
6	8.80	14.10	28	14.05	5.90
7	8.80	11.10	29	24.35	3.40
8	2.80	14.10	30	24.35	0.40
9	-0.20	12.10	31	-26.10	-2.25
10	-3.20	14.10	32	-26.10	-5.25
11	-3.20	11.10	33	-20.65	-14.10
12	-9.20	14.10	34	-17.85	-14.10
13	-9.20	11.10	35	-14.85	-14.10
14	-15.20	14.10	36	-11.85	-14.10
15	-15.20	11.10	37	-3.10	-14.10
16	-20.10	14.10	38	-0.10	-14.10
17	-18.20	11.10	39	2.90	-14.10
18	-26.10	14.10	40	5.70	-14.10
19	-21.35	5.20	41	14.30	-14.10
20	-24.35	6.20	42	17.10	-14.10
21	-12.85	0.40	43	20.10	-14.10
22	-12.85	3.40	44	23.10	-14.10

NOTE 4

PIN	PIN POSITION		PIN	PIN POSITION	
	X	Y		X	Y
1	26.10	-14.10	23	-4.85	-3.40
2	20.10	-14.10	24	-4.85	-0.40
3	20.90	-11.10	25	4.30	-4.40
4	14.80	-14.10	26	7.30	-4.40
5	17.90	-11.10	27	14.05	-2.90
6	8.80	-14.10	28	14.05	-5.90
7	8.80	-11.10	29	24.35	-3.40
8	2.80	-14.10	30	24.35	-0.40
9	-0.20	-12.10	31	-26.10	2.25
10	-3.20	-14.10	32	-26.10	5.25
11	-3.20	-11.10	33	-20.65	14.10
12	-9.20	-14.10	34	-17.85	14.10
13	-9.20	-11.10	35	-14.85	14.10
14	-15.20	-14.10	36	-11.85	14.10
15	-15.20	-11.10	37	-3.10	14.10
16	-20.10	-14.10	38	-0.10	14.10
17	-18.20	-11.10	39	2.90	14.10
18	-26.10	-14.10	40	5.70	14.10
19	-21.35	-5.20	41	14.30	14.10
20	-24.35	-6.20	42	17.10	14.10
21	-12.85	-0.40	43	20.10	14.10
22	-12.85	-3.40	44	23.10	14.10



DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	11.50	12.00	12.50
A3	15.50	16.00	16.50
A4	12.83 BSC		
A5	0.10	0.20	0.30
b	1.61	1.66	1.71
b1	0.75	0.80	0.85
D	70.50	71.00	71.50
D1	82.00	82.50	83.00
D2	81.50	82.00	82.50
E	36.90	37.40	37.90
E2	30.30	30.80	31.30
P	4.10	4.30	4.50
P1	9.30	9.50	9.70
P2	1.80	2.00	2.20

NOTES:

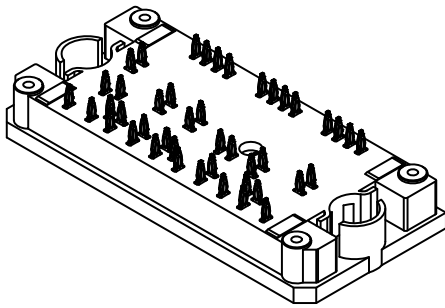
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A4.
- POSITION OF THE CENTER OF THE TERMINALS IS DETERMINED FROM DATUM B THE CENTER OF DIMENSION D, X DIRECTION, AND FROM DATUM A, Y DIRECTION. POSITIONAL TOLERANCE, AS NOTED IN DRAWING, APPLIES TO EACH TERMINAL IN BOTH DIRECTIONS.
- PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.

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DESCRIPTION:	PIM44, 71x37.4	PAGE 1 OF 2

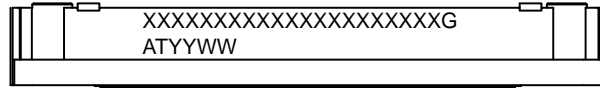
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**PIM44, 71x37.4**  
**CASE 180AS**  
**ISSUE O**

DATE 15 JUN 2018




**GENERIC  
MARKING DIAGRAM\***



XXXXX = Specific Device Code  
G = Pb-Free Package  
AT = Assembly & Test Site Code  
YYWW = Year and Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>PIM44, 71x37.4</b>	<b>PAGE 2 OF 2</b>

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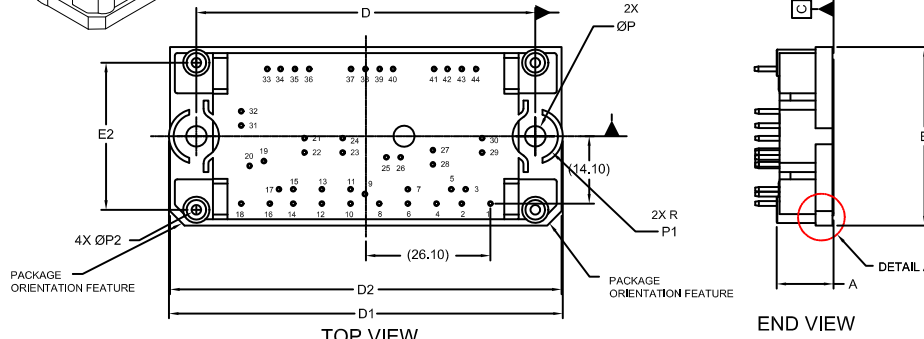
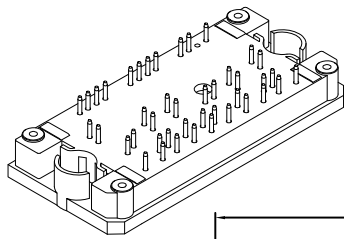
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

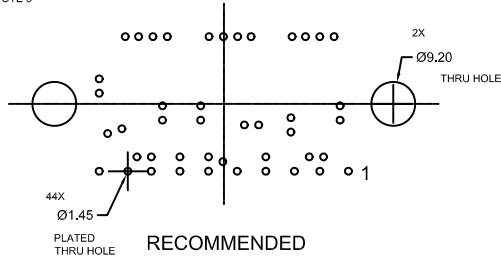
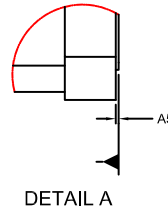
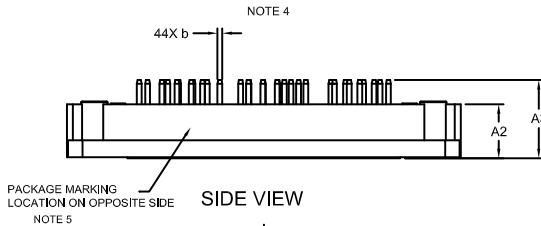


## PIM44, 71x37.4 (SOLDER PINS) CASE 180BN ISSUE 0

DATE 08 OCT 2019

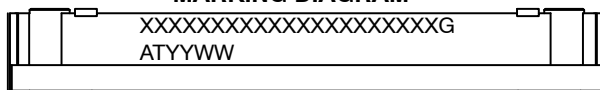


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.50	12.00	12.50
A2	10.90	11.40	11.90
A3	15.90	16.40	16.90
A5	0.00	0.30	0.60
b	0.90	1.00	1.10
D	70.50	71.00	71.50
D1	82.00	82.50	83.00
D2	81.50	82.00	82.50
E	36.90	37.40	37.90
E2	30.30	30.80	31.30
P	4.30	4.40	4.50
P1	4.55	4.75	4.95
P2	2.00 REF		



\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM.D.

### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
G = Pb-Free Package  
AT = Assembly & Test Site Code  
YYWW = Year and Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTE 4

PIN	PIN POSITION		PIN	PIN POSITION	
	X	Y		X	Y
1	26.10	-14.10	23	-4.85	-3.40
2	20.10	-14.10	24	-4.85	-0.40
3	20.90	-11.10	25	4.30	-4.40
4	14.80	-14.10	26	7.30	-4.40
5	17.90	-11.10	27	14.05	-2.90
6	8.80	-14.10	28	14.05	-5.90
7	8.80	-11.10	29	24.35	-3.40
8	2.80	-14.10	30	24.35	-0.40
9	-0.20	-12.10	31	-26.10	2.25
10	-3.20	-14.10	32	-26.10	5.25
11	-3.20	-11.10	33	-20.65	14.10
12	-9.20	-14.10	34	-17.85	14.10
13	-9.20	-11.10	35	-14.85	14.10
14	-15.20	-14.10	36	-11.85	14.10
15	-15.20	-11.10	37	-3.10	14.10
16	-20.10	-14.10	38	-0.10	14.10
17	-18.20	-11.10	39	2.90	14.10
18	-26.10	-14.10	40	5.70	14.10
19	-21.35	-5.20	41	14.30	14.10
20	-24.35	-6.20	42	17.10	14.10
21	-12.85	-0.40	43	20.10	14.10
22	-12.85	-3.40	44	23.10	14.10

#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSIONS b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 1.00 AND 3.00 FROM THE TERMINAL TIP.
- POSITION OF THE CENTER OF THE TERMINALS AND MOUNTING HOLES IS DETERMINED FROM DATUM B THE CENTER OF DIMENSION D, X DIRECTION, AND FROM DATUM A, Y DIRECTION. POSITIONAL TOLERANCE, AS NOTED IN THE DRAWING, APPLIES TO EACH TERMINAL IN BOTH DIRECTIONS.
- PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.

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