

QOPACK Module

Product Preview

NXH80T120L3Q0S3G/S3TG, NXH80T120L3Q0P3G

The NXH80T120L3Q0S3/P3G is a power module containing a T-type neutral point clamped (NPC) three level inverter stage. The integrated field stop trench IGBTs and fast recovery diodes provide lower conduction losses and switching losses, enabling designers to achieve high efficiency and superior reliability.

Features

- Low Switching Loss
- Low V_{CESAT}
- Compact 65.9 mm x 32.5 mm x 12 mm Package
- Options with Pre-applied Thermal Interface Material (TIM) and Without Pre-applied TIM
- Options with Solderable Pins and Press-fit Pins
- Thermistor

Typical Applications

- Solar Inverter
- Uninterruptable Power Supplies

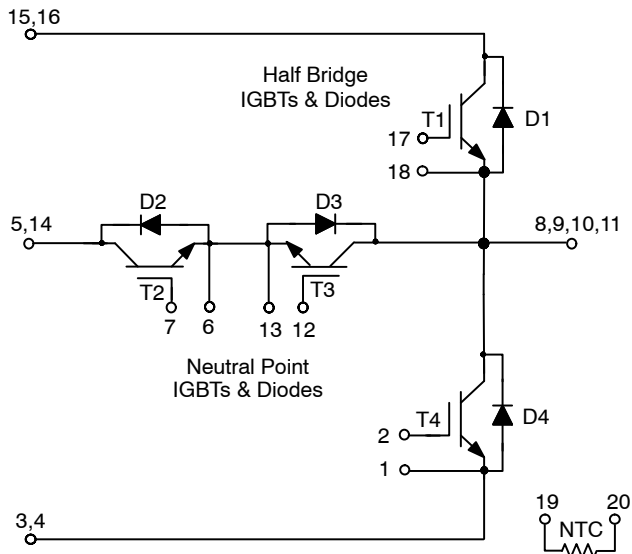


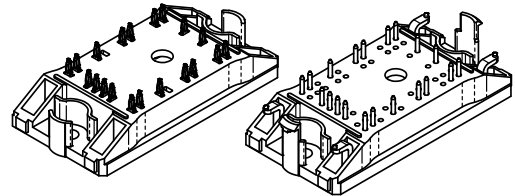
Figure 1. Schematic Diagram

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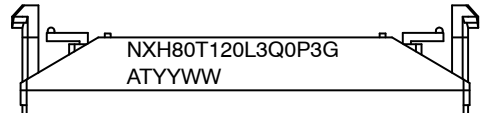
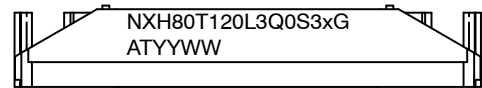
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QOPACK
CASE 180AA
PRESS-FIT PINS

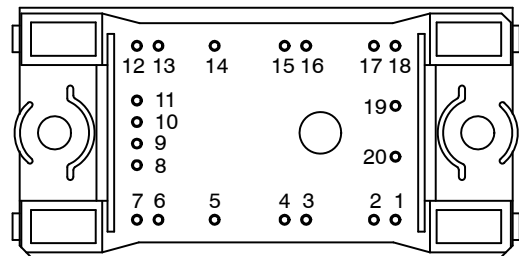
QOPACK
CASE 180AB
SOLDERABLE PINS

MARKING DIAGRAMS



NXH80T120L3Q0S3G = Specific Device Code
S3xG = S3G or S3TG
G = Pb-free Package
A = Assembly Site Code
T = Test Site Code
YYWW = Year and Work Week Code

PIN ASSIGNMENTS



ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 16 of this data sheet.

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Table 1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
HALF BRIDGE IGBT			
Collector–Emitter Voltage	V_{CES}	1200	V
Gate–Emitter Voltage	V_{GE}	± 20	V
Continuous Collector Current @ $T_c = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_C	75	A
Pulsed Collector Current ($T_J = 175^\circ\text{C}$)	I_{Cpulse}	225	A
Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	P_{tot}	188	W
Minimum Operating Junction Temperature	T_{JMIN}	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	175	$^\circ\text{C}$
NEUTRAL POINT IGBT			
Collector–Emitter Voltage	V_{CES}	650	V
Gate–Emitter Voltage	V_{GE}	± 20	V
Continuous Collector Current @ $T_c = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_C	50	A
Pulsed Collector Current ($T_J = 175^\circ\text{C}$)	I_{Cpulse}	150	A
Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	P_{tot}	82	W
Minimum Operating Junction Temperature	T_{JMIN}	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	150	$^\circ\text{C}$
HALF BRIDGE DIODE			
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Continuous Forward Current @ $T_c = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_F	37	A
Repetitive Peak Forward Current ($T_J = 175^\circ\text{C}$)	I_{FRM}	111	A
Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	P_{tot}	79	W
Minimum Operating Junction Temperature	T_{JMIN}	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	175	$^\circ\text{C}$
NEUTRAL POINT DIODE			
Peak Repetitive Reverse Voltage	V_{RRM}	650	V
Continuous Forward Current @ $T_c = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_F	37	A
Repetitive Peak Forward Current ($T_J = 175^\circ\text{C}$)	I_{FRM}	111	A
Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	P_{tot}	68	W
Minimum Operating Junction Temperature	T_{JMIN}	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	150	$^\circ\text{C}$
THERMAL PROPERTIES			
Maximum Operating Junction Temperature under Switching Conditions	T_{VJOP}	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to 125	$^\circ\text{C}$
Storage Temperature Range (TIM)	T_{stg}	-25 to 40	$^\circ\text{C}$
INSULATION PROPERTIES			
Isolation test voltage, $t = 1$ sec, 50 Hz	V_{is}	4000	V_{RMS}
Creepage distance		12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

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Table 2. ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
HALF BRIDGE IGBT CHARACTERISTICS						
Collector–Emitter Cutoff Current	$V_{GE} = 0\text{ V}, V_{CE} = 1200\text{ V}$	I_{CES}	–	–	300	μA
Collector–Emitter Saturation Voltage	$V_{GE} = 15\text{ V}, I_C = 80\text{ A}, T_J = 25^\circ\text{C}$	$V_{CE(sat)}$	–	1.7	2.4	V
	$V_{GE} = 15\text{ V}, I_C = 80\text{ A}, T_J = 150^\circ\text{C}$		–	1.8	–	
Gate–Emitter Threshold Voltage	$V_{GE} = V_{CE}, I_C = 2\text{ mA}$	$V_{GE(TH)}$	4.6	5.6	6.5	V
Gate Leakage Current	$V_{GE} = 20\text{ V}, V_{CE} = 0\text{ V}$	I_{GES}	–	–	300	nA
Turn-on Delay Time	$T_J = 25^\circ\text{C}$ $V_{CE} = 350\text{ V}, I_C = 60\text{ A}$ $V_{GE} = \pm 15\text{ V}, R_G = 4.7\ \Omega$	$t_{d(on)}$	–	51	–	ns
Rise Time		t_r	–	27	–	
Turn-off Delay Time		$t_{d(off)}$	–	200	–	
Fall Time		t_f	–	40	–	
Turn-on Switching Loss per Pulse		E_{on}	–	0.74	–	
Turn off Switching Loss per Pulse	E_{off}	–	1.41	–		
Turn-on Delay Time	$T_J = 125^\circ\text{C}$ $V_{CE} = 350\text{ V}, I_C = 60\text{ A}$ $V_{GE} = \pm 15\text{ V}, R_G = 4.7\ \Omega$	$t_{d(on)}$	–	45	–	ns
Rise Time		t_r	–	30	–	
Turn-off Delay Time		$t_{d(off)}$	–	230	–	
Fall Time		t_f	–	110	–	
Turn-on Switching Loss per Pulse		E_{on}	–	1.11	–	
Turn off Switching Loss per Pulse	E_{off}	–	2.17	–		
Input Capacitance	$V_{CE} = 20\text{ V}, V_{GE} = 0\text{ V}, f = 10\text{ kHz}$	C_{ies}	–	18150	–	pF
Output Capacitance		C_{oes}	–	345	–	
Reverse Transfer Capacitance		C_{res}	–	295	–	
Total Gate Charge	$V_{CE} = 600\text{ V}, I_C = 80\text{ A}, V_{GE} = \pm 15\text{ V}$	Q_g	–	817	–	nC
Thermal Resistance – chip-to–heatsink	Thermal grease, Thickness = 76 μm , $\lambda = 2.9\text{ W/mK}$	R_{thJH}	–	0.51	–	$^\circ\text{C/W}$

NEUTRAL POINT DIODE CHARACTERISTICS

Diode Forward Voltage	$I_F = 50\text{ A}, T_J = 25^\circ\text{C}$	V_F	–	1.38	2.1	V
	$I_F = 50\text{ A}, T_J = 150^\circ\text{C}$		–	1.27	–	
Reverse Recovery Time	$T_J = 25^\circ\text{C}$ $V_{CE} = 350\text{ V}, I_C = 60\text{ A}$ $V_{GE} = \pm 15\text{ V}, R_G = 4.7\ \Omega$	t_{rr}	–	32	–	ns
Reverse Recovery Charge		Q_{rr}	–	1.35	–	μC
Peak Reverse Recovery Current		I_{RRM}	–	64	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	1100	–	$\text{A}/\mu\text{s}$
Reverse Recovery Energy		E_{rr}	–	280	–	μJ
Reverse Recovery Time	$T_J = 125^\circ\text{C}$ $V_{CE} = 350\text{ V}, I_C = 60\text{ A}$ $V_{GE} = \pm 15\text{ V}, R_G = 4.7\ \Omega$	t_{rr}	–	85	–	ns
Reverse Recovery Charge		Q_{rr}	–	3	–	μC
Peak Reverse Recovery Current		I_{RRM}	–	78	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	6500	–	$\text{A}/\mu\text{s}$
Reverse Recovery Energy		E_{rr}	–	1390	–	μJ
Thermal Resistance – chip-to–heatsink	Thermal grease, Thickness = 76 μm , $\lambda = 2.9\text{ W/mK}$	R_{thJH}	–	1.39	–	$^\circ\text{C/W}$

NEUTRAL POINT IGBT CHARACTERISTICS

Collector–Emitter Cutoff Current	$V_{GE} = 0\text{ V}, V_{CE} = 600\text{ V}$	I_{CES}	–	–	200	μA
Collector–Emitter Saturation Voltage	$V_{GE} = 15\text{ V}, I_C = 50\text{ A}, T_J = 25^\circ\text{C}$	$V_{CE(sat)}$	–	1.0	1.4	V
	$V_{GE} = 15\text{ V}, I_C = 50\text{ A}, T_J = 150^\circ\text{C}$		–	0.93	–	
Gate–Emitter Threshold Voltage	$V_{GE} = V_{CE}, I_C = 250\ \mu\text{A}$	$V_{GE(TH)}$	3	3.6	5	V
Gate Leakage Current	$V_{GE} = 20\text{ V}, V_{CE} = 0\text{ V}$	I_{GES}	–	–	500	nA

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Table 2. ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
NEUTRAL POINT IGBT CHARACTERISTICS						
Turn-on Delay Time	$T_J = 25^\circ\text{C}$ $V_{CE} = 350\text{ V}, I_C = 60\text{ A}$ $V_{GE} = \pm 15\text{ V}, R_G = 20\ \Omega$	$t_{d(on)}$	-	65	-	ns
Rise Time		t_r	-	20	-	
Turn-off Delay Time		$t_{d(off)}$	-	660	-	
Fall Time		t_f	-	20	-	
Turn-on Switching Loss per Pulse		E_{on}	-	1.37	-	mJ
Turn off Switching Loss per Pulse		E_{off}	-	0.9	-	
Turn-on Delay Time	$T_J = 125^\circ\text{C}$ $V_{CE} = 350\text{ V}, I_C = 60\text{ A}$ $V_{GE} = \pm 15\text{ V}, R_G = 20\ \Omega$	$t_{d(on)}$	-	70	-	ns
Rise Time		t_r	-	28	-	
Turn-off Delay Time		$t_{d(off)}$	-	720	-	
Fall Time		t_f	-	30	-	
Turn-on Switching Loss per Pulse		E_{on}	-	2.45	-	mJ
Turn off Switching Loss per Pulse		E_{off}	-	1.0	-	
Input Capacitance	$V_{CE} = 20\text{ V}, V_{GE} = 0\text{ V}, f = 10\text{ kHz}$	C_{ies}	-	16881	-	pF
Output Capacitance		C_{oes}	-	107	-	
Reverse Transfer Capacitance		C_{res}	-	94	-	
Total Gate Charge	$V_{CE} = 480\text{ V}, I_C = 50\text{ A}, V_{GE} = \pm 15\text{ V}$	Q_g	-	830	-	nC
Thermal Resistance – chip-to-heatsink	Thermal grease, Thickness = 76 μm , $\lambda = 2.9\text{ W/mK}$	R_{thJH}	-	1.16	-	$^\circ\text{C/W}$

HALF BRIDGE DIODE CHARACTERISTICS

Diode Forward Voltage	$I_F = 40\text{ A}, T_J = 25^\circ\text{C}$	V_F	-	2.43	3.10	V
	$I_F = 40\text{ A}, T_J = 150^\circ\text{C}$		-	1.63	-	
Reverse recovery time	$T_J = 25^\circ\text{C}$ $V_{CE} = 350\text{ V}, I_C = 60\text{ A}$ $V_{GE} = \pm 15\text{ V}, R_G = 62\ \Omega$	t_{rr}	-	45	-	ns
Reverse recovery charge		Q_{rr}	-	2	-	μC
Peak reverse recovery current		I_{RRM}	-	140	-	A
Peak rate of fall of recovery current		di/dt	-	860	-	$\text{A}/\mu\text{s}$
Reverse recovery energy		E_{rr}	-	310	-	μJ
Reverse recovery time		$T_J = 125^\circ\text{C}$ $V_{CE} = 350\text{ V}, I_C = 60\text{ A}$ $V_{GE} = \pm 15\text{ V}, R_G = 62\ \Omega$	t_{rr}	-	75	-
Reverse recovery charge	Q_{rr}		-	5.5	-	μC
Peak reverse recovery current	I_{RRM}		-	125	-	A
Peak rate of fall of recovery current	di/dt		-	740	-	$\text{A}/\mu\text{s}$
Reverse recovery energy	E_{rr}		-	640	-	μJ
Thermal Resistance – chip-to-heatsink	Thermal grease, Thickness = 76 μm , $\lambda = 2.9\text{ W/mK}$		R_{thJH}	-	1.2	-

THERMISTOR CHARACTERISTICS

Nominal resistance		R	-	22	-	k Ω
Nominal resistance	$T = 100^\circ\text{C}$	R	-	1468	-	Ω
Deviation of R25		$\Delta R/R$	-5	-	5	%
Power dissipation		P_D	-	200	-	mW
Power dissipation constant			-	2	-	mW/K
B-value	B(25/50), tolerance $\pm 3\%$		-	-	3950	K
B-value	B(25/100), tolerance $\pm 3\%$		-	-	3998	K
NTC reference					B	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT AND DIODE

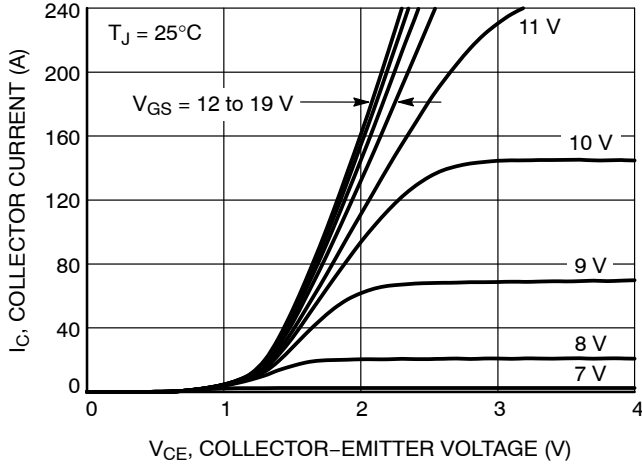


Figure 2. Typical Output Characteristics

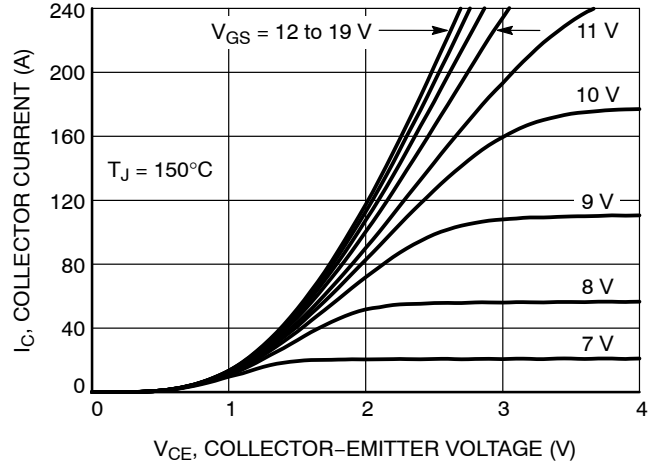


Figure 3. Typical Output Characteristics

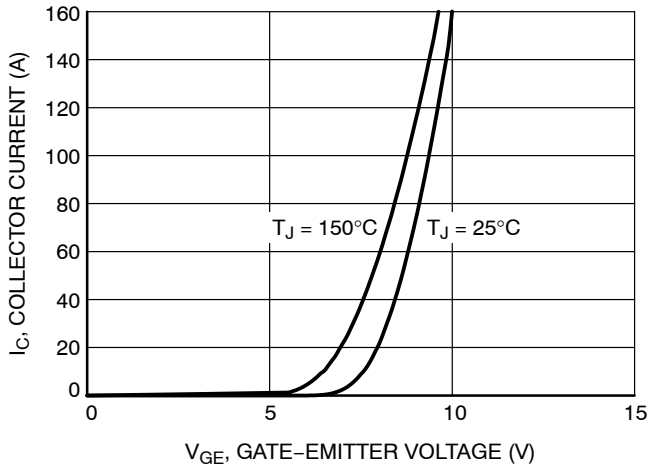


Figure 4. Typical Transfer Characteristics

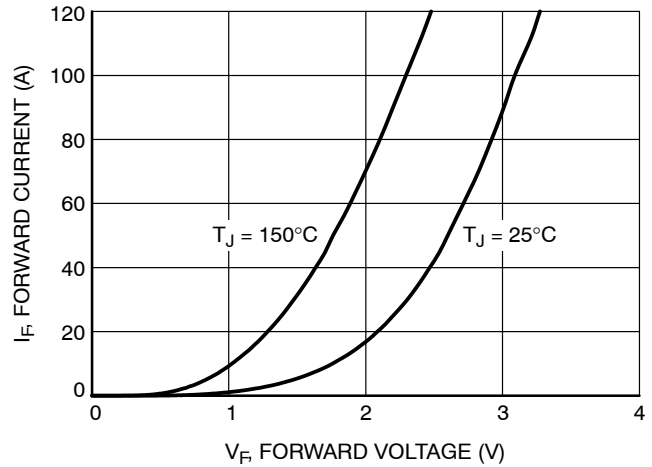


Figure 5. Typical Diode Forward Characteristics

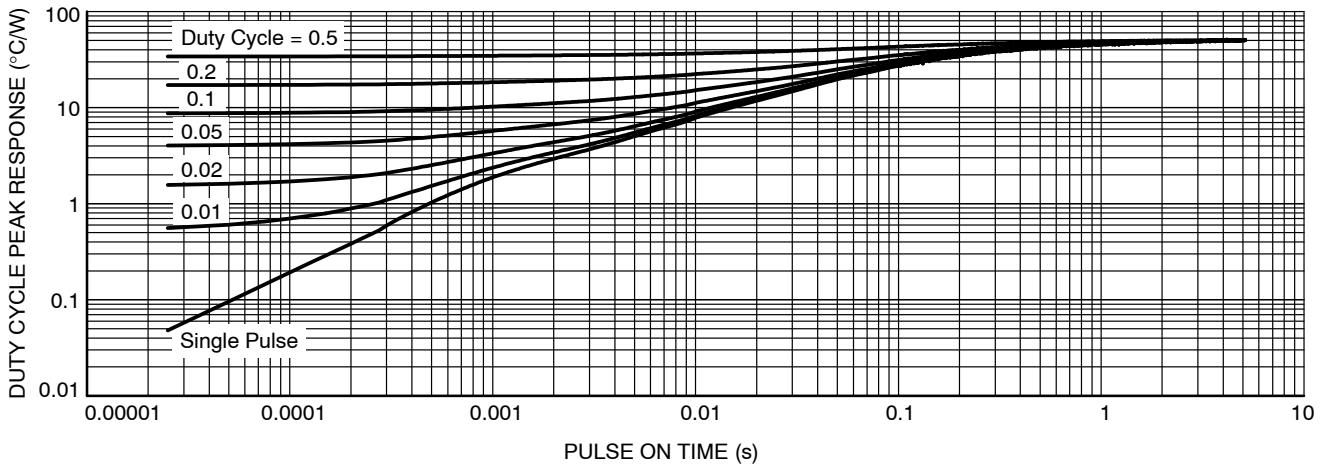


Figure 6. Transient Thermal Impedance (Half Bridge IGBT)

NXH80T120L3Q0S3G/S3TG, NXH80T120L3Q0P3G

TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT AND DIODE

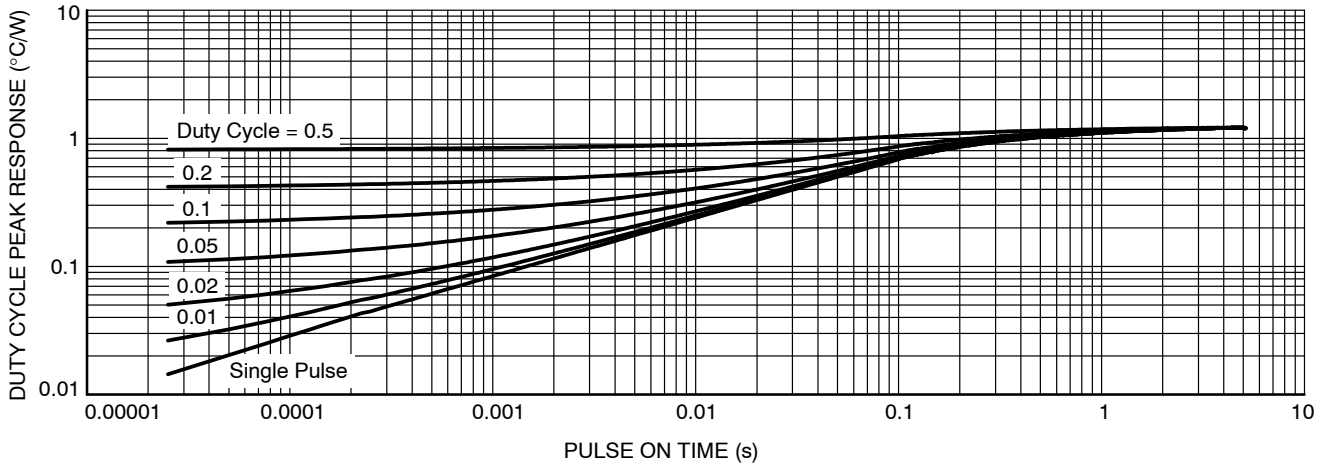


Figure 7. Transient Thermal Impedance (Half Bridge Diode)

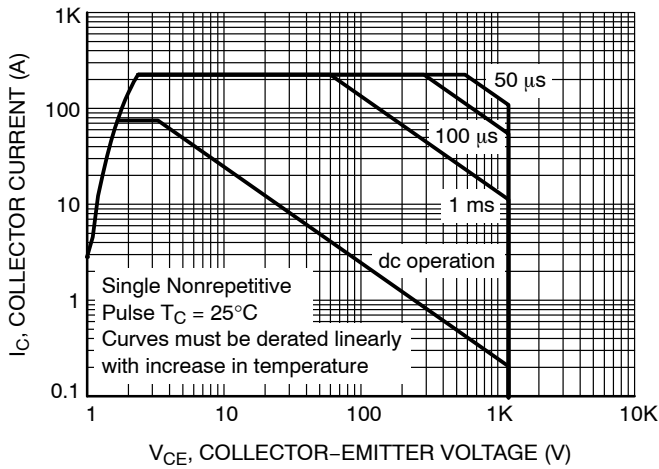


Figure 8. FB Safe Operating Area

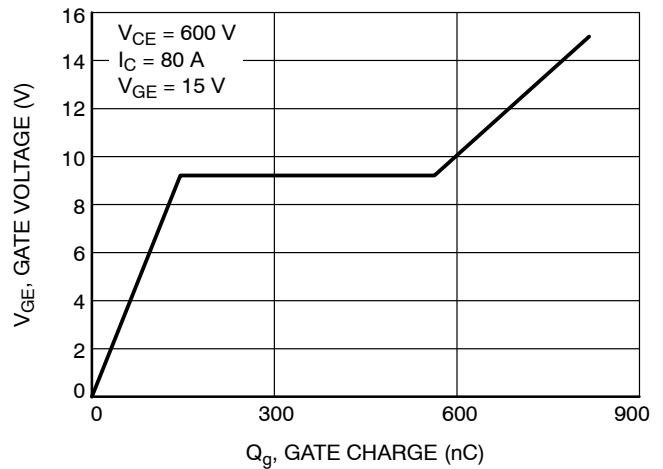


Figure 9. Gate Voltage vs. Gate Charge

NXH80T120L3Q0S3G/S3TG, NXH80T120L3Q0P3G

TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT AND DIODE

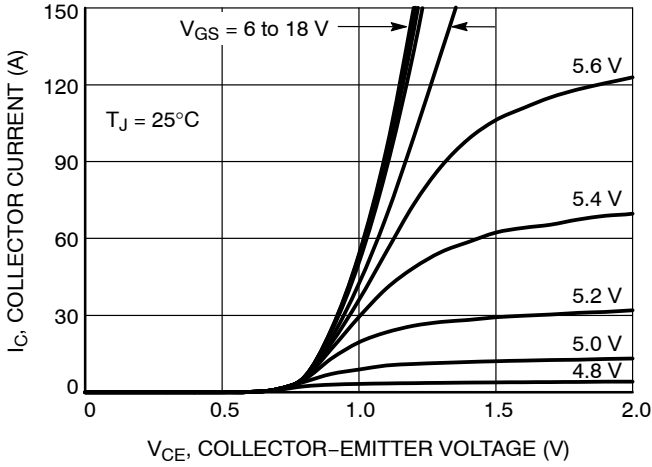


Figure 10. Typical Output Characteristics

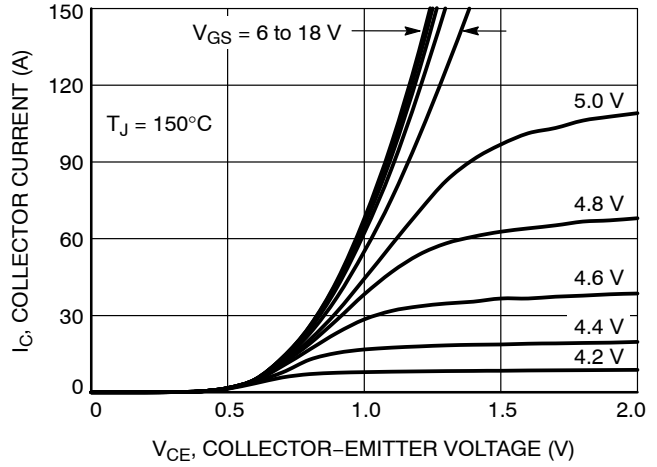


Figure 11. Typical Output Characteristics

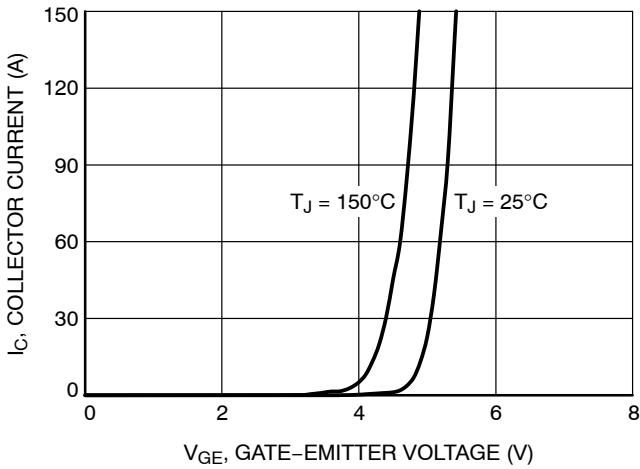


Figure 12. Typical Transfer Characteristics

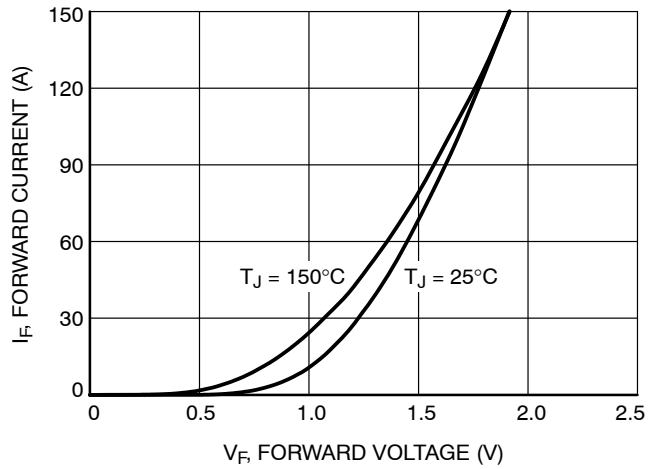


Figure 13. Typical Diode Forward Characteristics

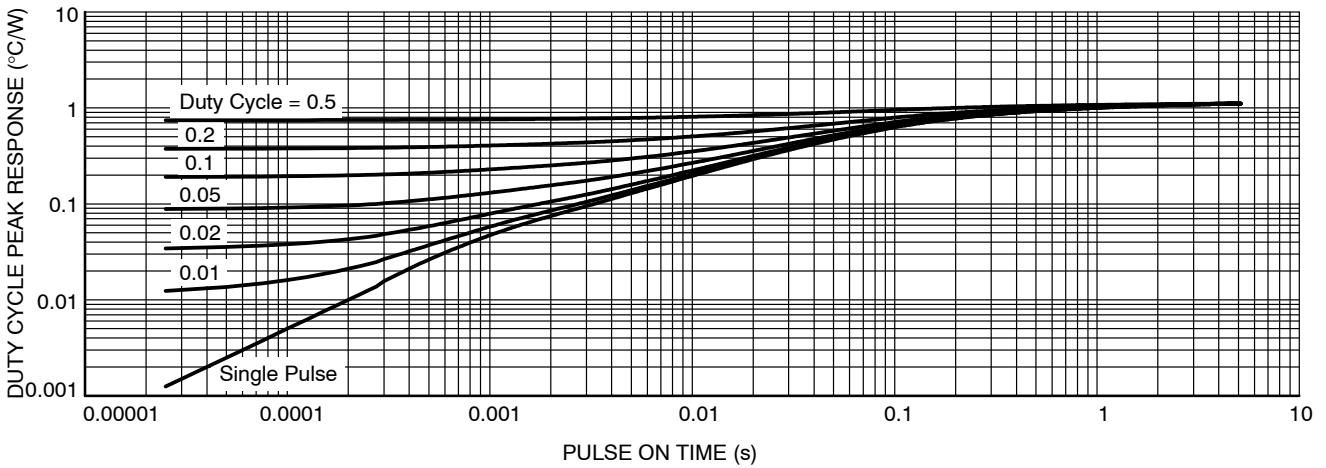


Figure 14. Transient Thermal Impedance (Neutral Point IGBT)

NXH80T120L3Q0S3G/S3TG, NXH80T120L3Q0P3G

TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT AND DIODE

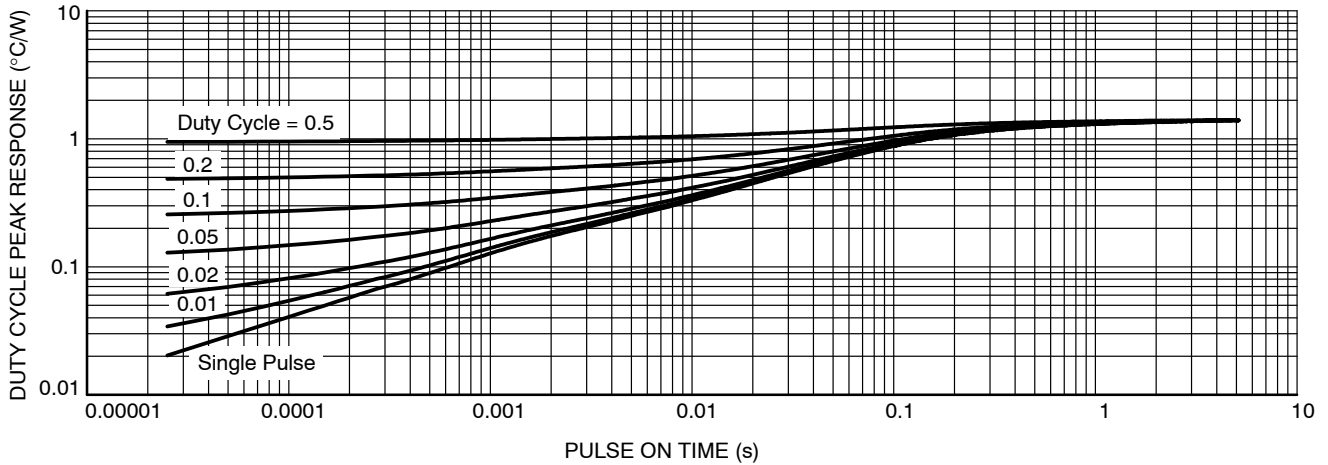


Figure 15. Transient Thermal Impedance (Neutral Point Diode)

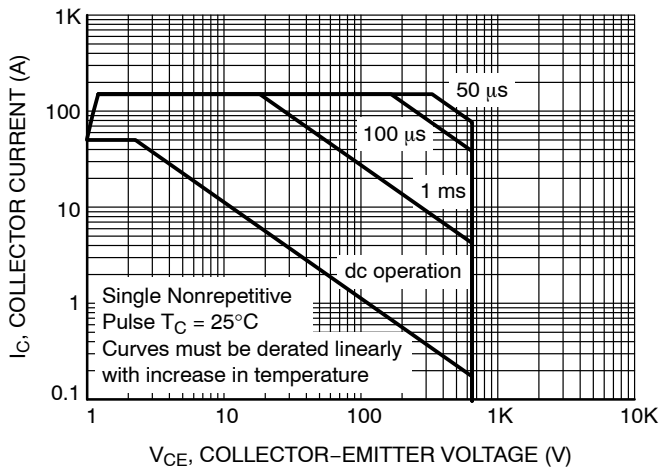


Figure 16. FB Safe Operating Area

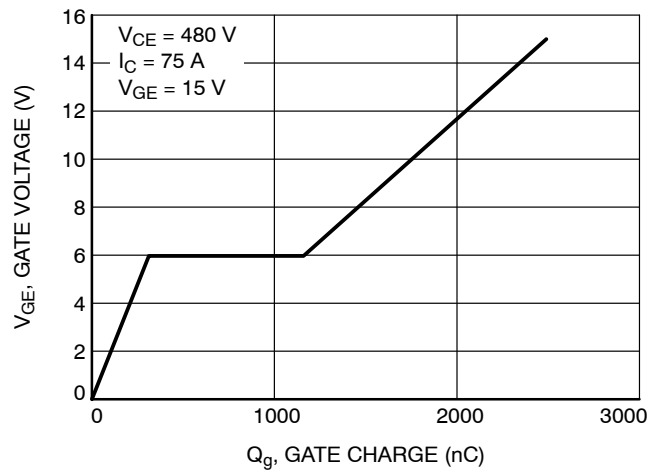


Figure 17. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT COMMUTATES NEUTRAL POINT DIODE

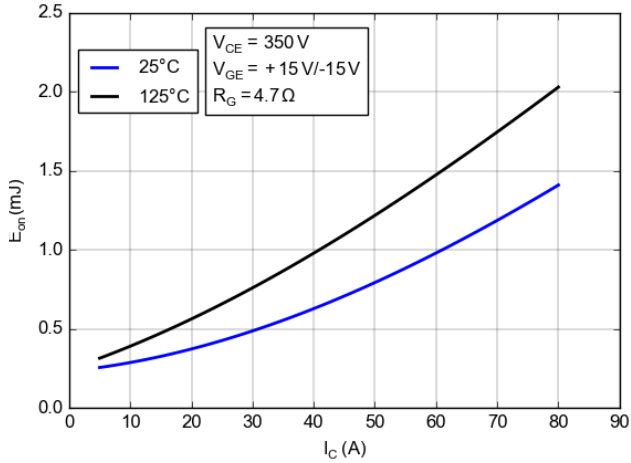


Figure 18. Typical Turn On Loss vs. I_C

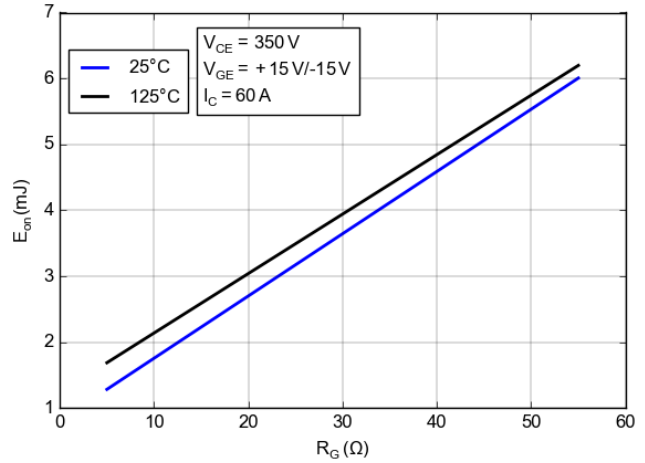


Figure 19. Typical Turn On Loss vs. R_G

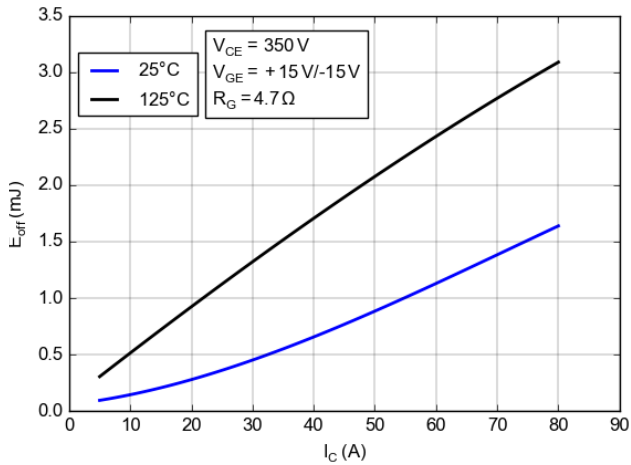


Figure 20. Typical Turn Off Loss vs. I_C

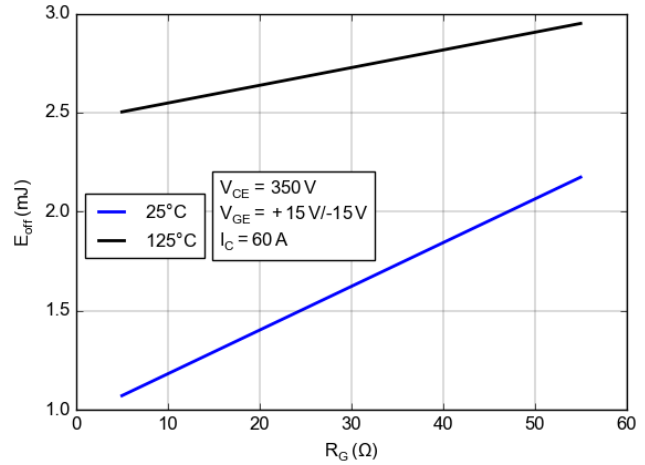


Figure 21. Typical Turn Off Loss vs. R_G

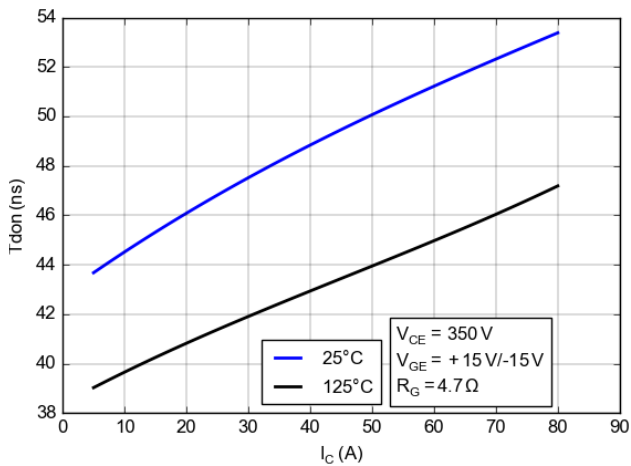


Figure 22. Typical Switching Times T_{don} vs. I_C

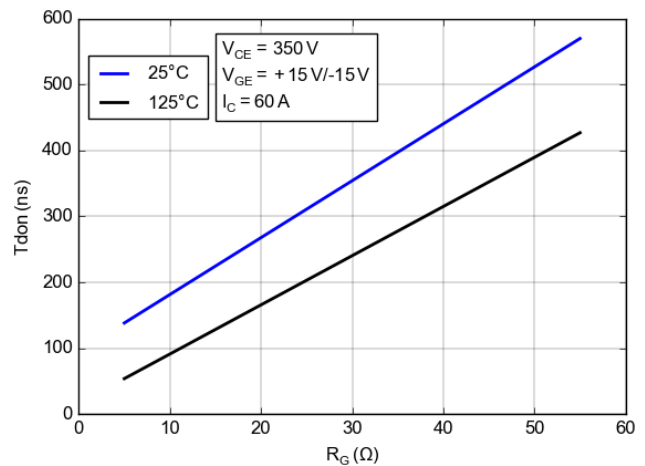


Figure 23. Typical Switching Times T_{don} vs. R_G

TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT COMMUTATES NEUTRAL POINT DIODE

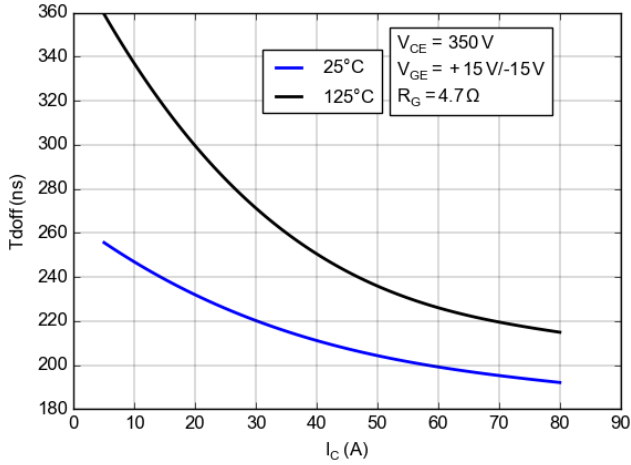


Figure 24. Typical Switching Times Tdoff vs. I_C

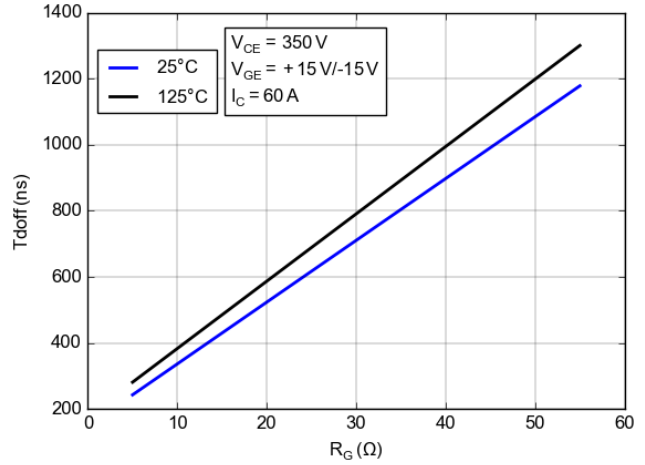


Figure 25. Typical Switching Times Tdoff vs. R_G

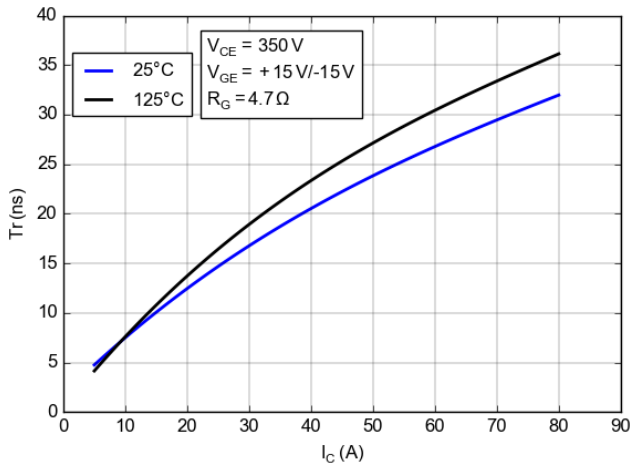


Figure 26. Typical Switching Times Tron vs. I_C

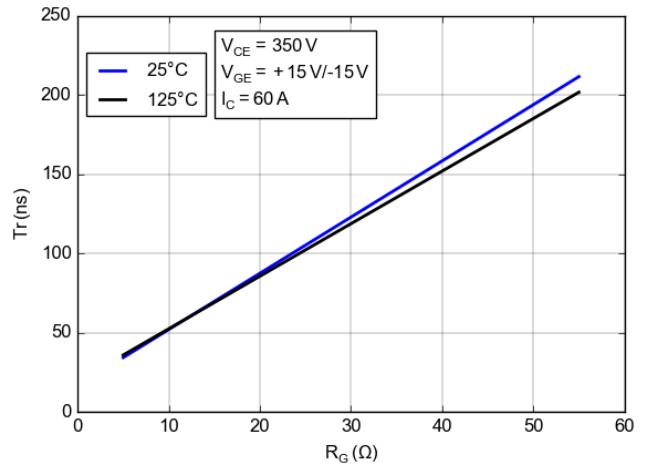


Figure 27. Typical Switching Times Tron vs. R_G

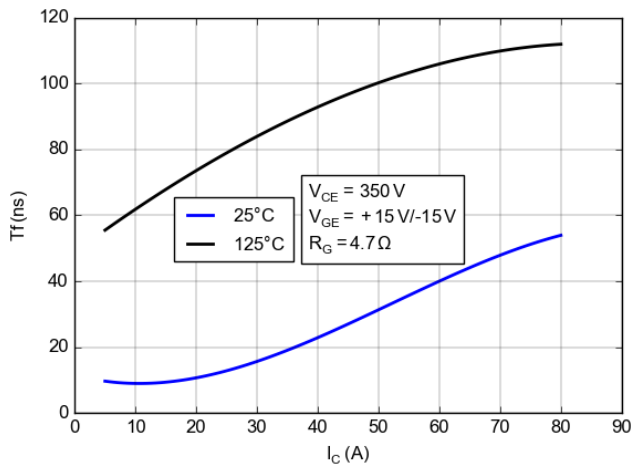


Figure 28. Typical Switching Times Tf vs. I_C

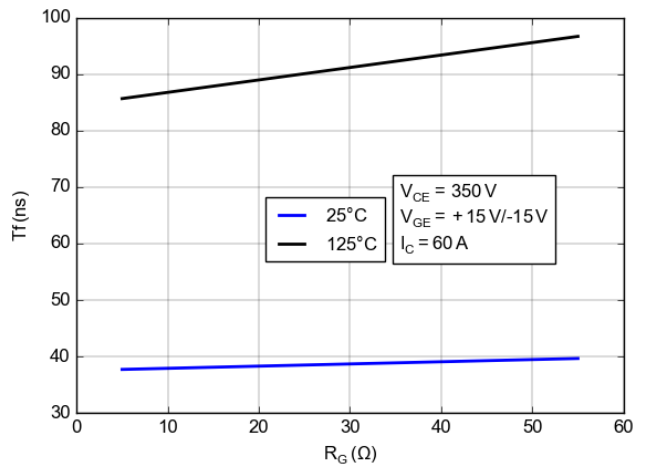


Figure 29. Typical Switching Times Tf vs. R_G

TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT COMMUTATES NEUTRAL POINT DIODE

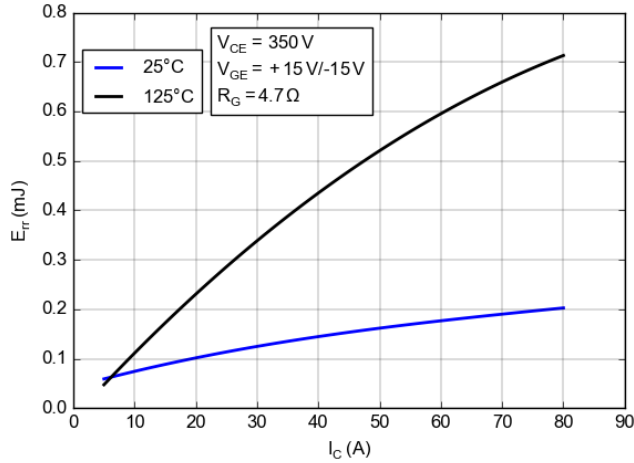


Figure 30. Typical Reverse Recovery Energy vs. I_C

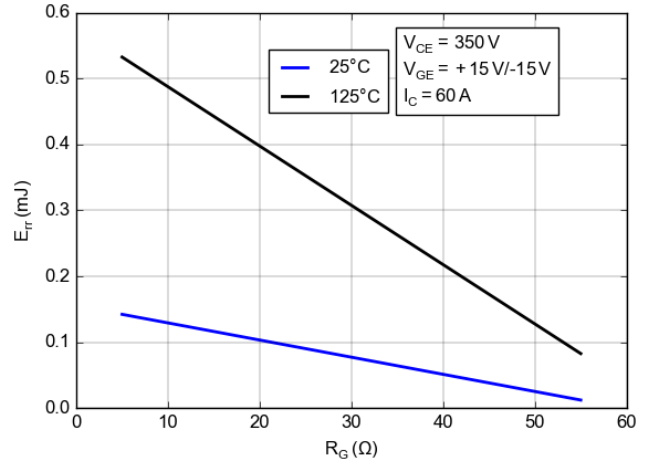


Figure 31. Typical Reverse Recovery Energy vs. R_G

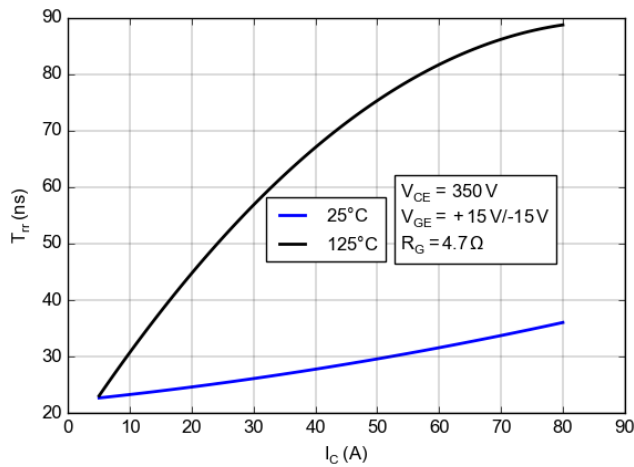


Figure 32. Typical Reverse Recovery Time vs. I_C

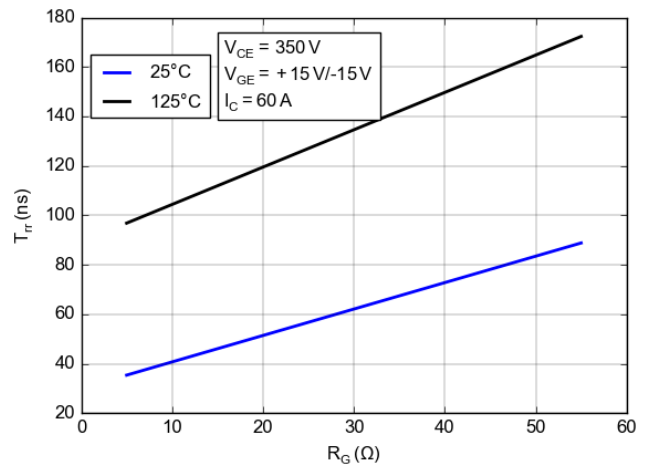


Figure 33. Typical Reverse Recovery Time vs. R_G

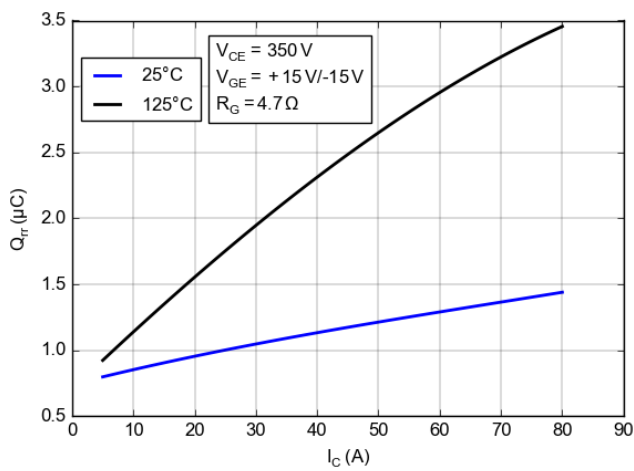


Figure 34. Typical Reverse Recovery Charge vs. I_C

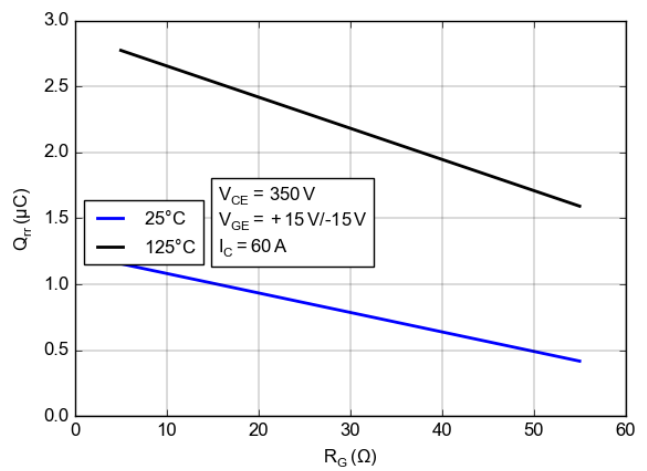


Figure 35. Typical Reverse Recovery Charge vs. R_G

NXH80T120L3Q0S3G/S3TG, NXH80T120L3Q0P3G

TYPICAL CHARACTERISTICS – HALF BRIDGE IGBT COMMUTATES NEUTRAL POINT DIODE

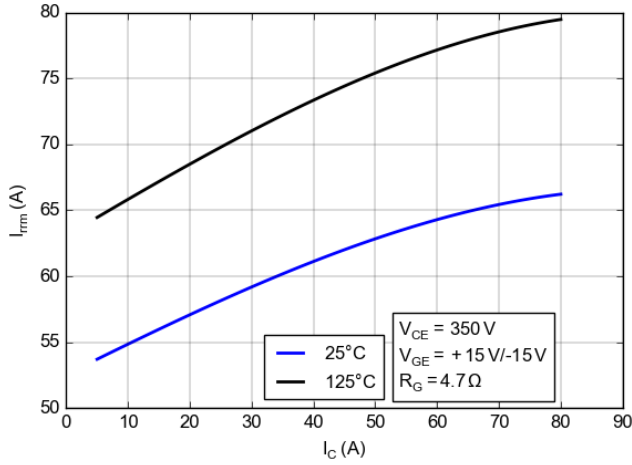


Figure 36. Typical Reverse Recovery Current vs. I_C

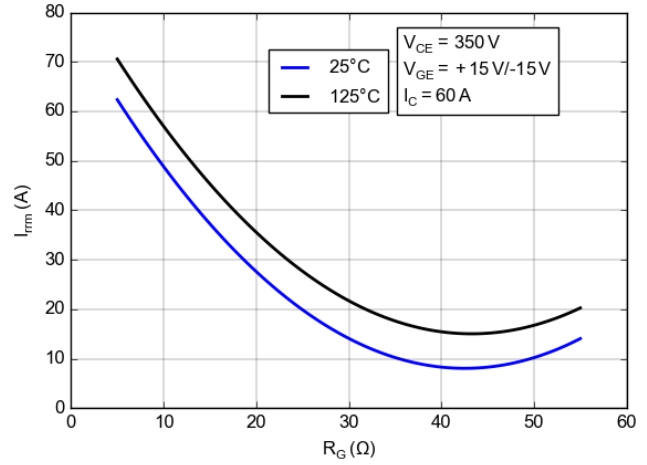


Figure 37. Typical Reverse Recovery Current vs. R_G

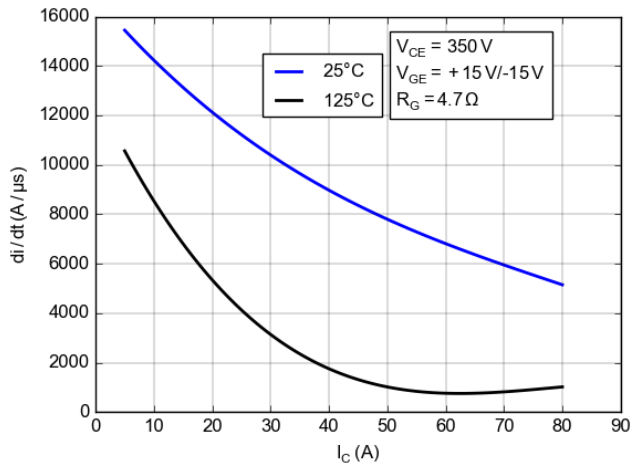


Figure 38. Typical di/dt vs. I_C

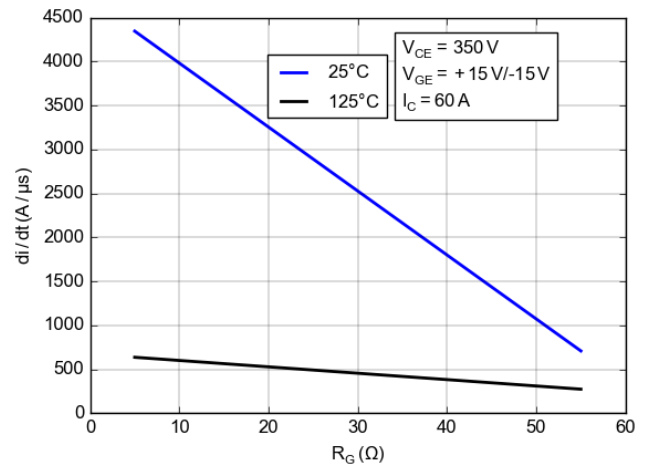


Figure 39. Typical di/dt vs. R_G

TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT COMMUTATES HALF BRIDGE DIODE

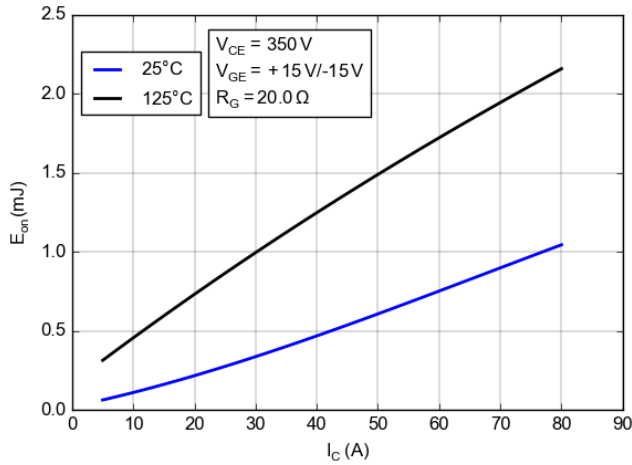


Figure 40. Typical Turn On Loss vs. I_C

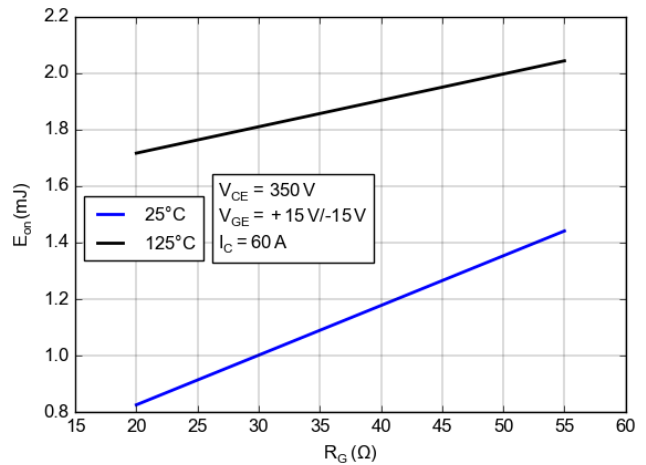


Figure 41. Typical Turn On Loss vs. R_G

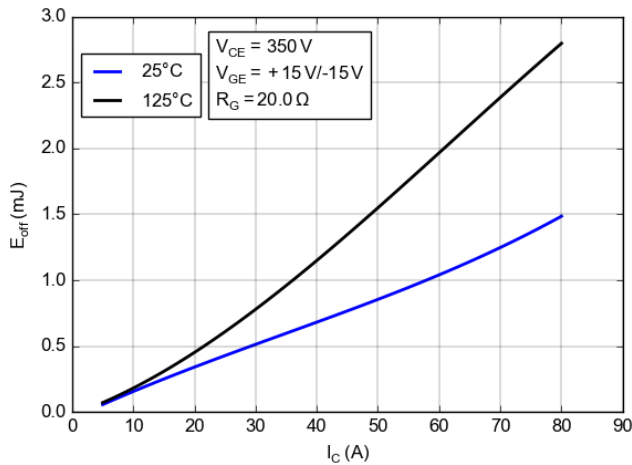


Figure 42. Typical Turn Off Loss vs. I_C

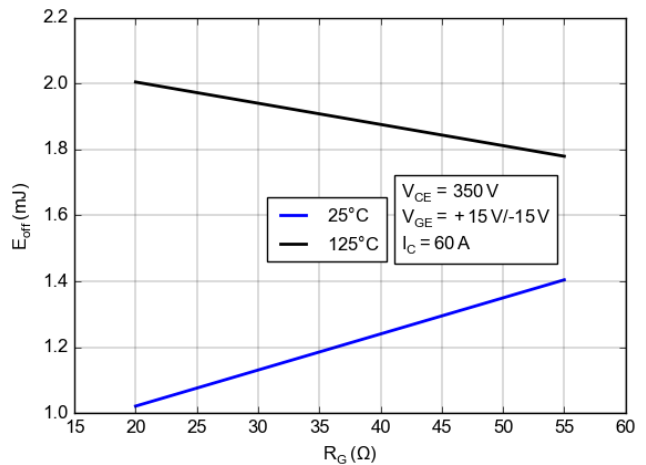


Figure 43. Typical Turn Off Loss vs. R_G

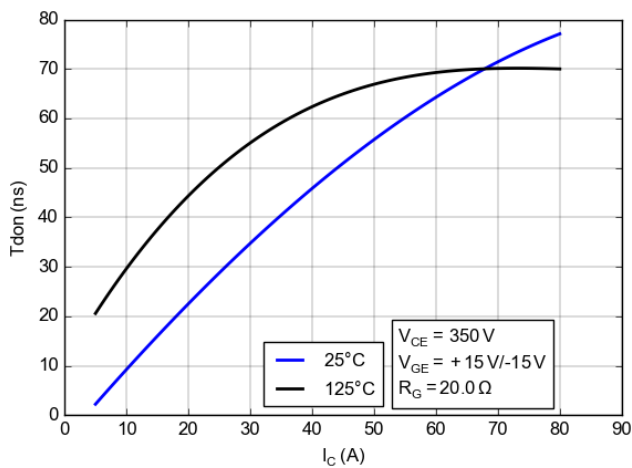


Figure 44. Typical Switching Times T_{don} vs. I_C

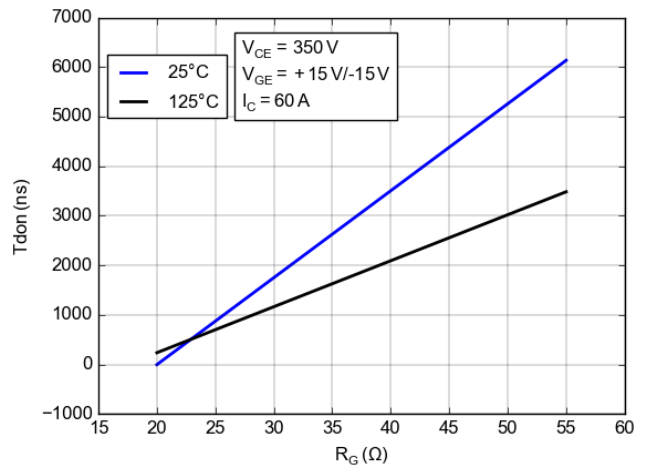


Figure 45. Typical Switching Times T_{don} vs. R_G

TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT COMMUTATES HALF BRIDGE DIODE

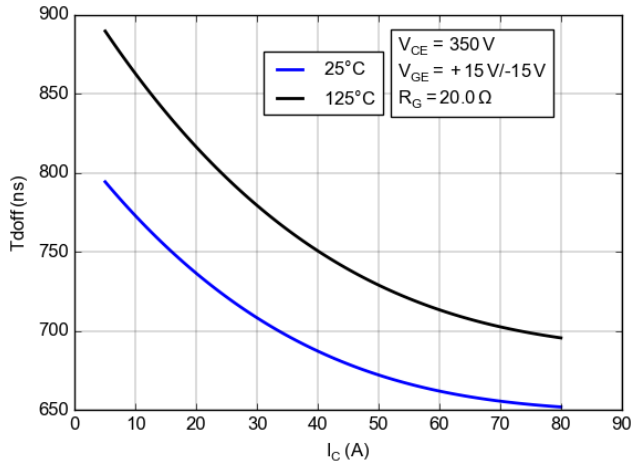


Figure 46. Typical Switching Times Tdoff vs. I_C

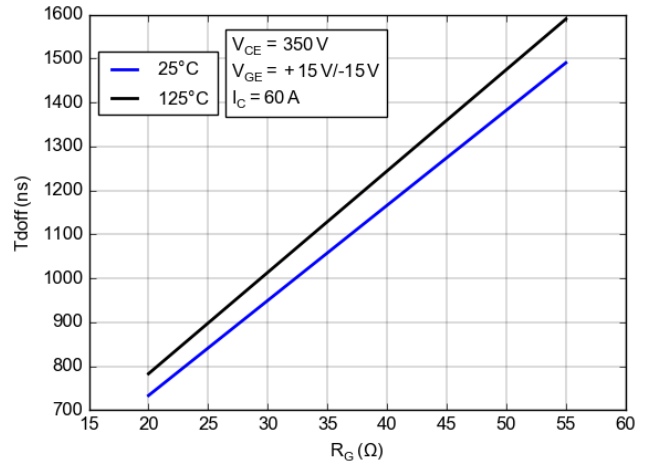


Figure 47. Typical Switching Times Tdoff vs. R_G

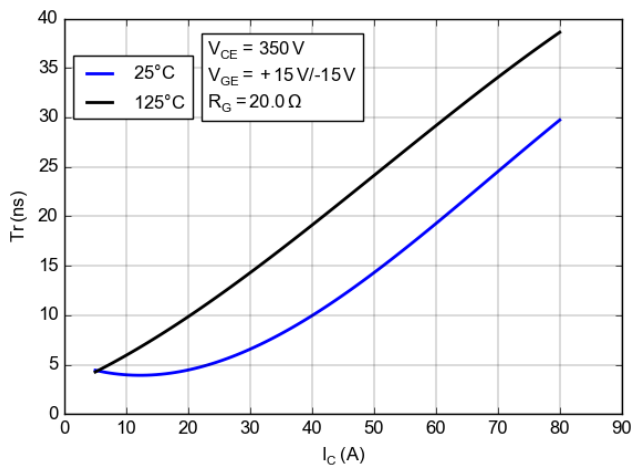


Figure 48. Typical Switching Times Tron vs. I_C

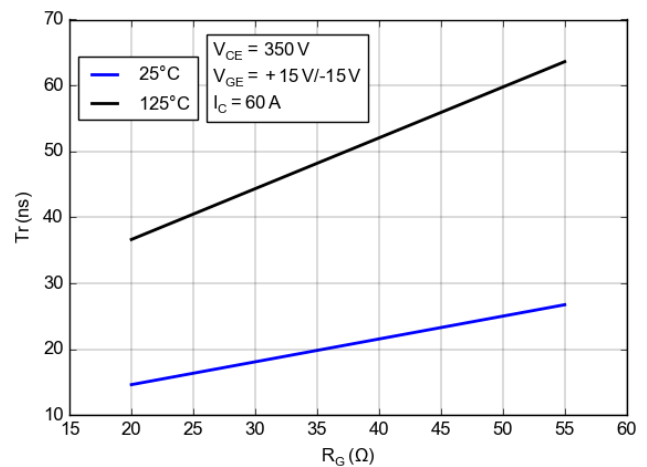


Figure 49. Typical Switching Times Tron vs. R_G

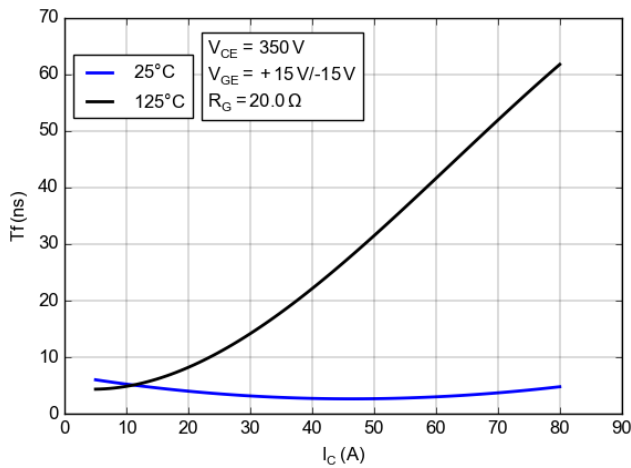


Figure 50. Typical Switching Times Tf vs. I_C

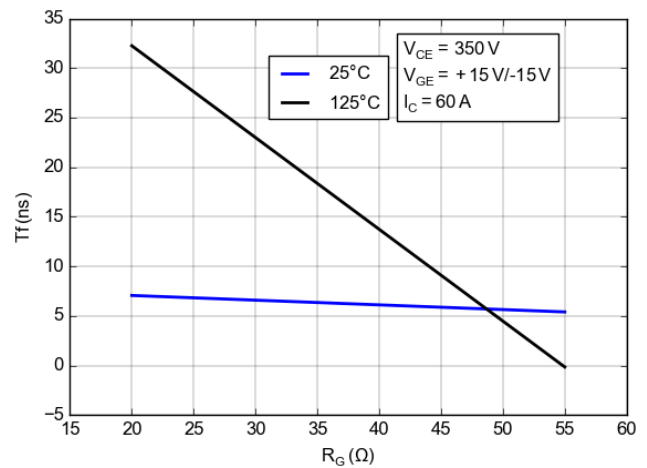


Figure 51. Typical Switching Times Tf vs. R_G

TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT COMMUTATES HALF BRIDGE DIODE

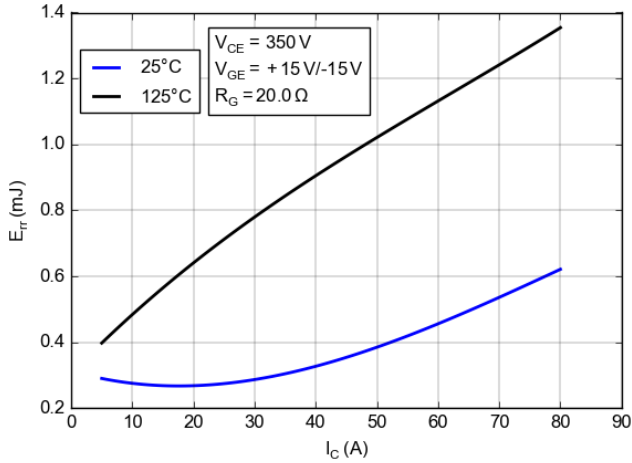


Figure 52. Typical Reverse Recovery Energy vs. I_C

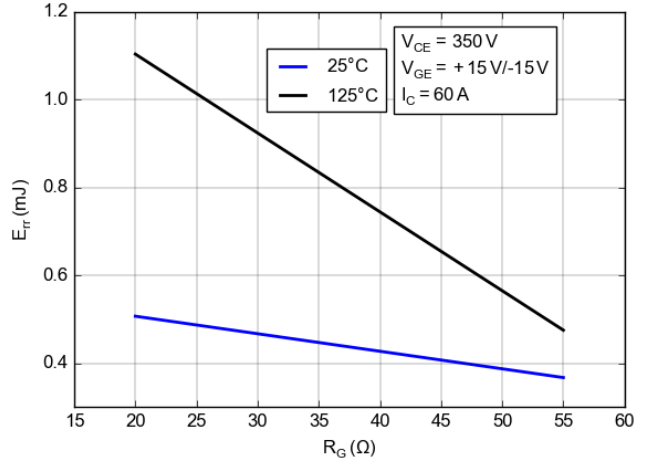


Figure 53. Typical Reverse Recovery Energy vs. R_G

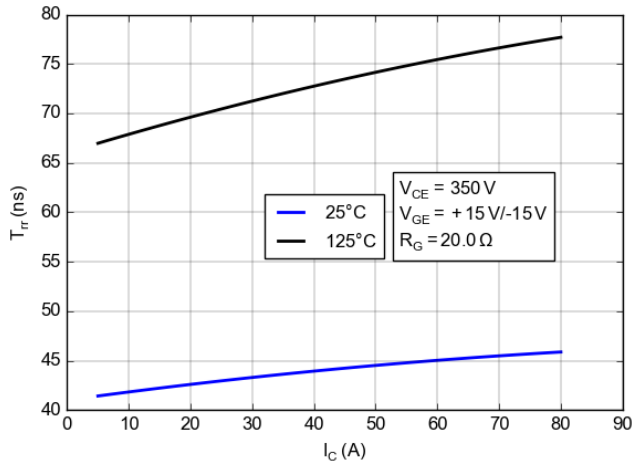


Figure 54. Typical Reverse Recovery Time vs. I_C

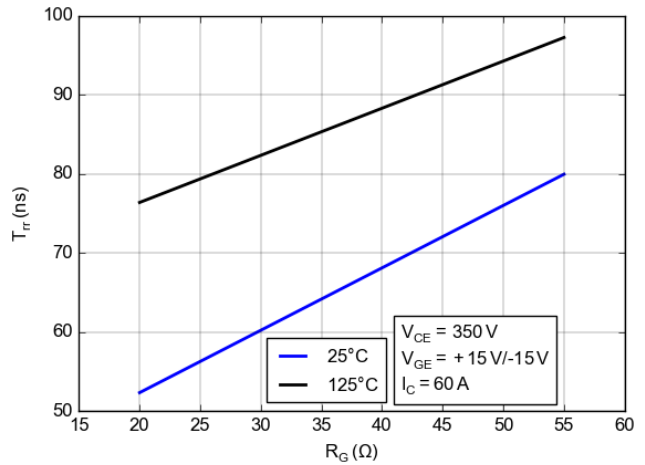


Figure 55. Typical Reverse Recovery Time vs. R_G

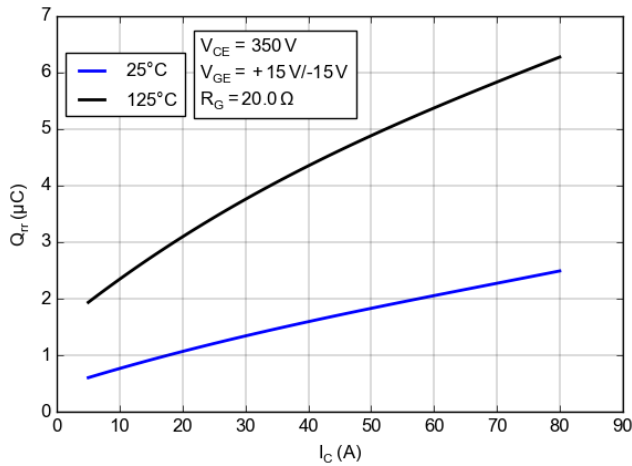


Figure 56. Typical Reverse Recovery Charge vs. I_C

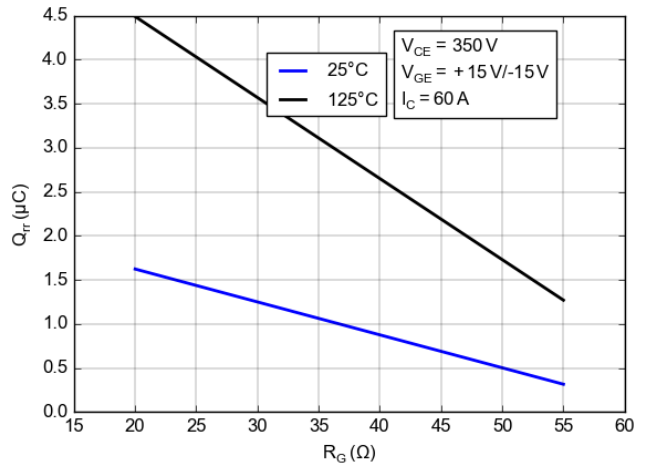


Figure 57. Typical Reverse Recovery Charge vs. R_G

NXH80T120L3Q0S3G/S3TG, NXH80T120L3Q0P3G

TYPICAL CHARACTERISTICS – NEUTRAL POINT IGBT COMMUTATES HALF BRIDGE DIODE

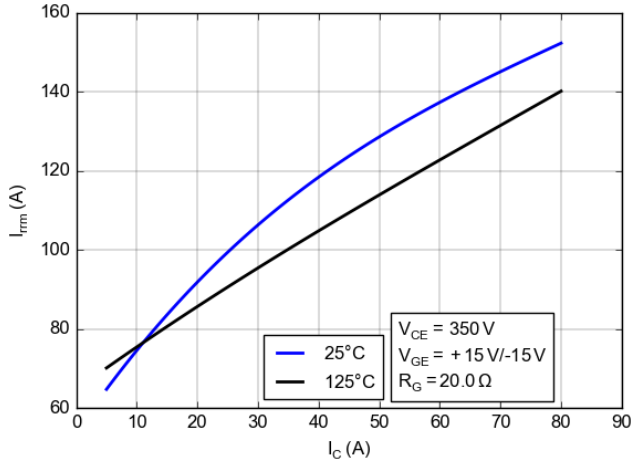


Figure 58. Typical Reverse Recovery Current vs. I_C

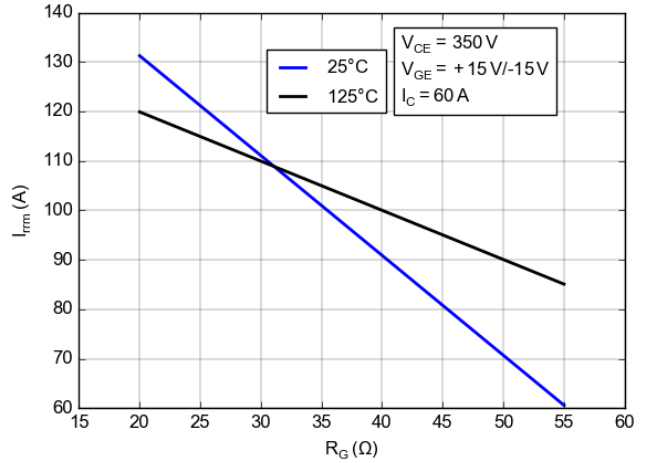


Figure 59. Typical Reverse Recovery Current vs. R_G

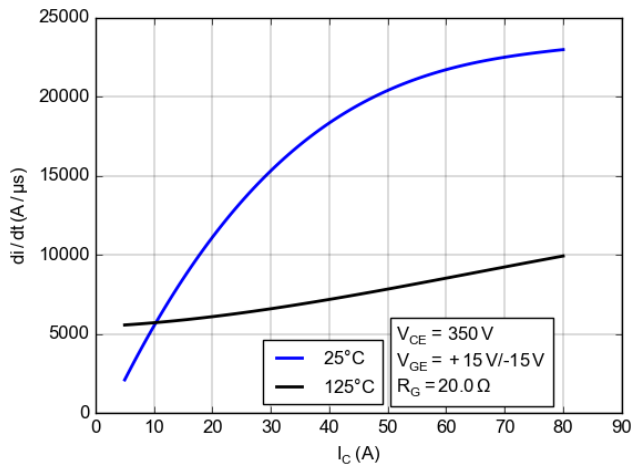


Figure 60. Typical di/dt vs I_C

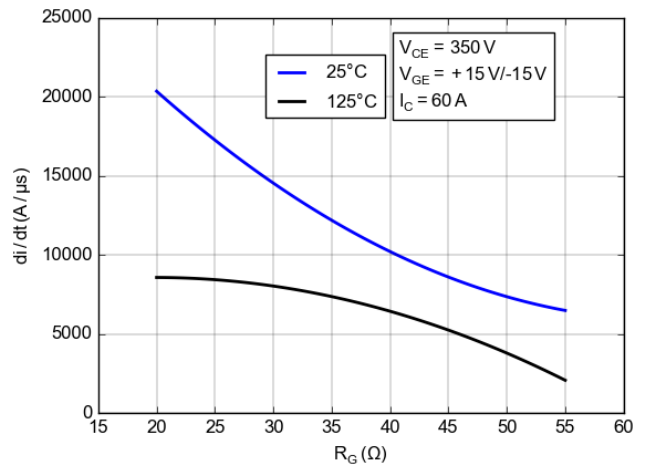


Figure 61. Typical di/dt vs R_G

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH80T120L3Q0P3G	NXH80T120L3Q0P3G	Q0PACK – Case 180AA (Pb-Free and Halide-Free)	24 Units / Blister Tray
NXH80T120L3Q0S3G	NXH80T120L3Q0S3G	Q0PACK – Case 180AB (Pb-Free and Halide-Free)	24 Units / Blister Tray
NXH80T120L3Q0S3TG	NXH80T120L3Q0S3TG	Q0PACK – Case 180AB with pre-applied thermal interface material (TIM) (Pb-Free and Halide-Free)	24 Units / Blister Tray

MECHANICAL CASE OUTLINE

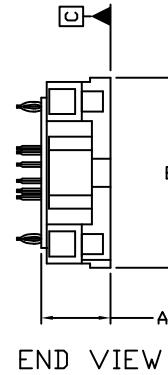
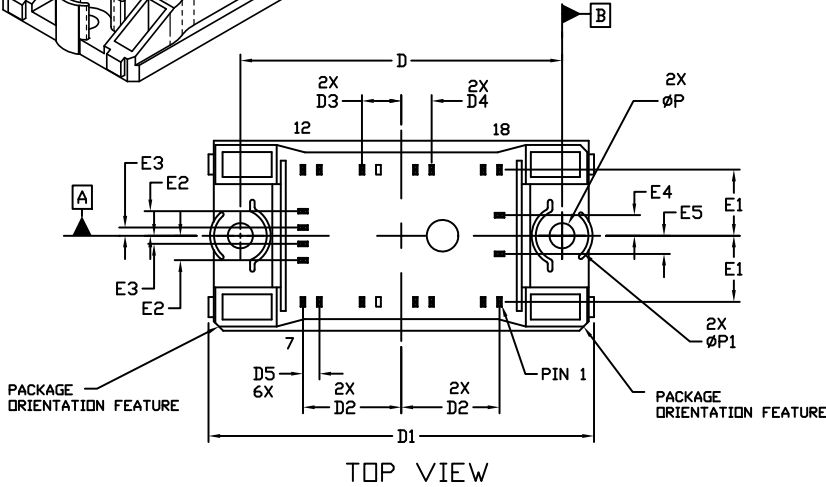
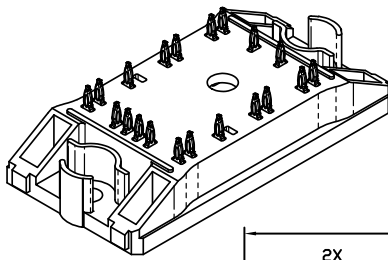
PACKAGE DIMENSIONS

ON Semiconductor®

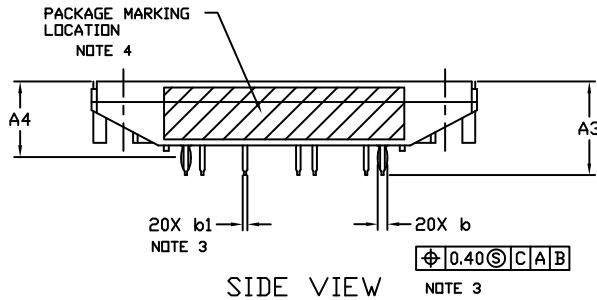


PIM20, 55x32.5 / Q0PACK
CASE 180AA
ISSUE D

DATE 07 AUG 2018

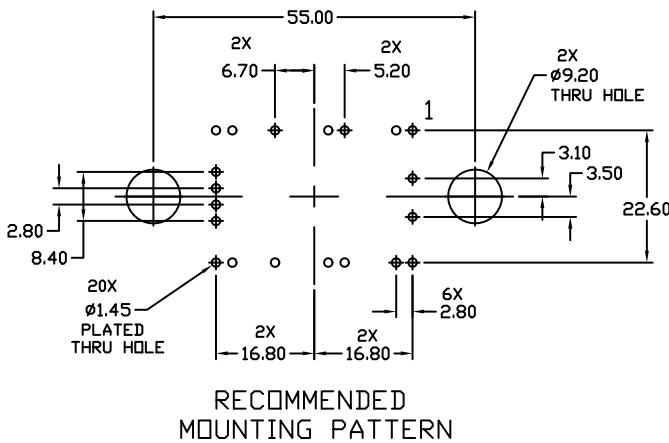


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.33	11.83	12.33
A3	15.50	16.00	16.50
A4	12.88 BSC		
b	1.61	1.66	1.71
b1	0.75	0.80	0.85
D	54.80	55.00	55.20
D1	65.70	67.90	70.10
D2	16.80 BSC		
D3	6.70 BSC		
D4	5.20 BSC		
D5	2.80 BSC		
E	32.30	32.50	32.70
E1	11.30 BSC		
E2	4.20 BSC		
E3	1.40 BSC		
E4	3.50 BSC		
E5	3.10 BSC		
P	4.10	4.30	4.50
P1	8.50	9.00	9.50

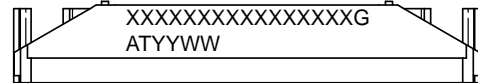


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A4.
4. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
 G = Pb-Free Package
 AT = Assembly & Test Site Code
 YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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MECHANICAL CASE OUTLINE

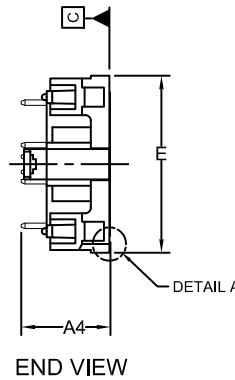
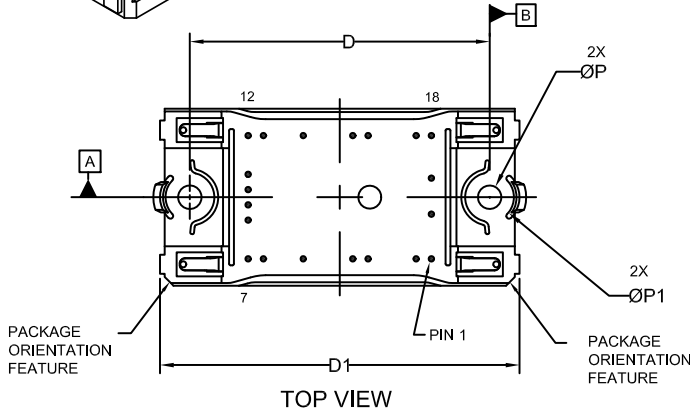
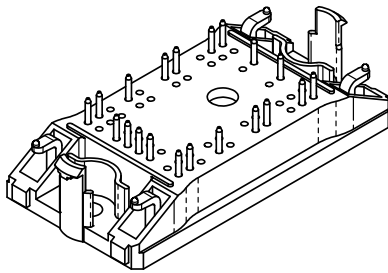
PACKAGE DIMENSIONS

ON Semiconductor®

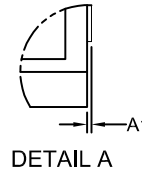
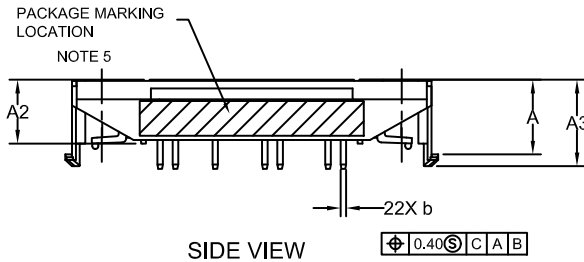


PIM20, 55x32.5 / Q0PACK CASE 180AB ISSUE D

DATE 21 NOV 2017



DIM	MILLIMETERS	
	MIN.	NOM.
A	13.50	13.90
A1	0.10	0.30
A2	11.50	11.90
A3	15.65	16.05
A4	16.35 REF	
b	0.95	1.05
D	54.80	55.20
D1	65.60	66.20
E	32.20	32.80
P	4.20	4.40
P1	8.90	9.10



NOTE 4

PIN	PIN POSITION		PIN	PIN POSITION	
	X	Y		X	Y
1	16.80	-11.30	11	-16.80	4.20
2	14.00	-11.30	12	-16.80	11.30
3	5.20	-11.30	13	-14.00	11.30
4	2.40	-11.30	14	-6.70	11.30
5	-6.70	-11.30	15	2.40	11.30
6	-14.00	-11.30	16	5.20	11.30
7	-16.80	-11.30	17	14.00	11.30
8	-16.80	-4.20	18	16.80	11.30
9	-16.80	-1.40	19	16.80	3.50
10	-16.80	1.40	20	16.80	-3.10

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 1.00 AND 3.00 FROM THE TERMINAL TIP.
- POSITION OF THE CENTER OF THE TERMINALS IS DETERMINED FROM DATUM B THE CENTER OF DIMENSION D, X DIRECTION, AND FROM DATUM A, Y DIRECTION. POSITIONAL TOLERANCE, AS NOTED IN DRAWING, APPLIES TO EACH TERMINAL IN BOTH DIRECTIONS.
- PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.

MOUNTING FOOTPRINT & MARKING DIAGRAM ON PAGE 2

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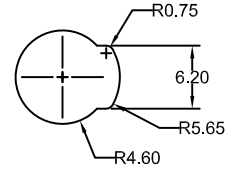
PIM20, 55x32.5 / Q0PACK
CASE 180AB
ISSUE D

DATE 21 NOV 2017

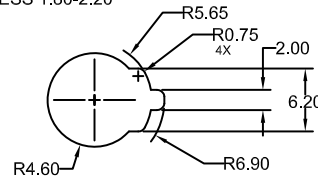
MOUNTING HOLE POSITION

PIN	PIN POSITION		PIN	PIN POSITION	
	X	Y		X	Y
1	16.80	11.30	11	-16.80	-4.20
2	14.00	11.30	12	-16.80	-11.30
3	5.20	11.30	13	-14.00	-11.30
4	2.40	11.30	14	-6.70	-11.30
5	-6.70	11.30	15	2.40	-11.30
6	-14.00	11.30	16	5.20	-11.30
7	-16.80	11.30	17	14.00	-11.30
8	-16.80	4.20	18	16.80	-11.30
9	-16.80	1.40	19	16.80	-3.50
10	-16.80	-1.40	20	16.80	3.10

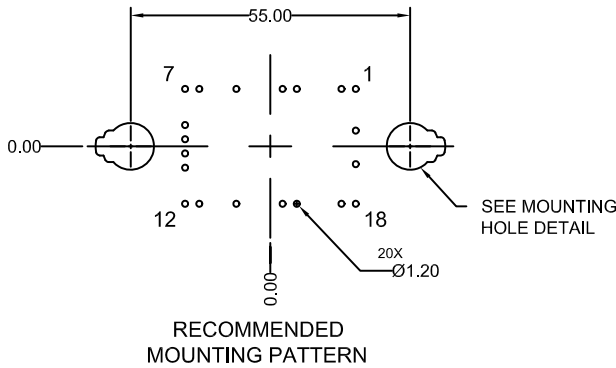
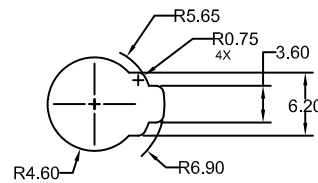
FOR PCB
THICKNESS 1.45-1.80



FOR PCB
THICKNESS 1.80-2.20

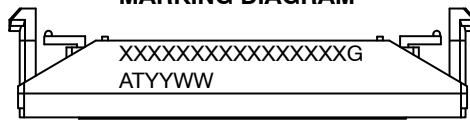


FOR PCB
THICKNESS 2.20-2.80



MOUNTING HOLE DETAIL

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
 G = Pb-Free Package
 AT = Assembly & Test Site Code
 YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	PIM20 55X32.5 / Q0PACK (SOLDER PIN)	PAGE 2 OF 2

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