

UM10541

NVT2008PW and NVT2010PW demo boards

Rev. 1 — 7 March 2012

User manual

Document information

Info	Content
Keywords	NVT, voltage translator, level translator, level shift, passive voltage translator, passive level translator, passive level shift, I2C-bus, SMBus, SPI, NVT2008, NVT2010
Abstract	NXP Voltage Translators (NVT) are used in bidirectional signaling voltage level translation applications for I/O buses with incompatible logic levels. The NVT2008 and NVT2010 are eight- and ten-channel voltage translators, operational from 1.0 V to 3.6 V at $V_{CC(A)}$ (low voltage side) and 1.8 V to 5.5 V at $V_{CC(B)}$ (high voltage side) without direction control for open-drain or push-pull I/O devices.



Revision history

Rev	Date	Description
v.1	20120307	user manual; initial release

Contact information

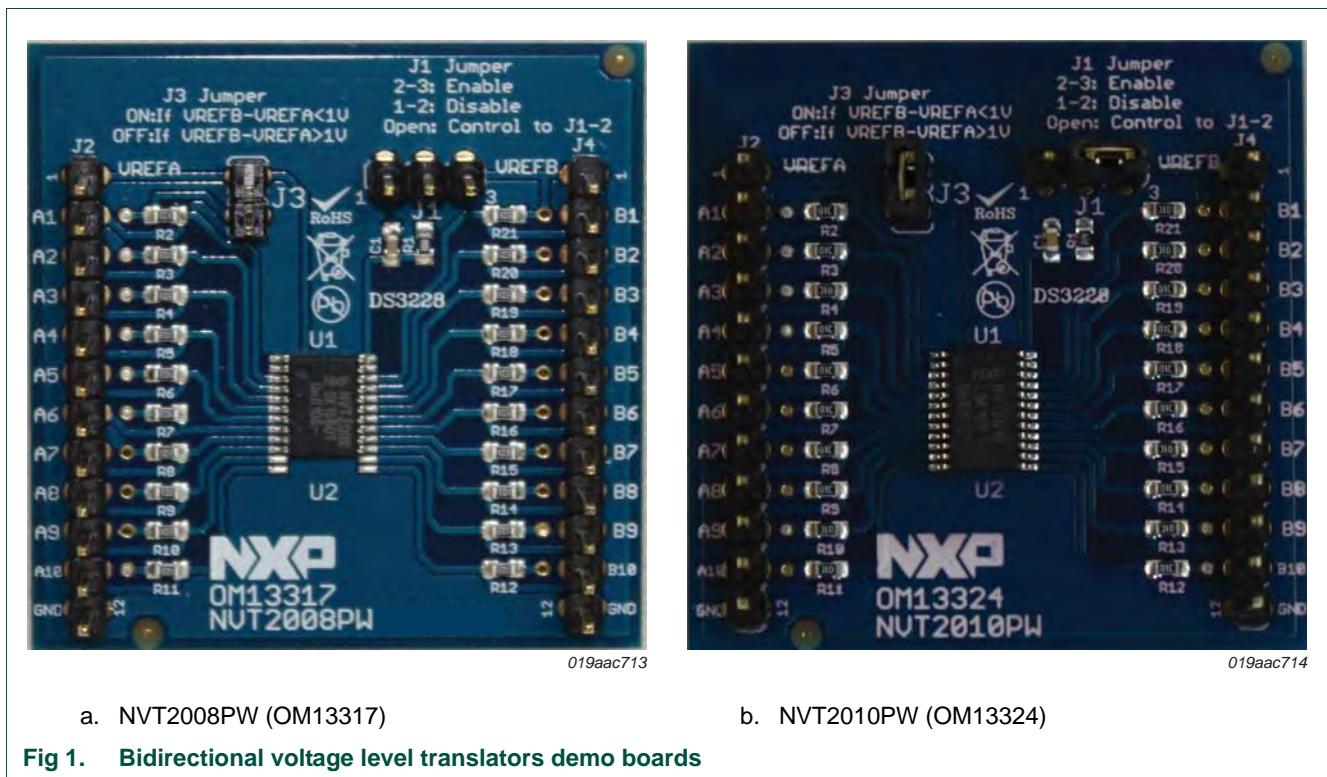
For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

The NVT2008PW (OM13317) and NVT2010PW (OM13324) demo boards are designed to let customers evaluate the NXP 8-channel and 10-channel bidirectional voltage level translators. The demo boards interface between device I/Os operating at different voltage levels. Since the NVT2008PW and NVT2010PW devices are passive devices, pull-up resistors may be needed depending on the I/O interface type (totem pole or open-drain), difference in translation voltage, and the translation direction (high-to-low voltage, low-to-high voltage, or bidirectional). The NVT2008PW and NVT2010PW devices allow translations between any voltages from 1.0 V to 5.5 V.

Please refer to NVT2008/NVT2010 data sheet ([Ref. 1](#)) and application note AN11127 ([Ref. 2](#)) for more detailed information.



2. Hardware description

2.1 Schematic

The demo boards contain footprints for the NVT2008PW and NVT2010PW devices, the jumpers, headers, and passive components are shared. The NVT2008PW and NVT2010PW demo board schematic is shown in [Figure 2](#). Pins 2 and 3 on J1 must be shorted to enable the part. Pins 1 and 12 on J2 are power and GND for the low voltage side. Pins 1 and 12 on J4 are power and GND for the high voltage side. All Bn I/O pins on the right side have 10 kΩ pull-up resistors to VREFB and all An I/O pins on the left side have 10 kΩ pull-up resistors to VREFA through jumper J3. A shunt must be installed at J3 if $VREFB - VREFA < 1\text{ V}$. If $VREFB - VREFA \geq 1\text{ V}$, then the J3 jumper should be open and resistors R2 through R11 must be removed. If they are not removed, then a resistive path exists between the A-side I/Os that can impact the efficiency and signal integrity of the solution.

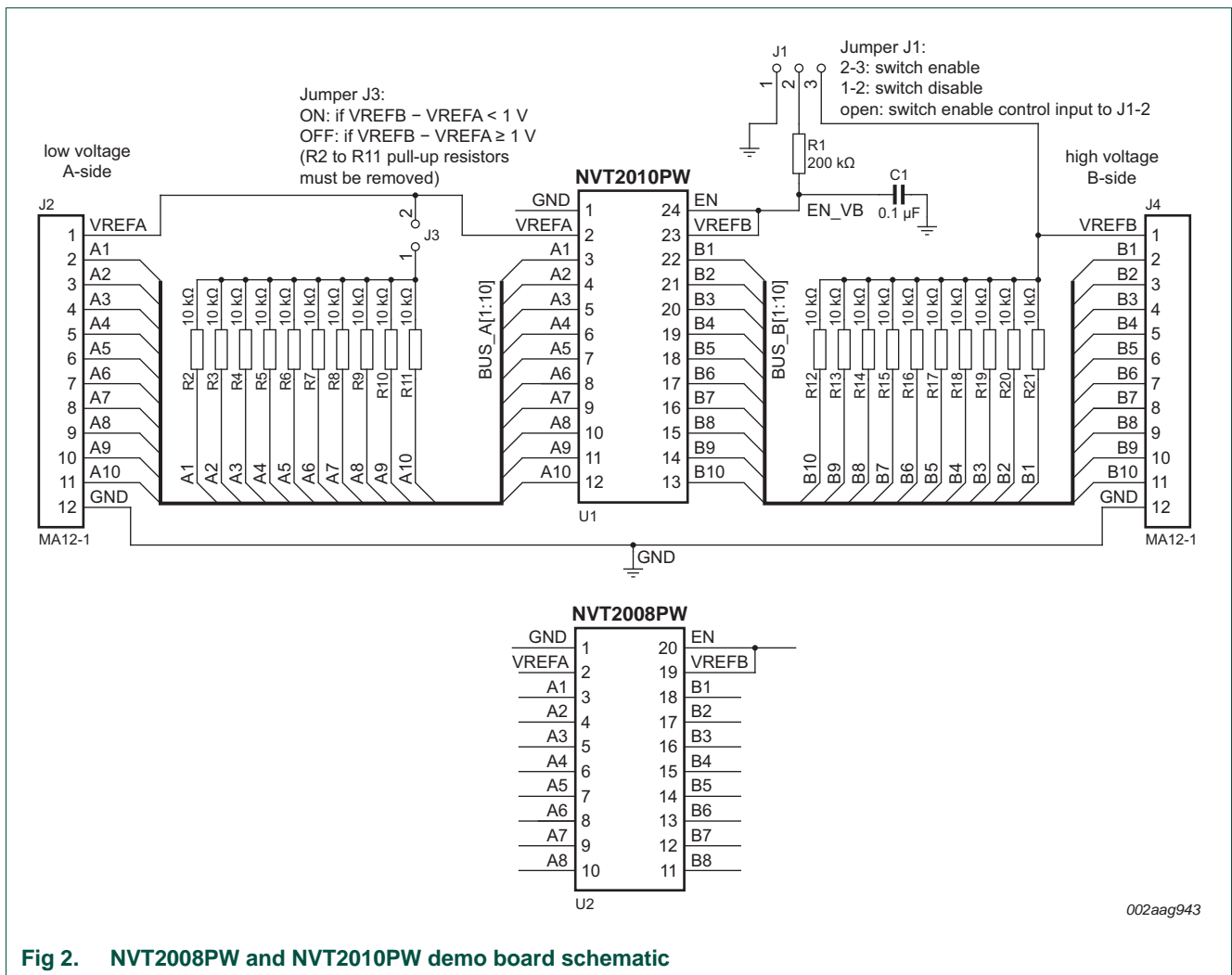


Fig 2. NVT2008PW and NVT2010PW demo board schematic

2.2 Jumper and header functions

The functions of the jumpers and headers on these demo boards are shown in [Table 1](#).

Table 1. Header descriptions for NVT2008PW (OM13317) and NVT2010PW (OM13324) demo boards

Jumper/header	Function	Notes
J1 (3-pin)	Device switch enable or disable control	Short pins 2 and 3 to enable the NVT2008PW or NVT2010PW device (default). When pins 1 and 2 are shorted, the device is disabled.
J2 (12-pin)	Low voltage VREFA, GND and An I/O signal connect pins	Pin 1 = VREFA: low voltage power. Pin 12 = GND: low voltage ground. A[1:8] are low voltage signals for NVT2008PW. A[1:10] are low voltage signals for NVT2010PW.
J3 (3-pin)	Connects 10 kΩ pull-up resistors to VREFA on low voltage side for VREFB – VREFA < 1 V application required	Short pins 1 and 2 to connect 10 kΩ pull-up resistors to VREFA on low voltage side (default). Remark: Pins 1 and 2 must be open and 10 kΩ pull-up resistors must be removed when VREFB – VREFA ≥ 1 V.
J4 (12-pin)	High voltage VREFB, GND and Bn I/O signal connect pins	Pin 1 = VREFB: high voltage power. Pin 12 = GND: high voltage ground. B[1:8] are high voltage signals for NVT2008PW. B[1:10] are high voltage signals for NVT2010PW.

3. References

- [1] NVT2008; NVT2010, “Bidirectional voltage-level translator for open-drain and push-pull applications” — Product data sheet; NXP Semiconductors; www.nxp.com/documents/data_sheet/NVT2008_NVT2010.pdf
- [2] AN11127, “Bidirectional voltage level translators NVT20xx, PCA9306, GTL2000, GTL2002, GTL2003, GTL2010” — application note; NXP Semiconductors; www.nxp.com/documents/application_note/AN11127.pdf

4. Legal information

4.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

4.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product

design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

4.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.