

UM10540

NVT2001GM and NVT2002DP demo boards

Rev. 1 — 7 March 2012

User manual

Document information

Info	Content
Keywords	NVT, voltage translator, level translator, level shift, passive voltage translator, passive level translator, passive level shift, I2C-bus, SMBus, SPI, NVT2001, NVT2002
Abstract	NXP Voltage Translators (NVT) are used in bidirectional signaling voltage level translation applications for I/O buses with incompatible logic levels. The NVT2001 and NVT2002 are single- and dual-channel voltage translators, operational from 1.0 V to 3.6 V at $V_{CC(A)}$ (low voltage side) and 1.8 V to 5.5 V at $V_{CC(B)}$ (high voltage side) without direction control for open-drain or push-pull I/O devices.



Revision history

Rev	Date	Description
v.1	20120307	user manual; initial release

Contact information

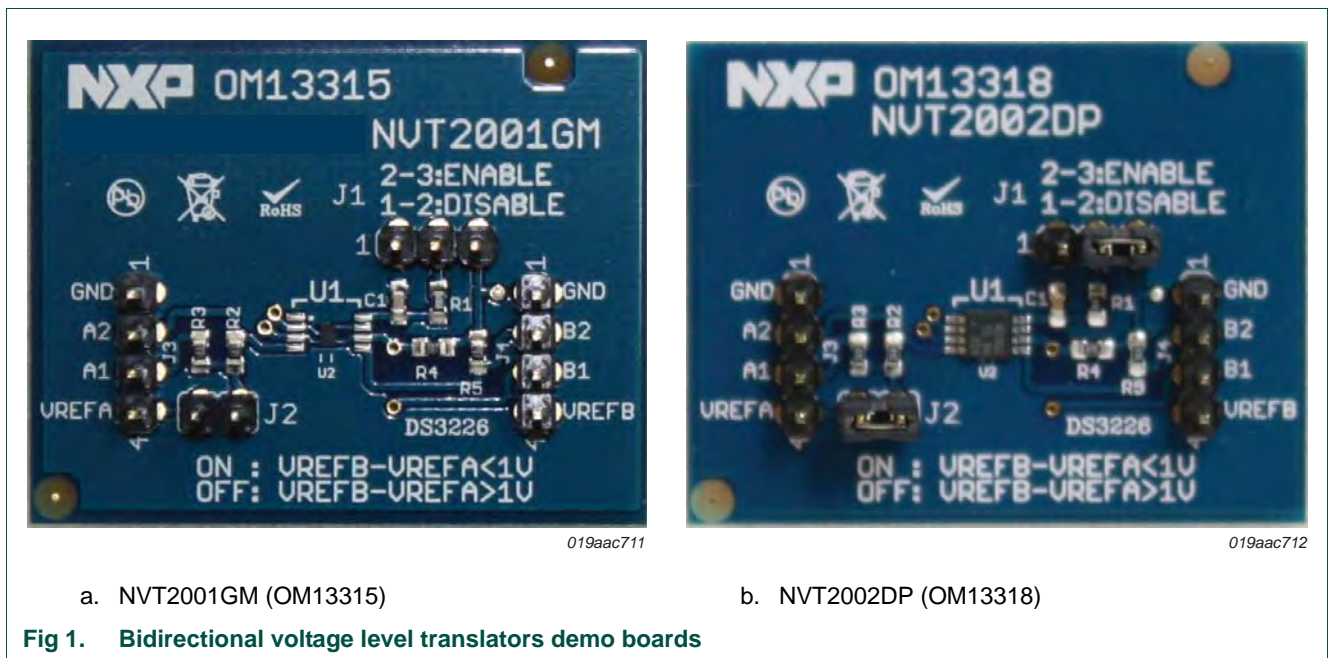
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1. Introduction

The NVT2001GM (OM13315) and NVT2002DP (OM13318) demo boards are designed to evaluate the NXP 1-channel or 2-channel bidirectional voltage level translators. The demo boards interface between device I/Os operating at different voltage levels. Since the NVT2001GM and NVT2002DP devices are passive devices, pull-up resistors may be needed depending on the I/O interface type (totem pole or open-drain), difference in translation voltage, and the translation direction (high to low voltage, low to high voltage, or bidirectional). The NVT2001GM and NVT2002DP devices allow translations between any voltages from 1.0 V to 5.5 V.

Please refer to NVT2001/NVT2002 data sheet ([Ref. 1](#)) and application note AN11127 ([Ref. 2](#)) for more detailed information.



2.2 Jumper and header functions

The functions of the jumpers and headers on these demo boards are shown in [Table 1](#).

Table 1. Header descriptions for NVT2001GM (OM13315) and NVT2002DP (OM13318) demo boards

Jumper/header	Function	Notes
J1 (3-pin)	Device switch enable or disable control	Short pins 2 and 3 to enable the NVT2001GM or NVT2002DP device (default). When pins 1 and 2 are shorted, the device is disabled.
J2 (2-pin)	Connects 10 kΩ pull-up resistors to VREFA on low voltage side for VREFB – VREFA < 1 V	Short pins 1 and 2 to connect 10 kΩ pull-up resistors to VREFA on low voltage side (default). Remark: Pins 1 and 2 must be open and 10 kΩ pull-up resistors must be removed when VREFB – VREFA ≥ 1 V.
J3 (4-pin)	Low voltage VREFA, GND and An I/O signal connect pins	Pin 1 = VREFA: low voltage power. Pin 4 = GND: low voltage ground. A1 is low voltage signal for NVT2001GM. A[1:2] are low voltage signals for NVT2002DP.
J4 (4-pin)	High voltage VREFB, GND and Bn I/O signal connect pins	Pin 1 = VREFB: high voltage power. Pin 4 = GND: high voltage ground. B1 is high voltage signal for NVT2001GM. B[1:2] are high voltage signals for NVT2002DP.

3. Abbreviations

Table 2. Abbreviations

Acronym	Description
I ² C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
SMBus	System Management Bus
SPI	Serial Peripheral Interface

4. References

- [1] NVT2001; NVT2002, “**Bidirectional voltage level translator for open-drain and push-pull applications**” — Product data sheet; NXP Semiconductors; www.nxp.com/documents/data_sheet/NVT2001_NVT2002.pdf
- [2] AN11127, “**Bidirectional voltage level translators NVT20xx, PCA9306, GTL2000, GTL2002, GTL2003, GTL2010**” — application note; NXP Semiconductors; www.nxp.com/documents/application_note/AN11127.pdf

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