

FEATURES

- Slew rate: 22 V/ μ s typical
- Settling time (0.01%): 1.2 μ s maximum
- Offset voltage: 200 μ V typical
- Open-loop gain: 1000 V/mV minimum
- Total harmonic distortion: 0.002% typical

APPLICATIONS

- Output amplifier for fast DACs
- Signal processing
- Instrumentation amplifiers
- Fast sample-and-holds
- Active filters
- Low distortion audio amplifiers
- Input buffer for ADCs
- Servo controllers

GENERAL DESCRIPTION

The **OP249** is a high speed, precision dual JFET op amp, similar to the popular single op amp. The **OP249** outperforms available dual amplifiers by providing superior speed with excellent dc performance. Ultrahigh open-loop gain (1 kV/mV minimum), low offset voltage, and superb gain linearity makes the **OP249** the industry's first true precision, dual high speed amplifier.

With a slew rate of 22 V/ μ s typical and a fast settling time of less than 1.2 μ s maximum to 0.01%, the **OP249** is an ideal choice for high speed bipolar DAC and ADC applications. The excellent dc performance of the **OP249** allows the full accuracy of high resolution CMOS DACs to be realized.

PIN CONFIGURATIONS

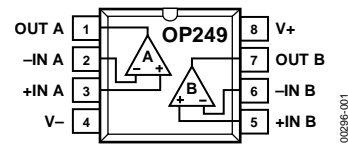


Figure 1. 8-Lead CERDIP (Q-8) and 8-Lead PDIP (N-8)

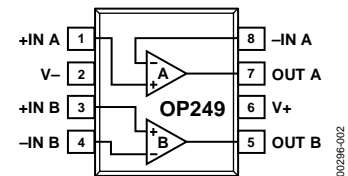


Figure 2. 8-Lead SOIC (R-8)

Symmetrical slew rate, even when driving large load, such as, 600 Ω or 200 pF of capacitance and ultralow distortion, make the **OP249** ideal for professional audio applications, active filters, high speed integrators, servo systems, and buffer amplifiers.

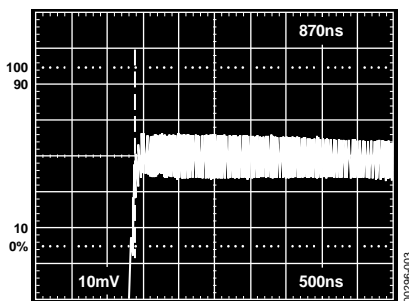


Figure 3. Fast Settling (0.01%)

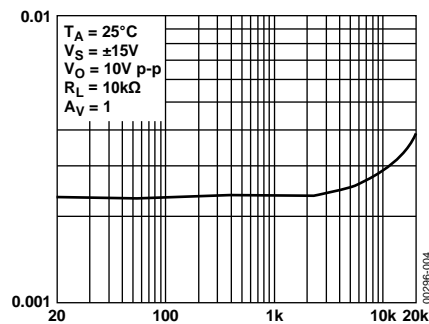


Figure 4. Low Distortion, $A_v = 1$, $R_L = 10\text{ k}\Omega$

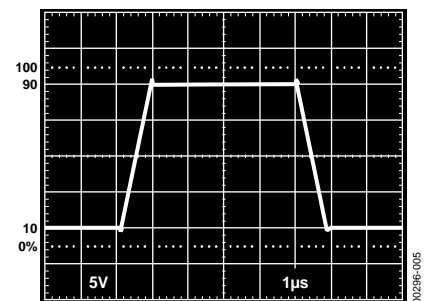


Figure 5. Excellent Output Drive, $R_L = 600\ \Omega$

Rev. I

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REVISION HISTORY

10/15—Rev. H to Rev. I

Changes to Features Section.....	1
Changes to Ordering Guide	8
Deleted Table 7.....	8

11/13—Rev. G to Rev. H

Changes to Figure 39 and Figure 41.....	13
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4/10—Rev. F to Rev. G

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Changes to Offset Voltage Parameter, Table 1	3
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Inserted OP249F Columns, Table 4	5
Changes to Discussion on Driving ADCs Section.....	16
Deleted Figure 52 and Figure 53.....	17

5/07—Rev. E to Rev. F

Updated Format.....	Universal
Changes to Table 1	3
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Changes to Figure 31	11
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Deleted OP249 SPICE Macro-Model Section	14
Deleted Figure 18; Renumbered Sequentially.....	14
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Updated Outline Dimensions	18
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9/01—Rev. D to Rev. E

Edits to Features and Pin Connections	1
Edits to Electrical Characteristics	2, 3
Edits to Absolute Maximum Ratings, Package Type, and Ordering Guide.....	4
Deleted Wafer Test Limits and Dice Characteristics Section	5
Edits to Typical Performance Characteristics.....	8
Edits to Macro-Model Figure.....	15
Edits to Outline Dimensions.....	17

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	OP249A			OP249F			Unit
			Min	Typ	Max	Min	Typ	Max	
Offset Voltage	V_{OS}	$V_{CM} = 0\text{ V}$		0.2	0.75		0.2	0.9	mV
Offset Stability				1.5			1.5		$\mu\text{V}/\text{month}$
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$		30	75		30	75	pA
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$		6	25		6	25	pA
Input Voltage Range ¹	IVR			12.5			12.5		V
			± 11			± 11			V
				-12.5			-12.5		V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{ V}$	80	90		80	90		dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$		12	31.6		12	50	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{ V}$, $R_L = 2\text{ k}\Omega$	1000	1400		500	1200		V/mV
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$		12.5			12.5		V
			± 12.0			± 12.0			V
				-12.5			-12.5		V
Short-Circuit Current Limit	I_{SC}	Output shorted to ground		36			36		mA
			± 20		± 50	± 20		± 50	mA
				-33			-33		mA
Supply Current	I_{SY}	No load, $V_O = 0\text{ V}$		5.6	7.0		5.6	7.0	mA
Slew Rate	SR	$R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$	18	22		18	22		V/ μs
Gain Bandwidth Product ²	GBW		3.5	4.7		3.5	4.7		MHz
Settling Time	t_S	10 V step 0.01% ³		0.9	1.2		0.9	1.2	μs
Phase Margin	Θ_M	0 dB gain		55			55		Degrees
Differential Input Impedance	Z_{IN}			$10^{12} 6$			$10^{12} 6$		ΩpF
Open-Loop Output Resistance	R_O			35			35		Ω
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2			2		μV p-p
Voltage Noise Density	e_n	$f_o = 10\text{ Hz}$		75			75		nV/ $\sqrt{\text{Hz}}$
		$f_o = 100\text{ Hz}$		26			26		nV/ $\sqrt{\text{Hz}}$
		$f_o = 1\text{ kHz}$		17			17		nV/ $\sqrt{\text{Hz}}$
		$f_o = 10\text{ kHz}$		16			16		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f_o = 1\text{ kHz}$		0.003			0.003		pA/ $\sqrt{\text{Hz}}$
Voltage Supply Range	V_S		± 4.5	± 15	± 18	± 4.5	± 15	± 18	V

¹ Guaranteed by CMR test.

² Guaranteed by design.

³ Settling time is sample tested.

$V_s = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	OP249G			Unit
			Min	Typ	Max	
Offset Voltage	V_{OS}	$V_{CM} = 0\text{ V}$		0.4	2.0	mV
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$		40	75	pA
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$		10	25	pA
Input Voltage Range ¹	IVR			12.5		V
			± 11			V
				-12.0		V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{ V}$	76	90		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$		12	50	$\mu\text{V/V}$
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{ V}$; $R_L = 2\text{ k}\Omega$	500	1100		V/mV
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$		12.5		V
			± 12.0			V
				-12.5		V
Short-Circuit Current Limit	I_{SC}	Output shorted to ground		36		mA
			± 20		± 50	mA
				-33		mA
Supply Current	I_{SY}	No load; $V_O = 0\text{ V}$		5.6	7.0	mA
Slew Rate	SR	$R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$	18	22		V/ μs
Gain Bandwidth Product ²	GBW			4.7		MHz
Settling Time	t_S	10 V step 0.01%		0.9	1.2	μs
Phase Margin	θ_M	0 dB gain		55		Degree
Differential Input Impedance	Z_{IN}			$10^{12} \parallel 6$		$\Omega \parallel \text{pF}$
Open-Loop Output Resistance	R_O			35		Ω
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f_o = 10\text{ Hz}$		75		nV/ $\sqrt{\text{Hz}}$
		$f_o = 100\text{ Hz}$		26		nV/ $\sqrt{\text{Hz}}$
		$f_o = 1\text{ kHz}$		17		nV/ $\sqrt{\text{Hz}}$
		$f_o = 10\text{ kHz}$		16		nV/ $\sqrt{\text{Hz}}$
		$f_o = 1\text{ kHz}$		0.003		pA/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f_o = 1\text{ kHz}$		0.003		pA/ $\sqrt{\text{Hz}}$
Voltage Supply Range	V_S		± 4.5	± 15	± 18	V

¹ Guaranteed by CMR test.

² Guaranteed by design.

$V_S = \pm 15\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for A grade, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	OP249A			Unit
			Min	Typ	Max	
Offset Voltage	V_{OS}	$V_{CM} = 0\text{ V}$		0.12	1.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}	$V_{CM} = 0\text{ V}$		1	10	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ¹	I_B			4	20	nA
Input Offset Current ¹	I_{OS}			0.04	4	nA
Input Voltage Range ²	IVR			12.5		V
			± 11			V
				-12.5		V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{ V}$	76	110		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V to } \pm 18\text{ V}$		5	50	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$; $V_O = \pm 10\text{ V}$	500	1400		V/mV
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$		12.5		V
			± 12			V
				-12.5		V
Supply Current	I_{SY}	No load, $V_O = 0\text{ V}$		5.6	7.0	mA

¹ $T_A = 125^\circ\text{C}$.

² Guaranteed by CMR test.

$V_S = \pm 15\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	OP249F			OP249G			Unit
			Min	Typ	Max	Min	Typ	Max	
Offset Voltage	V_{OS}	$V_{CM} = 0\text{ V}$		0.5	1.1		1.0	3.6	mV
Offset Voltage Temperature Coefficient	TCV_{OS}	$V_{CM} = 0\text{ V}$		2.2	12		6	25	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ¹	I_B			0.3	4.0		0.5	4.5	nA
Input Offset Current ¹	I_{OS}			0.02	1.2		0.04	1.5	nA
Input Voltage Range ²	IVR			12.5			12.5		V
			± 11			± 11			V
				-12.5			-12.5		V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{ V}$	80	90		76	95		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V to } \pm 18\text{ V}$		7	100		10	100	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$; $V_O = \pm 10\text{ V}$	250	1200		250	1200		V/mV
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$		12.5			12.5		V
			± 12			± 12.0			V
				-12.5			-12.5		V
Supply Current	I_{SY}	No load, $V_O = 0\text{ V}$		5.6	7.0		5.6	7.0	mA

¹ $T_A = 85^\circ\text{C}$.

² Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter ¹	Rating
Supply Voltage	±18 V
Input Voltage ²	±18 V
Differential Input Voltage ²	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	
OP249A (Q)	−55°C to +125°C
OP249F (Q)	−40°C to +85°C
OP249G (N, R)	−40°C to +85°C
Junction Temperature Range	
OP249A (Q), OP249F (Q)	−65°C to +175°C
OP249G (N, R)	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

¹ Absolute maximum ratings apply to packaged parts, unless otherwise noted.

² For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 6. Thermal Resistance

Package Type	θ_{JA} ¹	θ_{JC}	Unit
8-Lead CERDIP (Q)	134	12	°C/W
8-Lead PDIP (N)	96	37	°C/W
8-Lead SOIC (R)	150	41	°C/W

¹ θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for device in socket for CERDIP and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

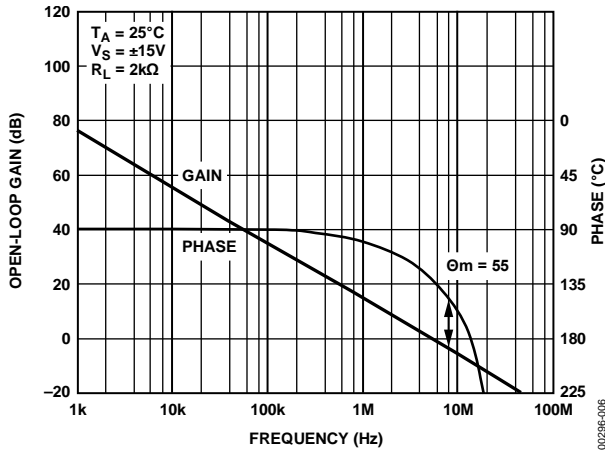


Figure 6. Open-Loop Gain, Phase vs. Frequency

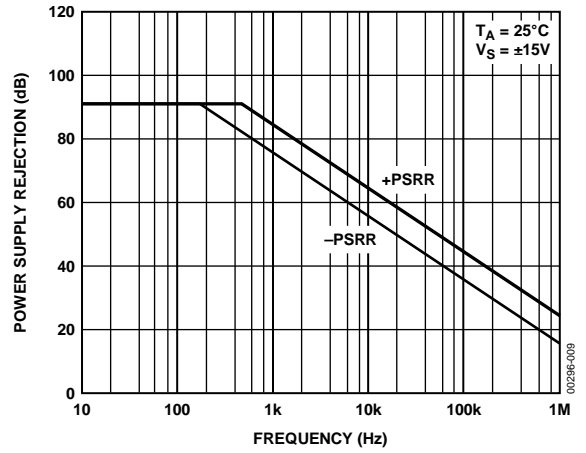


Figure 9. Power Supply Rejection vs. Frequency

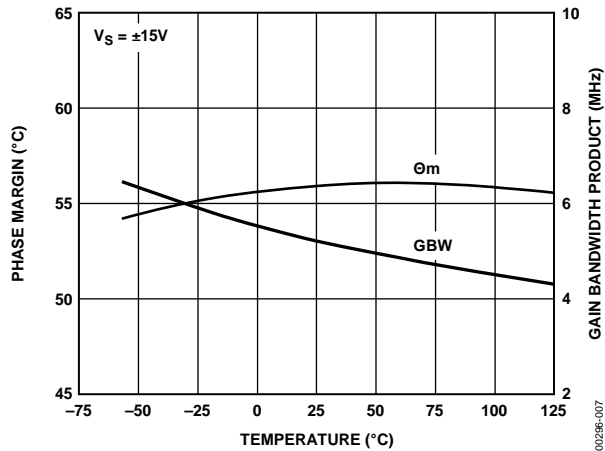


Figure 7. Phase Margin, Gain Bandwidth Product vs. Temperature

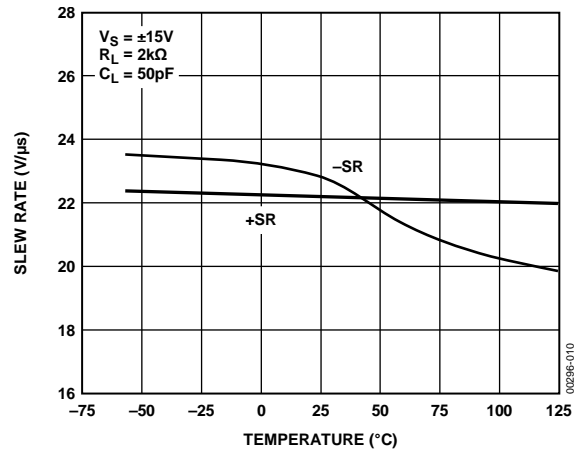


Figure 10. Slew Rate vs. Temperature

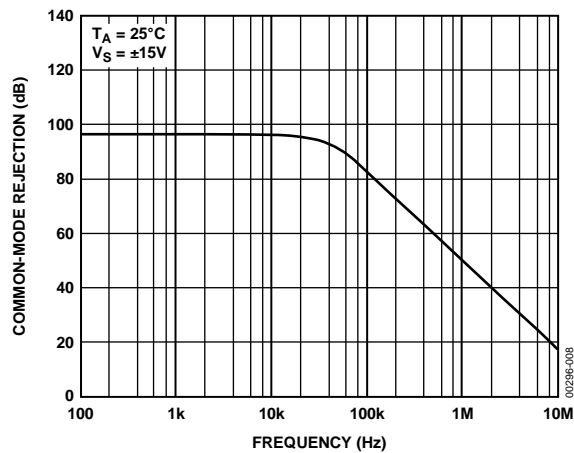


Figure 8. Common-Mode Rejection vs. Frequency

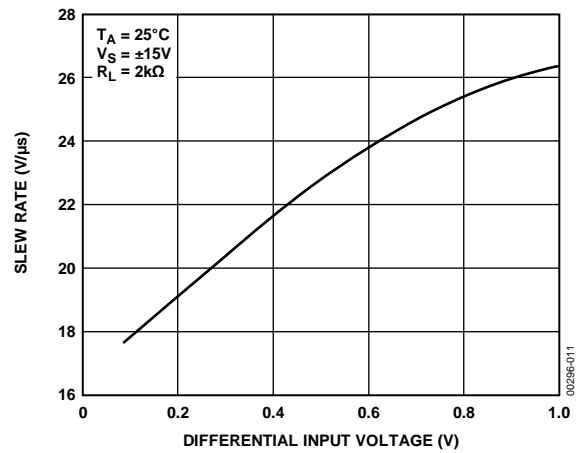


Figure 11. Slew Rate vs. Differential Input Voltage

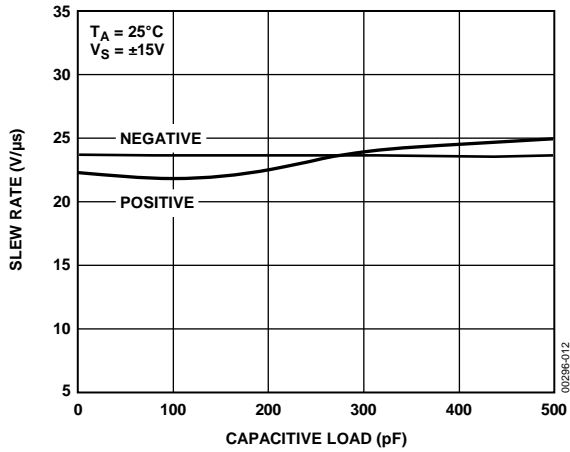


Figure 12. Slew Rate vs. Capacitive Load

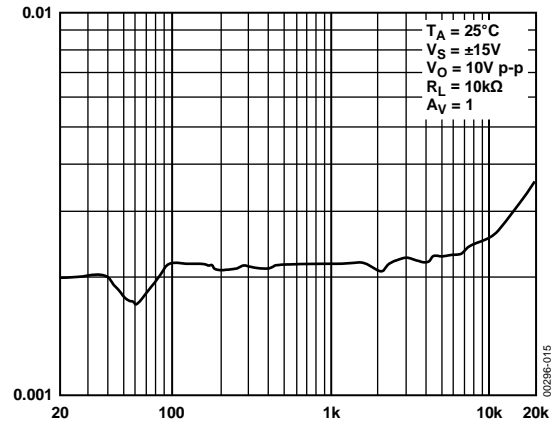


Figure 15. Distortion vs. Frequency

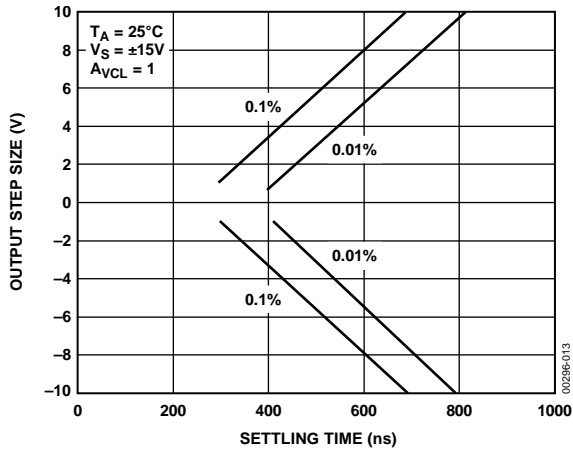


Figure 13. Step Size vs. Settling Time

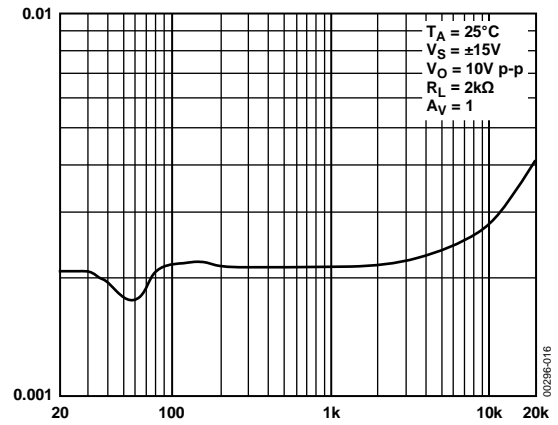


Figure 16. Distortion vs. Frequency

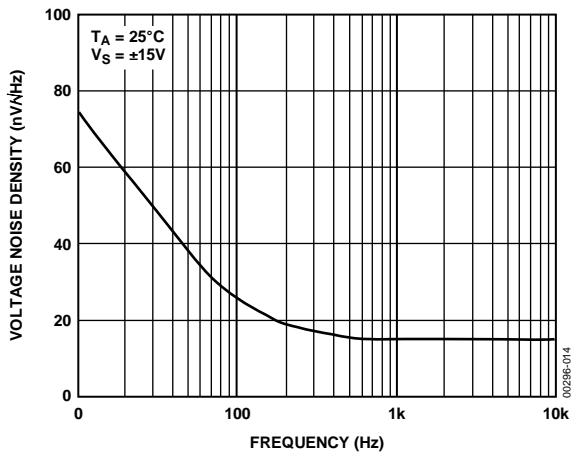


Figure 14. Voltage Noise Density vs. Frequency

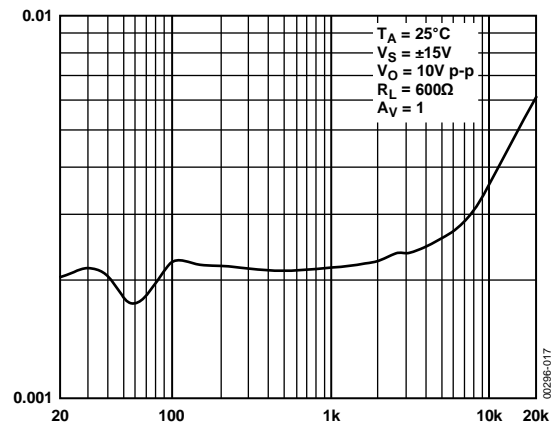


Figure 17. Distortion vs. Frequency

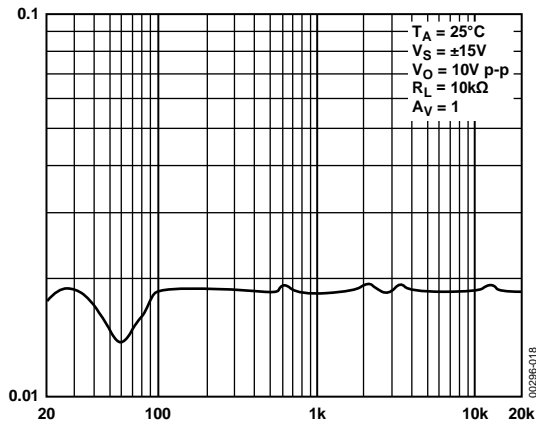
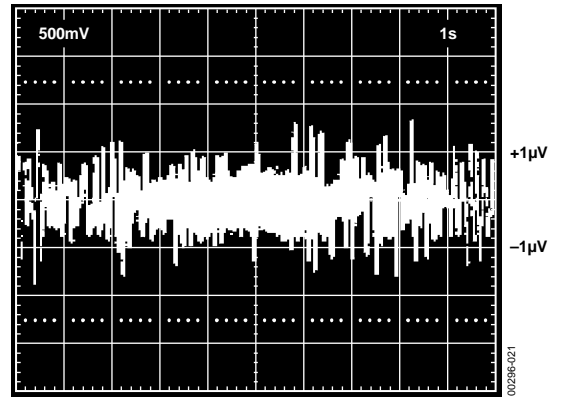


Figure 18. Distortion vs. Frequency



BANDWIDTH (0.1Hz TO 10Hz)
 $T_A = 25^\circ\text{C}, V_S = \pm 15\text{V}$

Figure 21. Low Frequency Noise

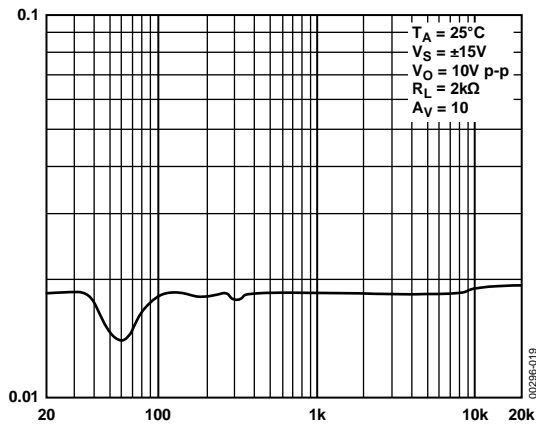


Figure 19. Distortion vs. Frequency

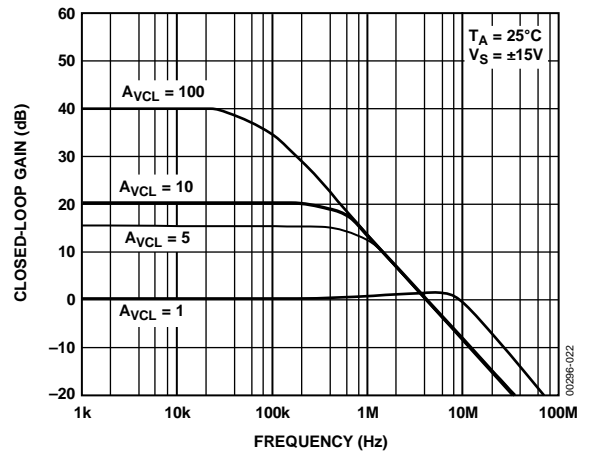


Figure 22. Closed-Loop Gain vs. Frequency

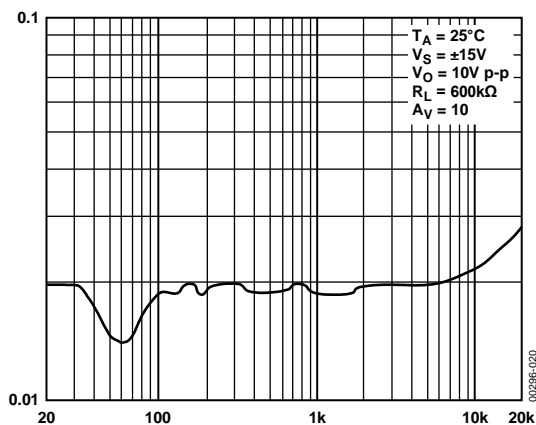


Figure 20. Distortion vs. Frequency

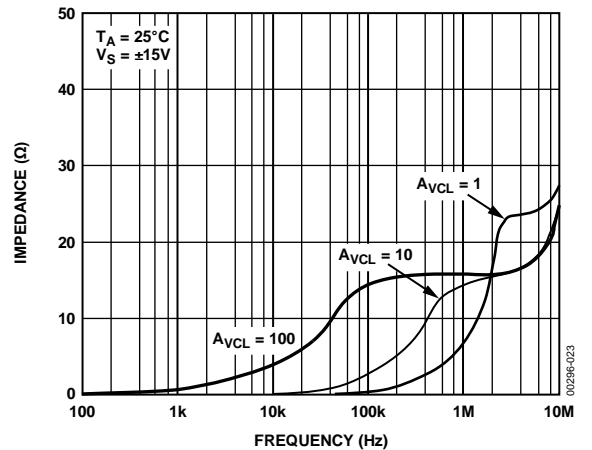


Figure 23. Closed-Loop Output Impedance vs. Frequency

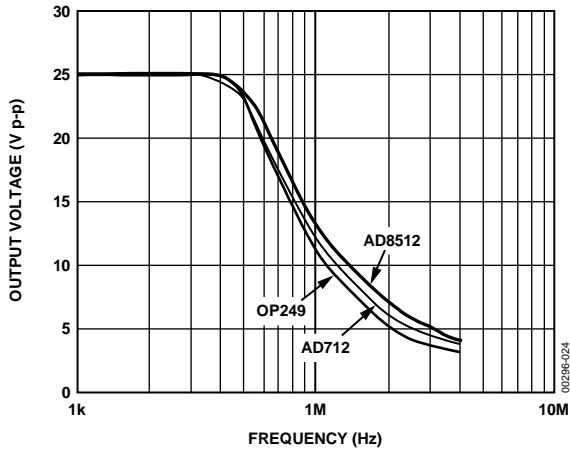


Figure 24. Output Voltage vs. Frequency

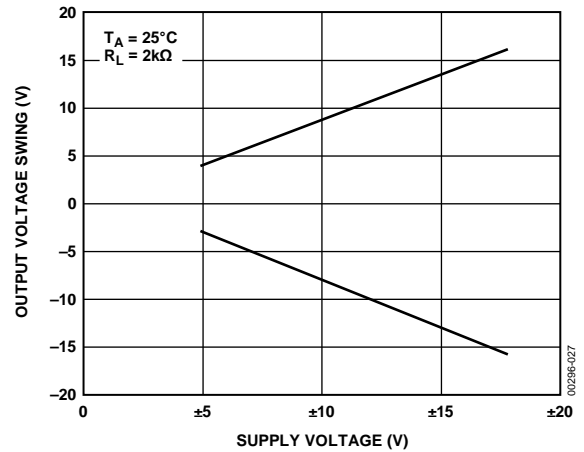


Figure 27. Output Voltage Swing vs. Supply Voltage

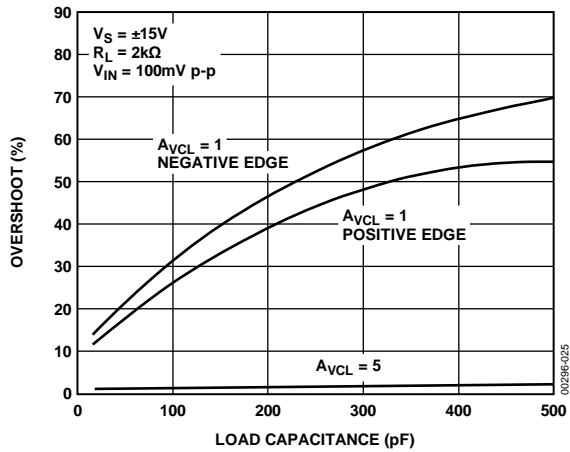


Figure 25. Small Overshoot vs. Load Capacitance

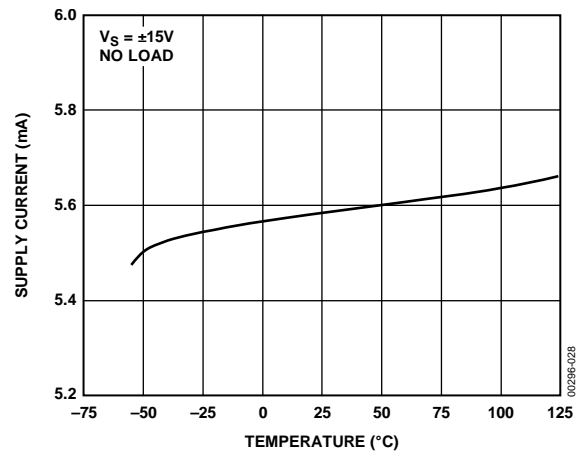


Figure 28. Supply Current vs. Temperature

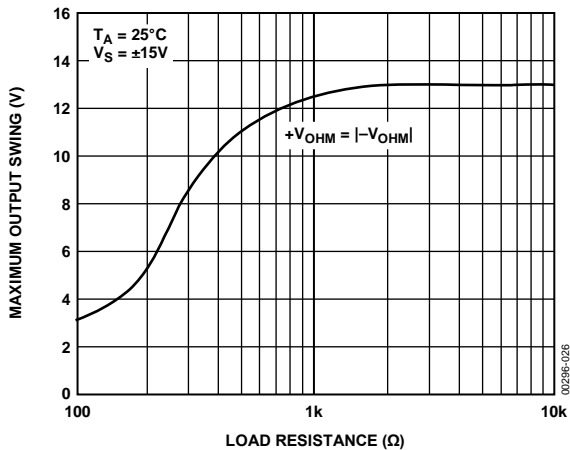


Figure 26. Maximum Output Voltage Swing vs. Load Resistance

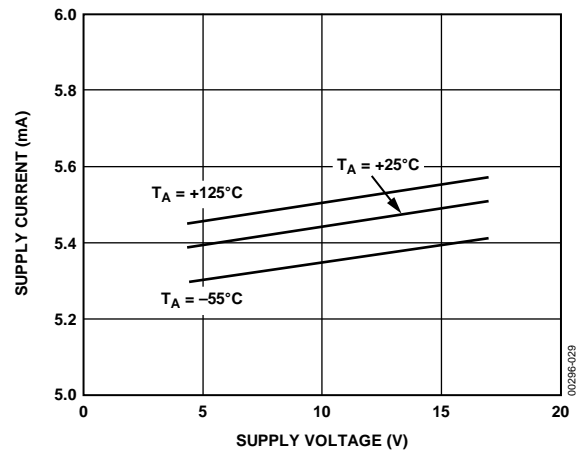


Figure 29. Supply Current vs. Supply Voltage

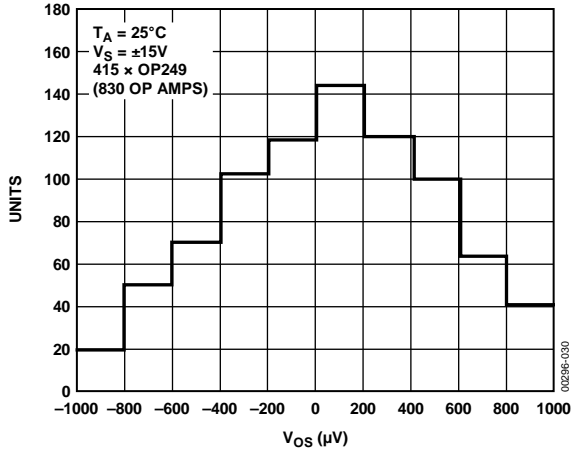


Figure 30. V_{OS} Distribution (N-8)

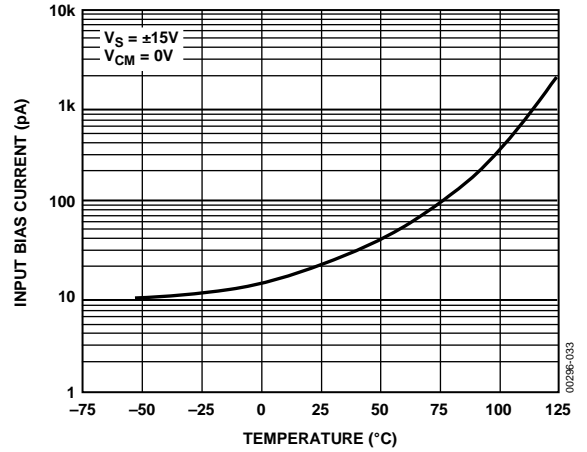


Figure 33. Input Bias Current vs. Temperature

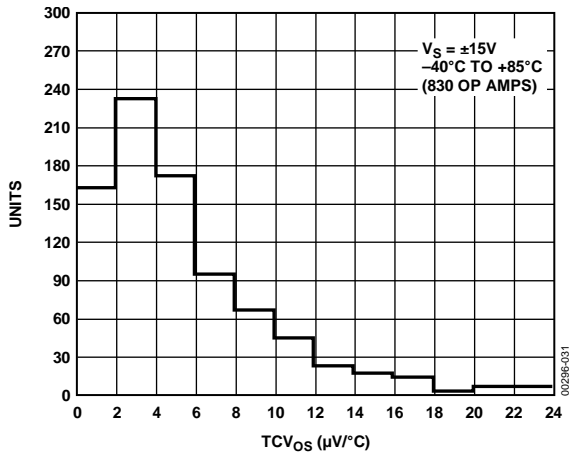


Figure 31. TCV_{OS} Distribution (N-8)

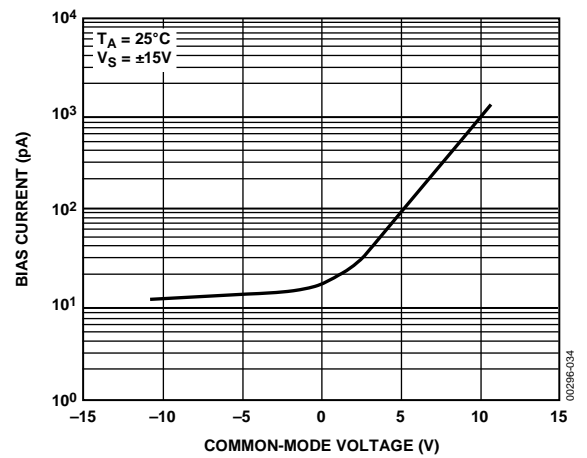


Figure 34. Bias Current vs. Common-Mode Voltage

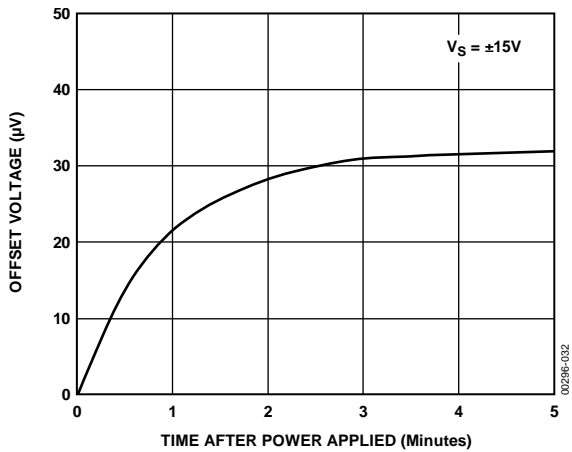


Figure 32. Offset Voltage Warm-Up Drift

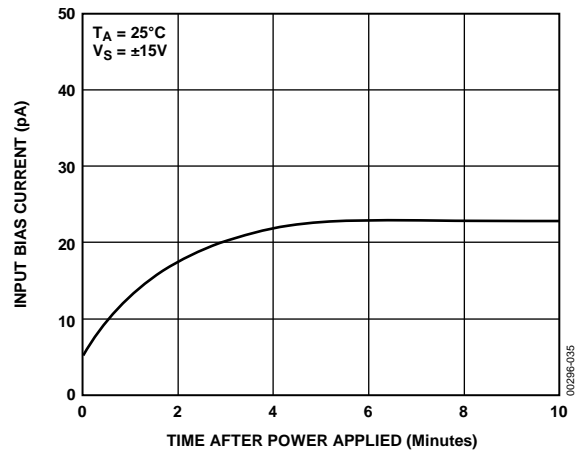


Figure 35. Bias Current Warm-Up Drift

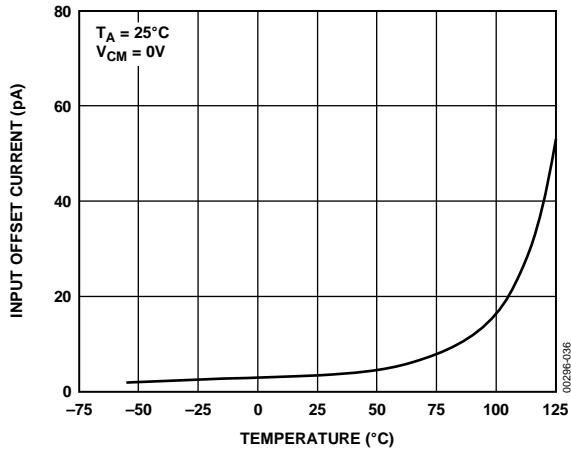


Figure 36. Input Offset Current vs. Temperature

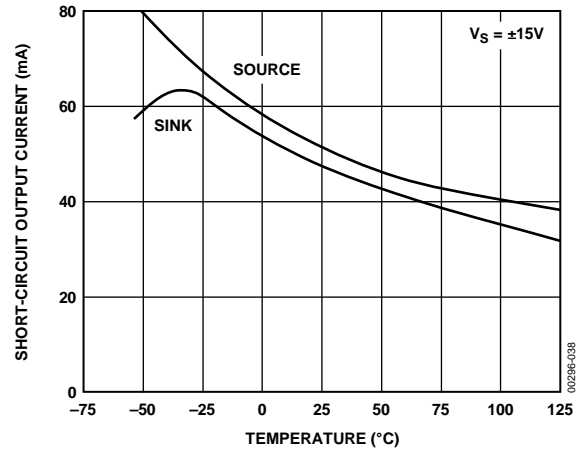


Figure 38. Short-Circuit Output Current vs. Junction Temperature

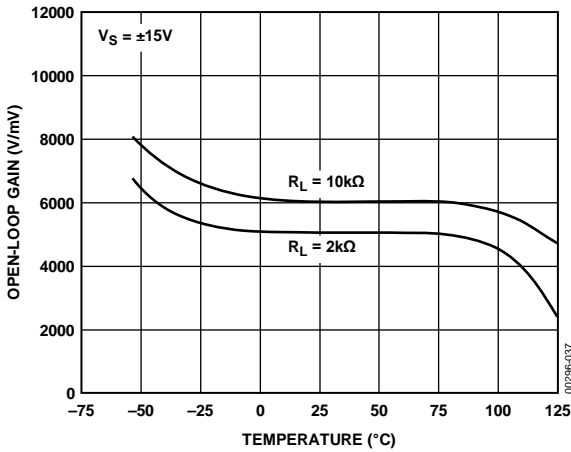


Figure 37. Open-Loop Gain vs. Temperature

APPLICATIONS INFORMATION

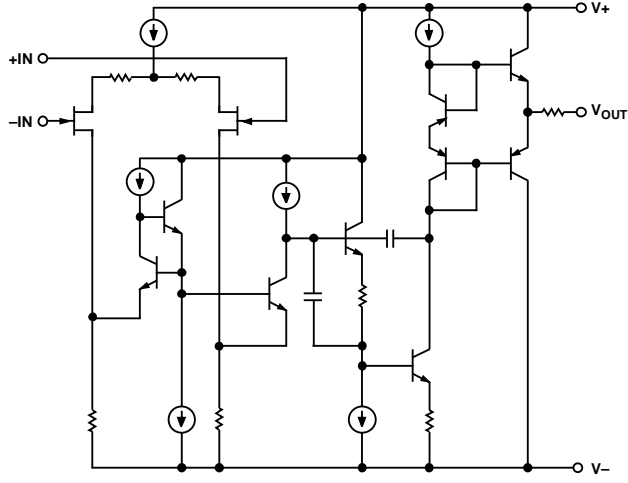


Figure 39. Simplified Schematic (1/2 OP249)

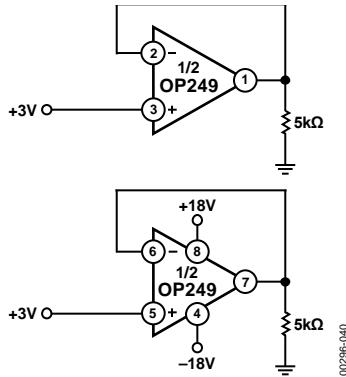
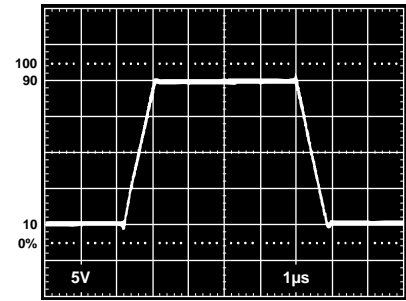


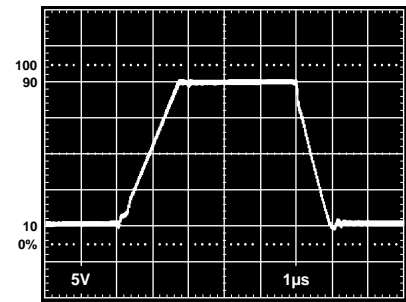
Figure 40. Burn-In Circuit

The OP249 represents a reliable JFET amplifier design, featuring an excellent combination of dc precision and high speed. A rugged output stage provides the ability to drive a 600 Ω load and still maintain a clean ac response. The OP249 features a large signal response that is more linear and symmetric than previously available JFET input amplifiers. Figure 41 compares the large signal response of the OP249 to other industry-standard dual JFET amplifiers.

Typically, the slewing performance of the JFET amplifier is specified as a number of V/μs. There is no discussion on the quality, that is, linearity and symmetry of the slewing response.



A) OP249



B) LT1057

Figure 41. Large-Signal Transient Response, $A_V = 1$, $V_{IN} = 20\text{ V p-p}$, $Z_L = 2\text{ k}\Omega // 200\text{ pF}$, $V_S = \pm 15\text{ V}$

The OP249 was carefully designed to provide symmetrically matched slew characteristics in both the negative and positive directions, even when driving a large output load.

The slewing limitation of the amplifier determines the maximum frequency at which a sinusoidal output can be obtained without significant distortion. However, it is important to note that the nonsymmetric slewing typical of previously available JFET amplifiers adds a higher series of harmonic energy content to the resulting response—and an additional dc output component. Examples of potential problems of nonsymmetric slewing behavior can be in audio amplifier applications, where a natural low distortion sound quality is desired and in servo or signal processing systems where a net dc offset cannot be tolerated. The linear and symmetric slewing feature of the OP249 makes it an ideal choice for applications that exceed the full power bandwidth range of the amplifier.

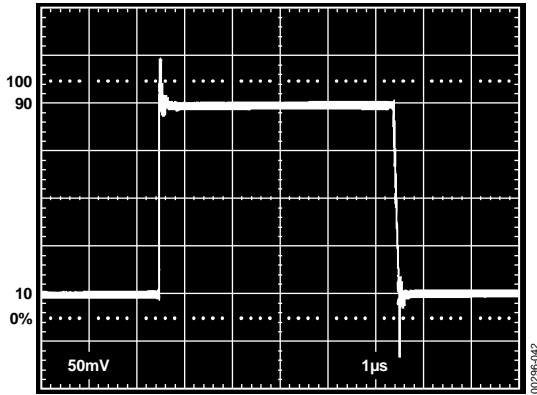


Figure 42. Small-Signal Transient Response, $A_v = 1$, $Z_L = 2\text{ k}\Omega \parallel 100\text{ pF}$, No Compensation, $V_S = \pm 15\text{ V}$

As with most JFET input amplifiers, the output of the OP249 can undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion does not damage the amplifier, nor does it cause an internal latch-up condition.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier. A 0.1 μF and a 10 μF capacitor should be placed between each supply pin and ground.

OPEN-LOOP GAIN LINEARITY

The OP249 has both an extremely high open-loop gain of 1 kV/mV minimum and constant gain linearity, which enhances its dc precision and provides superb accuracy in high closed-loop gain applications. Figure 43 illustrates the typical open-loop gain linearity—high gain accuracy is assured, even when driving a 600 Ω load.

OFFSET VOLTAGE ADJUSTMENT

The inherent low offset voltage of the OP249 makes offset adjustments unnecessary in most applications. However, where a lower offset error is required, balancing can be performed with simple external circuitry, as shown in Figure 44 and Figure 45.

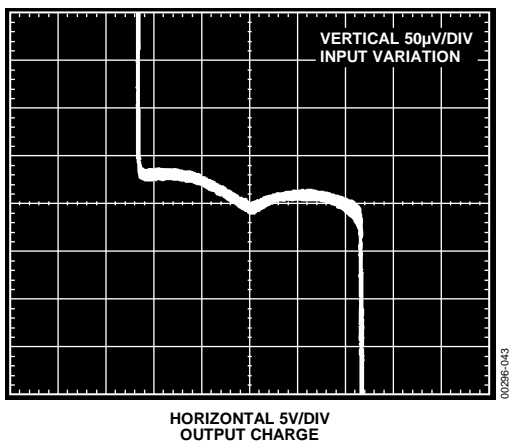


Figure 43. Open-Loop Gain Linearity; Variation in Open-Loop Gain Results in Errors in High Closed-Loop Gain Circuits; $R_L = 600\ \Omega$, $V_S = \pm 15\text{ V}$

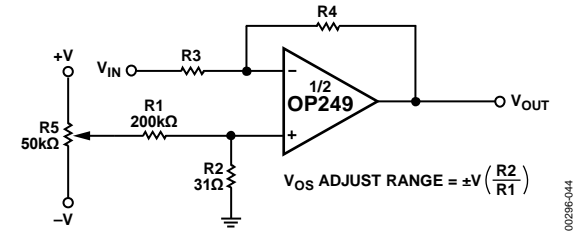


Figure 44. Offset Adjustment for Inverting Amplifier Configuration

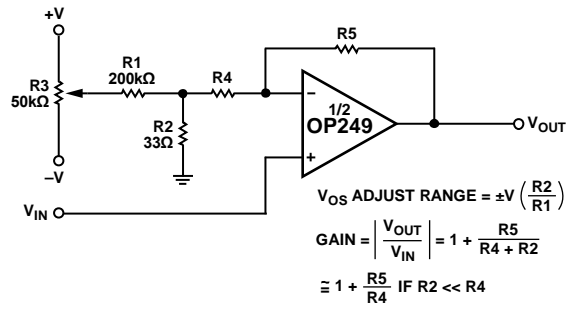


Figure 45. Offset Adjustment for Noninverting Amplifier Configuration

In Figure 44, the offset adjustment is made by supplying a small voltage at the noninverting input of the amplifier. Resistors R1 and R2 attenuate the potentiometer voltage, providing a $\pm 2.5\text{ mV}$ (with $V_S = \pm 15\text{ V}$) adjustment range, referred to the input.

Figure 45 shows the offset adjustment for the noninverting amplifier configuration, also providing a $\pm 2.5\text{ mV}$ adjustment range. As shown in the equations in Figure 45, if R4 is not much greater than R2, a resulting closed-loop gain error must be accounted for.

SETTLING TIME

The settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. The error bands on the output are 5 mV and 0.5 mV, respectively, for 0.1% and 0.01% accuracy.

Figure 46 shows the settling time of the OP249, which is typically 870 ns. Moreover, problems in settling response, such as thermal tails and long-term ringing, are nonexistent.

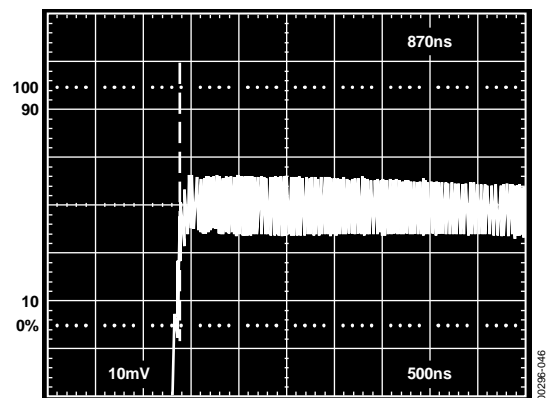


Figure 46. Settling Characteristics of the OP249 to 0.01%

DAC OUTPUT AMPLIFIER

Unity-gain stability, a low offset voltage of 300 μV typical, and a fast settling time of 870 ns to 0.01%, makes the OP249 an ideal amplifier for fast DACs.

For CMOS DAC applications, the low offset voltage of the OP249 results in excellent linearity performance. CMOS DACs, such as the PM7545, typically have a code-dependent output resistance variation between 11 k Ω and 33 k Ω . The change in output resistance, in conjunction with the 11 k Ω feedback resistor, results in a noise gain change, which causes variations in the offset error, increasing linearity errors. The OP249 features low offset voltage error, minimizing this effect and maintaining 12-bit linearity performance over the full-scale range of the converter.

Because the DAC output capacitance appears at the inputs of the op amp, it is essential that the amplifier be adequately compensated. Compensation increases the phase margin and ensures an optimal overall settling response. The required lead compensation is achieved with Capacitor C in Figure 48.

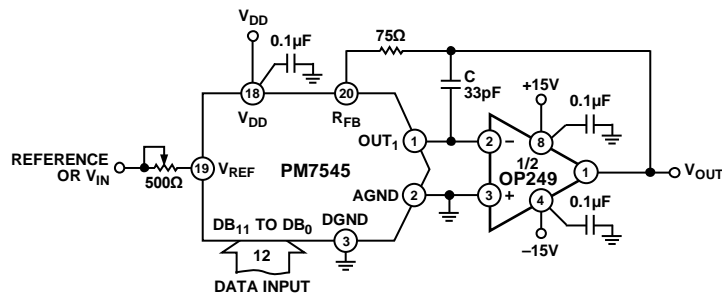


Figure 47. Fast Settling and Low Offset Error of the OP249 Enhances CMOS DAC Performance—Unipolar Operation

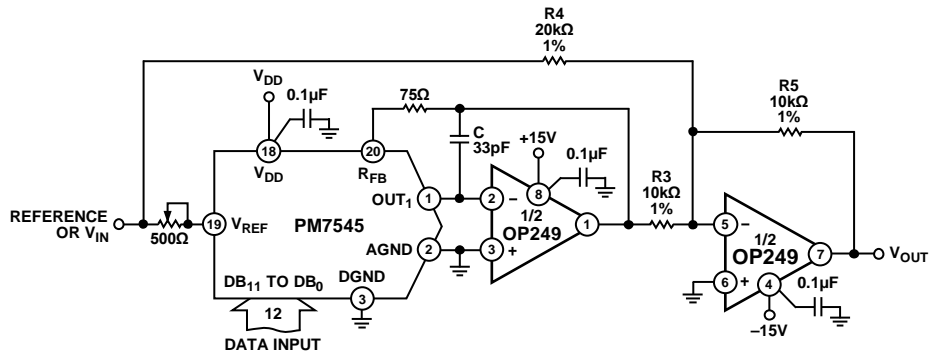


Figure 48. Fast Settling and Low Offset Error of the OP249 Enhances CMOS DAC Performance—Bipolar Operation

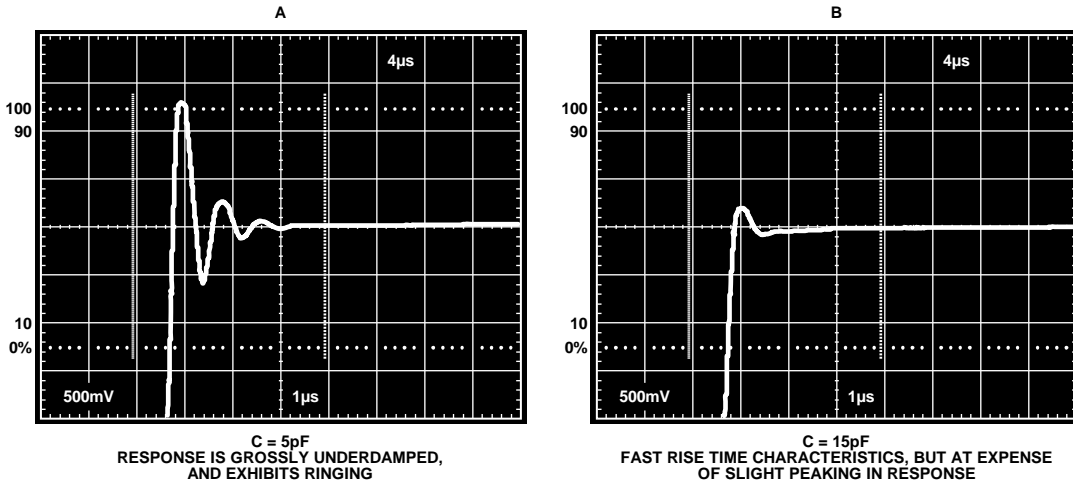


Figure 49. Effect of Altering Compensation from Circuit in Figure 47—PM7545 CMOS DAC with 1/2 OP249, Unipolar Operation; Critically Damped Response Is Obtained with $C \approx 33 \text{ pF}$

Figure 49 illustrates the effect of altering the compensation on the output response of the circuit in Figure 47. Compensation is required to address the combined effect of the output capacitance of the DAC, the input capacitance of the op amp, and any stray capacitance. Slight adjustments to the compensation capacitor may be required to optimize settling response for any given application.

The settling time of the combination of the current output DAC and the op amp can be approximated by

$$t_{s \text{ TOTAL}} = \sqrt{(t_{s \text{ DAC}})^2 + (t_{s \text{ AMP}})^2}$$

The actual overall settling time is affected by the noise gain of the amplifier, the applied compensation, and the equivalent input capacitance at the input of the amplifier.

DISCUSSION ON DRIVING ADCs

Settling characteristics of op amps also include the ability of the amplifier to recover, that is, settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR-type ADC. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output settles before the converter makes a comparison decision, which prevents linearity errors or missing codes.

Figure 50 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing current generator provides the transient change in output load current of 1 mA.

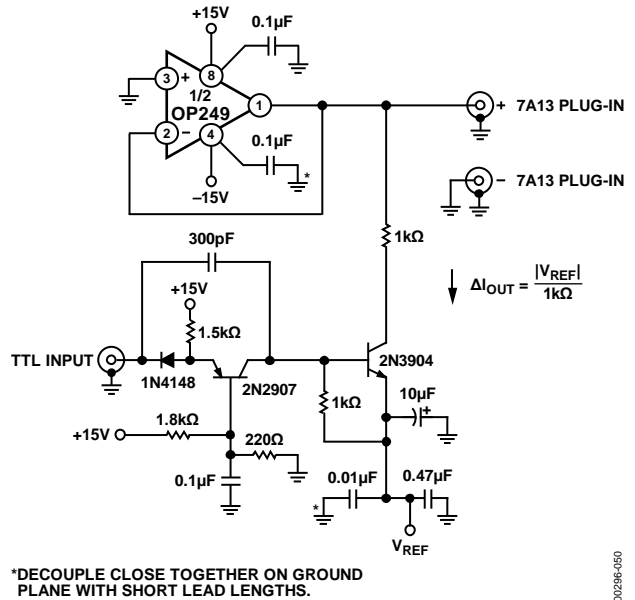


Figure 50. Transient Output Impedance Test Fixture

As seen in Figure 51, the OP249 has an extremely fast recovery of 247 ns (to 0.01%) for a 1 mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

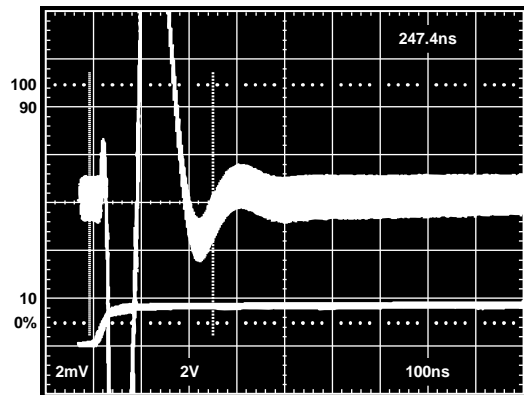
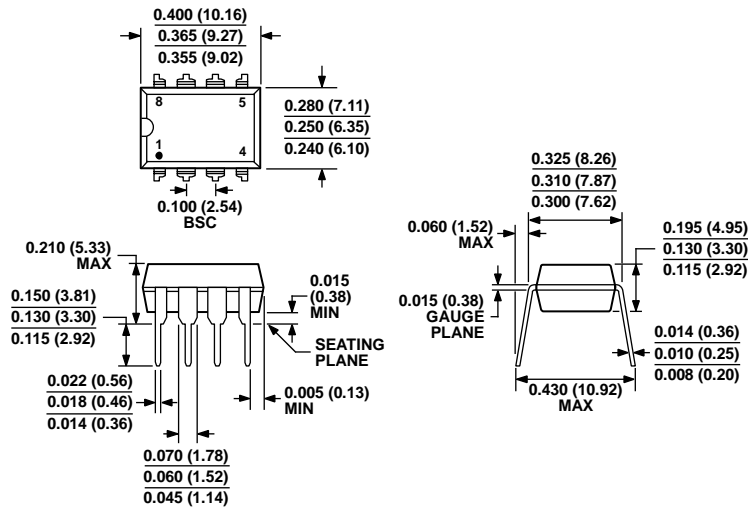


Figure 51. Transient Recovery Time of the OP249 from a 1 mA Load Transient to 0.01%

OUTLINE DIMENSIONS

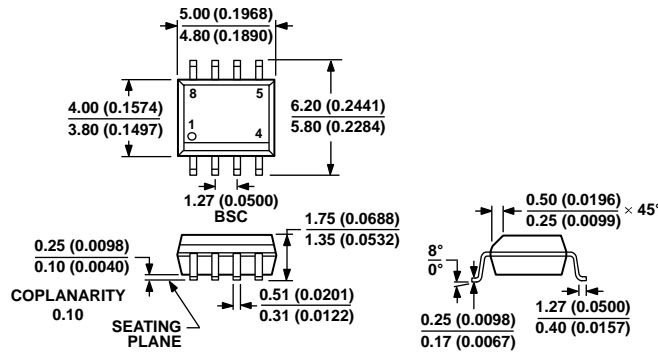


COMPLIANT TO JEDEC STANDARDS MS-001
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 52. 8-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-8)

Dimensions shown in inches and (millimeters)

070606F-A



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 53. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

012407F-A