

# DE5-Net

## FPGA Development Kit User Manual



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# Chapter 1

## *Overview*

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This chapter provides an overview of the DE5-Net Development Board and installation guide.

### **1.1 General Description**

The Terasic DE5-Net Stratix V GX FPGA Development Kit provides the ideal hardware solution for designs that demand high capacity and bandwidth memory interfacing, ultra-low latency communication, and power efficiency. With a full-height, 3/4-length form-factor package, the DE5-Net is designed for the most demanding high-end applications, empowered with the top-of-the-line Altera Stratix V GX, delivering the best system-level integration and flexibility in the industry.

The Stratix® V GX FPGA features integrated transceivers that transfer at a maximum of 12.5 Gbps, allowing the DE5-Net to be fully compliant with version 3.0 of the PCI Express standard, as well as allowing an ultra low-latency, straight connections to four external 10G SFP+ modules. Not relying on an external PHY will accelerate mainstream development of network applications enabling customers to deploy designs for a broad range of high-speed connectivity applications. For designs that demand high capacity and high speed for memory and storage, the DE5-Net delivers with two independent banks of DDR3 SO-DIMM RAM, four independent banks of QDRII+ SRAM, high-speed parallel flash memory, and four SATA ports. The feature-set of the DE5-Net fully supports all high-intensity applications such as low-latency trading, cloud computing, high-performance computing, data acquisition, network processing, and signal processing.

## 1.2 Key Features

The following hardware is implemented on the DE5-Net board:

### ■ FPGA

- Altera Stratix® V GX FPGA (5SGXEA7N2F45C2)

### ■ FPGA Configuration

- On-Board USB Blaster II or JTAG header for FPGA programming
- Fast passive parallel (FPPx32) configuration via MAX II CPLD and flash memory

### ■ General user input/output:

- 10 LEDs
- 4 push-buttons
- 4 slide switches
- 2 seven-segment displays

### ■ Clock System

- 50MHz Oscillator
- Programmable oscillators Si570, CDCM61001 and CDCM61004
- One SMA connector for external clock input
- One SMA connector for clock output

### ■ Memory

- DDR3 SO-DIMM SDRAM
- QDRII+ SRAM
- FLASH

### ■ Communication Ports

- Four SFP+ connectors
- Two Serial ATA host ports
- Two Serial ATA device ports
- PCI Express (PCIe) x8 edge connector
- One RS422 transceiver with RJ45 connector

## ■ System Monitor and Control

- Temperature sensor
- Fan control

## ■ Power

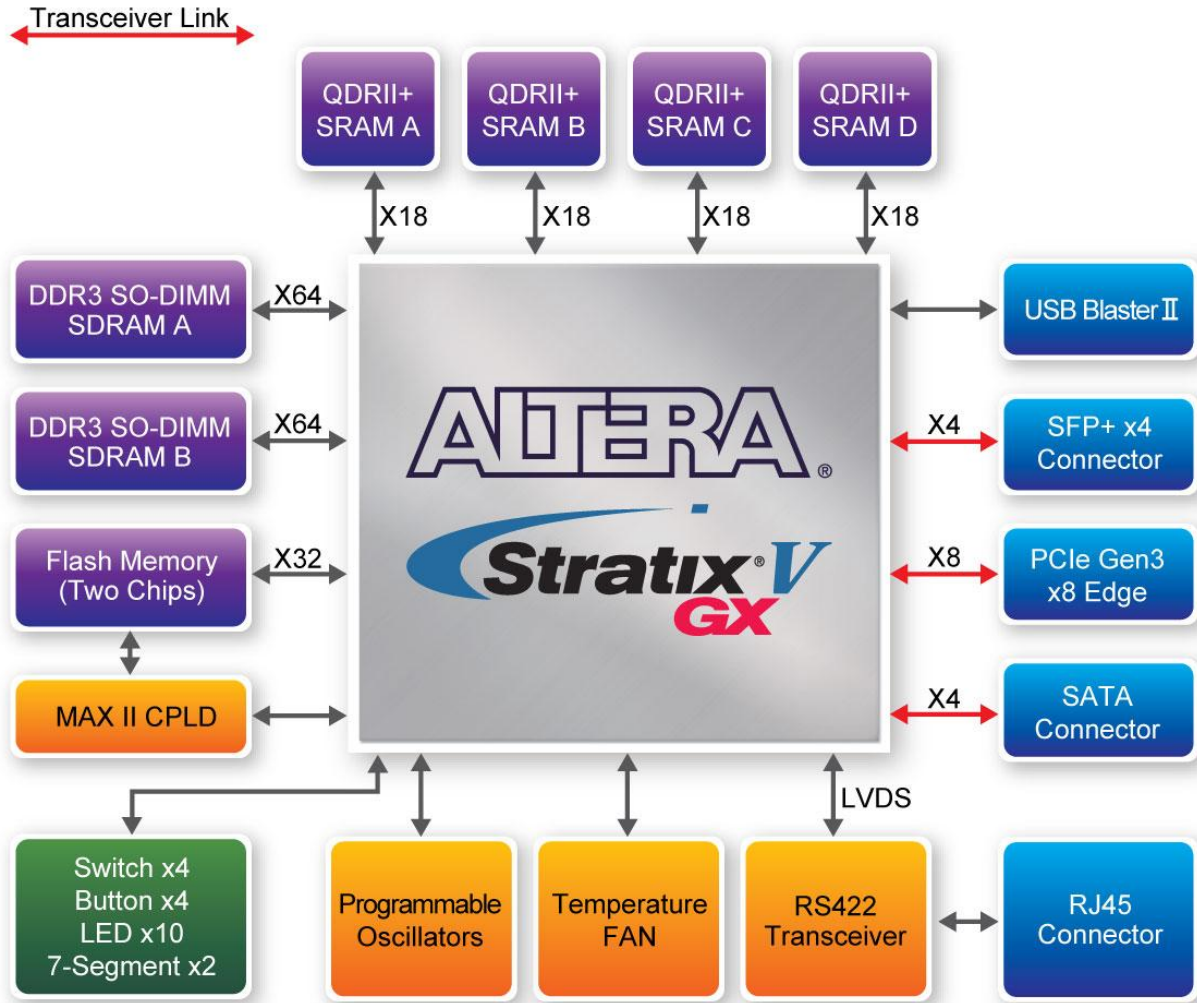
- PCI Express 6-pin power connector, 12V DC Input
- PCI Express edge connector power

## ■ Mechanical Specification

- PCI Express full-height and 3/4-length

# 1.3 Block Diagram

**Figure 1-1** shows the block diagram of the DE5-Net board. To provide maximum flexibility for the users, all key components are connected with the Stratix V GX FPGA device. Thus, users can configure the FPGA to implement any system design.



**Figure 1-1 Block diagram of the DE5-Net board**

Below is more detailed information regarding the blocks in **Figure 1-1**.

## Stratix V GX FPGA

- 5SGXEA7N2F45C2
- 622,000 logic elements (LEs)
- 50-Mbits embedded memory
- 48 transceivers (12.5Gbps)
- 512 18-bit x 18-bit multipliers
- 256 27-bit x 27-bit DSP blocks

- 2 PCI Express hard IP blocks
- 840 user I/Os
- 210 full-duplex LVDS channels
- 28 phase locked loops (PLLs)

## **JTAG Header and FPGA Configuration**

- On-board USB Blaster II or JTAG header for use with the Quartus Prime Programmer
- MAXII CPLD EPM2210 System Controller and Fast Passive Parallel (FPP) configuration

## **Memory devices**

- 32MB QDRII+ SRAM
- Up to 8GB DDR3 SO-DIMM SDRAM
- 256MB FLASH

## **General user I/O**

- 10 user controllable LEDs
- 4 user push buttons
- 4 user slide switches
- 2 seven-segment displays

## **On-Board Clock**

- 50MHz oscillator
- Programming PLL providing clock for 10G SFP+ transceiver
- Programming PLL providing clock for SATA or 1G SFP+ transceiver

## **Four Serial ATA ports**

- SATA 3.0 standard at 6Gbps signaling rate



## **Four SFP+ ports**

- Four SFP+ connector (10 Gbps+)

## **PCI Express x8 edge connector**

- Support for PCIe Gen1/2/3
- Edge connector for PC motherboard with x8 or x16 PCI Express slot

## **Power Source**

- PCI Express 6-pin DC 12V power
- PCI Express edge connector power

## Board Components

This chapter introduces all the important components on the DE5-Net.

### 2.1 Board Overview

Figure 2-1 is the top and bottom view of the DE5-Net development board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location of the connectors and key components.

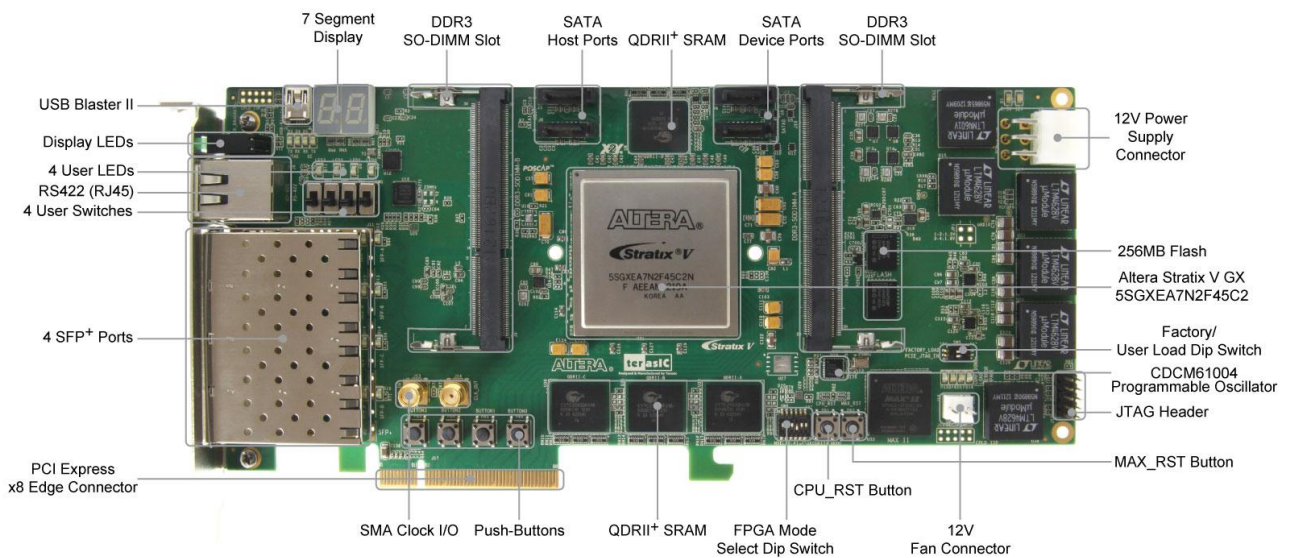


Figure 2-1 FPGA Board (Top)

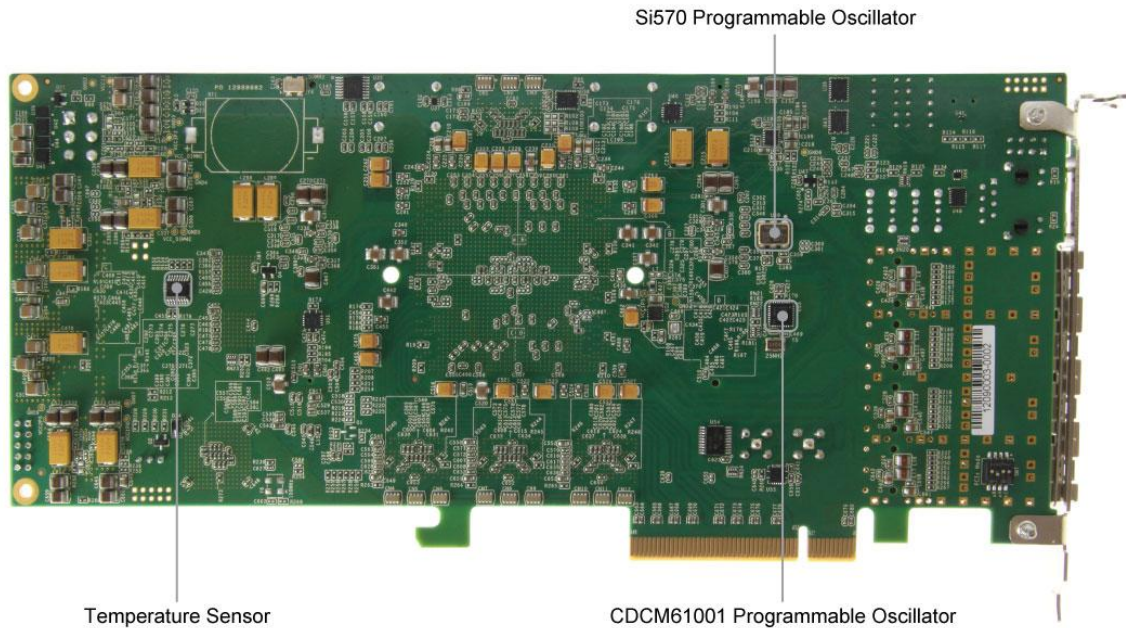


Figure 2-2 FPGA Board (Bottom)

## 2.2 Configuration, Status and Setup

### ■ Configure

The FPGA board supports two configuration methods for the Stratix V FPGA:

- Configure the FPGA using the on-board USB-Blaster II.
- Flash memory configuration of the FPGA using stored images from the flash memory on power-up.

For programming by on-board USB-Blaster II, the following procedures show how to download a configuration bit stream into the Stratix V GX FPGA:

- Make sure that power is provided to the FPGA board
- Connect your PC to the FPGA board using a mini-USB cable and make sure the USB-Blaster II driver is installed on PC.
- Launch Quartus Prime programmer and make sure the USB-Blaster II is detected.
- In Quartus Prime Programmer, add the configuration bit stream file (.sof), check the associated “Program/Configure” item, and click “Start” to start FPGA programming.

## ■ Status LED

The FPGA Board development board includes board-specific status LEDs to indicate board status. Please refer to [Table 2-1](#) for the description of the LED indicator.

**Table 2-1 Status LED**

<i>Board Reference</i>	<i>LED Name</i>	<i>Description</i>
D2	12-V Power	Illuminates when 12-V power is active.
D1	3.3-V Power	Illuminates when 3.3-V power is active.
D15	CONF DONE	Illuminates when the FPGA is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D16	Loading	Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA. Driven by the MAX II CPLD EPM2210 System Controller with the Embedded Blaster CPLD.
D17	Error	Illuminates when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.
D18	PAGE	Illuminates when FPGA is configured by the factory configuration bit stream.

## ■ Setup PCI Express Control DIP switch

The PCI Express Control DIP switch (SW7) is provided to enable or disable different configurations of the PCIe Connector. [Table 2-2](#) lists the switch controls and description.

**Table 2-2 SW3 PCIe Control DIP Switch**

<i>Board Reference</i>	<i>Signal Name</i>	<i>Description</i>	<i>Default</i>
SW7.1	PCIE_PRSENT2n_x1	On : Enable x1 presence detect Off: Disable x1 presence detect	Off
SW7.2	PCIE_PRSENT2n_x4	On : Enable x4 presence detect Off: Disable x4 presence detect	Off
SW7.3	PCIE_PRSENT2n_x8	On : Enable x8 presence detect Off: Disable x8 presence detect	On

## ■ Setup Configure Mode Control DIP switch

The Configure Mode Control DIP switch (SW6) is provided to specify the configuration mode of the FPGA. As currently only one mode is supported, please set all positions as shown in **Figure 2-3**.

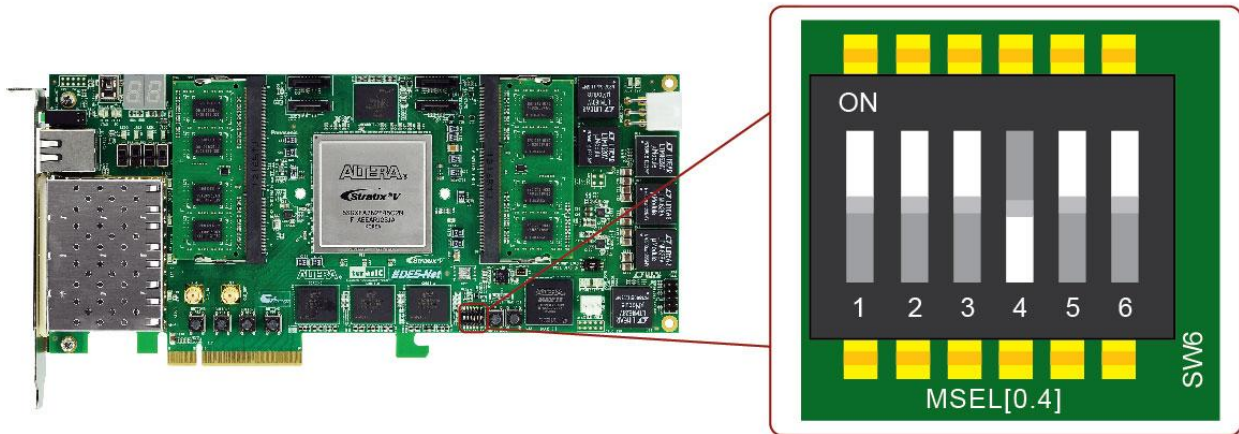


Figure 2-3 6-Position DIP switch for Configure Mode

## ■ Select Flash Image for Configuration

The Image Select DIP switch (SW5) is provided to specify the image for configuration of the FPGA. Setting Position 2 of SW5 to high (right) specifies the default factory image to be loaded, as shown in **Figure 2-4**. Setting Position 2 of SW5 to low (left) specifies the DE5-Net to load a user-defined image, as shown in **Figure 2-5**.

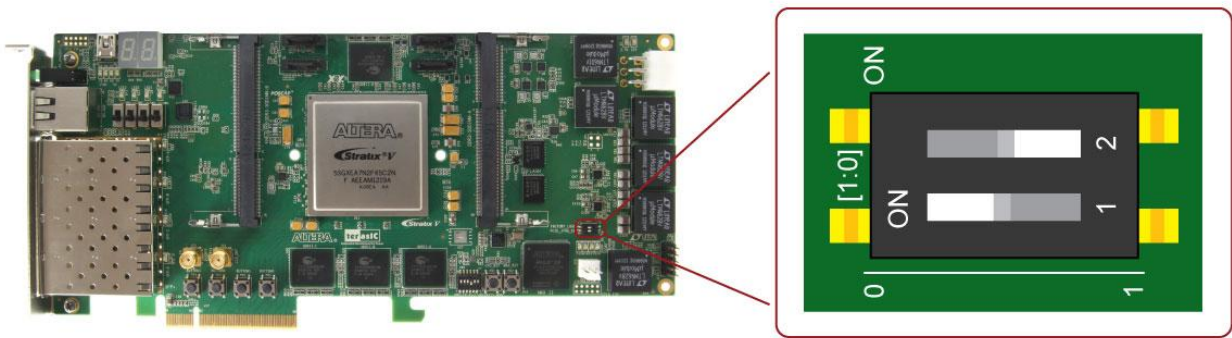


Figure 2-4 2-position DIP switch for Image Select – Factory Image Load

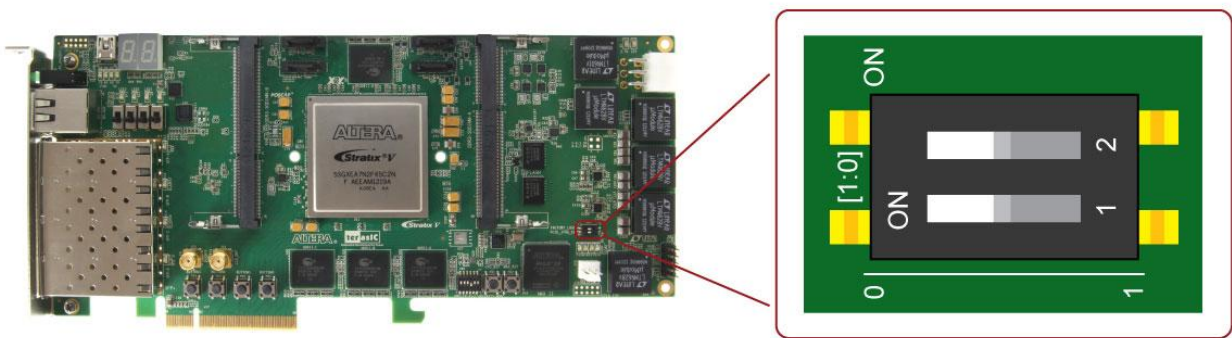


Figure 2-5 2-position DIP switch for Image Select – User Image Load

## 2.3 General User Input/Output

This section describes the user I/O interface to the FPGA.

### ■ User Defined Push-buttons

The FPGA board includes four user defined push-buttons that allow users to interact with the Stratix V GX device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. **Table 2-3** lists the board references, signal names and their corresponding Stratix V GX device pin numbers.

Table 2-3 Push-button Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix V GX Pin Number
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PB6	BUTTON0	High Logic Level when the button is not pressed	2.5-V	PIN_AK15
PB5	BUTTON1		2.5-V	PIN_AK14
PB4	BUTTON2		2.5-V	PIN_AL14
PB3	BUTTON3		2.5-V	PIN_AL15

## ■ User-Defined Slide Switch

There are four slide switches on the FPGA board to provide additional FPGA input control. When a slide switch is in the DOWN position or the UPPER position, it provides a low logic level or a high logic level to the Stratix V GX FPGA, respectively, as shown in [Figure 2-6](#).

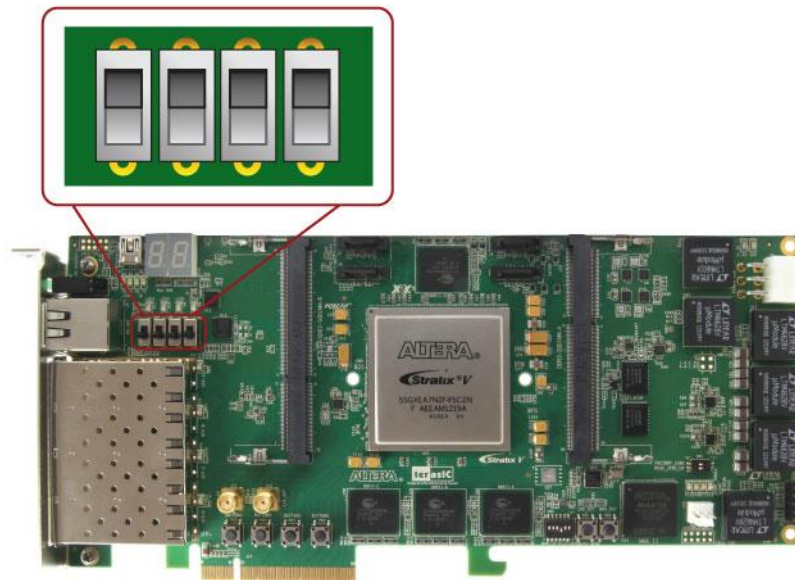


Figure 2-6 4 Slide switches

[Table 2-4](#) lists the signal names and their corresponding Stratix V GX device pin numbers.

**Table 2-4 Slide Switch Pin Assignments, Schematic Signal Names, and Functions**

<i>Board Reference</i>	<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
SW0	SW0	High logic level when SW in the UPPER position.	1.8-V	PIN_B25
SW1	SW1		1.8-V	PIN_A25
SW2	SW2		1.8-V	PIN_B23

SW3	SW3		1.8-V	PIN_A23
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## ■ User-Defined LEDs

The FPGA board consists of 10 user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix V GX device. Each LED is driven directly by the Stratix V GX FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in [Table 2-5](#).

**Table 2-5 User LEDs Pin Assignments, Schematic Signal Names, and Functions**

<i>Board Reference</i>	<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
D8	LED0	Driving a logic 0 on the I/O port turns the LED ON.	2.5-V	PIN_AW37
D9	LED1		2.5-V	PIN_AV37
D10	LED2	Driving a logic 1 on the I/O port turns the LED OFF.	2.5-V	PIN_BB36
D11	LED3		2.5-V	PIN_BB39
D7-1	LED_BRACKET0		2.5-V	PIN_AH15
D7-3	LED_BRACKET1		2.5-V	PIN_AH13
D7-5	LED_BRACKET2		2.5-V	PIN_AJ13
D7-7	LED_BRACKET3		2.5-V	PIN_AJ14
J8-10	LED_RJ45_L		2.5-V	PIN_AG15
J8-12	LED_RJ45_R		2.5-V	PIN_AG16

## ■ 7-Segment Displays

The FPGA board has two 7-segment displays. As indicated in the schematic in [Figure 2-7](#), the seven segments are connected to pins of the Stratix V GX FPGA. Applying a low or high logic level to a segment will turn it on or turn it off, respectively.

Each segment in a display is identified by an index listed from 0 to 6 with the positions given in [Figure 2-8](#). In addition, the decimal point is identified as DP. [Table 2-6](#) shows the mapping of the FPGA pin assignments to the 7-segment displays.



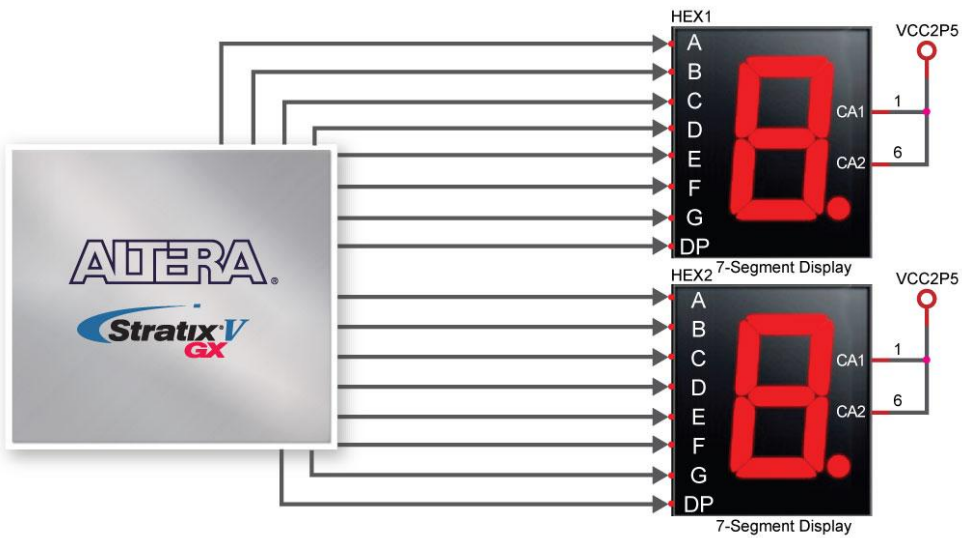


Figure 2-7 Connection between 7-segment displays and Stratix V GX FPGA



Figure 2-8 Position and index of each segment in a 7-segment display

Table 2-6 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix V GX Pin Number
HEX1	HEX1_D0	User-Defined 7-Segment Display. Driving logic 0 on the I/O port turns the 7-segment signal ON. Driving logic 1 on the I/O port turns the 7-segment signal OFF.	1.5-V	PIN_H18
HEX1	HEX1_D1		1.5-V	PIN_G16
HEX1	HEX1_D2		1.5-V	PIN_F16
HEX1	HEX1_D3		1.5-V	PIN_A7
HEX1	HEX1_D4		1.5-V	PIN_B7
HEX1	HEX1_D5		1.5-V	PIN_C9
HEX1	HEX1_D6		1.5-V	PIN_D10

HEX1	HEX1_DP		1.5-V	PIN_E9
HEX0	HEX0_D0		1.5-V	PIN_G8
HEX0	HEX0_D1		1.5-V	PIN_H8
HEX0	HEX0_D2		1.5-V	PIN_J9
HEX0	HEX0_D3		1.5-V	PIN_K10
HEX0	HEX0_D4		1.5-V	PIN_K8
HEX0	HEX0_D5		1.5-V	PIN_K9
HEX0	HEX0_D6		1.5-V	PIN_N8
HEX0	HEX0_DP		1.5-V	PIN_P8

## 2.4 Temperature Sensor and Fan Control

The FPGA board is equipped with a temperature sensor, MAX1619, which provides temperature sensing and over-temperature alert. These functions are accomplished by connecting the temperature sensor to the internal temperature sensing diode of the Stratix V GX device. The temperature status and alarm threshold registers of the temperature sensor can be programmed by a two-wire SMBus, which is connected to the Stratix V GX FPGA. In addition, the 7-bit POR slave address for this sensor is set to '0011000b'.

An optional 3-pin +12V fan located on J15 of the FPGA board is intended to reduce the temperature of the FPGA. Users can control the fan to turn on/off depending on the measured system temperature. The FAN is turned on when the FAN\_CTRL pin is driven to a high logic level.

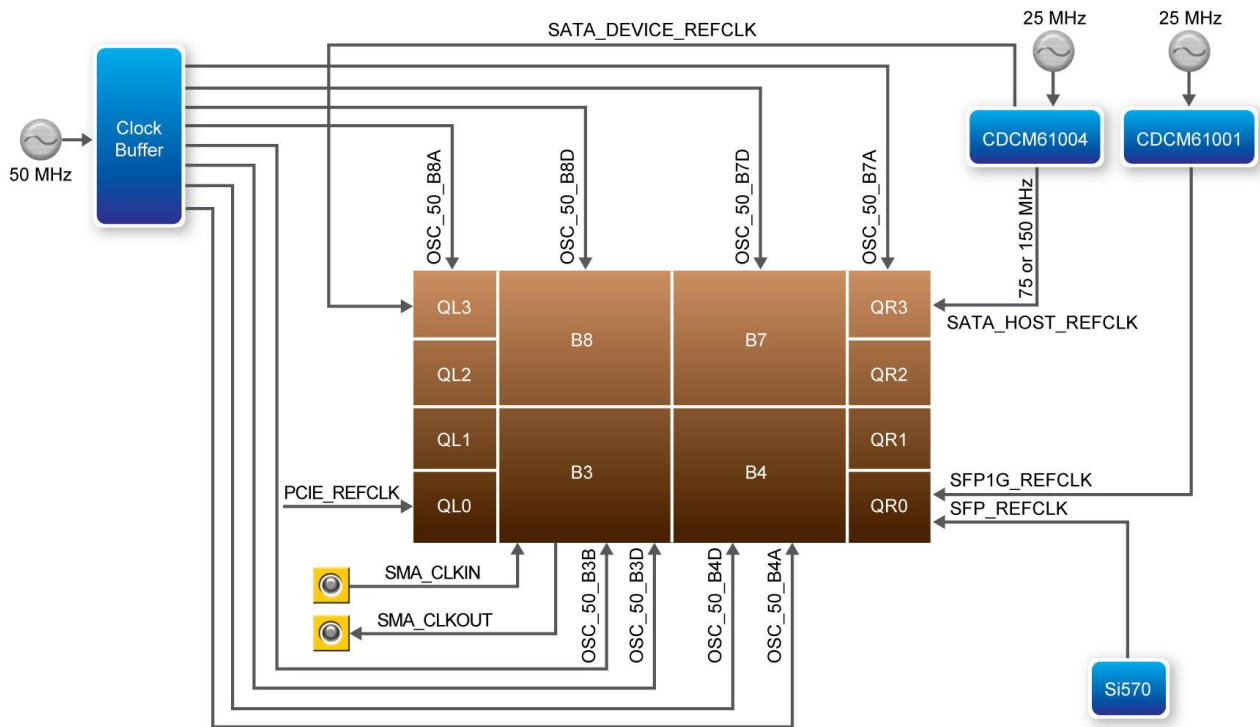
The pin assignments for the associated interface are listed in [Table 2-7](#).

**Table 2-7 Temperature Sensor Pin Assignments, Schematic Signal Names, and Functions**

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
TEMPDIODEp	Positive pin of temperature diode in Stratix V	1.8-V	PIN_P6
TEMPDIODEn	Negative pin of temperature diode in Stratix V	1.8-V	PIN_P7
TEMP_CLK	SMBus clock	2.5-V	PIN_D21
TEMP_DATAT	SMBus data	2.5-V	PIN_D20
TEMP_OVERT_n	SMBus alert (interrupt)	2.5-V	PIN_C22
TEMP_INT_n	SMBus alert (interrupt)	2.5-V	PIN_C21
FAN_CTRL	Fan control	2.5-V	PIN_AR32

## 2.5 Clock Circuit

The development board includes one 50 MHz and three programmable oscillators. **Figure 2-9** shows the default frequencies of on-board all external clocks going to the Stratix V GX FPGA. The figures also show an off-board external clock from PCI Express Host to the FPGA.



**Figure 2-9** Clock circuit of the FPGA Board

A clock buffer is used to duplicate the 50 MHz oscillator, so each bank of FPGA I/O bank 3/4/7/8 has two clock inputs. The three programming oscillators are low-jitter oscillators which are used to provide special and high quality clock signals for high-speed transceivers. **Figure 2-10** shows the control circuits of programmable oscillators. The clock generator controller in the MAX II CPLD can be used to program the CDCM61001 and CDCM61004 to generate 1G Ethernet SFP+ and SATA reference clocks respectively. The Si570 programmable clock generator is programmed via an I2C serial interface to generate the 10G Ethernet SFP+ reference clock. Two SMA connectors provide external clock input and clock output respectively.

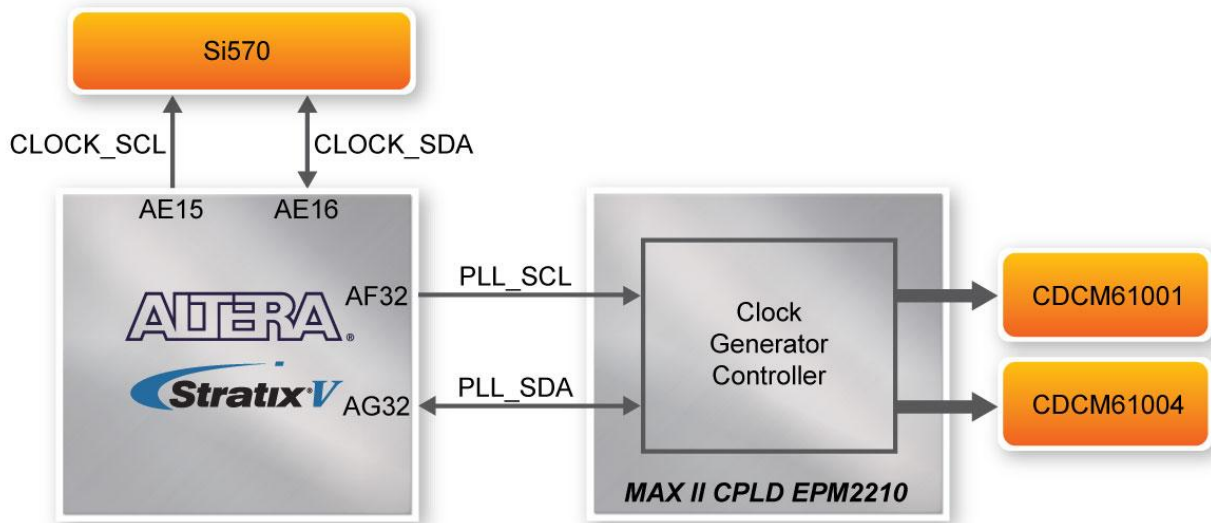


Figure 2-10 Control circuits of Programmable Oscillators

Table 2-8 lists the clock source, signal names, default frequency and their corresponding Stratix V GX device pin numbers.

Table 2-8 Clock Source, Signal Name, Default Frequency, Pin Assignments and Functions

Source	Schematic Signal Name	Default Frequency	I/O Standard	Stratix V GX Pin Number	Application
Y4	OSC_50_B3B	50.0 MHz	2.5-V	PIN_AW35	
	OSC_50_B3D		1.8-V	PIN_BC28	
	OSC_50_B4A		1.8-V	PIN_AP10	
	OSC_50_B4D		1.8-V	PIN_AY18	
	OSC_50_B7A		1.5-V	PIN_M8	
	OSC_50_B7D		1.5-V	PIN_J18	
	OSC_50_B8A		1.5-V	PIN_R36	
	OSC_50_B8D		1.8-V	PIN_R25	
J13	SMA_CLKIN	User Defined	2.5V	PIN_BB33	External Clock Input
J14	SMA_CLKOUT	User Defined	2.5V	PIN_AV34	Clock Output
U49	SFP_REFCLK_p	100.0 MHz	LVDS	PIN_AK7	10G SFP+
U53	SFP1G_REFCLK_p	125.0 MHz	LVDS	PIN_AH6	1G SFP+
U28	SATA_HOST_REFCLK_p	125.0 MHz	LVDS	PIN_V6	SATA HOST
U28	SATA_DEVICE_REFCLK_p	125.0 MHz	LVDS	PIN_V39	SATA DEVICE

J17	PCIE_REFCLK_p	From Host	LVDS	PIN_AK38	PCI Express
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**Table 2-9** lists the programmable oscillator control pins, signal names, I/O standard and their corresponding Stratix V GX device pin numbers.

**Table 2-9 Programmable oscillator control pin, Signal Name, I/O standard, Pin Assignments and Descriptions**

<i>Programmable Oscillator</i>	<i>Schematic Signal Name</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>	<i>Description</i>
Si570 (U49)	CLOCK_SCL	2.5-V	PIN_AE15	I2C bus, direct connected with Si570
	CLOCK_SDA	2.5-V	PIN_AE16	
CDCM61001 (U53)	PLL_SCL	2.5-V	PIN_AF32	I2C bus, connected with MAX II CPLD
	PLL_SDA	2.5-V	PIN_AG32	
CDCM61004 (U28)	PLL_SCL	2.5-V	PIN_AF32	I2C bus, connected with MAX II CPLD
	PLL_SDA	2.5-V	PIN_AG32	

## 2.6 RS-422 Serial Port

The RS-422 is designed to perform communication between boards, allowing a transmission speed of up to 20 Mbps. **Figure 2-11** shows the RS-422 block diagram of the development board. The full-duplex LTC2855 is used to translate the RS-422 signal, and the RJ45 is used as an external connector for the RS-422 signal.

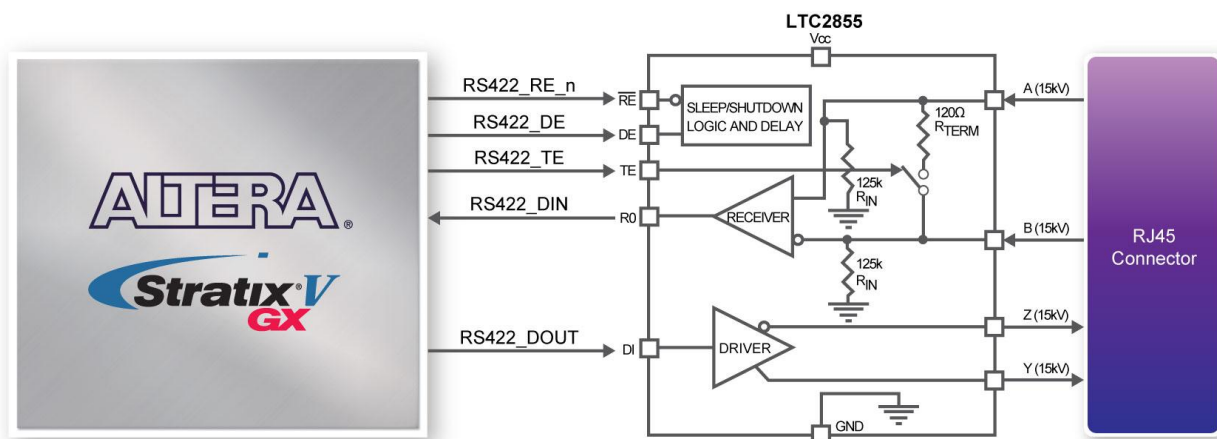


Figure 2-11 Block Diagram of RS-422

Table 2-10 lists the RS-422 pin assignments, signal names and functions.

Table 2-10 RS-422 Pin Assignments, Schematic Signal Names, and Functions

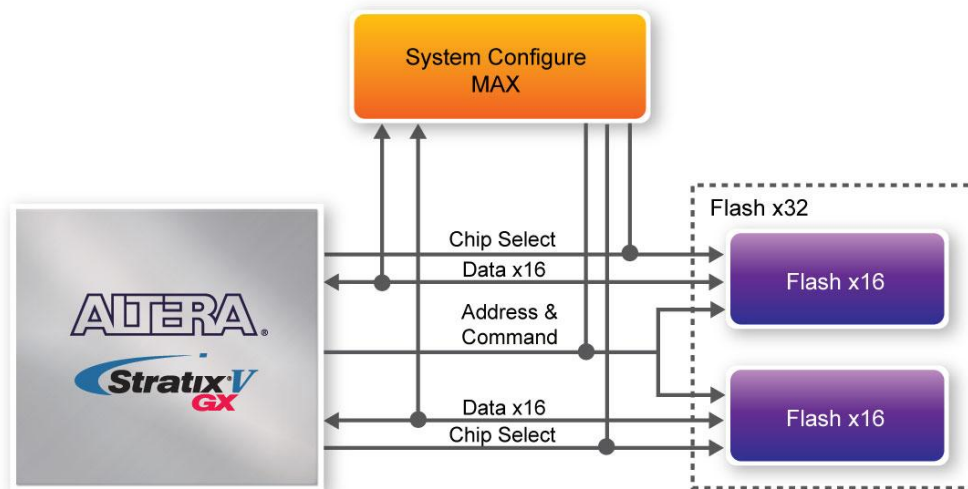
Schematic Signal Name	Description	I/O Standard	Stratix V GX Pin Number
RS422_DE	Driver Enable. A high on DE enables the driver. A low input will force the driver outputs into a high impedance state.	2.5-V	PIN_AG14
RS422_DIN	Receiver Output. The data is send to FPGA.		PIN_AE18
RS422_DOUT	Driver Input. The data is sent from FPGA.		PIN_AE17
RS422_RE_n	Receiver Enable. A low enables the receiver. A high input forces the receiver output into a high impedance state.		PIN_AF17
RS422_TE	Internal Termination Resistance Enable. A high input will connect a termination resistor (120Ω typical) between pins A and B.		PIN_AF16

## 2.7 FLASH Memory

The development board has two 1Gb CFI-compatible synchronous flash devices for non-volatile

storage of FPGA configuration data, user application data, and user code space.

Each interface has a 16-bit data bus and the two devices combined allow for FPP x32 configuration. This device is part of the shared flash and MAX (FM) bus, which connects to the flash memory and MAX II CPLD (EPM2210) System Controller. **Figure 2-12** shows the connections between the Flash, MAX and Stratix V GX FPGA.



**Figure 2-12 Connection between the Flash, Max and Stratix V GX FPGA**

**Table 2-11** lists the flash pin assignments, signal names, and functions.

**Table 2-11 Flash Memory Pin Assignments, Schematic Signal Names, and Functions**

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
FSM_A0	Address bus	2.5-V	PIN_AU32
FSM_A1	Address bus	2.5-V	PIN_AH30
FSM_A2	Address bus	2.5-V	PIN_AJ30
FSM_A3	Address bus	2.5-V	PIN_AH31
FSM_A4	Address bus	2.5-V	PIN_AK30
FSM_A5	Address bus	2.5-V	PIN_AJ32
FSM_A6	Address bus	2.5-V	PIN_AG33
FSM_A7	Address bus	2.5-V	PIN_AL30
FSM_A8	Address bus	2.5-V	PIN_AK33
FSM_A9	Address bus	2.5-V	PIN_AJ33
FSM_A10	Address bus	2.5-V	PIN_AN30
FSM_A11	Address bus	2.5-V	PIN_AH33

FSM_A12	Address bus	2.5-V	PIN_AK32
FSM_A13	Address bus	2.5-V	PIN_AM32
FSM_A14	Address bus	2.5-V	PIN_AM31
FSM_A15	Address bus	2.5-V	PIN_AL31
FSM_A16	Address bus	2.5-V	PIN_AN33
FSM_A17	Address bus	2.5-V	PIN_AP33
FSM_A18	Address bus	2.5-V	PIN_AT32
FSM_A19	Address bus	2.5-V	PIN_AT29
FSM_A20	Address bus	2.5-V	PIN_AP31
FSM_A21	Address bus	2.5-V	PIN_AR30
FSM_A22	Address bus	2.5-V	PIN_AU30
FSM_A23	Address bus	2.5-V	PIN_AJ31
FSM_A24	Address bus	2.5-V	PIN_AP30
FSM_A25	Address bus	2.5-V	PIN_AN31
FSM_A26	Address bus	2.5-V	PIN_AT30
FSM_D0	Data bus	2.5-V	PIN_AG26
FSM_D1	Data bus	2.5-V	PIN_AD33
FSM_D2	Data bus	2.5-V	PIN_AE34
FSM_D3	Data bus	2.5-V	PIN_AF31
FSM_D4	Data bus	2.5-V	PIN_AG28
FSM_D5	Data bus	2.5-V	PIN_AG30
FSM_D6	Data bus	2.5-V	PIN_AF29
FSM_D7	Data bus	2.5-V	PIN_AE29
FSM_D8	Data bus	2.5-V	PIN_AG25
FSM_D9	Data bus	2.5-V	PIN_AF34
FSM_D10	Data bus	2.5-V	PIN_AE33
FSM_D11	Data bus	2.5-V	PIN_AE31
FSM_D12	Data bus	2.5-V	PIN_AF28
FSM_D13	Data bus	2.5-V	PIN_AE30
FSM_D14	Data bus	2.5-V	PIN_AG29
FSM_D15	Data bus	2.5-V	PIN_AG27
FSM_D16	Data bus	2.5-V	PIN_AP28
FSM_D17	Data bus	2.5-V	PIN_AN28
FSM_D18	Data bus	2.5-V	PIN_AU31
FSM_D19	Data bus	2.5-V	PIN_AW32
FSM_D20	Data bus	2.5-V	PIN_BD32
FSM_D21	Data bus	2.5-V	PIN_AY31
FSM_D22	Data bus	2.5-V	PIN_BA30
FSM_D23	Data bus	2.5-V	PIN_BB30
FSM_D24	Data bus	2.5-V	PIN_AM29
FSM_D25	Data bus	2.5-V	PIN_AR29



FSM_D26	Data bus	2.5-V	PIN_AV31
FSM_D27	Data bus	2.5-V	PIN_AV32
FSM_D28	Data bus	2.5-V	PIN_BC31
FSM_D29	Data bus	2.5-V	PIN_AW30
FSM_D30	Data bus	2.5-V	PIN_BC32
FSM_D31	Data bus	2.5-V	PIN_BD31
FLASH_CLK	Clock	2.5-V	PIN_AL29
FLASH_RESET_n	Reset	2.5-V	PIN_AE28
FLASH_CE_n[0]	Chip enable of of flash-0	2.5-V	PIN_AE27
FLASH_CE_n[1]	Chip enable of of flash-1	2.5-V	PIN_BA31
FLASH_OE_n	Output enable	2.5-V	PIN_AY30
FLASH_WE_n	Write enable	2.5-V	PIN_AR31
FLASH_ADV_n	Address valid	2.5-V	PIN_AK29
FLASH_RDY_BSY_n[0]	Ready of flash-0	2.5-V	PIN_BA29
FLASH_RDY_BSY_n[1]	Ready of flash-1	2.5-V	PIN_BB32

## 2.8 DDR3 SO-DIMM

The development board supports two independent banks of DDR3 SDRAM SO-DIMM. Each DDR3 SODIMM socket is wired to support a maximum capacity of 8GB with a 64-bit data bus. Using differential DQS signaling for the DDR3 SDRAM interfaces, it is capable of running at up to 800MHz memory clock for a maximum theoretical bandwidth up to 95.4Gbps. **Figure 2-13** shows the connections between the DDR3 SDRAM SO-DIMMs and Stratix V GX FPGA.

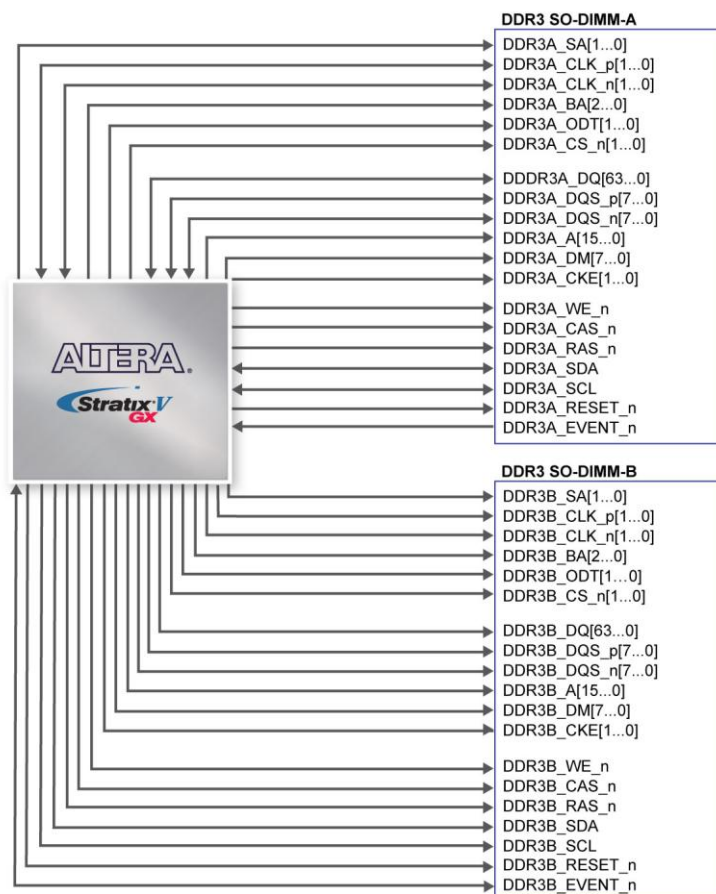


Figure 2-13 Connection between the DDR3 and Stratix V GX FPGA

The pin assignments for DDR3 SDRAM SO-DIMM Bank-A and Bank-B are listed in [Table 2-12](#) and [Table 2-13](#), in respectively.

Table 2-12 DDR3-A Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Stratix V GX Pin Number
DDR3A_DQ0	Data [0]	SSTL-15 Class I	PIN_A35
DDR3A_DQ1	Data [1]	SSTL-15 Class I	PIN_A34
DDR3A_DQ2	Data [2]	SSTL-15 Class I	PIN_D36
DDR3A_DQ3	Data [3]	SSTL-15 Class I	PIN_C33
DDR3A_DQ4	Data [4]	SSTL-15 Class I	PIN_B32
DDR3A_DQ5	Data [5]	SSTL-15 Class I	PIN_D35
DDR3A_DQ6	Data [6]	SSTL-15 Class I	PIN_D33
DDR3A_DQ7	Data [7]	SSTL-15 Class I	PIN_E33
DDR3A_DQ8	Data [8]	SSTL-15 Class I	PIN_A32
DDR3A_DQ9	Data [9]	SSTL-15 Class I	PIN_A31

DDR3A_DQ10	Data [10]	SSTL-15 Class I	PIN_C30
DDR3A_DQ11	Data [11]	SSTL-15 Class I	PIN_D30
DDR3A_DQ12	Data [12]	SSTL-15 Class I	PIN_B29
DDR3A_DQ13	Data [13]	SSTL-15 Class I	PIN_E30
DDR3A_DQ14	Data [14]	SSTL-15 Class I	PIN_F31
DDR3A_DQ15	Data [15]	SSTL-15 Class I	PIN_G31
DDR3A_DQ16	Data [16]	SSTL-15 Class I	PIN_F35
DDR3A_DQ17	Data [17]	SSTL-15 Class I	PIN_G34
DDR3A_DQ18	Data [18]	SSTL-15 Class I	PIN_J33
DDR3A_DQ19	Data [19]	SSTL-15 Class I	PIN_J34
DDR3A_DQ20	Data [20]	SSTL-15 Class I	PIN_F34
DDR3A_DQ21	Data [21]	SSTL-15 Class I	PIN_E35
DDR3A_DQ22	Data [22]	SSTL-15 Class I	PIN_J31
DDR3A_DQ23	Data [23]	SSTL-15 Class I	PIN_K31
DDR3A_DQ24	Data [24]	SSTL-15 Class I	PIN_P34
DDR3A_DQ25	Data [25]	SSTL-15 Class I	PIN_R33
DDR3A_DQ26	Data [26]	SSTL-15 Class I	PIN_M34
DDR3A_DQ27	Data [27]	SSTL-15 Class I	PIN_L33
DDR3A_DQ28	Data [28]	SSTL-15 Class I	PIN_R34
DDR3A_DQ29	Data [29]	SSTL-15 Class I	PIN_T34
DDR3A_DQ30	Data [30]	SSTL-15 Class I	PIN_W34
DDR3A_DQ31	Data [31]	SSTL-15 Class I	PIN_V35
DDR3A_DQ32	Data [32]	SSTL-15 Class I	PIN_P33
DDR3A_DQ33	Data [33]	SSTL-15 Class I	PIN_P32
DDR3A_DQ34	Data [34]	SSTL-15 Class I	PIN_V33
DDR3A_DQ35	Data [35]	SSTL-15 Class I	PIN_V34
DDR3A_DQ36	Data [36]	SSTL-15 Class I	PIN_N31
DDR3A_DQ37	Data [37]	SSTL-15 Class I	PIN_M31
DDR3A_DQ38	Data [38]	SSTL-15 Class I	PIN_U32
DDR3A_DQ39	Data [39]	SSTL-15 Class I	PIN_U33
DDR3A_DQ40	Data [40]	SSTL-15 Class I	PIN_R31
DDR3A_DQ41	Data [41]	SSTL-15 Class I	PIN_W31
DDR3A_DQ42	Data [42]	SSTL-15 Class I	PIN_U30
DDR3A_DQ43	Data [43]	SSTL-15 Class I	PIN_P31
DDR3A_DQ44	Data [44]	SSTL-15 Class I	PIN_T31
DDR3A_DQ45	Data [45]	SSTL-15 Class I	PIN_Y32
DDR3A_DQ46	Data [46]	SSTL-15 Class I	PIN_T29
DDR3A_DQ47	Data [47]	SSTL-15 Class I	PIN_P30
DDR3A_DQ48	Data [48]	SSTL-15 Class I	PIN_H32
DDR3A_DQ49	Data [49]	SSTL-15 Class I	PIN_H31
DDR3A_DQ50	Data [50]	SSTL-15 Class I	PIN_L30
DDR3A_DQ51	Data [51]	SSTL-15 Class I	PIN_L29
DDR3A_DQ52	Data [52]	SSTL-15 Class I	PIN_F32

DDR3A_DQ53	Data [53]	SSTL-15 Class I	PIN_G32
DDR3A_DQ54	Data [54]	SSTL-15 Class I	PIN_M30
DDR3A_DQ55	Data [55]	SSTL-15 Class I	PIN_N29
DDR3A_DQ56	Data [56]	SSTL-15 Class I	PIN_U29
DDR3A_DQ57	Data [57]	SSTL-15 Class I	PIN_V28
DDR3A_DQ58	Data [58]	SSTL-15 Class I	PIN_Y28
DDR3A_DQ59	Data [59]	SSTL-15 Class I	PIN_W29
DDR3A_DQ60	Data [60]	SSTL-15 Class I	PIN_V30
DDR3A_DQ61	Data [61]	SSTL-15 Class I	PIN_V29
DDR3A_DQ62	Data [62]	SSTL-15 Class I	PIN_W28
DDR3A_DQ63	Data [63]	SSTL-15 Class I	PIN_Y27
DDR3A_DQS0	Data Strobe p[0]	Differential 1.5-V SSTL Class I	PIN_C34
DDR3A_DQS_n0	Data Strobe n[0]	Differential 1.5-V SSTL Class I	PIN_B34
DDR3A_DQS1	Data Strobe p[1]	Differential 1.5-V SSTL Class I	PIN_C31
DDR3A_DQS_n1	Data Strobe n[1]	Differential 1.5-V SSTL Class I	PIN_B31
DDR3A_DQS2	Data Strobe p[2]	Differential 1.5-V SSTL Class I	PIN_H35
DDR3A_DQS_n2	Data Strobe n[2]	Differential 1.5-V SSTL Class I	PIN_G35
DDR3A_DQS3	Data Strobe p[3]	Differential 1.5-V SSTL Class I	PIN_U35
DDR3A_DQS_n3	Data Strobe n[4]	Differential 1.5-V SSTL Class I	PIN_T35
DDR3A_DQS4	Data Strobe p[4]	Differential 1.5-V SSTL Class I	PIN_T33
DDR3A_DQS_n4	Data Strobe n[4]	Differential 1.5-V SSTL Class I	PIN_T32
DDR3A_DQS5	Data Strobe p[5]	Differential 1.5-V SSTL Class I	PIN_T30
DDR3A_DQS_n5	Data Strobe n[5]	Differential 1.5-V SSTL Class I	PIN_R30
DDR3A_DQS6	Data Strobe p[6]	Differential 1.5-V SSTL Class I	PIN_J30
DDR3A_DQS_n6	Data Strobe n[6]	Differential 1.5-V SSTL Class I	PIN_H30
DDR3A_DQS7	Data Strobe p[7]	Differential 1.5-V SSTL Class I	PIN_Y30
DDR3A_DQS_n7	Data Strobe n[7]	Differential 1.5-V SSTL Class I	PIN_Y29
DDR3A_DM0	Data Mask [0]	SSTL-15 Class I	PIN_C36
DDR3A_DM1	Data Mask [1]	SSTL-15 Class I	PIN_E32
DDR3A_DM2	Data Mask [2]	SSTL-15 Class I	PIN_H34
DDR3A_DM3	Data Mask [3]	SSTL-15 Class I	PIN_L32
DDR3A_DM4	Data Mask [4]	SSTL-15 Class I	PIN_N32
DDR3A_DM5	Data Mask [5]	SSTL-15 Class I	PIN_W32
DDR3A_DM6	Data Mask [6]	SSTL-15 Class I	PIN_K30
DDR3A_DM7	Data Mask [7]	SSTL-15 Class I	PIN_T28
DDR3A_A0	Address [0]	SSTL-15 Class I	PIN_M39
DDR3A_A1	Address [1]	SSTL-15 Class I	PIN_L35
DDR3A_A2	Address [2]	SSTL-15 Class I	PIN_N38
DDR3A_A3	Address [3]	SSTL-15 Class I	PIN_L36
DDR3A_A4	Address [4]	SSTL-15 Class I	PIN_H36
DDR3A_A5	Address [5]	SSTL-15 Class I	PIN_K29
DDR3A_A6	Address [6]	SSTL-15 Class I	PIN_D37
DDR3A_A7	Address [7]	SSTL-15 Class I	PIN_K35

DDR3A_A8	Address [8]	SSTL-15 Class I	PIN_K32
DDR3A_A9	Address [9]	SSTL-15 Class I	PIN_K37
DDR3A_A10	Address [10]	SSTL-15 Class I	PIN_M38
DDR3A_A11	Address [11]	SSTL-15 Class I	PIN_C37
DDR3A_A12	Address [12]	SSTL-15 Class I	PIN_K36
DDR3A_A13	Address [13]	SSTL-15 Class I	PIN_M33
DDR3A_A14	Address [14]	SSTL-15 Class I	PIN_K34
DDR3A_A15	Address [15]	SSTL-15 Class I	PIN_B38
DDR3A_RAS_n	Row Address Strobe	SSTL-15 Class I	PIN_P38
DDR3A_CAS_n	Column Address Strobe	SSTL-15 Class I	PIN_M36
DDR3A_BA0	Bank Address [0]	SSTL-15 Class I	PIN_M37
DDR3A_BA1	Bank Address [1]	SSTL-15 Class I	PIN_P39
DDR3A_BA2	Bank Address [2]	SSTL-15 Class I	PIN_J36
DDR3A_CK0	Clock p0	Differential 1.5-V SSTL Class I	PIN_G37
DDR3A_CK_n0	Clock n0	Differential 1.5-V SSTL Class I	PIN_F36
DDR3A_CK1	Clock p1	Differential 1.5-V SSTL Class I	PIN_J37
DDR3A_CK_n1	Clock n1	Differential 1.5-V SSTL Class I	PIN_H37
DDR3A_CKE0	Clock Enable pin 0	SSTL-15 Class I	PIN_E36
DDR3A_CKE1	Clock Enable pin 1	SSTL-15 Class I	PIN_B35
DDR3A_ODT0	On Die Termination[0]	SSTL-15 Class I	PIN_V36
DDR3A_ODT1	On Die Termination[1]	SSTL-15 Class I	PIN_W35
DDR3A_WE_n	Write Enable	SSTL-15 Class I	PIN_N37
DDR3A_CS_n0	Chip Select [0]	SSTL-15 Class I	PIN_P36
DDR3A_CS_n1	Chip Select [1]	SSTL-15 Class I	PIN_R28
DDR3A_RESET_n	Chip Reset	SSTL-15 Class I	PIN_H33
DDR3A_EVENT_n	Chip Temperature Event	SSTL-15 Class I	PIN_K19
DDR3A_SDA	Chip I2C Serial Clock	1.5V	PIN_P15
DDR3A_SCL	Chip I2C Serial Data Bus	1.5V	PIN_C15

Table 2-13 DDR3-B Pin Assignments, Schematic Signal Names, and Functions

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
DDR3B_DQ0	Data [0]	SSTL-15 Class I	PIN_Y17
DDR3B_DQ1	Data [1]	SSTL-15 Class I	PIN_W17
DDR3B_DQ2	Data [2]	SSTL-15 Class I	PIN_V15
DDR3B_DQ3	Data [3]	SSTL-15 Class I	PIN_T15
DDR3B_DQ4	Data [4]	SSTL-15 Class I	PIN_V13
DDR3B_DQ5	Data [5]	SSTL-15 Class I	PIN_V16
DDR3B_DQ6	Data [6]	SSTL-15 Class I	PIN_W14
DDR3B_DQ7	Data [7]	SSTL-15 Class I	PIN_U15

DDR3B_DQ8	Data [8]	SSTL-15 Class I	PIN_T17
DDR3B_DQ9	Data [9]	SSTL-15 Class I	PIN_T16
DDR3B_DQ10	Data [10]	SSTL-15 Class I	PIN_R16
DDR3B_DQ11	Data [11]	SSTL-15 Class I	PIN_P16
DDR3B_DQ12	Data [12]	SSTL-15 Class I	PIN_N16
DDR3B_DQ13	Data [13]	SSTL-15 Class I	PIN_M15
DDR3B_DQ14	Data [14]	SSTL-15 Class I	PIN_M14
DDR3B_DQ15	Data [15]	SSTL-15 Class I	PIN_L14
DDR3B_DQ16	Data [16]	SSTL-15 Class I	PIN_T14
DDR3B_DQ17	Data [17]	SSTL-15 Class I	PIN_U14
DDR3B_DQ18	Data [18]	SSTL-15 Class I	PIN_U11
DDR3B_DQ19	Data [19]	SSTL-15 Class I	PIN_T13
DDR3B_DQ20	Data [20]	SSTL-15 Class I	PIN_U12
DDR3B_DQ21	Data [21]	SSTL-15 Class I	PIN_R13
DDR3B_DQ22	Data [22]	SSTL-15 Class I	PIN_P13
DDR3B_DQ23	Data [23]	SSTL-15 Class I	PIN_N13
DDR3B_DQ24	Data [24]	SSTL-15 Class I	PIN_K12
DDR3B_DQ25	Data [25]	SSTL-15 Class I	PIN_J12
DDR3B_DQ26	Data [26]	SSTL-15 Class I	PIN_J10
DDR3B_DQ27	Data [27]	SSTL-15 Class I	PIN_H12
DDR3B_DQ28	Data [28]	SSTL-15 Class I	PIN_N11
DDR3B_DQ29	Data [29]	SSTL-15 Class I	PIN_M11
DDR3B_DQ30	Data [30]	SSTL-15 Class I	PIN_H10
DDR3B_DQ31	Data [31]	SSTL-15 Class I	PIN_H11
DDR3B_DQ32	Data [32]	SSTL-15 Class I	PIN_T10
DDR3B_DQ33	Data [33]	SSTL-15 Class I	PIN_R10
DDR3B_DQ34	Data [34]	SSTL-15 Class I	PIN_M12
DDR3B_DQ35	Data [35]	SSTL-15 Class I	PIN_L12
DDR3B_DQ36	Data [36]	SSTL-15 Class I	PIN_V10
DDR3B_DQ37	Data [37]	SSTL-15 Class I	PIN_V9
DDR3B_DQ38	Data [38]	SSTL-15 Class I	PIN_R12
DDR3B_DQ39	Data [39]	SSTL-15 Class I	PIN_P12
DDR3B_DQ40	Data [40]	SSTL-15 Class I	PIN_D14
DDR3B_DQ41	Data [41]	SSTL-15 Class I	PIN_C13
DDR3B_DQ42	Data [42]	SSTL-15 Class I	PIN_B14
DDR3B_DQ43	Data [43]	SSTL-15 Class I	PIN_B13
DDR3B_DQ44	Data [44]	SSTL-15 Class I	PIN_E14
DDR3B_DQ45	Data [45]	SSTL-15 Class I	PIN_F14
DDR3B_DQ46	Data [46]	SSTL-15 Class I	PIN_A14
DDR3B_DQ47	Data [47]	SSTL-15 Class I	PIN_A13
DDR3B_DQ48	Data [48]	SSTL-15 Class I	PIN_K13
DDR3B_DQ49	Data [49]	SSTL-15 Class I	PIN_K16
DDR3B_DQ50	Data [50]	SSTL-15 Class I	PIN_H13

DDR3B_DQ51	Data [51]	SSTL-15 Class I	PIN_H14
DDR3B_DQ52	Data [52]	SSTL-15 Class I	PIN_J13
DDR3B_DQ53	Data [53]	SSTL-15 Class I	PIN_J16
DDR3B_DQ54	Data [54]	SSTL-15 Class I	PIN_G13
DDR3B_DQ55	Data [55]	SSTL-15 Class I	PIN_F13
DDR3B_DQ56	Data [56]	SSTL-15 Class I	PIN_D11
DDR3B_DQ57	Data [57]	SSTL-15 Class I	PIN_C10
DDR3B_DQ58	Data [58]	SSTL-15 Class I	PIN_A10
DDR3B_DQ59	Data [59]	SSTL-15 Class I	PIN_B10
DDR3B_DQ60	Data [60]	SSTL-15 Class I	PIN_G11
DDR3B_DQ61	Data [61]	SSTL-15 Class I	PIN_F11
DDR3B_DQ62	Data [62]	SSTL-15 Class I	PIN_E11
DDR3B_DQ63	Data [63]	SSTL-15 Class I	PIN_E12
DDR3B_DQS0	Data Strobe p[0]	Differential 1.5-V SSTL Class I	PIN_Y16
DDR3B_DQS_n0	Data Strobe n[0]	Differential 1.5-V SSTL Class I	PIN_W16
DDR3B_DQS1	Data Strobe p[1]	Differential 1.5-V SSTL Class I	PIN_V17
DDR3B_DQS_n1	Data Strobe n[1]	Differential 1.5-V SSTL Class I	PIN_U17
DDR3B_DQS2	Data Strobe p[2]	Differential 1.5-V SSTL Class I	PIN_P14
DDR3B_DQS_n2	Data Strobe n[2]	Differential 1.5-V SSTL Class I	PIN_N14
DDR3B_DQS3	Data Strobe p[3]	Differential 1.5-V SSTL Class I	PIN_K11
DDR3B_DQS_n3	Data Strobe n[3]	Differential 1.5-V SSTL Class I	PIN_L11
DDR3B_DQS4	Data Strobe p[4]	Differential 1.5-V SSTL Class I	PIN_U9
DDR3B_DQS_n4	Data Strobe n[4]	Differential 1.5-V SSTL Class I	PIN_T9
DDR3B_DQS5	Data Strobe p[5]	Differential 1.5-V SSTL Class I	PIN_E15
DDR3B_DQS_n5	Data Strobe n[5]	Differential 1.5-V SSTL Class I	PIN_D15
DDR3B_DQS6	Data Strobe p[6]	Differential 1.5-V SSTL Class I	PIN_L15
DDR3B_DQS_n6	Data Strobe n[6]	Differential 1.5-V SSTL Class I	PIN_K14
DDR3B_DQS7	Data Strobe p[7]	Differential 1.5-V SSTL Class I	PIN_D12
DDR3B_DQS_n7	Data Strobe n[7]	Differential 1.5-V SSTL Class I	PIN_C12
DDR3B_DM0	Data Mask [0]	SSTL-15 Class I	PIN_R15
DDR3B_DM1	Data Mask [1]	SSTL-15 Class I	PIN_K15
DDR3B_DM2	Data Mask [2]	SSTL-15 Class I	PIN_V12
DDR3B_DM3	Data Mask [3]	SSTL-15 Class I	PIN_G10
DDR3B_DM4	Data Mask [4]	SSTL-15 Class I	PIN_T12
DDR3B_DM5	Data Mask [5]	SSTL-15 Class I	PIN_C16
DDR3B_DM6	Data Mask [6]	SSTL-15 Class I	PIN_H15
DDR3B_DM7	Data Mask [7]	SSTL-15 Class I	PIN_B11
DDR3B_A0	Address [0]	SSTL-15 Class I	PIN_G17
DDR3B_A1	Address [1]	SSTL-15 Class I	PIN_F17
DDR3B_A2	Address [2]	SSTL-15 Class I	PIN_N17
DDR3B_A3	Address [3]	SSTL-15 Class I	PIN_F19
DDR3B_A4	Address [4]	SSTL-15 Class I	PIN_N19
DDR3B_A5	Address [5]	SSTL-15 Class I	PIN_H16

DDR3B_A6	Address [6]	SSTL-15 Class I	PIN_M17
DDR3B_A7	Address [7]	SSTL-15 Class I	PIN_T18
DDR3B_A8	Address [8]	SSTL-15 Class I	PIN_H17
DDR3B_A9	Address [9]	SSTL-15 Class I	PIN_J19
DDR3B_A10	Address [10]	SSTL-15 Class I	PIN_C19
DDR3B_A11	Address [11]	SSTL-15 Class I	PIN_R18
DDR3B_A12	Address [12]	SSTL-15 Class I	PIN_K18
DDR3B_A13	Address [13]	SSTL-15 Class I	PIN_E18
DDR3B_A14	Address [14]	SSTL-15 Class I	PIN_T19
DDR3B_A15	Address [15]	SSTL-15 Class I	PIN_R19
DDR3B_RAS_n	Row Address Strobe	SSTL-15 Class I	PIN_H19
DDR3B_CAS_n	Column Address Strobe	SSTL-15 Class I	PIN_A17
DDR3B_BA0	Bank Address [0]	SSTL-15 Class I	PIN_C18
DDR3B_BA1	Bank Address [1]	SSTL-15 Class I	PIN_G19
DDR3B_BA2	Bank Address [2]	SSTL-15 Class I	PIN_M20
DDR3B_CK0	Clock p0	Differential 1.5-V SSTL Class I	PIN_B16
DDR3B_CK_n0	Clock n0	Differential 1.5-V SSTL Class I	PIN_A16
DDR3B_CK1	Clock p1	Differential 1.5-V SSTL Class I	PIN_E17
DDR3B_CK_n1	Clock n1	Differential 1.5-V SSTL Class I	PIN_D17
DDR3B_CKE0	Clock Enable pin 0	SSTL-15 Class I	PIN_P17
DDR3B_CKE1	Clock Enable pin 1	SSTL-15 Class I	PIN_V18
DDR3B_ODT0	On Die Termination[0]	SSTL-15 Class I	PIN_M18
DDR3B_ODT1	On Die Termination[1]	SSTL-15 Class I	PIN_A19
DDR3B_WE_n	Write Enable	SSTL-15 Class I	PIN_D18
DDR3B_CS_n0	Chip Select [0]	SSTL-15 Class I	PIN_B19
DDR3B_CS_n1	Chip Select [1]	SSTL-15 Class I	PIN_B17
DDR3B_RESET_n	Chip Reset	SSTL-15 Class I	PIN_T20
DDR3B_EVENT_n	Chip Reset	SSTL-15 Class I	PIN_K17
DDR3B_SDA	Chip I2C Serial Clock	1.5V	PIN_P19
DDR3B_SCL	Chip I2C Serial Data Bus	1.5V	PIN_P18

## 2.9 QDRII+ SRAM

The development board supports four independent QDRII+ SRAM memory devices for very-high speed and low-latency memory access. Each of QDRII+ has a x18 interface, providing addressing to a device of up to a 8MB (not including parity bits). The QDRII+ has separate read and write data ports with DDR signaling at up to 550 MHz.

**Table 2-14**, **Table 2-15** and **Table 2-16** lists the QDRII+ SRAM Bank A, B, C and D pin assignments, signal names relative to the Stratix I GX device, in respectively.



**Table 2-14 QDRII+ SRAM A Pin Assignments, Schematic Signal Names, and Functions**

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
QDRIIA_A0	Address bus[0]	1.8-V HSTL Class I	PIN_AU29
QDRIIA_A1	Address bus[1]	1.8-V HSTL Class I	PIN_BA28
QDRIIA_A2	Address bus[2]	1.8-V HSTL Class I	PIN_AP27
QDRIIA_A3	Address bus[3]	1.8-V HSTL Class I	PIN_AK27
QDRIIA_A4	Address bus[4]	1.8-V HSTL Class I	PIN_AN27
QDRIIA_A5	Address bus[5]	1.8-V HSTL Class I	PIN_AM28
QDRIIA_A6	Address bus[6]	1.8-V HSTL Class I	PIN_AV28
QDRIIA_A7	Address bus[7]	1.8-V HSTL Class I	PIN_AY27
QDRIIA_A8	Address bus[8]	1.8-V HSTL Class I	PIN_BC29
QDRIIA_A9	Address bus[9]	1.8-V HSTL Class I	PIN_AU28
QDRIIA_A10	Address bus[10]	1.8-V HSTL Class I	PIN_AW27
QDRIIA_A11	Address bus[11]	1.8-V HSTL Class I	PIN_AY28
QDRIIA_A12	Address bus[12]	1.8-V HSTL Class I	PIN_BD28
QDRIIA_A13	Address bus[13]	1.8-V HSTL Class I	PIN_AV29
QDRIIA_A14	Address bus[14]	1.8-V HSTL Class I	PIN_AW29
QDRIIA_A15	Address bus[15]	1.8-V HSTL Class I	PIN_BB29
QDRIIA_A16	Address bus[16]	1.8-V HSTL Class I	PIN_BD29
QDRIIA_A17	Address bus[17]	1.8-V HSTL Class I	PIN_AL27
QDRIIA_A18	Address bus[18]	1.8-V HSTL Class I	PIN_AR27
QDRIIA_A19	Address bus[19]	1.8-V HSTL Class I	PIN_AL28
QDRIIA_A20	Address bus[20]	1.8-V HSTL Class I	PIN_AR28
QDRIIA_D0	Write data bus[0]	1.8-V HSTL Class I	PIN_AH28
QDRIIA_D1	Write data bus[1]	1.8-V HSTL Class I	PIN_AH27
QDRIIA_D2	Write data bus[2]	1.8-V HSTL Class I	PIN_AH25
QDRIIA_D3	Write data bus[3]	1.8-V HSTL Class I	PIN_AJ28
QDRIIA_D4	Write data bus[4]	1.8-V HSTL Class I	PIN_AJ27
QDRIIA_D5	Write data bus[5]	1.8-V HSTL Class I	PIN_AJ26
QDRIIA_D6	Write data bus[6]	1.8-V HSTL Class I	PIN_AJ25
QDRIIA_D7	Write data bus[7]	1.8-V HSTL Class I	PIN_AL25
QDRIIA_D8	Write data bus[8]	1.8-V HSTL Class I	PIN_AH24
QDRIIA_D9	Write data bus[9]	1.8-V HSTL Class I	PIN_AN25
QDRIIA_D10	Write data bus[10]	1.8-V HSTL Class I	PIN_AM26
QDRIIA_D11	Write data bus[11]	1.8-V HSTL Class I	PIN_AM25
QDRIIA_D12	Write data bus[12]	1.8-V HSTL Class I	PIN_AL26
QDRIIA_D13	Write data bus[13]	1.8-V HSTL Class I	PIN_AK26
QDRIIA_D14	Write data bus[14]	1.8-V HSTL Class I	PIN_AU27
QDRIIA_D15	Write data bus[15]	1.8-V HSTL Class I	PIN_AU26
QDRIIA_D16	Write data bus[16]	1.8-V HSTL Class I	PIN_AV26
QDRIIA_D17	Write data bus[17]	1.8-V HSTL Class I	PIN_AW26
QDRIIA_Q0	Read Data bus[0]	1.8-V HSTL Class I	PIN_AK23

QDRIIA_Q1	Read Data bus[1]	1.8-V HSTL Class I	PIN_BB26
QDRIIA_Q2	Read Data bus[2]	1.8-V HSTL Class I	PIN_BD26
QDRIIA_Q3	Read Data bus[3]	1.8-V HSTL Class I	PIN_BA24
QDRIIA_Q4	Read Data bus[4]	1.8-V HSTL Class I	PIN_AL23
QDRIIA_Q5	Read Data bus[5]	1.8-V HSTL Class I	PIN_AJ23
QDRIIA_Q6	Read Data bus[6]	1.8-V HSTL Class I	PIN_AL21
QDRIIA_Q7	Read Data bus[7]	1.8-V HSTL Class I	PIN_AK21
QDRIIA_Q8	Read Data bus[8]	1.8-V HSTL Class I	PIN_AJ22
QDRIIA_Q9	Read Data bus[9]	1.8-V HSTL Class I	PIN_AW24
QDRIIA_Q10	Read Data bus[10]	1.8-V HSTL Class I	PIN_BC26
QDRIIA_Q11	Read Data bus[11]	1.8-V HSTL Class I	PIN_AY25
QDRIIA_Q12	Read Data bus[12]	1.8-V HSTL Class I	PIN_AU24
QDRIIA_Q13	Read Data bus[13]	1.8-V HSTL Class I	PIN_AV25
QDRIIA_Q14	Read Data bus[14]	1.8-V HSTL Class I	PIN_AU25
QDRIIA_Q15	Read Data bus[15]	1.8-V HSTL Class I	PIN_AR25
QDRIIA_Q16	Read Data bus[16]	1.8-V HSTL Class I	PIN_AP24
QDRIIA_Q17	Read Data bus[17]	1.8-V HSTL Class I	PIN_AL24
QDRIIA_BWS_n0	Byte Write select[0]	1.8-V HSTL Class I	PIN_AJ24
QDRIIA_BWS_n1	Byte Write select[1]	1.8-V HSTL Class I	PIN_AT27
QDRIIA_K_P	Clock P	Differential 1.8-V HSTL Class I	PIN_AP25
QDRIIA_K_N	Clock N	Differential 1.8-V HSTL Class I	PIN_AR26
QDRIIA_CQ_P	Echo clock P	1.8-V HSTL Class I	PIN_AH22
QDRIIA_CQ_N	Echo clock N	1.8-V HSTL Class I	PIN_BA25
QDRIIA_RPS_n	Report Select	1.8-V HSTL Class I	PIN_AT26
QDRIIA_WPS_n	Write Port Select	1.8-V HSTL Class I	PIN_AK24
QDRIIA_DOFF_n	DLL enable	1.8-V HSTL Class I	PIN_AR23
QDRIIA_ODT	On-Die Termination Input	1.8-V HSTL Class I	PIN_AN23
QDRII_QVLD	Valid Output Indicator	1.8-V HSTL Class I	PIN_AM23

Table 2-15 QDRII+ SRAM B Pin Assignments, Schematic Signal Names, and Functions

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
QDRIIB_A0	Address bus[0]	1.8-V HSTL Class I	PIN_AR24
QDRIIB_A1	Address bus[1]	1.8-V HSTL Class I	PIN_BB23
QDRIIB_A2	Address bus[2]	1.8-V HSTL Class I	PIN_AK20
QDRIIB_A3	Address bus[3]	1.8-V HSTL Class I	PIN_AJ19
QDRIIB_A4	Address bus[4]	1.8-V HSTL Class I	PIN_AL20
QDRIIB_A5	Address bus[5]	1.8-V HSTL Class I	PIN_AG19
QDRIIB_A6	Address bus[6]	1.8-V HSTL Class I	PIN_AT23

QDRIIB_A7	Address bus[7]	1.8-V HSTL Class I	PIN_AU23
QDRIIB_A8	Address bus[8]	1.8-V HSTL Class I	PIN_AV23
QDRIIB_A9	Address bus[9]	1.8-V HSTL Class I	PIN_AM22
QDRIIB_A10	Address bus[10]	1.8-V HSTL Class I	PIN_AJ20
QDRIIB_A11	Address bus[11]	1.8-V HSTL Class I	PIN_AG20
QDRIIB_A12	Address bus[12]	1.8-V HSTL Class I	PIN_AW23
QDRIIB_A13	Address bus[13]	1.8-V HSTL Class I	PIN_BB24
QDRIIB_A14	Address bus[14]	1.8-V HSTL Class I	PIN_AY24
QDRIIB_A15	Address bus[15]	1.8-V HSTL Class I	PIN_BD23
QDRIIB_A16	Address bus[16]	1.8-V HSTL Class I	PIN_BC23
QDRIIB_A17	Address bus[17]	1.8-V HSTL Class I	PIN_AG21
QDRIIB_A18	Address bus[18]	1.8-V HSTL Class I	PIN_AM20
QDRIIB_A19	Address bus[19]	1.8-V HSTL Class I	PIN_AK18
QDRIIB_A20	Address bus[20]	1.8-V HSTL Class I	PIN_AN22
QDRIIB_D0	Write data bus[0]	1.8-V HSTL Class I	PIN_BB21
QDRIIB_D1	Write data bus[1]	1.8-V HSTL Class I	PIN_BD20
QDRIIB_D2	Write data bus[2]	1.8-V HSTL Class I	PIN_BC20
QDRIIB_D3	Write data bus[3]	1.8-V HSTL Class I	PIN_AR22
QDRIIB_D4	Write data bus[4]	1.8-V HSTL Class I	PIN_BB20
QDRIIB_D5	Write data bus[5]	1.8-V HSTL Class I	PIN_AU22
QDRIIB_D6	Write data bus[6]	1.8-V HSTL Class I	PIN_BA21
QDRIIB_D7	Write data bus[7]	1.8-V HSTL Class I	PIN_AY21
QDRIIB_D8	Write data bus[8]	1.8-V HSTL Class I	PIN_AW21
QDRIIB_D9	Write data bus[9]	1.8-V HSTL Class I	PIN_AT21
QDRIIB_D10	Write data bus[10]	1.8-V HSTL Class I	PIN_AR21
QDRIIB_D11	Write data bus[11]	1.8-V HSTL Class I	PIN_AP21
QDRIIB_D12	Write data bus[12]	1.8-V HSTL Class I	PIN_BD22
QDRIIB_D13	Write data bus[13]	1.8-V HSTL Class I	PIN_BC22
QDRIIB_D14	Write data bus[14]	1.8-V HSTL Class I	PIN_BA22
QDRIIB_D15	Write data bus[15]	1.8-V HSTL Class I	PIN_AV22
QDRIIB_D16	Write data bus[16]	1.8-V HSTL Class I	PIN_AY22
QDRIIB_D17	Write data bus[17]	1.8-V HSTL Class I	PIN_AW22
QDRIIB_Q0	Read Data bus[0]	1.8-V HSTL Class I	PIN_AR19
QDRIIB_Q1	Read Data bus[1]	1.8-V HSTL Class I	PIN_AM19
QDRIIB_Q2	Read Data bus[2]	1.8-V HSTL Class I	PIN_AL19
QDRIIB_Q3	Read Data bus[3]	1.8-V HSTL Class I	PIN_AM17
QDRIIB_Q4	Read Data bus[4]	1.8-V HSTL Class I	PIN_AL18
QDRIIB_Q5	Read Data bus[5]	1.8-V HSTL Class I	PIN_AN19
QDRIIB_Q6	Read Data bus[6]	1.8-V HSTL Class I	PIN_AU18
QDRIIB_Q7	Read Data bus[7]	1.8-V HSTL Class I	PIN_AK17
QDRIIB_Q8	Read Data bus[8]	1.8-V HSTL Class I	PIN_AL17
QDRIIB_Q9	Read Data bus[9]	1.8-V HSTL Class I	PIN_AG17
QDRIIB_Q10	Read Data bus[10]	1.8-V HSTL Class I	PIN_AJ18

QDRIIB_Q11	Read Data bus[11]	1.8-V HSTL Class I	PIN_AJ17
QDRIIB_Q12	Read Data bus[12]	1.8-V HSTL Class I	PIN_AG18
QDRIIB_Q13	Read Data bus[13]	1.8-V HSTL Class I	PIN_AU19
QDRIIB_Q14	Read Data bus[14]	1.8-V HSTL Class I	PIN_AW19
QDRIIB_Q15	Read Data bus[15]	1.8-V HSTL Class I	PIN_AV19
QDRIIB_Q16	Read Data bus[16]	1.8-V HSTL Class I	PIN_AP19
QDRIIB_Q17	Read Data bus[17]	1.8-V HSTL Class I	PIN_AN20
QDRIIB_BWS_n0	Byte Write select[0]	1.8-V HSTL Class I	PIN_AV20
QDRIIB_BWS_n1	Byte Write select[1]	1.8-V HSTL Class I	PIN_AU21
QDRIIB_K_p	Clock P	Differential 1.8-V HSTL Class I	PIN_AR20
QDRIIB_K_n	Clock N	Differential 1.8-V HSTL Class I	PIN_AT20
QDRIIB_CQ_p	Echo clock P	1.8-V HSTL Class I	PIN_AJ15
QDRIIB_CQ_n	Echo clock N	1.8-V HSTL Class I	PIN_AP18
QDRIIB_RPS_n	Report Select	1.8-V HSTL Class I	PIN_AW20
QDRIIB_WPS_n	Write Port Select	1.8-V HSTL Class I	PIN_AU20
QDRIIB_DOFF_n	PLL Turn Off	1.8-V HSTL Class I	PIN_AH19
QDRIIB_ODT	On-Die Termination Input	1.8-V HSTL Class I	PIN_AH18
QDRIIB_QVLD	Valid Output Indicator	1.8-V HSTL Class I	PIN_AJ16

**Table 2-16 QDRII+ SRAM C Pin Assignments, Schematic Signal Names, and Functions**

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
QDRIIC_A0	Address bus[0]	1.8-V HSTL Class I	PIN_AV16
QDRIIC_A1	Address bus[1]	1.8-V HSTL Class I	PIN_AW16
QDRIIC_A2	Address bus[2]	1.8-V HSTL Class I	PIN_AP16
QDRIIC_A3	Address bus[3]	1.8-V HSTL Class I	PIN_AW9
QDRIIC_A4	Address bus[4]	1.8-V HSTL Class I	PIN_BD7
QDRIIC_A5	Address bus[5]	1.8-V HSTL Class I	PIN_BC7
QDRIIC_A6	Address bus[6]	1.8-V HSTL Class I	PIN_AR17
QDRIIC_A7	Address bus[7]	1.8-V HSTL Class I	PIN_AR18
QDRIIC_A8	Address bus[8]	1.8-V HSTL Class I	PIN_AT17
QDRIIC_A9	Address bus[9]	1.8-V HSTL Class I	PIN_BB9
QDRIIC_A10	Address bus[10]	1.8-V HSTL Class I	PIN_AH21
QDRIIC_A11	Address bus[11]	1.8-V HSTL Class I	PIN_AG20
QDRIIC_A12	Address bus[12]	1.8-V HSTL Class I	PIN_AU16
QDRIIC_A13	Address bus[13]	1.8-V HSTL Class I	PIN_BB8
QDRIIC_A14	Address bus[14]	1.8-V HSTL Class I	PIN_AT18
QDRIIC_A15	Address bus[15]	1.8-V HSTL Class I	PIN_AW17
QDRIIC_A16	Address bus[16]	1.8-V HSTL Class I	PIN_AV17
QDRIIC_A17	Address bus[17]	1.8-V HSTL Class I	PIN_AU8
QDRIIC_A18	Address bus[18]	1.8-V HSTL Class I	PIN_AT9

QDRIIC_A19	Address bus[19]	1.8-V HSTL Class I	PIN_AV8
QDRIIC_A20	Address bus[20]	1.8-V HSTL Class I	PIN_AN17
QDRIIC_D0	Write data bus[0]	1.8-V HSTL Class I	PIN_AG9
QDRIIC_D1	Write data bus[1]	1.8-V HSTL Class I	PIN_AG10
QDRIIC_D2	Write data bus[2]	1.8-V HSTL Class I	PIN_AG12
QDRIIC_D3	Write data bus[3]	1.8-V HSTL Class I	PIN_AG11
QDRIIC_D4	Write data bus[4]	1.8-V HSTL Class I	PIN_AV10
QDRIIC_D5	Write data bus[5]	1.8-V HSTL Class I	PIN_AH12
QDRIIC_D6	Write data bus[6]	1.8-V HSTL Class I	PIN_AK12
QDRIIC_D7	Write data bus[7]	1.8-V HSTL Class I	PIN_AL12
QDRIIC_D8	Write data bus[8]	1.8-V HSTL Class I	PIN_AJ12
QDRIIC_D9	Write data bus[9]	1.8-V HSTL Class I	PIN_AN12
QDRIIC_D10	Write data bus[10]	1.8-V HSTL Class I	PIN_AM13
QDRIIC_D11	Write data bus[11]	1.8-V HSTL Class I	PIN_AR12
QDRIIC_D12	Write data bus[12]	1.8-V HSTL Class I	PIN_AR13
QDRIIC_D13	Write data bus[13]	1.8-V HSTL Class I	PIN_AU9
QDRIIC_D14	Write data bus[14]	1.8-V HSTL Class I	PIN_AU10
QDRIIC_D15	Write data bus[15]	1.8-V HSTL Class I	PIN_AU11
QDRIIC_D16	Write data bus[16]	1.8-V HSTL Class I	PIN_AV11
QDRIIC_D17	Write data bus[17]	1.8-V HSTL Class I	PIN_AT12
QDRIIC_Q0	Read Data bus[0]	1.8-V HSTL Class I	PIN_BA12
QDRIIC_Q1	Read Data bus[1]	1.8-V HSTL Class I	PIN_AF14
QDRIIC_Q2	Read Data bus[2]	1.8-V HSTL Class I	PIN_AE13
QDRIIC_Q3	Read Data bus[3]	1.8-V HSTL Class I	PIN_AD14
QDRIIC_Q4	Read Data bus[4]	1.8-V HSTL Class I	PIN_AE12
QDRIIC_Q5	Read Data bus[5]	1.8-V HSTL Class I	PIN_AF11
QDRIIC_Q6	Read Data bus[6]	1.8-V HSTL Class I	PIN_AE11
QDRIIC_Q7	Read Data bus[7]	1.8-V HSTL Class I	PIN_AE10
QDRIIC_Q8	Read Data bus[8]	1.8-V HSTL Class I	PIN_AE9
QDRIIC_Q9	Read Data bus[9]	1.8-V HSTL Class I	PIN_BB11
QDRIIC_Q10	Read Data bus[10]	1.8-V HSTL Class I	PIN_AW11
QDRIIC_Q11	Read Data bus[11]	1.8-V HSTL Class I	PIN_AF10
QDRIIC_Q12	Read Data bus[12]	1.8-V HSTL Class I	PIN_AY12
QDRIIC_Q13	Read Data bus[13]	1.8-V HSTL Class I	PIN_AW10
QDRIIC_Q14	Read Data bus[14]	1.8-V HSTL Class I	PIN_AY10
QDRIIC_Q15	Read Data bus[15]	1.8-V HSTL Class I	PIN_BB12
QDRIIC_Q16	Read Data bus[16]	1.8-V HSTL Class I	PIN_BC10
QDRIIC_Q17	Read Data bus[17]	1.8-V HSTL Class I	PIN_BA10
QDRIIC_BWS_n0	Byte Write select[0]	1.8-V HSTL Class I	PIN_AJ11
QDRIIC_BWS_n1	Byte Write select[1]	1.8-V HSTL Class I	PIN_AJ10
QDRIIC_K_p	Clock P	Differential 1.8-V HSTL Class I	PIN_AP12
QDRIIC_K_n	Clock N	Differential 1.8-V HSTL Class I	PIN_AP13

QDRIIC_CQ_p	Echo clock P	1.8-V HSTL Class I	PIN_BC11
QDRIIC_CQ_n	Echo clock N	1.8-V HSTL Class I	PIN_AF13
QDRIIC_RPS_n	Report Select	1.8-V HSTL Class I	PIN_AH10
QDRIIC_WPS_n	Write Port Select	1.8-V HSTL Class I	PIN_AL11
QDRIIC_DOFF_n	PLL Turn Off	1.8-V HSTL Class I	PIN_AE14
QDRIIC_ODT	On-Die Termination Input	1.8-V HSTL Class I	PIN_BD10
QDRIIC_QVLD	Valid Output Indicator	1.8-V HSTL Class I	PIN_BD11

**Table 2-17 QDRII+ SRAM D Pin Assignments, Schematic Signal Names, and Functions**

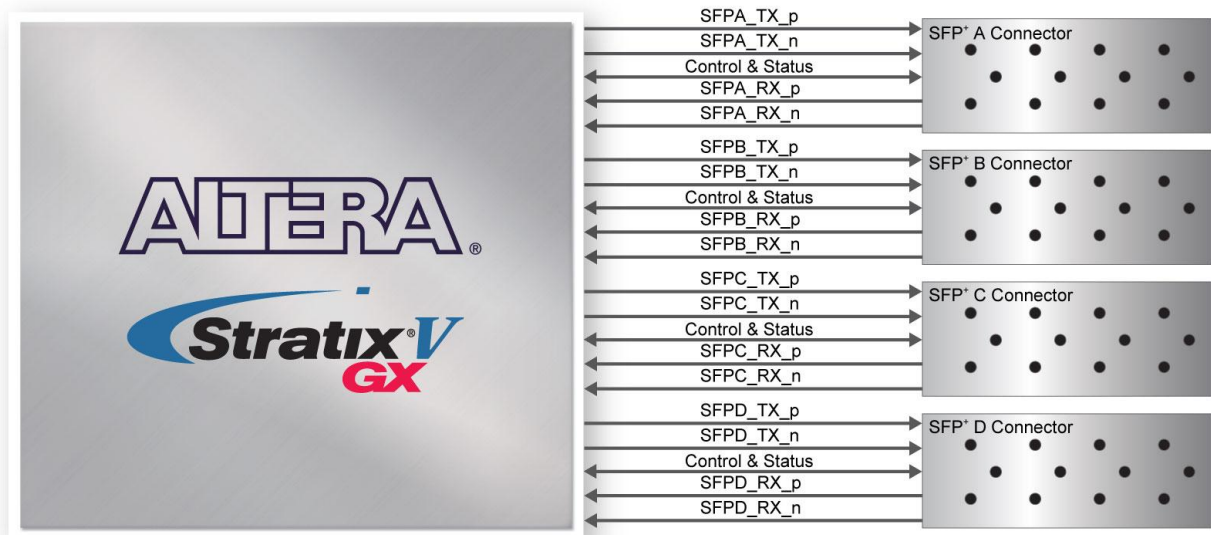
<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
QDRIID_A0	Address bus[0]	1.8-V HSTL Class I	PIN_N26
QDRIID_A1	Address bus[1]	1.8-V HSTL Class I	PIN_P28
QDRIID_A2	Address bus[2]	1.8-V HSTL Class I	PIN_N28
QDRIID_A3	Address bus[3]	1.8-V HSTL Class I	PIN_L26
QDRIID_A4	Address bus[4]	1.8-V HSTL Class I	PIN_K27
QDRIID_A5	Address bus[5]	1.8-V HSTL Class I	PIN_L27
QDRIID_A6	Address bus[6]	1.8-V HSTL Class I	PIN_U26
QDRIID_A7	Address bus[7]	1.8-V HSTL Class I	PIN_T26
QDRIID_A8	Address bus[8]	1.8-V HSTL Class I	PIN_T27
QDRIID_A9	Address bus[9]	1.8-V HSTL Class I	PIN_V27
QDRIID_A10	Address bus[10]	1.8-V HSTL Class I	PIN_U27
QDRIID_A11	Address bus[11]	1.8-V HSTL Class I	PIN_R27
QDRIID_A12	Address bus[12]	1.8-V HSTL Class I	PIN_P27
QDRIID_A13	Address bus[13]	1.8-V HSTL Class I	PIN_V25
QDRIID_A14	Address bus[14]	1.8-V HSTL Class I	PIN_V26
QDRIID_A15	Address bus[15]	1.8-V HSTL Class I	PIN_T25
QDRIID_A16	Address bus[16]	1.8-V HSTL Class I	PIN_P26
QDRIID_A17	Address bus[17]	1.8-V HSTL Class I	PIN_M27
QDRIID_A18	Address bus[18]	1.8-V HSTL Class I	PIN_M28
QDRIID_A19	Address bus[19]	1.8-V HSTL Class I	PIN_P29
QDRIID_A20	Address bus[20]	1.8-V HSTL Class I	PIN_D29
QDRIID_D0	Write data bus[0]	1.8-V HSTL Class I	PIN_H25
QDRIID_D1	Write data bus[1]	1.8-V HSTL Class I	PIN_H24
QDRIID_D2	Write data bus[2]	1.8-V HSTL Class I	PIN_H23
QDRIID_D3	Write data bus[3]	1.8-V HSTL Class I	PIN_J25
QDRIID_D4	Write data bus[4]	1.8-V HSTL Class I	PIN_J24
QDRIID_D5	Write data bus[5]	1.8-V HSTL Class I	PIN_K25
QDRIID_D6	Write data bus[6]	1.8-V HSTL Class I	PIN_D26

QDRIID_D7	Write data bus[7]	1.8-V HSTL Class I	PIN_F25
QDRIID_D8	Write data bus[8]	1.8-V HSTL Class I	PIN_G25
QDRIID_D9	Write data bus[9]	1.8-V HSTL Class I	PIN_N23
QDRIID_D10	Write data bus[10]	1.8-V HSTL Class I	PIN_P24
QDRIID_D11	Write data bus[11]	1.8-V HSTL Class I	PIN_P23
QDRIID_D12	Write data bus[12]	1.8-V HSTL Class I	PIN_L24
QDRIID_D13	Write data bus[13]	1.8-V HSTL Class I	PIN_R24
QDRIID_D14	Write data bus[14]	1.8-V HSTL Class I	PIN_U23
QDRIID_D15	Write data bus[15]	1.8-V HSTL Class I	PIN_U24
QDRIID_D16	Write data bus[16]	1.8-V HSTL Class I	PIN_T24
QDRIID_D17	Write data bus[17]	1.8-V HSTL Class I	PIN_T23
QDRIID_Q0	Read Data bus[0]	1.8-V HSTL Class I	PIN_C27
QDRIID_Q1	Read Data bus[1]	1.8-V HSTL Class I	PIN_A26
QDRIID_Q2	Read Data bus[2]	1.8-V HSTL Class I	PIN_B26
QDRIID_Q3	Read Data bus[3]	1.8-V HSTL Class I	PIN_F26
QDRIID_Q4	Read Data bus[4]	1.8-V HSTL Class I	PIN_G26
QDRIID_Q5	Read Data bus[5]	1.8-V HSTL Class I	PIN_C28
QDRIID_Q6	Read Data bus[6]	1.8-V HSTL Class I	PIN_A29
QDRIID_Q7	Read Data bus[7]	1.8-V HSTL Class I	PIN_A28
QDRIID_Q8	Read Data bus[8]	1.8-V HSTL Class I	PIN_B28
QDRIID_Q9	Read Data bus[9]	1.8-V HSTL Class I	PIN_G28
QDRIID_Q10	Read Data bus[10]	1.8-V HSTL Class I	PIN_F28
QDRIID_Q11	Read Data bus[11]	1.8-V HSTL Class I	PIN_D27
QDRIID_Q12	Read Data bus[12]	1.8-V HSTL Class I	PIN_G29
QDRIID_Q13	Read Data bus[13]	1.8-V HSTL Class I	PIN_F29
QDRIID_Q14	Read Data bus[14]	1.8-V HSTL Class I	PIN_H28
QDRIID_Q15	Read Data bus[15]	1.8-V HSTL Class I	PIN_K28
QDRIID_Q16	Read Data bus[16]	1.8-V HSTL Class I	PIN_J28
QDRIID_Q17	Read Data bus[17]	1.8-V HSTL Class I	PIN_H29
QDRIID_BWS_n0	Byte Write select[0]	1.8-V HSTL Class I	PIN_E26
QDRIID_BWS_n1	Byte Write select[1]	1.8-V HSTL Class I	PIN_K26
QDRIID_K_p	Clock P	Differential 1.8-V HSTL Class I	PIN_L23
QDRIID_K_n	Clock N	Differential 1.8-V HSTL Class I	PIN_K24
QDRIID_CQ_p	Echo clock P	1.8-V HSTL Class I	PIN_E29
QDRIID_CQ_n	Echo clock N	1.8-V HSTL Class I	PIN_H27
QDRIID_RPS_n	Report Select	1.8-V HSTL Class I	PIN_F24
QDRIID_WPS_n	Write Port Select	1.8-V HSTL Class I	PIN_M23
QDRIID_DOFF_n	PLL Turn Off	1.8-V HSTL Class I	PIN_E27
QDRIID_ODT	On-Die Termination Input	1.8-V HSTL Class I	PIN_H26

QDRIID_QVLD	Valid Output Indicator	1.8-V HSTL Class I	PIN_J27
-------------	------------------------	--------------------	---------

## 2.10 SFP+ Ports

The development board has four independent 10G SFP+ connectors that use one transceiver channel each from the Stratix V GX FPGA device. These modules take in serial data from the Stratix V GX FPGA device and transform them to optical signals. The board includes cage assemblies for the SFP+ connectors. **Figure 2-14** shows the connections between the SFP+ and Stratix V GX FPGA.



**Figure 2-14 Connection between the SFP+ and Stratix V GX FPGA**

**Table 2-18** and **Table 2-19** list the SFP+ A, B, C and D pin assignments and signal names relative to the Stratix V GX device.

**Table 2-18 SFP+ A Pin Assignments, Schematic Signal Names, and Functions**

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
SFPA_TX_p	Transmitter data	1.4-V PCML	PIN_AG4
SFPA_TX_n	Transmitter data	1.4-V PCML	PIN_AG3



SFPA_RX_p	Receiver data	1.4-V PCML	PIN_AK2
SFPA_RX_n	Receiver data	1.4-V PCML	PIN_AK1
SFPA_LOS	Signal loss indicator	2.5V	PIN_F22
SFPA_MOD0_PRSNT_n	Module present	2.5V	PIN_E21
SFPA_MOD1_SCL	Serial 2-wire clock	2.5V	PIN_B20
SFPA_MOD2_SDA	Serial 2-wire data	2.5V	PIN_A20
SFPA_RATESEL0	Rate select 0	2.5V	PIN_E20
SFPA_RATESEL1	Rate select 1	2.5V	PIN_G22
SFPA_TXDISABLE	Turns off and disables the transmitter output	2.5V	PIN_B22
SFPA_TXFAULT	Transmitter fault	2.5V	PIN_A22

**Table 2-19 SFP+ B Pin Assignments, Schematic Signal Names, and Functions**

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
SFPB_TX_p	Transmitter data	1.4-V PCML	PIN_AL4
SFPB_TX_n	Transmitter data	1.4-V PCML	PIN_AL3
SFPB_RX_p	Receiver data	1.4-V PCML	PIN_AP2
SFPB_RX_n	Receiver data	1.4-V PCML	PIN_AP1
SFPB_LOS	Signal loss indicator	2.5V	PIN_R22
SFPB_MOD0_PRSNT_n	Module present	2.5V	PIN_K22
SFPB_MOD1_SCL	Serial 2-wire clock	2.5V	PIN_K21
SFPB_MOD2_SDA	Serial 2-wire data	2.5V	PIN_K20
SFPB_RATESEL0	Rate select 0	2.5V	PIN_R21
SFPB_RATESEL1	Rate select 1	2.5V	PIN_T22
SFPB_TXDISABLE	Turns off and disables the transmitter output	2.5V	PIN_H22
SFPB_TXFAULT	Transmitter fault	2.5V	PIN_H20

**Table 2-20 SFP+ C Pin Assignments, Schematic Signal Names, and Functions**

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
SFPC_TX_p	Transmitter data	1.4-V PCML	PIN_AT6
SFPC_TX_n	Transmitter data	1.4-V PCML	PIN_AT5
SFPC_RX_p	Receiver data	1.4-V PCML	PIN_AW4
SFPC_RX_n	Receiver data	1.4-V PCML	PIN_AW3
SFPC_LOS	Signal loss indicator	2.5V	PIN_L21
SFPC_MOD0_PRSNT_n	Module present	2.5V	PIN_J21
SFPC_MOD1_SCL	Serial 2-wire clock	2.5V	PIN_H21
SFPC_MOD2_SDA	Serial 2-wire data	2.5V	PIN_G20
SFPC_RATESEL0	Rate select 0	2.5V	PIN_J22
SFPC_RATESEL1	Rate select 1	2.5V	PIN_P21
SFPC_TXDISABLE	Turns off and disables the transmitter output	2.5V	PIN_F21
SFPC_TXFAULT	Transmitter fault	2.5V	PIN_F20

**Table 2-21 SFP+ C Pin Assignments, Schematic Signal Names, and Functions**

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
SFPD_TX_p	Transmitter data	1.4-V PCML	PIN_AY6
SFPD_TX_n	Transmitter data	1.4-V PCML	PIN_AY5
SFPD_RX_p	Receiver data	1.4-V PCML	PIN_BB2
SFPD_RX_n	Receiver data	1.4-V PCML	PIN_BB1
SFPD_LOS	Signal loss indicator	2.5V	PIN_N22
SFPD_MOD0_PRSENT_n	Module present	2.5V	PIN_V20
SFPD_MOD1_SCL	Serial 2-wire clock	2.5V	PIN_U21
SFPD_MOD2_SDA	Serial 2-wire data	2.5V	PIN_V19
SFPD_RATESEL0	Rate select 0	2.5V	PIN_V21
SFPD_RATESEL1	Rate select 1	2.5V	PIN_M22
SFPD_TXDISABLE	Turns off and disables the transmitter output	2.5V	PIN_U20
SFPD_TXFAULT	Transmitter fault	2.5V	PIN_T21

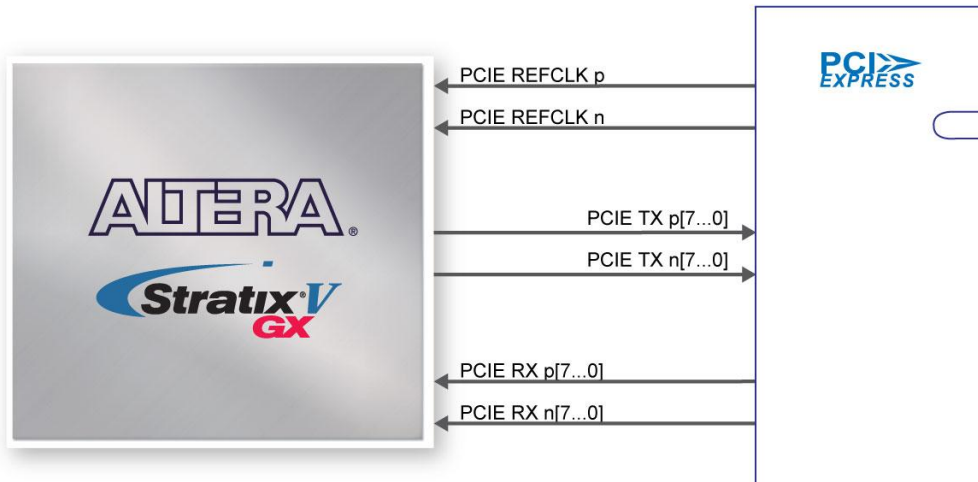
## 2.11 PCI Express

The FPGA development board is designed to fit entirely into a PC motherboard with x8 or x16 PCI Express slot. Utilizing built-in transceivers on a Stratix V GX device, it is able to provide a fully integrated PCI Express-compliant solution for multi-lane (x1, x4, and x8) applications. With the PCI Express hard IP block incorporated in the Stratix V GX device, it will allow users to implement simple and fast protocol, as well as saving logic resources for logic application. **Figure 2-15** presents the pin connection established between the Stratix V GX and PCI Express.

The PCI Express interface supports complete PCI Express Gen1 at 2.5Gbps/lane, Gen2 at 5.0Gbps/lane, and Gen3 at 8.0Gbps/lane protocol stack solution compliant to PCI Express base specification 3.0 that includes PHY-MAC, Data Link, and transaction layer circuitry embedded in PCI Express hard IP blocks.

Please note that it is a requirement that you connect the PCIe external power connector to 6-pin 12V DC power connector in the FPGA to avoid FPGA damage due to insufficient power. The PCIE\_REFCLK\_p signal is a differential input that is driven from the PC motherboard on this board through the PCIe edge connector. A DIP switch (SW7) is connected to the PCI Express to allow different configurations to enable a x1, x4, or x8 PCIe.

**Table 2-22** summarizes the PCI Express pin assignments of the signal names relative to the Stratix V GX FPGA.



**Figure 2-15** PCI Express pin connection

**Table 2-22** PCI Express Pin Assignments, Schematic Signal Names, and Functions

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
PCIE_TX_p0	Add-in card transmit bus	1.4-V PCML	PIN_AY39
PCIE_TX_n0	Add-in card transmit bus	1.4-V PCML	PIN_AY40
PCIE_TX_p1	Add-in card transmit bus	1.4-V PCML	PIN_AV39
PCIE_TX_n1	Add-in card transmit bus	1.4-V PCML	PIN_AV40
PCIE_TX_p2	Add-in card transmit bus	1.4-V PCML	PIN_AT39
PCIE_TX_n2	Add-in card transmit bus	1.4-V PCML	PIN_AT40
PCIE_TX_p3	Add-in card transmit bus	1.4-V PCML	PIN_AU41
PCIE_TX_n3	Add-in card transmit bus	1.4-V PCML	PIN_AU42
PCIE_TX_p4	Add-in card transmit bus	1.4-V PCML	PIN_AN41
PCIE_TX_n4	Add-in card transmit bus	1.4-V PCML	PIN_AN42
PCIE_TX_p5	Add-in card transmit bus	1.4-V PCML	PIN_AL41
PCIE_TX_n5	Add-in card transmit bus	1.4-V PCML	PIN_AL42
PCIE_TX_p6	Add-in card transmit bus	1.4-V PCML	PIN_AJ41
PCIE_TX_n6	Add-in card transmit bus	1.4-V PCML	PIN_AJ42
PCIE_TX_p7	Add-in card transmit bus	1.4-V PCML	PIN_AG41
PCIE_TX_n7	Add-in card transmit bus	1.4-V PCML	PIN_AG42
PCIE_RX_p0	Add-in card receive bus	1.4-V PCML	PIN_BB43

PCIE_RX_n0	Add-in card receive bus	1.4-V PCML	PIN_BB44
PCIE_RX_p1	Add-in card receive bus	1.4-V PCML	PIN_BA41
PCIE_RX_n1	Add-in card receive bus	1.4-V PCML	PIN_BA42
PCIE_RX_p2	Add-in card receive bus	1.4-V PCML	PIN_AW41
PCIE_RX_n2	Add-in card receive bus	1.4-V PCML	PIN_AW42
PCIE_RX_p3	Add-in card receive bus	1.4-V PCML	PIN_AY43
PCIE_RX_n3	Add-in card receive bus	1.4-V PCML	PIN_AY44
PCIE_RX_p4	Add-in card receive bus	1.4-V PCML	PIN_AT43
PCIE_RX_n4	Add-in card receive bus	1.4-V PCML	PIN_AT44
PCIE_RX_p5	Add-in card receive bus	1.4-V PCML	PIN_AP43
PCIE_RX_n5	Add-in card receive bus	1.4-V PCML	PIN_AP44
PCIE_RX_p6	Add-in card receive bus	1.4-V PCML	PIN_AM43
PCIE_RX_n6	Add-in card receive bus	1.4-V PCML	PIN_AM44
PCIE_RX_p7	Add-in card receive bus	1.4-V PCML	PIN_AK43
PCIE_RX_n7	Add-in card receive bus	1.4-V PCML	PIN_AK44
PCIE_REFCLK_p	Motherboard reference clock	HCSL	PIN_AK38
PCIE_REFCLK_n	Motherboard reference clock	HCSL	PIN_AK39
PCIE_PERST_n	Reset	2.5-V	PIN_AU33
PCIE_SMBCLK	SMB clock	2.5-V	PIN_BD34
PCIE_SMBDAT	SMB data	2.5-V	PIN_AT33
PCIE_WAKE_n	Wake signal	2.5-V	PIN_BD35
PCIE_PRSENT1n	Hot plug detect	-	-
PCIE_PRSENT2n_x1	Hot plug detect x1 PCIe slot enabled using SW3 dip switch	-	-
PCIE_PRSENT2n_x4	Hot plug detect x4 PCIe slot enabled using SW3 dip switch	-	-
PCIE_PRSENT2n_x8	Hot plug detect x8 PCIe slot enabled using SW3 dip switch	-	-

## 2.12 SATA

Four Serial ATA (SATA) ports are available on the FPGA development board which are computer bus standard with a primary function of transferring data between the motherboard and mass storage devices (such as hard drives, optical drives, and solid-state disks). Supporting a storage interface is just one of many different applications an FPGA can be used in storage appliances. The Stratix V GX device can bridge different protocols such as bridging simple bus I/Os like PCI Express (PCIe) to SATA or network interfaces such as Gigabit Ethernet (GbE) to SATA. The SATA interface supports SATA 3.0 standard with connection speed of 6 Gbps based on Stratix V GX device with integrated transceivers compliant to SATA electrical standards.

The four Serial ATA (SATA) ports include two available ports for device and two available ports for host capable of implementing SATA solution with a design that consists of both host and target (device side) functions. **Figure 2-16** depicts the host and device design examples.



**Figure 2-16 PC and storage device connection to the Stratix V GX FPGA**

The transmitter and receiver signals of the SATA ports are connected directly to the Stratix V GX transceiver channels to provide SATA IO connectivity to both host and target devices. To verify the functionality of the SATA host/device ports, a connection can be established between the two ports by using a SATA cable as **Figure 2-17** depicts the associated signals connected. **Figure 2-17** lists the SATA pin assignments, signal names and functions.

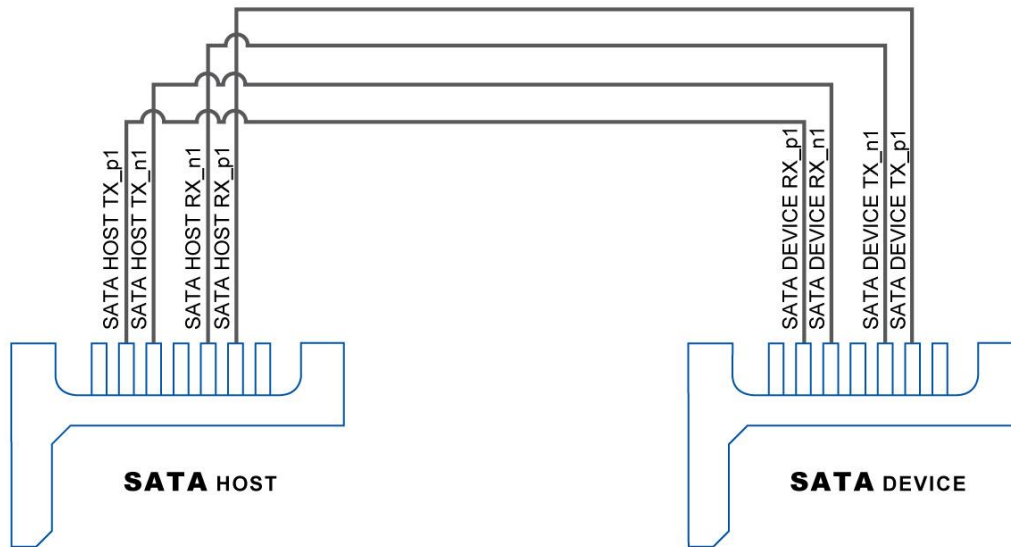


Figure 2-17 Pin connection between SATA connectors

Table 2-23 lists the SATA pin assignments, signal names and functions.

Table 2-23 Serial ATA Pin Assignments, Schematic Signal Names, and Functions

<i>Schematic Signal Name</i>	<i>Description</i>	<i>I/O Standard</i>	<i>Stratix V GX Pin Number</i>
<b>Device</b>			
SATA_DEVICE_RX_p0	Differential receive data input after DC blocking capacitor	1.4-V PCML	PIN_K43
SATA_DEVICE_RX_n0	Differential receive data input after DC blocking capacitor	1.4-V PCML	PIN_K44
SATA_DEVICE_TX_n0	Differential transmit data output before DC blocking capacitor	1.4-V PCML	PIN_K40
SATA_DEVICE_TX_p0	Differential transmit data output before DC blocking capacitor	1.4-V PCML	PIN_K39
SATA_DEVICE_RX_p1	Differential receive data input after DC blocking capacitor	1.4-V PCML	PIN_H43
SATA_DEVICE_RX_n1	Differential receive data input after DC blocking capacitor	1.4-V PCML	PIN_H44
SATA_DEVICE_TX_n1	Differential transmit data output before DC blocking capacitor	1.4-V PCML	PIN_H40
SATA_DEVICE_TX_p1	Differential transmit data output before DC blocking capacitor	1.4-V PCML	PIN_H39
SATA_DEVICE_REFCLK_p	Reference Clock	HCSL	PIN_V39

SATA_DEVICE_REFCLK_n	Reference Clock	HCSL	PIN_V40
<b>Host</b>			
SATA_HOST_TX_p0	Differential transmit data output before DC blocking capacitor	1.4-V PCML	PIN_K6
SATA_HOST_TX_n0	Differential transmit data output before DC blocking capacitor	1.4-V PCML	PIN_K5
SATA_HOST_RX_n0	Differential receive data input after DC blocking capacitor	1.4-V PCML	PIN_K1
SATA_HOST_RX_p0	Differential receive data input after DC blocking capacitor	1.4-V PCML	PIN_K2
SATA_HOST_TX_p1	Differential transmit data output before DC blocking capacitor	1.4-V PCML	PIN_H6
SATA_HOST_TX_n1	Differential transmit data output before DC blocking capacitor	1.4-V PCML	PIN_H5
SATA_HOST_RX_n1	Differential receive data input after DC blocking capacitor	1.4-V PCML	PIN_H1
SATA_HOST_RX_p1	Differential receive data input after DC blocking capacitor	1.4-V PCML	PIN_H2
SATA_HOST_REFCLK_p	Reference Clock	HCSL	PIN_V6
SATA_HOST_REFCLK_n	Reference Clock	HCSL	PIN_V5

## Chapter 3

# *System Builder*

---

This chapter describes how users can create a custom design project on the FPGA board by using the Software Tools – System Builder.

### **3.1 Introduction**

The System Builder is a Windows based software utility, designed to assist users to create a Quartus Prime project for the FPGA board within minutes. The generated Quartus Prime project files include:

- Quartus Prime Project File (.qpf)
- Quartus Prime Setting File (.qsf)
- Top-Level Design File (.v)
- External PLL Controller (.v)
- Synopsis Design Constraints file (.sdc)
- Pin Assignment Document (.htm)

The System Builder not only can generate the files above, but can also provide error-checking rules to handle situation that are prone to errors. The common mistakes that users encounter are the following:

- Board damaged for wrong pin/bank voltage assignment.
- Board malfunction caused by wrong device connections or missing pin counts for connected ends.
- Performance dropped because of improper pin assignments



## 3.2 General Design Flow

This section will introduce the general design flow to build a project for the FPGA board via the System Builder. The general design flow is illustrated in the **Figure 3-1**.

Users should launch System Builder and create a new project according to their design requirements. When users complete the settings, the System Builder will generate two major files which include top-level design file (.v) and the Quartus Prime setting file (.qsf).

The top-level design file contains top-level Verilog wrapper for users to add their own design/logic. The Quartus Prime setting file contains information such as FPGA device type, top-level pin assignment, and I/O standard for each user-defined I/O pin.

Finally, Quartus Prime programmer must be used to download SOF file to the FPGA board using JTAG interface.

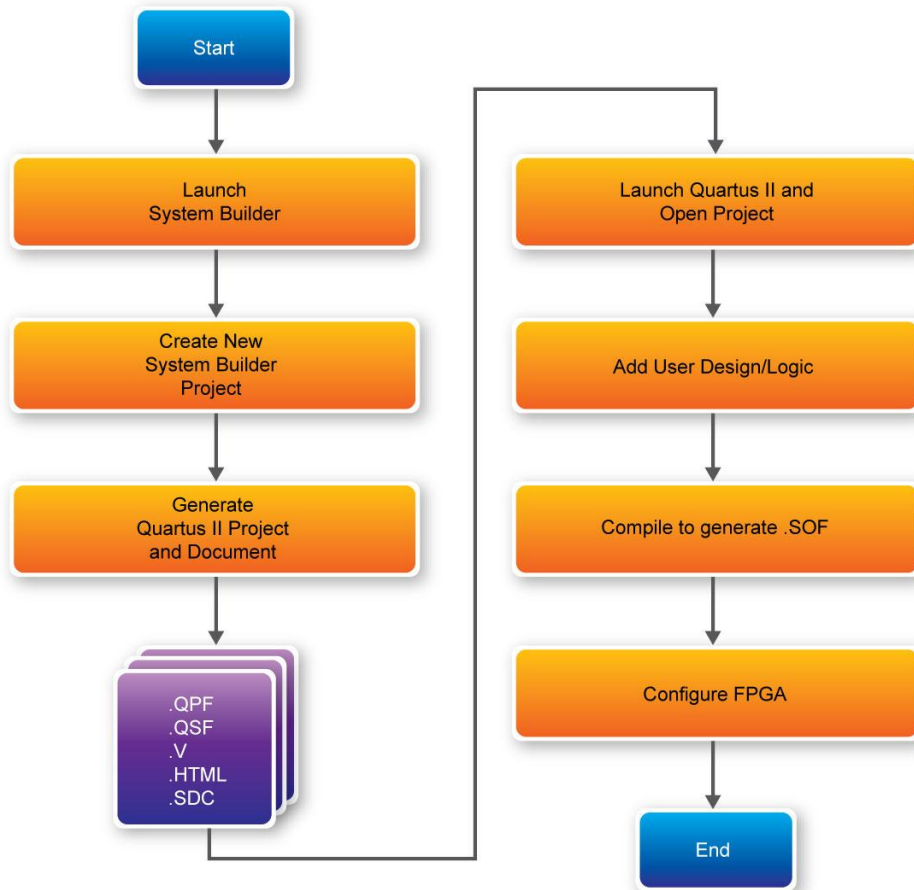


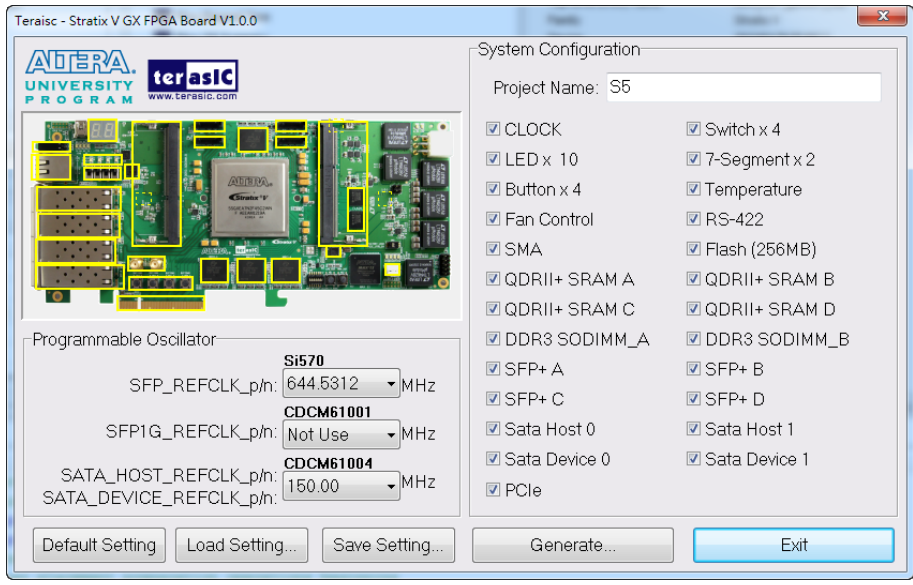
Figure 3-1 The general design flow of building a design

### 3.3 Using System Builder

This section provides the detail procedures on how the System Builder is used.

#### ■ Install and launch the System Builder

The System Builder is located in the directory: "**Tools\SystemBuilder**" in the System CD. Users can copy the whole folder to a host computer without installing the utility. Before using the System Builder, execute the **SystemBuilder.exe** on the host computer as appears in **Figure 3-2**.

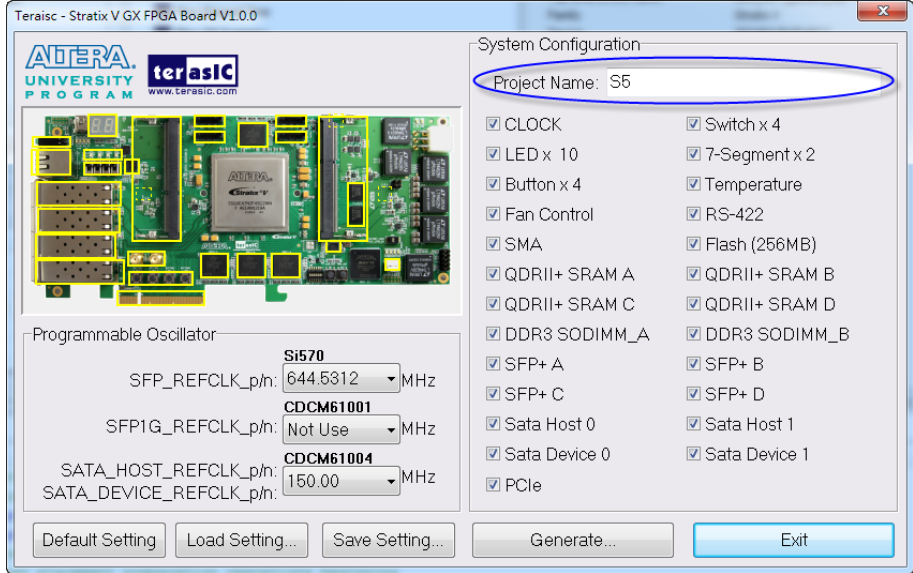


**Figure 3-2 The System Builder window**

■ **Select Board Type and Input Project Name**

Select the target board type and input project name as show in **Figure 3-3**.

■ **Project Name: Specify the project name as it is automatically assigned to the name of the top-level design entity.**



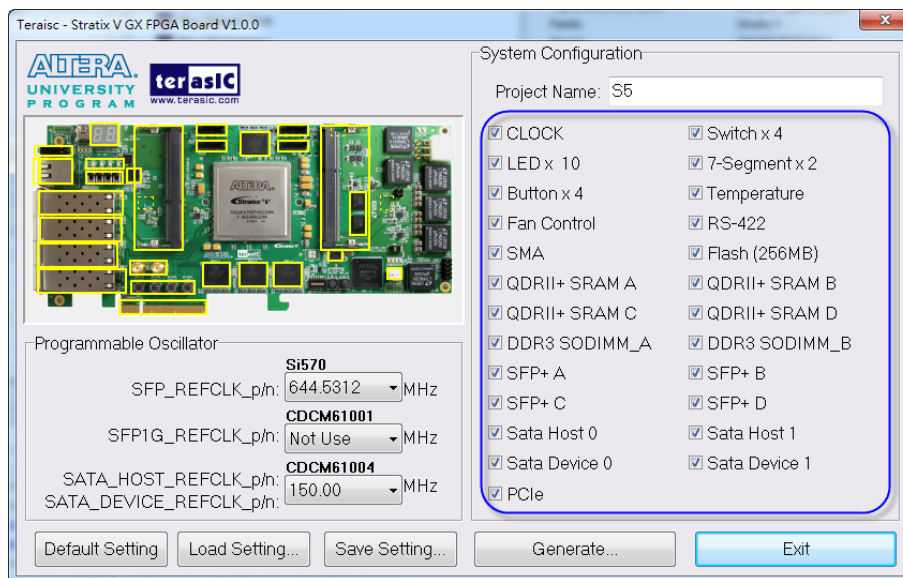
**Figure 3-3 The Quartus Project Name**

■ **System Configuration**

Under System Configuration users are given the flexibility of enabling their choice of components

on the FPGA as shown in **Figure 3-4**. Each component of the FPGA board is listed where users can enable or disable a component according to their design by simply marking a check or removing the check in the field provided. If the component is enabled, the System Builder will automatically generate the associated pin assignments including the pin name, pin location, pin direction, and I/O standards.

**Note:** The pin assignments for some components (e.g. DDR3 and SFP+) require associated controller codes in the Quartus project otherwise Quartus will result in compilation errors. Therefore, do not select them if they are not necessary in your design. To use the DDR3 controller, please refer to the DDR3 SDRAM demonstration in Chapter 6.



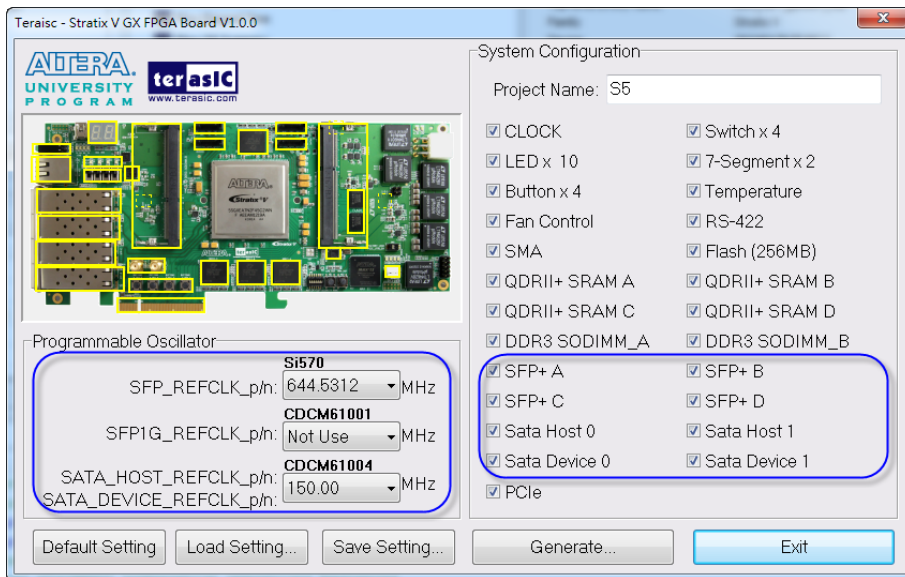
**Figure 3-4 System Configuration Group**

## ■ Programmable Oscillator

There are two external oscillators on-board that provide reference clocks for the following signals SFP\_REFCLK, SFP1G\_REFCLK, SATA\_HOST\_REFCLK and SATA\_DEVICE\_REFCLK. To use these oscillators, users can select the desired frequency on the Programmable Oscillator group, as shown in **Figure 3-5**. SFP+ or SATA should be checked before users can start to specify the desired frequency in the programmable oscillators.

As the Quartus project is created, System Builder automatically generates the associated controller according to users' desired frequency in Verilog which facilitates users' implementation as no additional control code is required to configure the programmable oscillator.

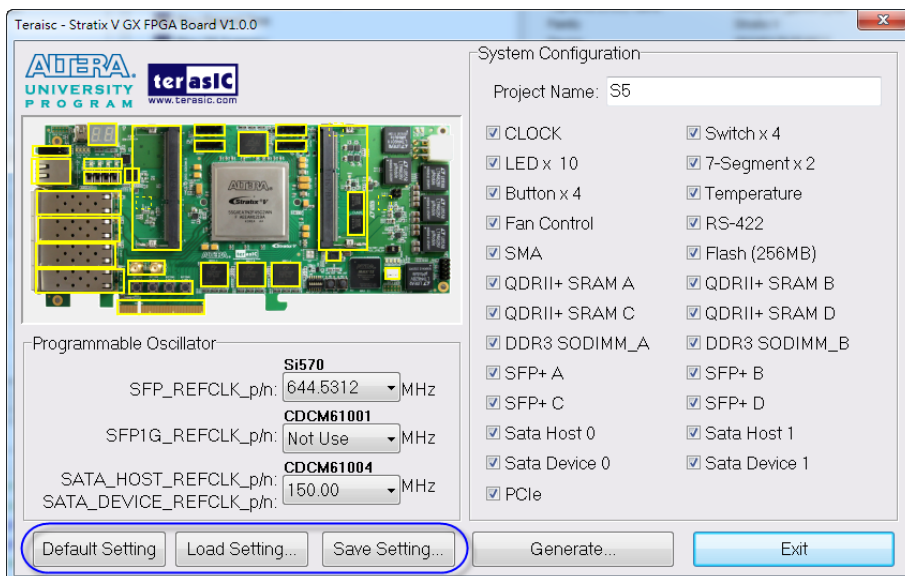
**Note:** If users need to dynamically change the frequency, they would need to modify the generated control code themselves.



**Figure 3-5 External Programmable Oscillators**

## ■ Project Setting Management

The System Builder also provides functions to restore default setting, loading a setting, and saving users' board configuration file shown in **Figure 3-6**. Users can save the current board configuration information into a .cfg file and load it to the System Builder.



**Figure 3-6 Project Settings**

## ■ Project Generation

When users press the **Generate** button, the System Builder will generate the corresponding Quartus Prime files and documents as listed in the **Table 3-1** in the directory specified by the user.

**Table 3-1 The files generated by System Builder**

No.	Filename	Description
1	<Project name>.v	Top level Verilog file for Quartus Prime
2	Si570_controller.v(*)	Si570 External Oscillator controller IP
3	<Project name>.qpf	Quartus Prime Project File
4	<Project name>.qsf	Quartus Prime Setting File
5	<Project name>.sdc	Synopsis Design Constraints file for Quartus Prime
6	<Project name>.htm	Pin Assignment Document

(\*) The Si570 Controller includes seven files: Si570\_controller.v, initial\_config.v, clock\_divider.v, edge\_detector.v, i2c\_reg\_controller.v, i2c\_controller.v and i2c\_bus\_controller.v.

Users can use Quartus Prime software to add custom logic into the project and compile the project to generate the SRAM Object File (.sof).

For Si570, the Controller will be instantiated in the Quartus Prime top-level file as listed below:

```

//=====
//  Configure SI570 as 644.5312 MHz =====
//=====

si570_controller si570_controller_inst (
    .iCLK(OSC_50_B3B), // system clock 50mhz
    .iRST_n(BUTTON[0]), // system reset;
    .iFREQ_MODE(3'b110),
    .I2C_CLK(CLOCK_SCL),
    .I2C_DATA(CLOCK_SDA),
    .oController_Ready()
);

```

For CDCM61001 and CDCM61004, the Controller will be instantiated in the Quartus Prime top-level file as listed below:

```
//=====
// CDCM61001/CDCM61004 External PLL Configuration
// Configure CDCM61001 as 125 MHz
// Configure CDCM61004 as 150 MHz
//=====

// Signal declarations
wire [ 3: 0] clk1_set_wr, clk2_set_wr, clk3_set_wr;
wire        rstn;
wire        conf_ready;
wire        counter_max;
wire [7:0]  counter_inc;
reg  [7:0]  auto_set_counter;
reg        conf_wr;

// Structural coding
assign clk1_set_wr = 4'd5; //125 MHz
assign clk2_set_wr = 4'd6; //150 MHz
assign clk3_set_wr = 4'd0; //Unchange

assign rstn = CPU_RESET_n;
assign counter_max = &auto_set_counter;
assign counter_inc = auto_set_counter + 1'b1;

always @(posedge OSC_50_B3B or negedge rstn)
    if(!rstn)
        begin
            auto_set_counter <= 0;
            conf_wr <= 0;
        end
    else if (counter_max)
        conf_wr <= 1;
    else
        auto_set_counter <= counter_inc;
```

```

ext_pll_ctrl ext_pll_ctrl_Inst (
    .osc_50 (OSC_50_B3B), //50MHZ
    .rstn (rstn),

    // device 1 (SFP1G_REFCLK_p)
    .clk1_set_wr (clk1_set_wr),
    .clk1_set_rd (),

    // device 2 (SATA_HOST_REFCLK_p/SATA_DEVICE_REFCLK_p)
    .clk2_set_wr (clk2_set_wr),
    .clk2_set_rd (),

    // device 3 (reserved)
    .clk3_set_wr (clk3_set_wr),
    .clk3_set_rd (),

    // setting trigger
    .conf_wr (conf_wr), // 1T 50MHz
    .conf_rd (), // 1T 50MHz

    // status
    .conf_ready (conf_ready),

    // 2-wire interface
    .max_sclk (PLL_SCL),
    .max_sdat (PLL_SDA)
);

```

If dynamic configuration for the oscillator is required, users need to modify the code according to users' desired behavior.



# Flash Programming

As you develop your own project using the Altera tools, you can program the flash memory device so that your own design loads from flash memory into the FPGA on power up. This chapter will describe how to use Altera Quartus Prime Programmer Tool to program the common flash interface (CFI) flash memory device on the FPGA board. The Stratix V GX FPGA development board ships with the CFI flash device preprogrammed with a default factory FPGA configuration for running the Parallel Flash Loader design example.

## 4.1 CFI Flash Memory Map

**Table 4-1** shows the default memory contents of two interlaced 1Gb (128MB) CFI flash device. Each flash device has a 16-bit data bus and the two combined flash devices allow for a 32-bit flash memory interface. For the factory default code to run correctly and update designs in the user memory, this memory map must not be altered.

**Table 4-1 Flash Memory Map (Byte Address)**

<i>Block Description</i>	<i>Size(KB)</i>	<i>Address Range</i>
<b>PFL option bits</b>	<b>64</b>	<b>0x00030000 – 0x0003FFFF</b>
<b>Factory hardware</b>	<b>33,280</b>	<b>0x00040000 – 0x020BFFFF</b>
<b>User hardware</b>	<b>33,280</b>	<b>0x020C0000 – 0x0413FFFF</b>
<b>Factory software</b>	<b>8,192</b>	<b>0x04140000 – 0x0493FFFF</b>
<b>User software and data</b>	<b>187,136</b>	<b>0x04940000 – 0x0FFFFFFF</b>

For user application, user hardware must be stored with start address **0x020C0000**, and the user's software is suggested to be stored with start address **0x04940000**. The NIOS II EDS tool **nios-2-flash-programmer** is used for programming the flash. Before programming, users need to translate their Quartus .sof and NIOS II .elf files into the .flash which is used by the

**nios-2-flash-programmer**. For .sof to .flash translation, NIOS II EDS tool **sof2flash** can be used. For the .elf to .flash translation, NIOS II EDS tool **elf2flash** can be used. For convenience, the System CD contains a batch file for file translation and flash programming with users given .sof and .elf file.

## 4.2 FPGA Configure Operation

Here is the procedure to enable FPGA configuration from Flash:

1. Please make sure the FPGA configuration data has been stored in the CFI flash.
2. Set the FPGA configuration mode to FPPx32 mode by setting SW6 MSEL[0:4] as 00010
3. Specify the configuration of the FPGA using the default Factory Configuration or User Configuration by setting SW5 according to **Figure 4-1**.
4. Power on the FPGA board or press MAX\_RST button if board is already powered on
5. When configuration is completed, the green Configure Done LED will light. If there is error, the red Configure Error LED will light.

## 4.3 Flash Programming with Users Design

Users can program the flash memory device so that a custom design loads from flash memory into the FPGA on power up. For convenience, the translation and programming batch files are available on the Demonstrations/Hello/flash\_programming\_batch folder in the System CD. There folder contains five files as shown in **Table 4-2**

**Table 4-2 Flash Memory Map (Byte Address)**

<i>Files Name</i>	<i>Description</i>
<b>S5_PFL.sof</b>	<b>Parallel Flash Loader Design</b>
<b>flash_program_ub2.bat</b>	<b>Top batch file to download S5_PFL.sof and launch batch flash_program_bashrc_ub2</b>
<b>flash_program_bashrc_ub2</b>	<b>Translate .sof and .elf into .flash and programming flash with the generated .flash file</b>
<b>Golden_top.sof</b>	<b>Hardware design file for Hello Demo</b>
<b>HELLO_NIOS.elf</b>	<b>Software design file for Hello Demo</b>

To apply the batch file to users' .sof and .elf file, users can change the .sof and .elf filename in the `flash_program_bashrc_ub2` file as shown in **Figure 4-2**.

```
sof2flash --input=Golden_top.sof --output=flash_hw.flash --offset=0x20C0000 --pfl  
elf2flash --base=0x0 --end=0x0FFFFFFF --reset=0x04940000 --input=HELLO_NIOS.elf --
```

**Figure 4-1 Change to users' .sof and .elf filename**

If your design does not contain a NIOS II processor, users can add “#” to comment (disable) the `elf2flash` and `nios-flash-programmer` commands in the `flash_program_bashrc_ub2` file as shown in **Figure 4-2**.

```
↓  
#conver to .flash↓  
"$SOPC_KIT_NIOS2/nios2_command_shell.sh" sof2flash --input=Golden_top.sof --output=flash_hw.↓  
"$SOPC_KIT_NIOS2/nios2_command_shell.sh" elf2flash --base=0x0 --end=0x0FFFFFFF --reset=0x049↓  
↓  
↓  
↓  
#Programming with .flash↓  
"$SOPC_KIT_NIOS2/nios2_command_shell.sh" nios2-flash-programmer --base=0x0 flash_hw.flash↓  
"$SOPC_KIT_NIOS2/nios2_command_shell.sh" nios2-flash-programmer --base=0x0 flash_sw.flash←
```

**Figure 4-2 Disable .elf translation and programming**

If your design includes a NIOS II processor and the NIOS II program is stored on external memory, users must to perform following items so the NIOS II program can be boot from flash successfully:

1. QSYS should include a Flash controller for the CFI Flash on the development board. Please ensure that the base address of the controller is 0x00, as shown in **Figure 4-3**.
2. In NIOS II processor options, select FLASH as reset vector memory and specify 0x04940000 as reset vector, as shown in **Figure 4-4**.

System Contents		Address Map	Clock Settings	Project Settings	Instance Parameters	System Inspector	HDL Example	Generation
Use	Connections	Name	Description	Export	Clock	Base		
<input checked="" type="checkbox"/>		cpu	Nios II Processor					
		clk	Clock Input	Click	sys_...			
		reset_n	Reset Input	Click	[clk]			
		data_master	Avalon Memory Mapped Master	Click	[clk]			IRQ 0
		instruction_master	Avalon Memory Mapped Master	Click	[clk]			
		jtag_debug_module_reset	Reset Output	Click	[clk]			
		jtag_debug_module	Avalon Memory Mapped Slave	Click	[clk]			0x11400800
		custom_instruction_master	Custom Instruction Master	Click				
		cfi_flash_atb_bridge_0	Tri-State Conduit Bridge					
		clk	Clock Input	Click	sys_...			
		reset	Reset Input	Click	[clk]			
		tcs	Tristate Conduit Slave	Click	[clk]			
		out	Conduit		cfi_fl...			
		ext_flash	Generic Tri-State Controller					
		clk	Clock Input	Click	sys_...			
		reset	Reset Input	Click	[clk]			
		uas	Avalon Memory Mapped Slave	Click	[clk]			0x00000000
		tcm	Tristate Conduit Master	Click	[clk]			

Figure 4-3 Flash Controller Settings in QSYS

Reset Vector	
Reset vector memory:	ext_flash.uas
Reset vector offset:	0x04940000
Reset vector:	0x04940000

Figure 4-4 Reset Vector Settings for NIOS II Processor

For implementation detail, users can refer the Hello example located in the CD folder:

Demonstrations/ Hello

## 4.4 Restore Factory Settings

This section describes how to restore the original factory contents to the flash memory device on the FPGA development board. Perform the following instructions:

1. Make sure the Nios II EDS and USB-Blaster II driver are installed.
2. Make sure the FPGA board and PC are connected with an UBS Cable.

3. Power on the FPGA board.
4. Copy the “Demonstrations/PFL/flash\_programming\_batch” folder under the CD to your PC’s local drive.
5. Execute the batch file flash\_program\_ub2.bat to start flash programming.
6. Power off the FPGA Board.
7. Set FPGA configure mode as FPPx32 Mode by setting SW6 MSEL[0:4] to 00010.
8. Specify configuration of the FPGA to Factory Hardware by setting the FACTORY\_LOAD dip in SW5 to the ‘1’ position.
9. Power on the FPGA Board, and the Configure Done LED should light.

Except for programming the Flash with the default code PFL, the batch file also writes PFL (Parallel Flash Loader) Option Bits data into the address 0x30000. The option bits data specifies 0x20C0000 as start address of your hardware design.

The NIOS II EDS tool **nios-2-flash-programmer** programs the Flash based on the Parallel Flasher Loader design in the FPGA. The Parallel Flash Loader design is included in the default code PFL and the source code is available in the folder Demonstrations/ PFL in System CD.

## Chapter 5

# *Programmable Oscillator*

This chapter describes how to program the two programmable oscillators Si570 and CDCM61004 on the FPGA board. Also, RTL code based and Nios based reference design are explained in the chapter. The source codes of these examples are all available on the FPGA System CD.

### 5.1 Overview

This section describes how to program Si570- and CDCM61004. For detail programming information, please refer to their datasheets which are available on the FPGA System CD.

#### ■ Si570

The Si570 utilizes Silicon Laboratories advanced DSPLL® circuitry to provide a low-jitter clock at any frequency. The Si570 are user-programmable to any output frequency from 10 to 945 MHz and select frequencies to 1400 MHz with < 1ppb resolution. The device is programmed via an I2C serial interface. The differential clock output of the Si570 directly connects to dedicated reference clock input of the Stratix V GX transceiver for SFP+ channels. Many applications can be implemented using this function. For example, the 10G Ethernet application can be designed onto this board by feeding a necessary clock frequency of 644.53125MHz or 322.265625MHz from the Si570.

**Figure 5-1** shows the block diagram of Si570 device. Users can modify the value of the three registers RFREQ, HS\_DIV, and N1 to generate the desired output frequency.

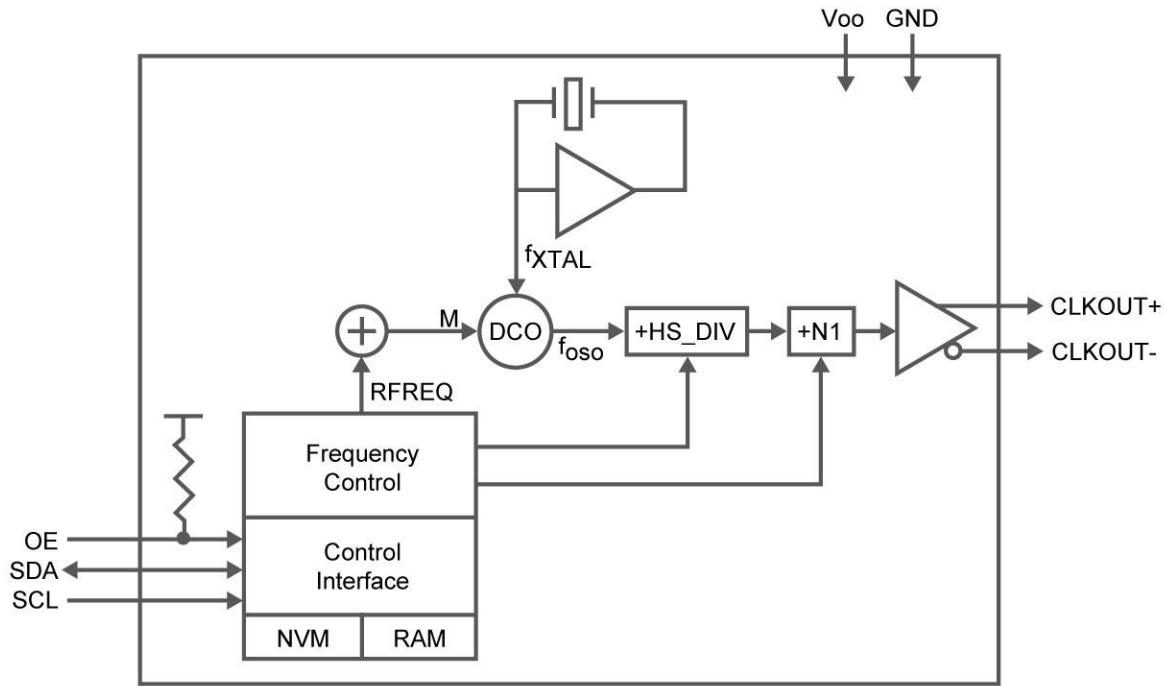


Figure 5-1 Si570 Block diagram

The output frequency is calculated using the following equation:

$$f_{out} = \frac{f_{DCO}}{\text{Output Dividers}} = \frac{f_{XTAL} \times RFREQ}{HSDIV \times N1}$$

When Si570 is powered on, the default output frequency is 100 MHz. Users can program the output frequency through the I2C interface using the following procedure.

6. Freeze the DCO (bit 4 of Register 137).
7. Write the new frequency configuration (RFREQ,HSDIV, and N1) to Register 7 – 12.
8. Unfreeze the DCO and assert the NewFreq bit (bit 6 of Register 135).

The I2C address of Si570 is zero and it supports fast mode operation whose transfer rate is up to 400 kbps. **Table 5-1** shows the register table for Si570.

**Table 5-1 Si570 Register Table**

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7	High Speed/N1 Dividers	HS_DIV[2:0]			N1[6:2]				
8	Reference Frequency	N1[1:0]		RFREQ[37:32]					
9	Reference Frequency	RFREQ[31:24]							
10	Reference Frequency	RFREQ[23:16]							
11	Reference Frequency	RFREQ[15:8]							
12	Reference Frequency	RFREQ[7:0]							
135	Reference Frequency	RST_REG	NewFreq	Freeze M	Freeze VCADC				RECALL
137	Reference Frequency				Freeze DCO				

Table 5-2 lists the register settings for some common used frequency.

**Table 5-2 Si570 Register Table**

Output Frequency (MHz)	HS_DIV	HS_DIV Register Setting	NI	NI Register Setting	REF_CLK Register Setting
100	9	101	6	0000101	02F40135A9(hex)
125	11	111	4	0000011	0302013B65(hex)
156.25	9	101	4	0000011	0313814290(hex)
250	11	111	2	0000001	0302013B65(hex)
312.5	9	101	2	0000001	0313814290(hex)
322.265625	4	000	4	0000011	02D1E127AF(hex)
644.53125	4	000	2	0000001	02D1E127AF(hex)



## ■ CDCM61004

The FPGA board includes another programmable PLL CDCM61004. The CDCM61004 supports output frequency range from 43.75 MHz to 683.264 MHz. It provides a parallel interface for selecting a desired output frequency. The Stratix V GX FPGA's IOs connect to the interface directly. The differential clock outputs of the CDCM61004 are designed for SFP+ and SATA applications on FPGA board.

When CDCM61004 is powered on, the default output frequency is 100 MHz. Users can change the output frequency by the following control pins:

1. PR0 and PR1
2. OD0, OD1, and OD2
3. RSTN
4. CE
5. OS0 and OS1

The following table lists the frequency which CDCM61004 can generate in the FPGA board.

PRESCALLR DIVIDER	FEEDBACK DIVIDER	OUTPUT DEVIDER	OUTPUT FREQUENCY(MHz)	APPLICATION
4	20	8	62.5	GigE
3	24	8	75	SATA
3	24	6	100	PCI Express
4	20	4	125	GigE
3	24	4	150	SATA
3	25	4	156.25	10 GigE
5	15	2	187.5	12 GigE
3	24	3	200	PCI Express
4	20	2	250	GigE
4	20	2	312.5	XGMII
3	25	1	625	10 GigE

The both values of PRESCALER DIVIDER and FEEDBACK DIVIDER can be specified by the PR0 and PR1 control pins according to the following table:

CONTROL INPUTS		PRESCALER DIVIDER	FEEDBACK DIVIDER
PR1	PR0		
0	0	3	24
0	1	5	15
1	0	3	25
1	1	4	20

The value of OUTPUT DIVIDER can be specified by the OD0, OD1 and OD2 control pins according to the following table:

CONTROL INPUTS			OUTPUT DIVIDER
OD2	OD1	OD0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	Reserved
1	0	1	6
1	1	0	Reserved
1	1	1	8

After specifying the desired output frequency in the parallel interface, developers must assert the output enable pin CE and control the RSTN pin to generate a rising signal to start the PLL Recalibration process. In the FPGA board, the required output type is LVDS, so always set OS0 and SO1 to 0 and 1, respectively.

## 5.2 Si570 Example by RTL

In this section we will demonstrate how to use the Terasic Si570 Controller implemented in Verilog to control the Si570 programmable oscillator on the FPGA board. This controller IP can configure the Si570 to output a clock with a specific frequency via I2C interface. For demonstration, the output clock is used to implement a counter where the MSB is used to drive an LED, so the user can get the result from the frequency of the LED blinking. We will also introduce the port declarations and associated parameter settings of this IP. **Figure 5-2** shows the block diagram of this demonstration.

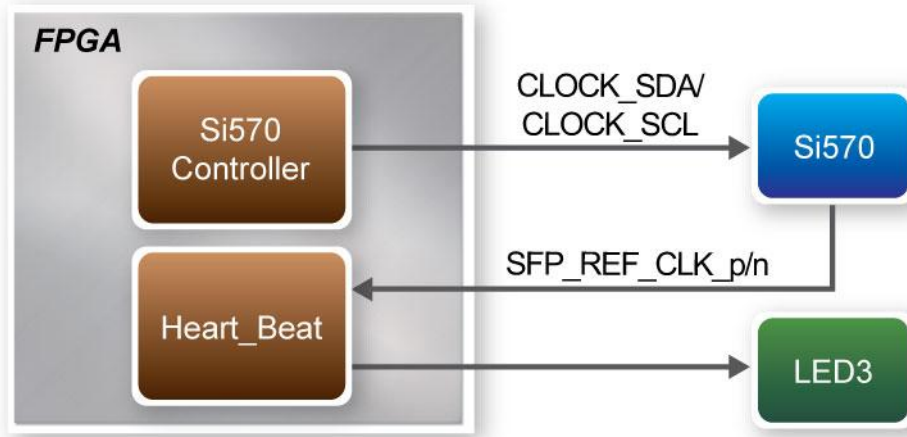


Figure 5-2 Block Diagram of this Demonstration

■ **Block Diagrams of Si570 Controller IP**

The block diagram of the Si570 controller is shown on **Figure 5-3**. Shown here are four blocks named `i2c_reg_controller`, `i2c_bus_controller`, `clock_divider` and `initial_config` in Si570 controller IP. Firstly, the `i2c_reg_controller` will generate an associated Si570 register value for the `i2c_bus_controller` based on user-desired frequency. Once `i2c_bus_controller` receives this data, it will transfer these settings to Si570 via serial clock and data bus using I2C protocol. The registers in Si570 will be configured and output the user-desired frequency.

Secondly, the `clock_divider` block will divide system clock (50 MHz) into 97.6 KHz which is used as I2C interface clock of `i2c_bus_controller`. Finally, the `initial_config` block will generate a control signal to drive `i2c_reg_controller` which allows the Si570 controller to configure Si570 based on default settings.

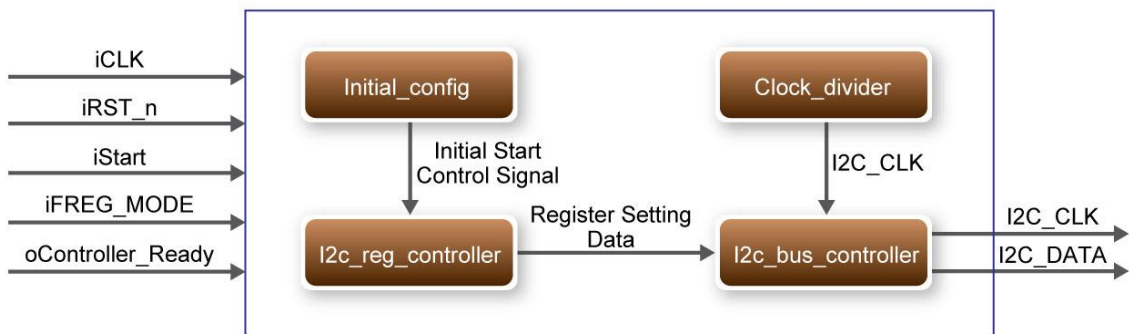


Figure 5-3 Block Diagram of Si570 Controller IP

## ■ Using Si570 Controller IP

Table 5-3 lists the instruction ports of Si570 Controller IP

**Table 5-3 Si570 Controller Instruction Ports**

Port	Direction	Description
iCLK	input	System Clock (50Mhz)
iRST_n	input	Synchronous Reset (0: Module Reset, 1: Normal)
iStart	input	Start to Configure ( positive edge trigger )
iFREG_MODE	input	Setting Si570 Output Frequency Value
oController_Ready	output	Si570 Configuration status ( 0: Configuration in Progress, 1: Configuration Complete)
I2C_DATA	inout	I2C Serial Data to/from Si570
I2C_CLK	output	I2C Serial Clock to Si570

To use the Si570 Controller, the first thing users need to determine is the desired output frequency in advance. The Si570 controller provides six optional clock frequencies. These options can be set through an input port named “iFREG\_MODE” in Si570 controller. The specified settings with corresponding frequencies are listed in Table 5-4. For example, setting “iFREG\_MODE” as 3'b110 will configure Si570 to output 655.53 MHz clock.

**Table 5-4 Si570 Controller Frequency Setting**

iFREG MODE Setting	Si570 Clock Frequency(MHz)
3'b000	100
3'b001	125
3'b010	156.25
3'b011	250
3'b100	312.25
3'b101	322.26
3'b110	644.53125
3'b111	100

When the output clock frequency is decided, the next thing users need to do is to enable the controller to configure Si570. Before sending enable signal to Si570 controller, users need to monitor an output port named “oController\_Ready”. This port indicates if Si570 controller is ready to be configured or not. If it is ready, logic high will be outputted and the user needs to send a high level logic to “iStart” port to enable the Si570 Controller as shown in Figure 5-4. During Si570 configuring, the logic level of “oController\_Ready” is low; when it rises to high again that means the user can configure another frequency value.

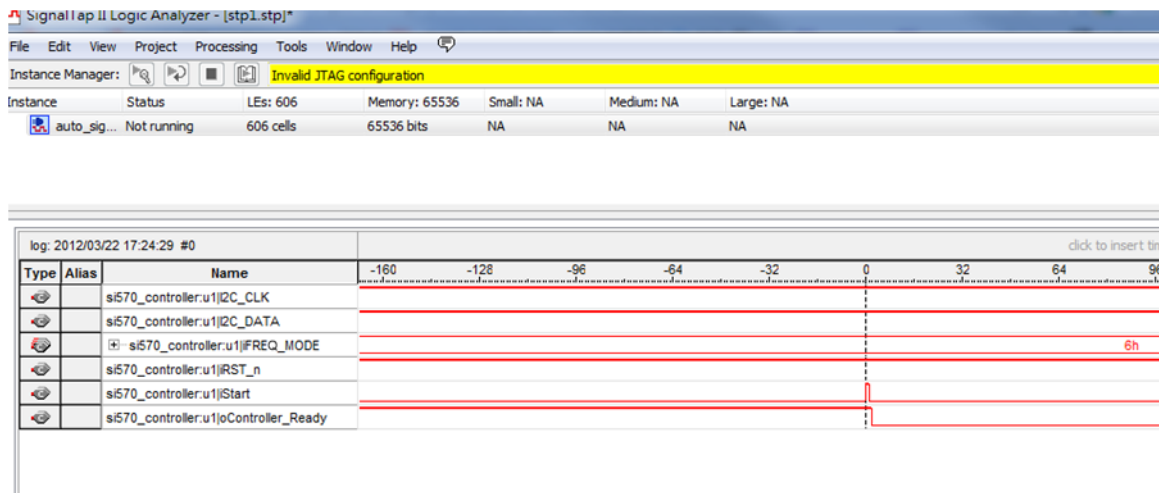


Figure 5-4 Timing Waveform of Si570 Controller

## ■ Modify Clock Parameter For Your Own Frequency

If all the six clock frequencies are not desired, you can perform the following steps to modify Si570 controller.

1. Open i2c\_reg\_controller.v
2. Locate the Verilog code shown below:

```

always @(*)
begin
  case(iFREQ_MODE)
    3'h0 : //100Mhz
      begin
        new_hs_div = 4'b0101 ;
        new_n1 = 8'b0000_1010 ;
        fdco = 28'h004_E200 ;
      end
    3'h1 : //125Mhz
      begin
        new_hs_div = 4'b0101 ;
        new_n1 = 8'b0000_1000 ;
        fdco = 28'h004_E200 ;
      end
  end
end

```

```

3'h2 : //156.25Mhz
begin
    new_hs_div = 4'b0100 ;
    new_n1 = 8'b0000_1000 ;
    fdco = 28'h004_E200 ;
end
3'h3 : //250Mhz
begin
    new_hs_div = 4'b0101 ;
    new_n1 = 8'b0000_0100 ;
    fdco = 28'h004_E200 ;
end
3'h4 : //312.5Mhz
begin
    new_hs_div = 4'b0100 ;
    new_n1 = 8'b0000_0100 ;
    fdco = 28'h004_E200 ;
end
3'h5 : //322.265625Mhz
begin
    new_hs_div = 4'b0100 ;
    new_n1 = 8'b0000_0100 ;
    fdco = 28'h005_0910 ;
end
3'h6 : //644.53125Mhz
begin
    new_hs_div = 4'b0100 ;
    new_n1 = 8'b0000_0010 ;
    fdco = 28'h005_0910 ;
end
default : //100Mhz
begin
    new_hs_div = 4'b0101 ;
    new_n1 = 8'b0000_1010 ;
    fdco = 28'h004_E200 ;
end
endcase

```

end

Users can get a desired frequency output from si570 by modifying these three parameters : **new\_hs\_div** ,**new\_n1** and **fdco**.

Detailed calculation method is in following equation:

$$fdco = output\ frequency * new\_hs\_div * new\_n1 * 64$$

There are three constraints for the equation:

1.  $4850 < output\ frequency * new\_hs\_div * new\_n1 < 5600$
2.  $4 \leq new\_hs\_div \leq 11$
3.  $1 \leq new\_n1 \leq 128$

For example, you want to get a 133.5 mhz clock, then

$$fdco = 133.5 \times 4 \times 10 \times 64 = 341760d = 0x53700$$

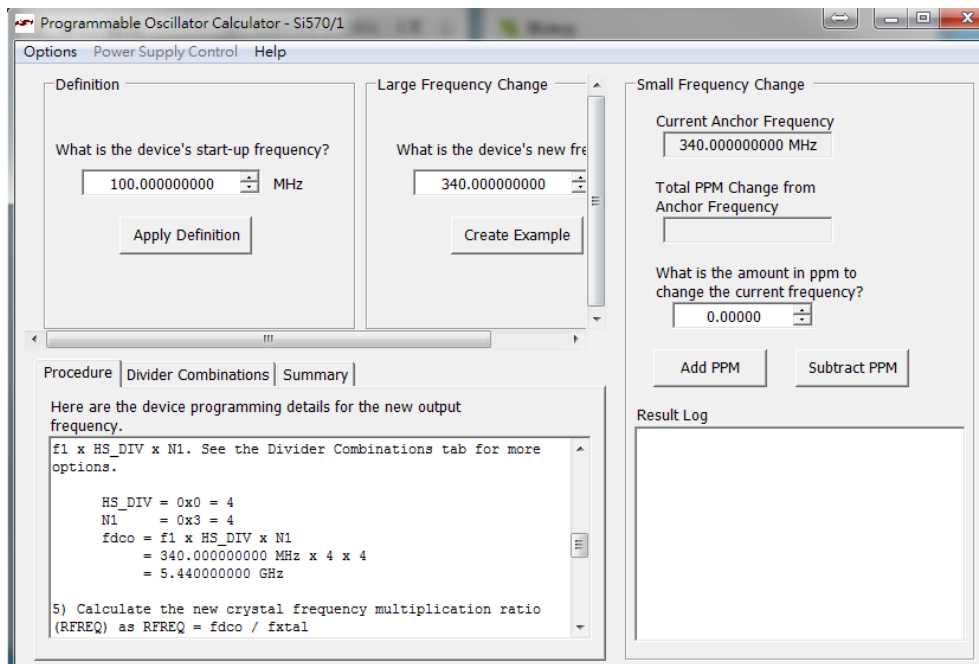
Find a mode in this RTL code section and modify these three parameters,as shown below:

```
new_hs_div = 3'b100 ;
new_n1 = 4'b1010 ;
fdco = 23'h05_3700 ;
```

In addition, Silicon Lab also provide the corresponding calculation tool.

Users can refer to the Programmable Oscillator tool (See **Figure 5-5**) mentioned in below link to calculate the values of new\_hs\_div and new\_n1, then, the fdco value can be calculated with above ftdo equation.

<http://www.silabs.com/products/clocksoscillators/oscillators/Pages/oscillator-software-development-tools.aspx>



**Figure 5-5 Programmable Oscillator Calculator tool**

In addition, if the user doesn't want Si570 controller to configure Si570 as soon as the FPGA configuration finishes, users can change settings in Si570\_controller.v, shown below.

```
initial_config initial_config(

.iCLK(iCLK), // system clock 50mhz
.iRST_n(iRST_n), // system reset
.oINITIAL_START(initial_start),
.iINITIAL_ENABLE(1'b1),
);
```

Changing the setting from ".iINITIAL\_ENABLE(1'b1)" to ".iINITIAL\_ENABLE(1'b0)" will disable the initialization function of Si570 Controller.

## ■ Design Tools

- Quartus Prime 16.1.2 Standard Edition

## ■ Demonstration Source Code



- Project directory: Si570\_Demonstration
- Bit stream used: Si570\_Demonstration.sof
- Demonstration Batch File : test\_ub2.bat
- Demo Batch File Folder: Si570\_Demonstration \demo\_batch

The demo batch file folders include the following files:

- Batch File: test\_ub2.bat
- FPGA Configuration File: Si570\_Demonstration.sof

## ■ Demonstration Setup

- Make sure Quartus Prime is installed on your PC.
- Connect the USB Blaster cable to the FPGA board and host PC. Install the USB Blaster II driver if necessary.
- Power on the FPGA board.
- Execute the demo batch file “test\_ub2.bat” under the batch file folder, Si570\_Demonstration\demo\_batch
- Press BUTTON1 to configure the Si570.
- Observe LED3 status.

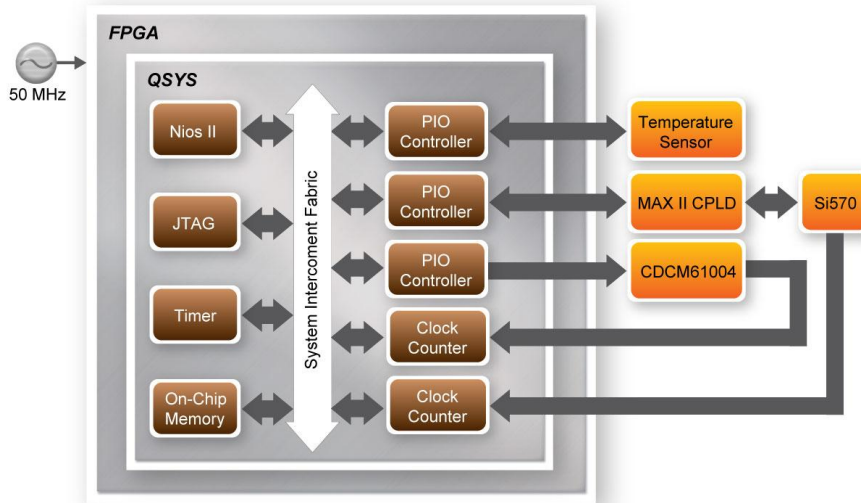
## 5.3 Si570 and CDCM Programming by Nios II

This demonstration shows how to use the Nios II processor to program both programmable oscillators Si570 and CDCM on the FPGA board. The demonstration also includes a function to monitor system temperature with the on-board temperature sensor.

### ■ System Block Diagram

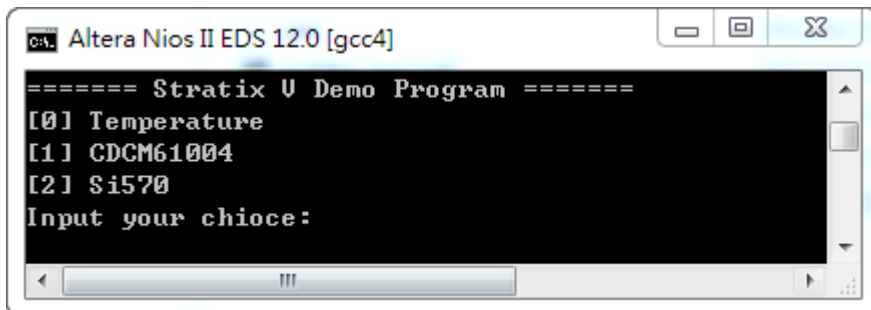
**Figure 5-5** shows the system block diagram of this demonstration. The system requires a 50 MHz clock provided from the board. The three peripheral temperature sensor, Si570, and CDCM61004 are all controlled by Nios II through the PIO controller. The temperature sensor and external PLL Si570 are controlled through I2C interface. The Nios II program toggles the PIO controller to implement the I2C protocol. The CDCM 61004 is programmed through the PIO directly. The Nios

II program is running in the on-chip memory.



**Figure 5-6 Block diagram of the Nios II Basic Demonstration**

The program provides a menu in nios-terminal, as shown in **Figure 5-6** to provide an interactive interface. With the menu, users can perform the test for the temperatures sensor and external PLL. Note, pressing ‘ENTER’ should be followed with the choice number.



**Figure 5-7 Menu of Demo Program**

In temperature test, the program will display local temperature and remote temperature. The remote temperature is the FPGA temperature, and the local temperature the board temperature where the temperature sensor located.

In the external PLL programming test, the program will program the PLL first, and subsequently will use TERCASIC QSYS custom CLOCK\_COUNTER IP to count the clock count in a specified period to check whether the output frequency is changed as configured. To avoid a Quartus Prime

compilation error, dummy transceiver controllers are created to receive the clock from the external PLL. Users can ignore the functionality of the transceiver controller in the demonstration.

For CDMC61004 programming, users must trigger the CLK\_RST\_n to notify the chip to perform PLL recalibration. For Si570 programming, please note the device I2C address is 0x00. Also, before configuring the output frequency, users must freeze the DCO (bit 4 of Register 137) first. After configuring the output frequency, users must un-freeze the DCO and assert the NewFreq bit (bit 7 of Register 135).

- Design Tools
- Quartus Prime 16.1.2 Standard Edition
- Nios II Eclipse 16.1.2
- Demonstration Source Code
- Quartus Prime Project directory: Nios\_BASIC\_DEMO
- Nios II Eclipse: Nios\_BASIC\_DEMO\Software
- Nios II IDE Project Compilation
- Before you attempt to compile the reference design under Nios II Eclipse, make sure the project is cleaned first by clicking on ‘Clean’ in the ‘Project’ menu of Nios II Eclipse.
- Demonstration Batch File

Demo Batch File Folder: *Nios\_BASIC\_DEMO\demo\_batch*

The demo batch file includes following files:

- Batch File for USB-Blaster II: test\_ub2.bat, test\_bashrc\_ub2
- FPGA Configure File: golen\_top.sof
- Nios II Program: Nios\_DEMO.elf

## ■ Demonstration Setup

- Make sure Quartus Prime and Nios II are installed on your PC.
- Power on the FPGA board.
- Use the USB Cable to connect your PC and the FPGA board and install USB Blaster II driver if necessary.
- Execute the demo batch file “test\_ub2.bat” under the batch file folder, Nios\_BASIC\_DEMO\demo\_batch
- After the Nios II program is downloaded and executed successfully, a prompt message will be displayed in nios2-terminal.

- For temperature test, please input key ‘0’ and press ‘Enter’ in the nios-terminal, , as shown in **Figure 5-7**.
- For programming PLL CDCD61004 test, please input key ‘1’ and press ‘Enter’ in the nios-terminal first, then select the desired output frequency , as shown in 158H158H **Figure 5-9**.
- For programming PLL Si570 test, please input key ‘2’ and press ‘Enter’ in the nios-terminal first, then select the desired output frequency , as shown in 159H159H **Figure 5-10**.

```

c:\ Altera Nios II EDS 12.0 [gcc4]
===== Stratix U Demo Program =====
[0] Temperature
[1] CDCM61004
[2] Si570
Input your chioce:0
Local Temperature:33
Remote Temperature:35
Temperature Test:PASS
===== Stratix U Demo Program =====
[0] Temperature
[1] CDCM61004
[2] Si570
Input your chioce:
  
```

Figure 5-8 Temperature Demo

```

Altera Nios II EDS 12.0 [gcc4]
===== Stratix U Demo Program =====
[0] Temperature
[1] CDCM61004
[2] $i570
Input your chioce:1
0: 62.500 MHz
1: 75.000 MHz
2: 100.000 MHz
3: 125.000 MHz
4: 150.000 MHz
5: 156.250 MHz
6: 187.500 MHz
7: 200.000 MHz
8: 250.000 MHz
9: 312.500 MHz
10: 625.000 MHz
Other:exit
please select:===== CDCM61004 Programming =====
625.000 MHz Test Result:
  SATA ref clock test PASS <clk1=998, clk2=12473>
CDCM61004 Test:PASS
===== Stratix U Demo Program =====
[0] Temperature
[1] CDCM61004
[2] $i570
Input your chioce:

```

Figure 5-9 CDCM 61004 Demo

```

Altera Nios II EDS 12.0 [gcc4]
===== Stratix U Demo Program =====
[0] Temperature
[1] CDCM61004
[2] $i570
Input your chioce:2
===== $i570 Programming =====
[0] 100.000000 MHz
[1] 125.000000 MHz
[2] 156.250000 MHz
[3] 250.000000 MHz
[4] 312.500000 MHz
[5] 322.265625 MHz
[6] 644.531250 MHz
[Other] exit
please select:6
HS_DIU=4h, M1=2h, REFEQ:2-die127afh
Reg-135, Reset/Freeze/Memory Control:40h
$i570/644.531250MHz clock test PASS <clk1=998, clk2=12866, expected clk2=12864>
$i570 Test:PASS
===== Stratix U Demo Program =====
[0] Temperature
[1] CDCM61004
[2] $i570
Input your chioce:

```

Figure 5-10 Si570 Demo

# Memory Reference Design

The FPGA development board includes two kinds of high-speed memories:

- DDR3 SDRAM: two independent banks, update to 800 MHz
- QDRII+ SRAM: four independent banks, update to 550 MHz

This chapter will show three examples which use the Altera Memory IP to perform memory test functions. The source codes of these examples are all available on the FPGA System CD. These three examples are:

- QDRII+ SRAM Test: Full test of the four banks of QDRII+ SRAM
- DDR3 SDRAM Test: Random test of the two banks of DDR3 SDRAM.
- DDR3 SDRAM Test by Nios II: Full test of one bank of DDR3 SDRAM with Nios II

*Note. 64-Bit Quartus Prime 16.1.2 Standard Edition or later is strongly recommended for compiling these projects.*

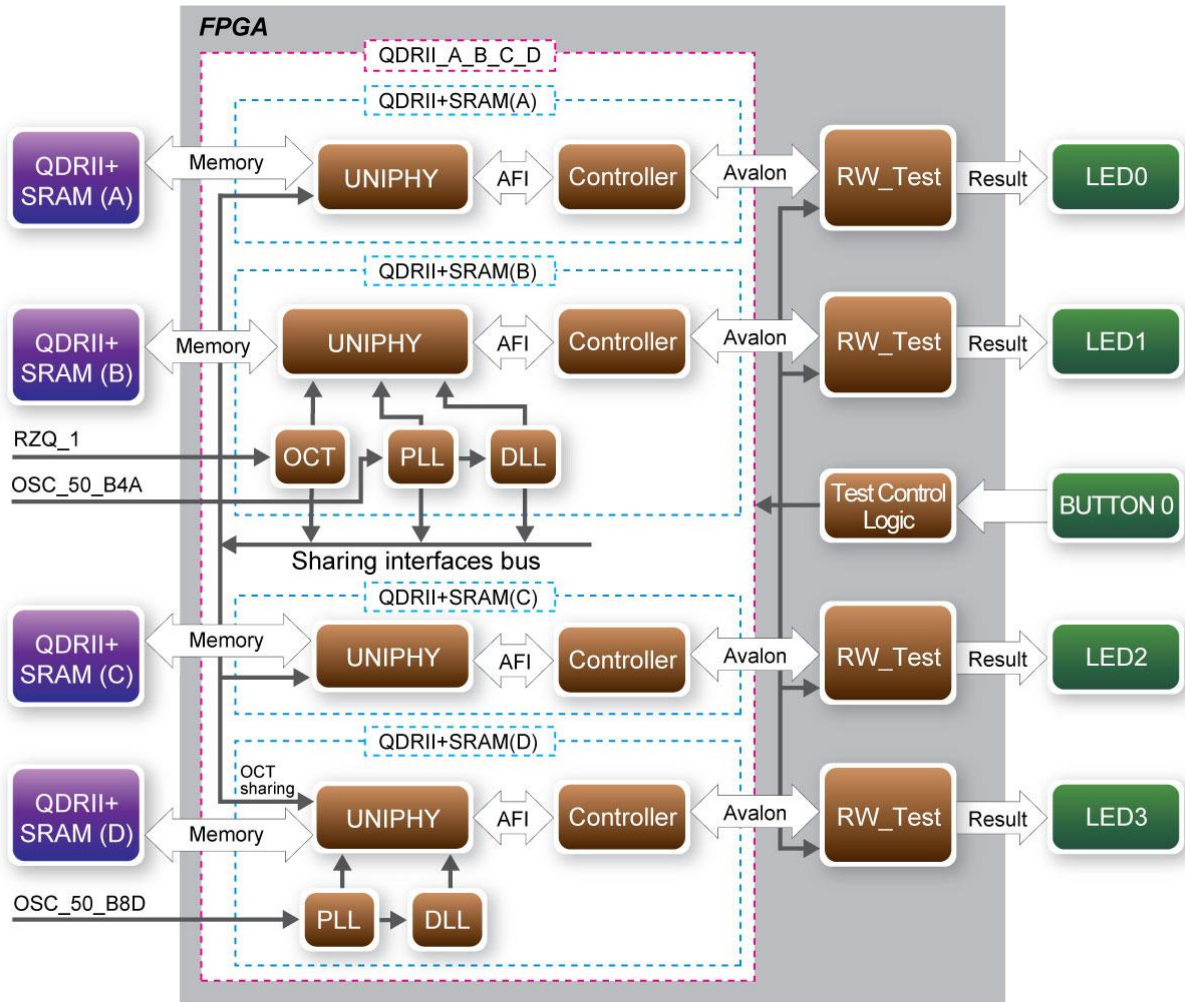
## 6.1 QDRII+ SRAM Test

QDR II/QDR II+ SRAM devices enable you to maximize memory bandwidth with separate read and write ports. The memory architecture features separate read and write ports operating twice per clock cycle to deliver a total of four data transfers per cycle. The resulting performance increase is particularly valuable in bandwidth-intensive and low-latency applications.

This demonstration utilizes four QDRII+ SRAMs on the FPGA board. It describes how to use Altera's "QDRII and QDRII+ SRAM Controller with UniPHY" IP to implement a memory test function. In the design, the four QDRII controllers share the PLL/DLL/OCT due to limited DLL numbers in the FPGA.

## ■ Function Block Diagram

Figure 6-1 shows the function block diagram of the demonstration. The four QDRII+ SRAM controllers are configured as a 72Mb controller. The QDRII+ SRAM IP generates a 550MHz clock as memory clock and a half-rate system clock, 275MHz, for the controllers.



**Figure 6-1 Function Block Diagram of the QDRII+ SRAM x4 Demonstration**

In this demonstration, four QDRII+ SRAM controllers are sharing the FPGA resources (OCT, PLL, and DLL), and the QDRII+ SRAM (B) is configured as the master to share the resource to the other three slave QDRII+ SRAM (A/C/D). QDRII+ SRAM (A/C) share OCT, PLL, DLL from QDRII+ SRAM (B). QDRII+ SRAM (D) shares OCT from QDRII+ SRAM (B) and it has its own PLL and DLL resources. The Avalon bus read/write test (**RW\_test**) modules read and write the entire memory space of each QDRII+ SRAM through the Avalon interface of each controller. In this project, the RW\_test module will first write the entire memory and then compare the read back data

with the regenerated data (the same sequence as the write data). Test control signals for four QDRII+ SRAMs will generate from BUTTON0 and four LEDs will indicate the test results of four QDRII+ SRAMs.

## ■ Altera QDRII and QDRII+ SRAM Controller with UniPHY

To use Altera QDRII+ SRAM controller, users need to perform the following steps in order:

1. Create correct pin assignments for QDRII+.
2. Setup correct parameters in QDRII+ SRAM controller dialog.
3. Perform “Analysis and Synthesis” by clicking Quartus menu: Process→Start→Start Analysis & Synthesis.
4. Run the TCL files generated by QDRII+ IP by clicking Quartus menu: Tools→TCL Scripts...

- Design Tools
- Quartus Prime 16.1.2 Standard Edition
- Demonstration Source Code
- Project directory: QDRIIx4\_Test
- Bit stream used: QDRIIx4\_Test.sof
- Demonstration Batch File

Demo Batch File Folder: *QDRIIx4\_Test\demo\_batch*

The demo batch files include the followings:

- Batch file for USB-Blaster II: test\_ub2.bat,
- FPGA configuration file: QDRIIx4\_Test.sof
- Demonstration Setup
- Make sure Quartus Prime is installed on your PC.
- Connect the USB cable to the FPGA board and host PC. Install the USB-Blaster II driver if necessary.
- Power on the FPGA Board.
- Execute the demo batch file “test\_ub2.bat” under the batch file folder, QDRIIx4\_Test\demo\_batch.
- Press BUTTON0 of the FPGA board to start the verification process. When BUTTON0 is held



down, all the LEDs will be turned off. All LEDs should turn back on to indicate test passes upon the release of BUTTON0.

- If any LED is not lit up after releasing BUTTON0, it indicates the corresponding QDRII+ SRAM test has failed. 161H161H **Table 6-1** lists the matchup for the four LEDs.
- Press BUTTON0 again to regenerate the test control signals for a repeat test.

**Table 6-1 LED Indicators**

<i>NAME</i>	<i>Description</i>
LED0	QDRII+ SRAM(A) test result
LED1	QDRII+ SRAM(B) test result
LED2	QDRII+ SRAM(C) test result
LED3	QDRII+ SRAM(D) test result

## 6.2 DDR3 SDRAM Test

This demonstration presents a memory test function on the two sodimm of DDR3-SDRAM on the FPGA board. The memory size of each DDR3 SDRAM sodimm used in this test is 2 GB.

### ■ Function Block Diagram

**Figure 6-2** shows the function block diagram of this demonstration. There are two DDR3 SDRAM controllers. One is the master controller which shares resources with a slave controller. The shared resources include delay-locked loops (DLLs), phase-locked loops (PLLs), and on-chip termination (OCT). The controller uses 50 MHz as a reference clock, generates one 800.0 MHz clock as memory clock, and generates one quarter-rate system clock 200.0 MHz for the controller itself.

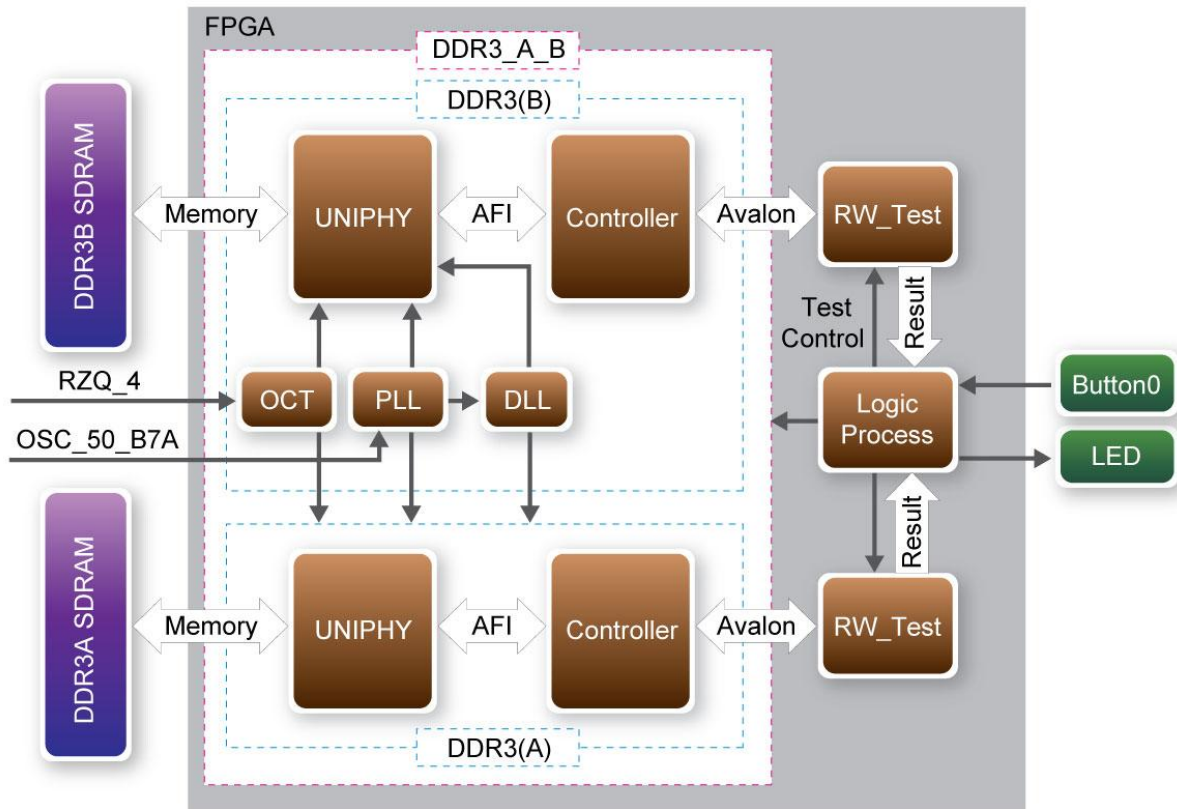


Figure 6-2 Block Diagram of the DDR3 SDRAM (2G) x2 Demonstration

## ■ Altera DDR3 SDRAM Controller with UniPHY

To use the Altera DDR3 controller, users need to perform three major steps:

1. Create correct pin assignments for the DDR3.
2. Setup correct parameters in the DDR3 controller dialog.
3. Perform “Analysis and Synthesis” by selecting from the Quartus Prime menu: Process→Start→Start Analysis & Synthesis.
4. Run the TCL files generated by DDR3 IP by selecting from the Quartus Prime menu: Tools→TCL Scripts...

## ■ Design Tools

- Quartus Prime 16.1.2 Standard Edition
- Demonstration Source Code
- Project directory: DDR3x2\_Test
- Bit stream used: DDR3x2\_Test.sof
- Demonstration Batch File

Demo Batch File Folder: *DDR3x2\_Test \demo\_batch*

The demo batch file includes following files:

- Batch File: test\_ub2.bat
- FPGA Configure File: DDR3x2\_Test .sof

## ■ Demonstration Setup

- Make sure Quartus Prime is installed on your PC.
- Connect the USB Blaster cable to the FPGA board and host PC. Install the USB Blaster II driver if necessary.
- Power on the FPGA board.
- Execute the demo batch file “test\_ub2.bat” under the batch file folder, DDR3x2\_Test \demo\_batch.
- Press BUTTON0 on the FPGA board to start the verification process. When BUTTON0 is pressed, all the LEDs (LED [3:0]) should turn on. At the instant of releasing BUTTON0, LED1, LED2, LED3 should start blinking. After approximately 5 seconds, LED1 and LED2 should stop blinking and stay on to indicate that the DDR3 (A) and DDR3 (B) have passed the test, respectively. Table 6-2 lists the LED indicators.
- If LED3 is not blinking, it means the 50MHz clock source is not working.
- If LED1 or LED2 do not start blinking after releasing BUTTON0, it indicates local\_init\_done or local\_cal\_success of the corresponding DDR3 failed.
- If LED1 or LED2 fail to remain on after 5 seconds, the corresponding DDR3 test has failed.
- Press BUTTON0 again to regenerate the test control signals for a repeat test.

**Table 6-2 LED Indicators**

<i>NAME</i>	<i>Description</i>
<b>LED0</b>	<b>Reset</b>
<b>LED1</b>	<b>DDR3 (A) test result</b>
<b>LED2</b>	<b>DDR3 (B) test result</b>
<b>LED3</b>	<b>Blinks</b>

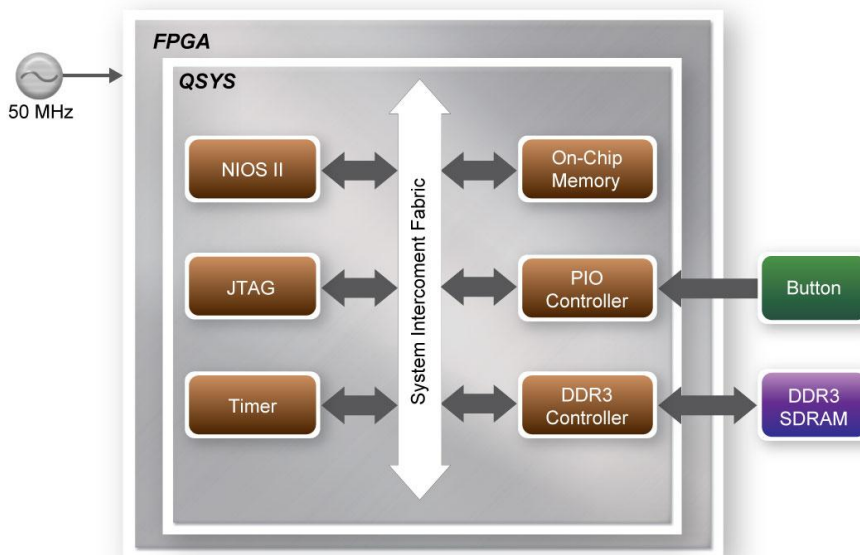
## 6.3 DDR3 SDRAM Test by Nios II

Many applications use a high performance RAM, such as a DDR3 SDRAM, to provide temporary storage. In this demonstration hardware and software designs are provided to illustrate how to

perform DDR3 memory access in QSYS. We describe how the Altera’s “DDR3 SDRAM Controller with UniPHY” IP is used to access a DDR3-SDRAM, and how the Nios II processor is used to read and write the SDRAM for hardware verification. The DDR3 SDRAM controller handles the complex aspects of using DDR3 SDRAM by initializing the memory devices, managing SDRAM banks, and keeping the devices refreshed at appropriate intervals.

## ■ System Block Diagram

**Figure 6-3** shows the system block diagram of this demonstration. The system requires a 50 MHz clock provided from the board. The DDR3 controller is configured as a 1 GB DDR3-800Mhz controller. The DDR3 IP generates one 800 MHz clock as SDRAM’s data clock and one quarter-rate system clock  $800/4=200$  MHz for those host controllers, e.g. Nios II processor, accessing the SDRAM. In the QSYS, Nios II and the On-Chip memory are designed running with the 233.333 MHz clock, and the Nios II program is running in the on-chip memory.



**Figure 6-3 Block diagram of the DDR3 Basic Demonstration**

The system flow is controlled by a Nios II program. First, the Nios II program writes test patterns into the whole 1 GB of SDRAM. Then, it calls Nios II system function, `alt_dache_flush_all`, to make sure all data has been written to SDRAM. Finally, it reads data from SDRAM for data verification. The program will show progress in JTAG-Terminal when writing/reading data to/from the SDRAM. When verification process is completed, the result is displayed in the JTAG-Terminal.

## ■ Altera DDR3 SDRAM Controller with UniPHY

To use Altera DDR3 controller, users need to perform the four major steps:

1. Create correct pin assignments for DDR3.
2. Setup correct parameters in DDR3 controller dialog.
3. Perform “Analysis and Synthesis” by clicking Quartus menu: Process→Start→Start Analysis & Synthesis.
4. Run the TCL files generated by DDR3 IP by clicking Quartus menu: Tools→TCL Scripts...

## ■ Quartus Prime Project

The Quartus Prime project is designed to only access DDR3-A or DDR3-B at same time due to the address space limitation of Nios II. Users can change the accessed memory target at Quartus compile time by defining the constant USE\_DDR3\_A for DDR3-A or constant USE\_DDR3\_B for DDR3-B bank. After the constant is defined, please perform Analysis and Synthesis and then run the TCL files generated by DDR3 IP before starting Quartus Prime compilation.

## ■ Design Tools

- Quartus Prime 16.1.2 Standard Edition
- Nios II Eclipse 16.1.2

## ■ Demonstration Source Code

- Quartus Project directory: Nios\_DDR3
- Nios II Eclipse: NIOS\_DDR3\Software
- Nios II Project Compilation

Before you attempt to compile the reference design under Nios II Eclipse, make sure the project is cleaned first by clicking ‘Clean’ from the ‘Project’ menu of Nios II Eclipse.

## ■ Demonstration Batch File

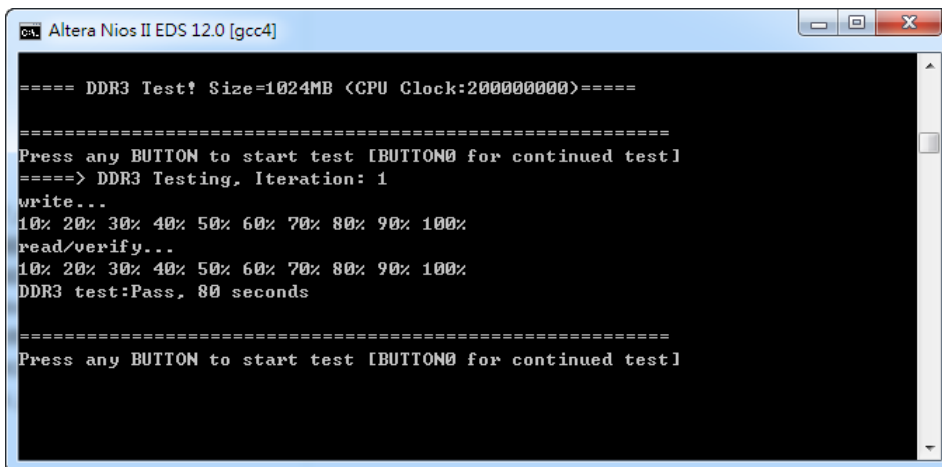
Demo Batch File Folder:

*Nios\_DDR3\demo\_batch\DDR3\_A* or

*Nios\_DDR3\demo\_batch\DDR3\_B*

The demo batch file includes following files:

- Batch File for USB-Blaseter II: test\_ub2.bat, test\_bashrc\_ub2
- FPGA Configure File: Golen\_top.sof
- Nios II Program: TEST\_DDR3.elf
- Demonstration Setup
- Make sure Quartus Prime and Nios II are installed on your PC.
- Power on the FPGA board.
- Use USB Cable to connect PC and the FPGA board and install USB Blaster II driver if necessary.
- Execute the demo batch file “test\_ub2.bat” under the batch file folder, NIOS\_DDR3\demo\_batch\DDR3\_A or NIOS\_DDR3\demo\_batch\DDR3\_B
- After Nios II program is downloaded and executed successfully, a prompt message will be displayed in nios2-terminal.
- Press Button1~Button0 of the FPGA board to start SDRAM verify process. Press Button0 for continued test and press any to terminate the continued test.
- The program will display progressing and result information, as shown in 164H164H **Figure 6-4**.



**Figure 6-4 Display Progress and Result Information for the DDR3 Demonstration**

# PCI Express Reference Design

PCI Express is commonly used in consumer, server, and industrial applications, to link motherboard-mounted peripherals. From this demonstration, it will show how the PC and FPGA communicate with each other through the PCI Express interface. V-Series Avalon-MM DMA for PCI Express IP is used in this demonstration. For detail about this IP, please refer to Altera document : [ug\\_pcie\\_avmm\\_dma.pdf](#).

## 7.1 PCI Express System Infrastructure

Figure 7-1 shows the infrastructure of the PCI Express System in this demonstration. It consists of two primary components: FPGA System and PC System. The FPGA System is developed based on V-Series Avalon-MM DMA for PCI Express. The application software on the PC side is developed by Terasic based on Altera’s PCIe kernel mode driver.

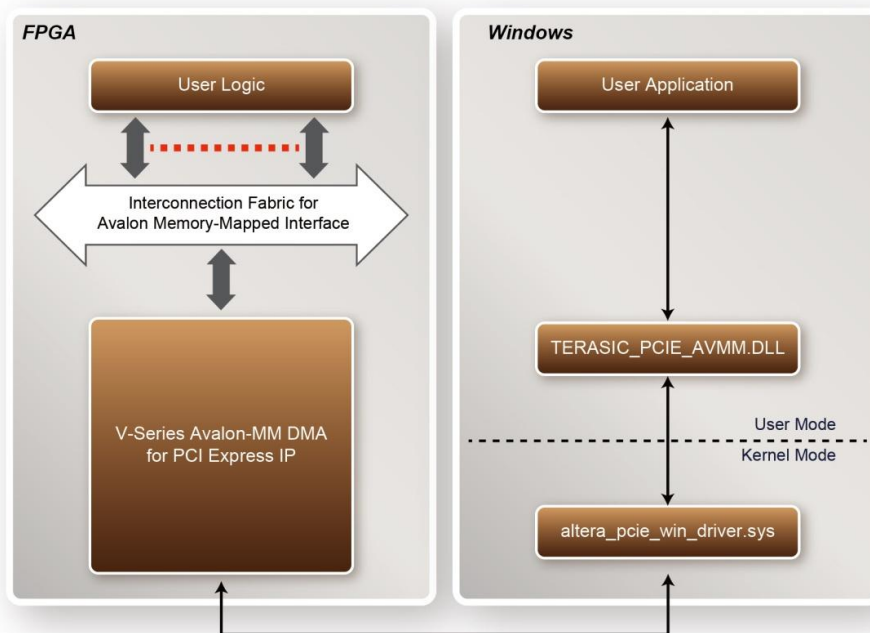


Figure 7-1 PCI Express System Infrastructure

## 7.2 PC PCI Express Software SDK

The FPGA System CD contains a PC Windows based SDK to allow users to develop their 64-bits software application on Windows XP/7/10 64-bits. The SDK is located in the “CDROM \demonstrations\PCIe\_SW\_KIT” folder which includes:

- PCI Express Driver
- PCI Express Library
- PCI Express Examples

The kernel mode driver assumes the PCIe vender ID (VID) is 0x1172 and the device ID (DID) is 0xE003. If different VID and DID are used in the design, users need to modify the PCIe vender ID (VID) and device ID (DID) in the driver INF file accordingly.

The PCI Express Library is implemented as a single DLL called Terasic\_Pcie\_AVMM.DLL. This file is a 64-bits DLL. With the DLL exported to the software API, users can easily communicate with the FPGA. The library provides the following functions:

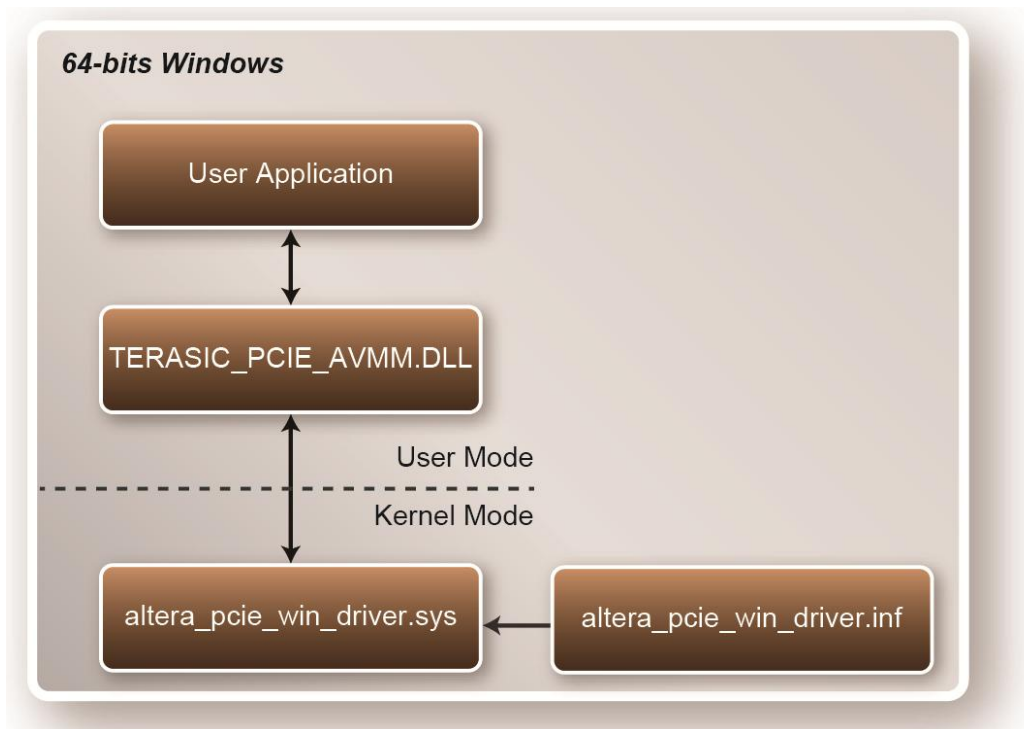
- Basic Data Read and Write
- Data Read and Write by DMA

For high performance data transmission, DMA is required as the read and write operations are specified under the hardware design on the FPGA.

### ■ PCI Express Software Stack

**Figure 7-2** shows the software stack for the PCI Express application software on 64-bit Windows. The PCI Express driver incorporated in the DLL library is called Terasic\_Pcie\_AVMM.dll. Users can develop their applications based on this DLL. The altera\_pcie\_win\_driver.sys kernel driver is provided by Altera.





**Figure 7-2 PCI Express Software Stack**

## ■ Install PCI Express Driver on Windows

The PCIe driver is located in the folder: “CDROM\Demonstrations\PCIe\_SW\_KIT\PCIe\_Driver “

The folder includes the following four files:

- Altera\_pcie\_win\_driver.cat
- Altera\_pcie\_win\_driver.inf
- Altera\_pcie\_win\_driver.sys
- WdfCoinstaller01011.dll

To install the PCI Express driver, execute the steps below:

1. Install the DE5-Net on the PCIe slot of the host PC
2. Make sure Altera Programmer and USB-Blaster II driver are installed
3. Execute test.bat in “CDROM\Demonstrations\PCIe\_Fundamental\demo\_batch” to configure the FPGA
4. Restart windows operation system
5. Click the Control Panel menu from the Windows Start menu. Click the Hardware and the Sound item before clicking the Device Manager to launch the Device Manager dialog. There will be a PCI Device item in the dialog, as shown in **Figure 7-3**. Move the mouse cursor to the PCI Device item and right click it to select the Update Driver Software... item.

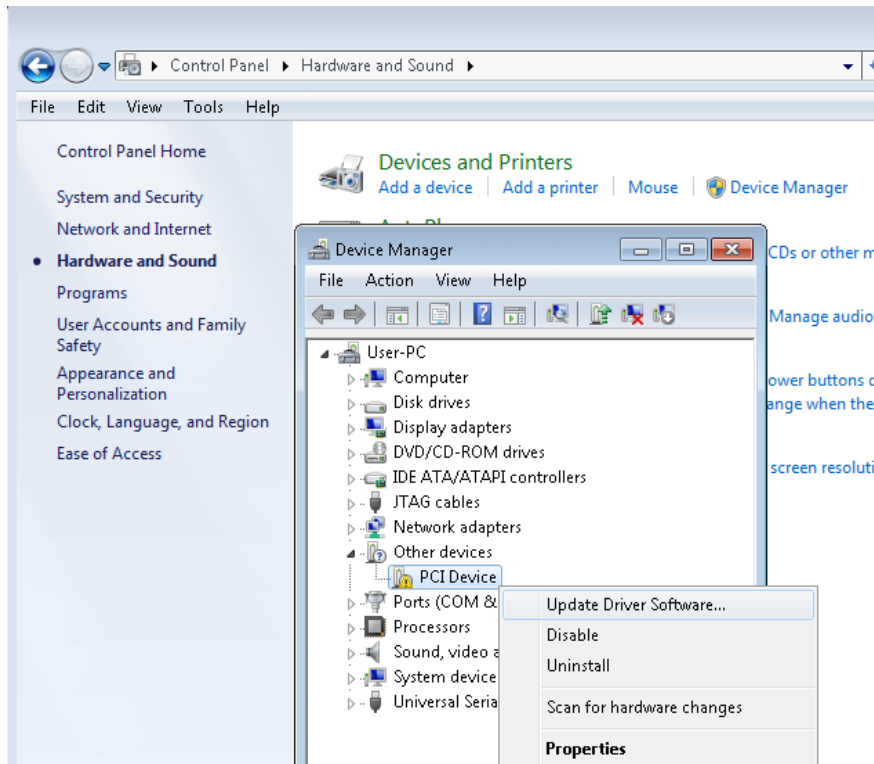


Figure 7-3 Screenshot of launching Update Driver Software dialog

6. In the **How do you want to search for driver software** dialog, click **Browse my computer for driver software** item, as shown in Figure 7-4. Click “OK” and then “Exit” to close the installation program.

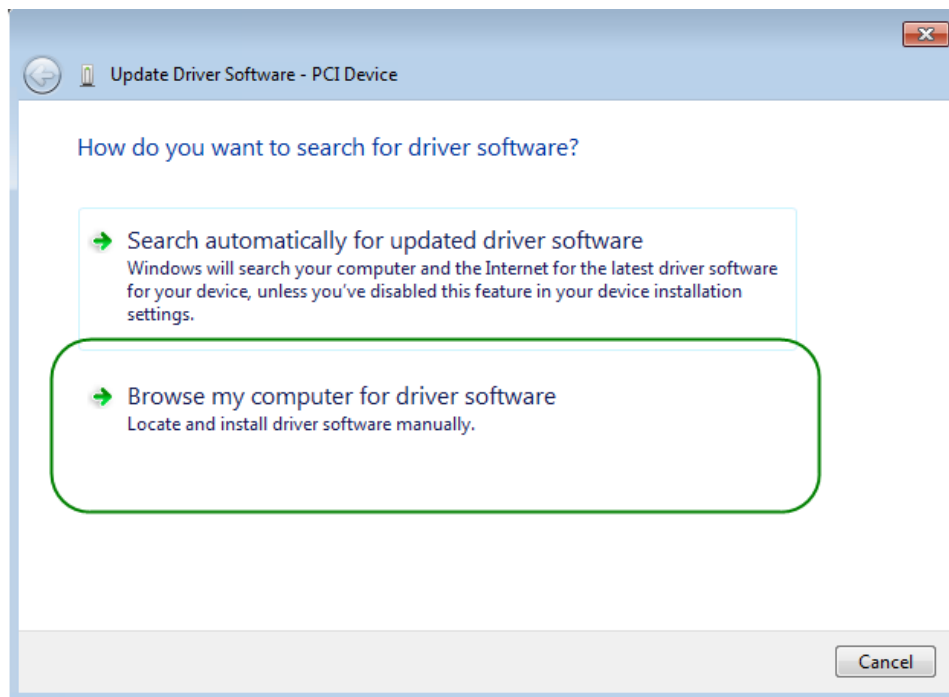
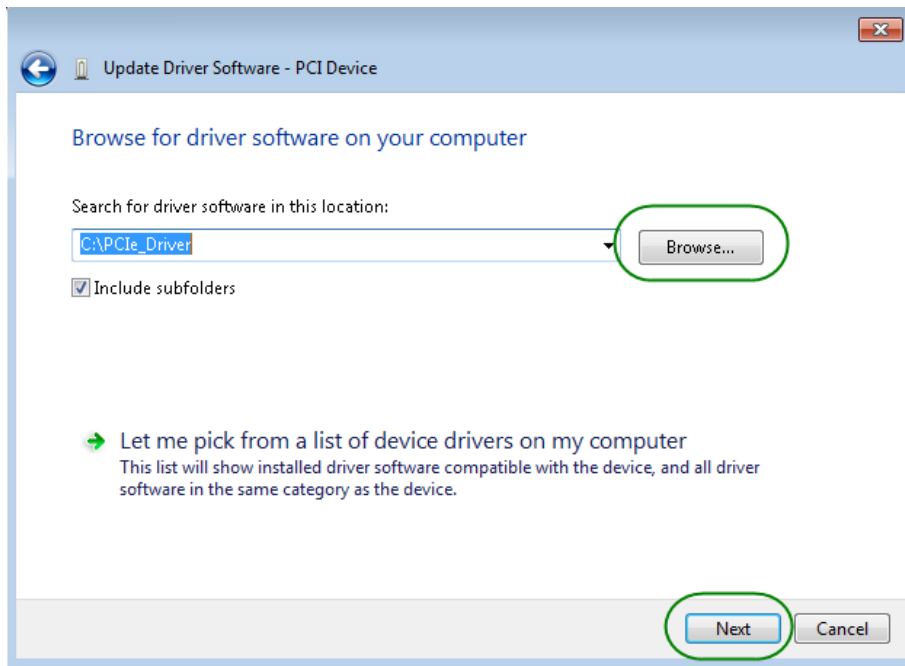


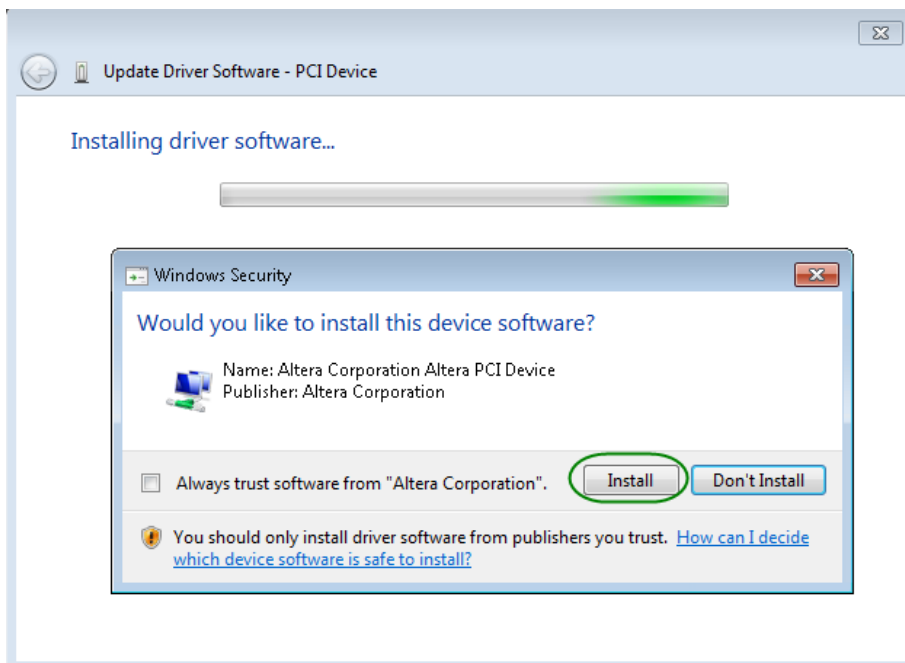
Figure 7-4 Dialog of Browse my computer for driver software

- In the **Browse for driver software on your computer** dialog, click the **Browse** button to specify the folder where altera\_pcie\_din\_driver.inf is located, as shown in **Figure 7-5**. Click the **Next** button.



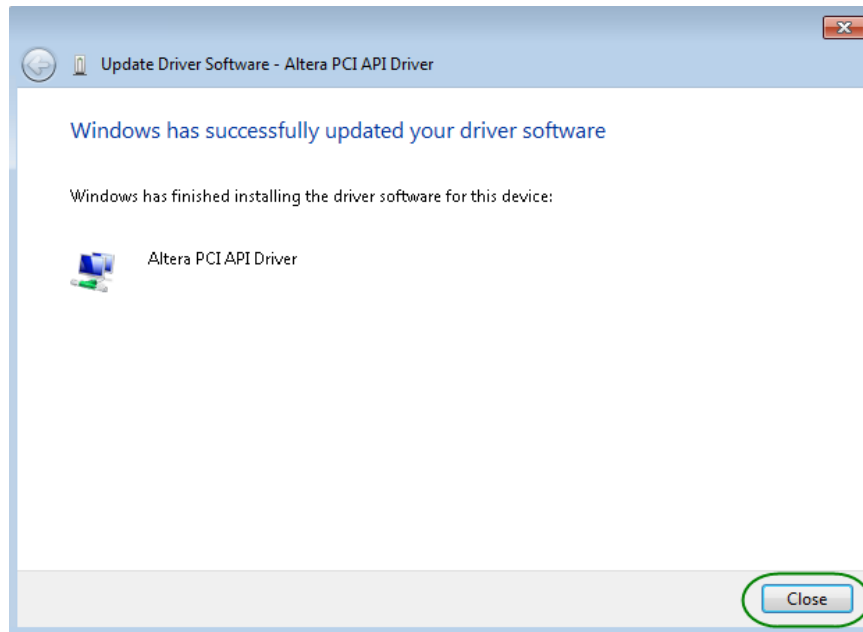
**Figure 7-5 Browse for driver software on your computer**

- When the **Windows Security** dialog appears, as shown **Figure 7-6**, click the **Install** button.



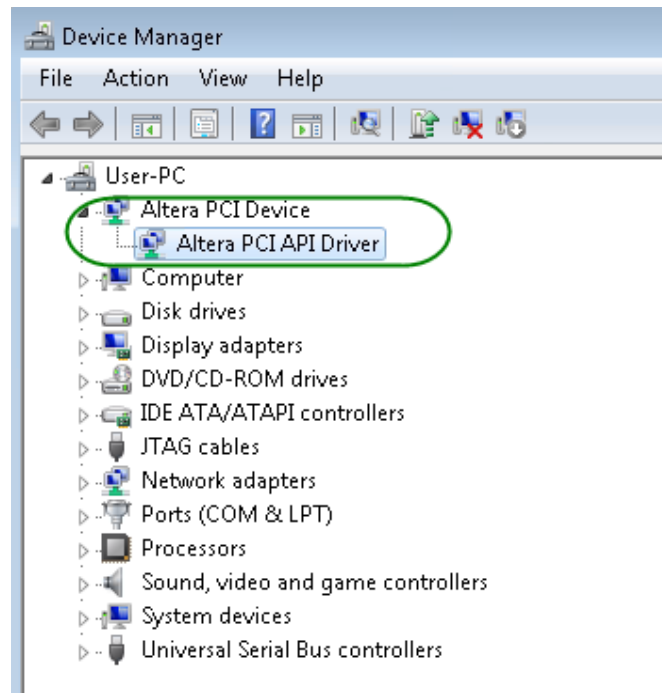
**Figure 7-6 Click Install in the dialog of Windows Security**

9. When the driver is installed successfully, the successfully dialog will appears, as shown in **Figure 7-7**. Click the **Close** button.



**Figure 7-7 Click Close when the installation of Altera PCI API Driver is complete**

10. Once the driver is successfully installed, users can see the **Altera PCI API Driver** under the device manager window, as shown in **Figure 7-8**.



**Figure 7-8 Altera PCI API Driver in Device Manager**

## ■ Create a Software Application

All necessary files to create a PCIe software application are located in the *CDROM\demonstration\PCIe\_SW\_KIT\PCIe\_Library* which includes the following files:

- Terasic\_PCIE\_AVMM.h
- Terasic\_PCIE\_AVMM.DLL (64-bit DLL)

Below lists the procedures to use the SDK files in users' C/C++ project :

- Create a 64-bit C/C++ project.
- Include Terasic\_PCIE\_AVMM.h in the C/C++ project.
- Copy Terasic\_PCIE\_AVMM.DLL to the folder where the project.exe is located.
- Dynamically load Terasic\_PCIE\_AVMM.DLL in C/C++ program. To load the DLL, please refer to the PCIe fundamental example below.
- Call the SDK API to implement the desired application.
- Terasic\_PCIE\_AVMM.DLL Software API

Users can easily communicate with the FPGA through the PCIe bus through the Terasic\_PCIE\_AVMM.DLL API. The details of API are described below:

## PCIE\_Open

<b>Function:</b>
Open a specified PCIe card with vendor ID, device ID, and matched card index.
<b>Prototype:</b>
<pre>PCIE_HANDLE PCIE_Open(     WORD wVendorID,     WORD wDeviceID,     WORD wCardIndex);</pre>
<b>Parameters:</b>
<p>wVendorID: Specify the desired vendor ID. A zero value means to ignore the vendor ID.</p> <p>wDeviceID: Specify the desired device ID. A zero value means to ignore the device ID.</p> <p>wCardIndex: Specify the matched card index, a zero based index, based on the matched vendor ID and device ID.</p>
<b>Return Value:</b>
<p>Return a handle to presents specified PCIe card. A positive value is return if the PCIe card is opened successfully. A value zero means failed to connect the target PCIe card.</p> <p>This handle value is used as a parameter for other functions, e.g. PCIE_Read32.</p> <p>Users need to call PCIE_Close to release handle once the handle is no more used.</p>

## PCIE\_Close

<b>Function:</b>
Close a handle associated to the PCIe card.
<b>Prototype:</b>
<pre>void PCIE_Close(     PCIE_HANDLE hPCIE);</pre>
<b>Parameters:</b>
<p>hPCIE: A PCIe handle return by PCIE_Open function.</p>
<b>Return Value:</b>
None.

## PCIE\_Read32

<b>Function:</b>
Read a 32-bit data from the FPGA board.

**Prototype:**

```
bool PCIE_Read32(
    PCIE_HANDLE hPCIE,
    PCIE_BAR PcieBar,
    PCIE_ADDRESS PcieAddress,
    DWORD * pdwData);
```

**Parameters:**

**hPCIE:**  
A PCIe handle return by PCIE\_Open function.

**PcieBar:**  
Specify the target BAR.

**PcieAddress:**  
Specify the target address in FPGA.

**pdwData:**  
A buffer to retrieve the 32-bit data.

**Return Value:**

Return TRUE if read data is successful; otherwise FALSE is returned.

## PCIE\_Write32

**Function:**

Write a 32-bit data to the FPGA Board.

**Prototype:**

```
bool PCIE_Write32(
    PCIE_HANDLE hPCIE,
    PCIE_BAR PcieBar,
    PCIE_ADDRESS PcieAddress,
    DWORD dwData);
```

**Parameters:**

**hPCIE:**  
A PCIe handle return by PCIE\_Open function.

**PcieBar:**  
Specify the target BAR.

**PcieAddress:**  
Specify the target address in FPGA.

**dwData:**  
Specify a 32-bit data which will be written to FPGA board.

**Return Value:**

Return TRUE if write data is successful; otherwise FALSE is returned.

## PCIE\_DmaRead

### Function:

Read data from the memory-mapped memory of FPGA board in DMA.

### Prototype:

```
bool PCIE_DmaRead(
    PCIE_HANDLE hPCIE,
    PCIE_LOCAL_ADDRESS LocalAddress,
    void *pBuffer,
    DWORD dwBufSize
);
```

### Parameters:

**hPCIE:**

A PCIe handle return by PCIE\_Open function.

**LocalAddress:**

Specify the target memory-mapped address in FPGA.

**pBuffer:**

A pointer to a memory buffer to retrieved the data from FPGA. The size of buffer should be equal or larger the dwBufSize.

**dwBufSize:**

Specify the byte number of data retrieved from FPGA.

### Return Value:

Return TRUE if read data is successful; otherwise FALSE is returned.

## PCIE\_DmaWrite

### Function:

Write data to the memory-mapped memory of FPGA board in DMA.

### Prototype:

```
bool PCIE_DmaWrite(
    PCIE_HANDLE hPCIE,
    PCIE_LOCAL_ADDRESS LocalAddress,
    void *pData,
    DWORD dwDataSize
);
```

### Parameters:

**hPCIE:**



A PCIe handle return by PCIE\_Open function.

LocalAddress:

Specify the target memory mapped address in FPGA.

pData:

A pointer to a memory buffer to store the data which will be written to FPGA.

dwDataSize:

Specify the byte number of data which will be written to FPGA.

**Return Value:**

Return TRUE if write data is successful; otherwise FALSE is returned.

## PCIE\_ConfigRead32

**Function:**

Read PCIe Configuration Table. Read a 32-bit data by given a byte offset.

**Prototype:**

```
bool PCIE_ConfigRead32 (
    PCIE_HANDLE hPCIE,
    DWORD Offset,
    DWORD *pdwData
);
```

**Parameters:**

hPCIE:

A PCIe handle return by PCIE\_Open function.

Offset:

Specify the target byte of offset in PCIe configuration table.

pdwData:

A 4-bytes buffer to retrieve the 32-bit data.

**Return Value:**

Return TRUE if read data is successful; otherwise FALSE is returned.

## 7.3 Reference Design - Fundamental

The application reference design shows how to implement fundamental control and data transfer in DMA. In the design, basic I/O is used to control the BUTTON and LED on the FPGA board. High-speed data transfer is performed by DMA.

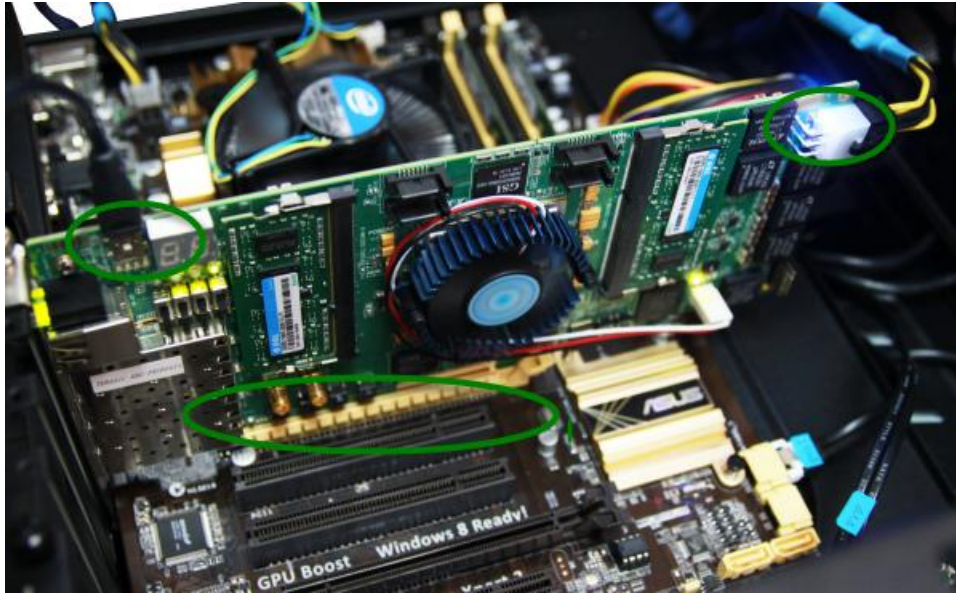
### ■ Demonstration Files Location

- The demo file is located in the batch folder:
  - CDROM\demonstrations\PCIe\_fundamental\Demo\_batch
- The folder includes following files:
  - FPGA Configuration File: PCIe\_fundamental.sof
  - Download Batch file: test.bat
  - Windows Application Software folder : windows\_app, includes

- ◆ PCIE\_FUNDAMENTAL.exe
- ◆ TERASIC\_PCIE\_AVMM.dll

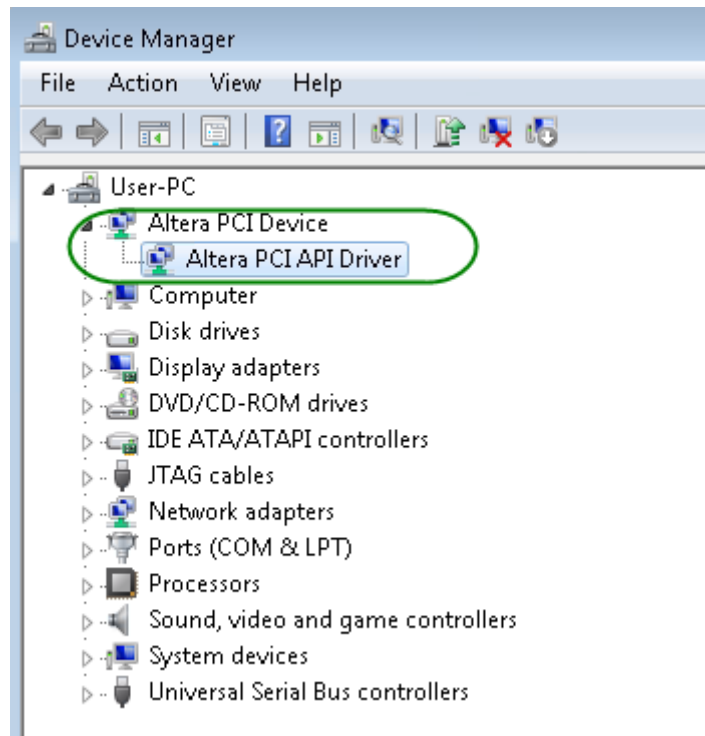
## ■ Demonstration Setup

1. Install the FPGA board on your PC as shown in **Figure 7-9**.



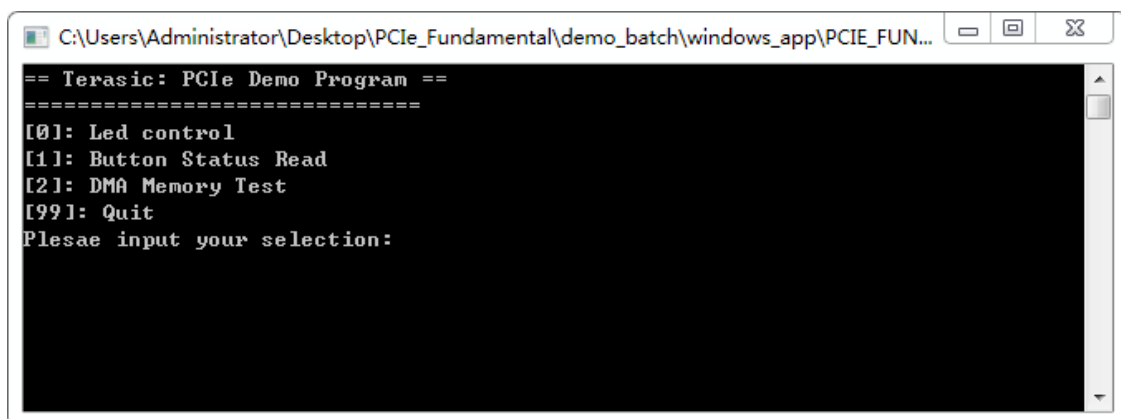
**Figure 7-9 FPGA board connect to PC**

2. Configure FPGA with PCIE\_Fundamental.sof by executing the test.bat.
3. Install PCIe driver if necessary. The driver is located in the folder:  
CDROM\Demonstration \PCIE\_SW\_KIT\PCIE\_Driver.
4. Restart Windows
5. Make sure the Windows has detected the FPGA Board by checking the Windows Control panel as shown in **Figure 7-10**.



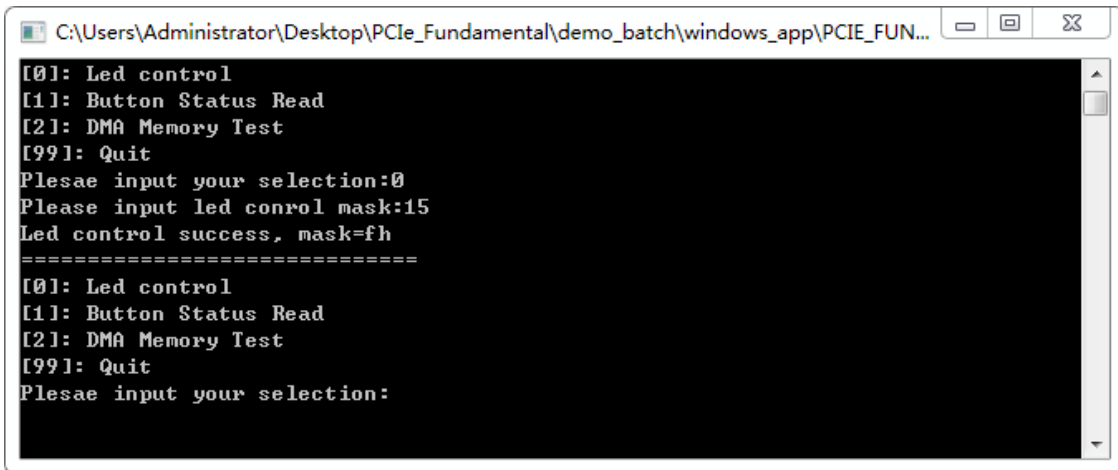
**Figure 7-10 Screenshot for PCIe Driver**

6. Goto windows\_app folder, execute PCIE\_FUNDMENTAL.exe. A menu will appear as shown in **Figure 7-11**.



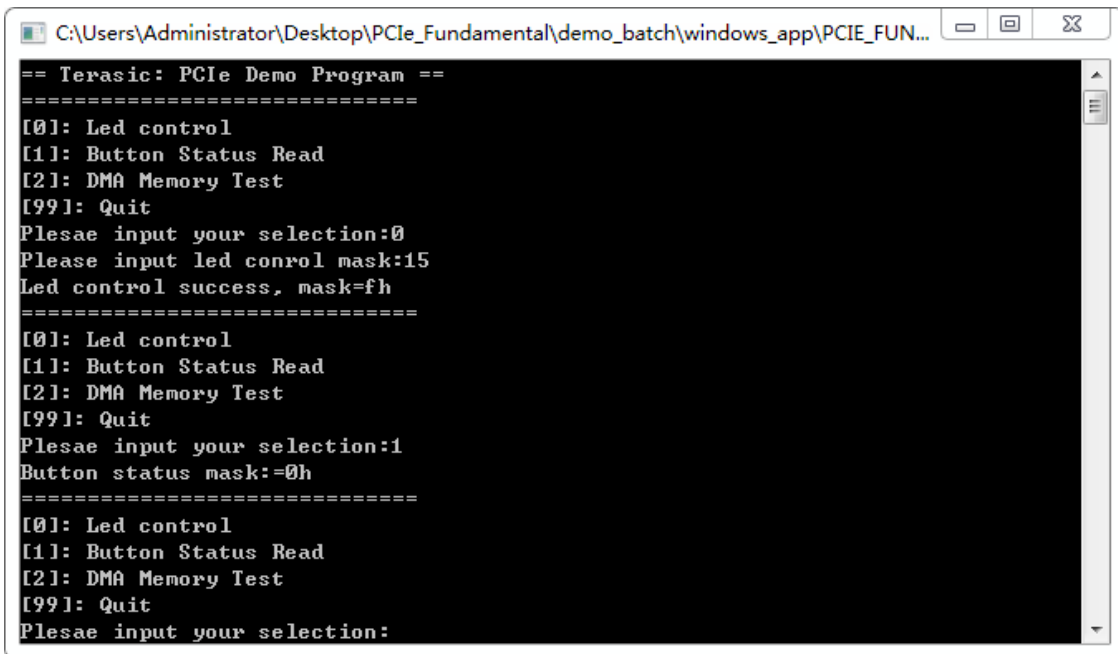
**Figure 7-11 Screenshot of Program Menu**

7. Type 0 followed by a ENTER key to select Led Control item, then input 15 (hex 0x0f) will make all led on as shown in **Figure 7-12**. If input 0(hex 0x00), all led will be turned off.



**Figure 7-12 Screenshot of LED Control**

8. Type 1 followed by an ENTER key to select Button Status Read item. The button status will be report as shown in **Figure 7-13**.



**Figure 7-13 Screenshot of Button Status Report**

9. Type-2 followed by an ENTER key to select DMA Testing item. The DMA test result will be report as shown in **Figure 7-14**.

```

C:\Users\Administrator\Desktop\PCIE_Fundamental\demo_batch\windows_app\PCIE_FUN...
== Terasic: PCIe Demo Program ==
=====
[0]: Led control
[1]: Button Status Read
[2]: DMA Memory Test
[99]: Quit
Plesae input your selection:0
Please input led control mask:15
Led control success, mask=fh
=====
[0]: Led control
[1]: Button Status Read
[2]: DMA Memory Test
[99]: Quit
Plesae input your selection:1
Button status mask:=0h
=====
[0]: Led control
[1]: Button Status Read
[2]: DMA Memory Test
[99]: Quit
Plesae input your selection:2
DMA-Memory (Size = 524288 bytes) pass
=====
[0]: Led control
[1]: Button Status Read
[2]: DMA Memory Test
[99]: Quit
Plesae input your selection:

```

**Figure 7-14 Screenshot of DMA Memory Test Result**

10. Type 99 followed by an ENTER key to exit this test program

## ■ Development Tools

- Quartus Prime 16.1.2 Standard Edition
- Visual C++ 2012

## ■ Demonstration Source Code Location

- Quartus Project: Demonstrations\PCIE\_Fundamental
- Visual C++ Project: Demonstrations\PCIE\_SW\_KIT\PCIE\_FUNDAMENTAL

## ■ FPGA Application Design

**Figure 7-15** shows the system block diagram in the FPGA system. In the Qsys, Altera PIO controller is used to control the LED and monitor the Button Status, and the On-Chip memory is

used for performing DMA testing. The PIO controllers and the On-Chip memory are connected to the PCI Express Hard IP controller through the Memory-Mapped Interface.

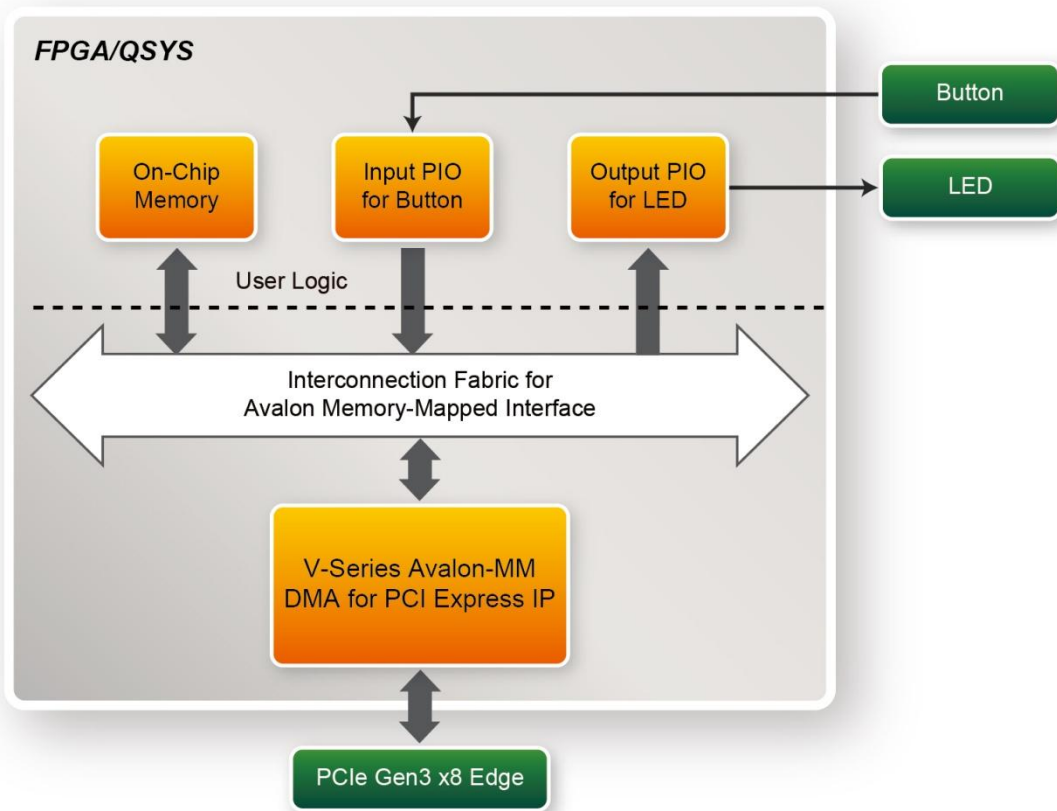


Figure 7-15 Hardware block diagram of the PCIe reference design

## ■ Windows Based Application Software Design

The application software project is built by Visual C++ 2012. The project includes the following major files:

Name	Description
PCIE_FUNDAMENTAL.cpp	Main program
PCIE.c	Implement dynamically load for
PCIE.h	TERAISC_PCIE_AVMM.DLL
TERASIC_PCIE_AVMM.h	SDK library file, defines constant and data structure

The main program PCIE\_FUNDAMENTAL.cpp includes the header file "PCIE.h" and defines the

controller address according to the FPGA design.

```
#define DEMO_PCIE_USER_BAR          PCIE_BAR4
#define DEMO_PCIE_IO_LED_ADDR      0x4000010
#define DEMO_PCIE_IO_BUTTON_ADDR   0x4000020
#define DEMO_PCIE_MEM_ADDR         0x00000000

#define MEM_SIZE                    (512*1024) //512KB
```

The base address of BUTTON and LED controllers are 0x4000010 and 0x4000020 based on PCIE\_BAR4, respectively. The on-chip memory base address is 0x00000000 relative to the DMA controller.

Before accessing the FPGA through PCI Express, the application first calls PCIE\_Load to dynamically load the Terasic\_PCIE\_AVMM.DLL. Then, it calls the PCIE\_Open to open the PCI Express driver. The constant DEFAULT\_PCIE\_VID and DEFAULT\_PCIE\_DID used in PCIE\_Open are defined in Terasic\_PCIE\_AVMM.h. If developer changes the Vendor ID, the Device ID, and the PCI Express IP, they also need to change the ID value defined in Terasic\_PCIE\_AVMM.h. If the return value of the PCIE\_Open is zero, it means the driver cannot be accessed successfully. In this case, please make sure:

- The FPGA is configured with the associated bit-stream file and the host is rebooted.
- The PCI express driver is loaded successfully.

The LED control is implemented by calling PCIE\_Write32 API, as shown below:

```
bPass = PCIE_Write32(hPCIE, DEMO_PCIE_USER_BAR, DEMO_PCIE_IO_LED_ADDR, (DWORD)Mask);
```

The button status query is implemented by calling the **PCIE\_Read32** API, as shown below:

```
PCIE_Read32(hPCIE, DEMO_PCIE_USER_BAR, DEMO_PCIE_IO_BUTTON_ADDR, &Status);
```

The memory-mapped memory read and write test is implemented by **PCIE\_DmaWrite** and **PCIE\_DmaRead** API, as shown below:

```
PCIE_DmaWrite(hPCIE, LocalAddr, pWrite, nTestSize);

PCIE_DmaRead(hPCIE, LocalAddr, pRead, nTestSize);
```



## 7.4 PCIe Reference Design – DDR3

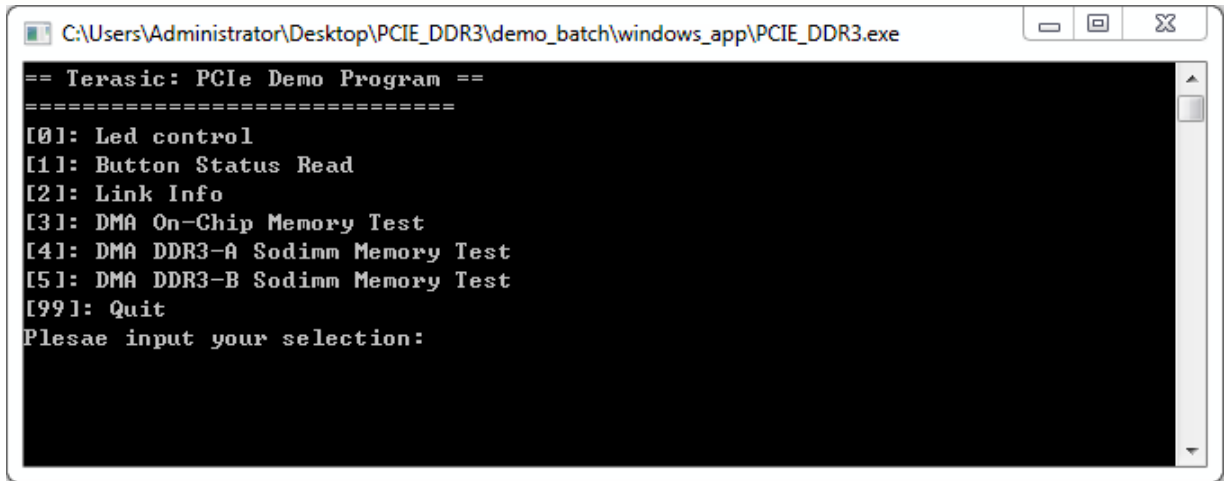
The application reference design shows how to add DDR3 Memory Controllers into the PCIe Quartus project based on the PCI\_Fundamental Quartus project and perform 2GB data DMA for both SODIMM. Also, this demo shows how to call “PCIE\_ConfigRead32” API to check PCIe link status.

### ■ Demonstration Files Location

- The demo file is located in the batch folder:
  - CDROM\demonstrations\PCIe\_DDR3\Demo\_batch
- The folder includes following files:
  - FPGA Configuration File: PCIe\_DDR3.sof
  - Download Batch file: test.bat
  - Windows Application Software folder : windows\_app, includes
    - ◆ PCIE\_DDR3.exe
    - ◆ TERASIC\_PCIE\_AVMM.dll

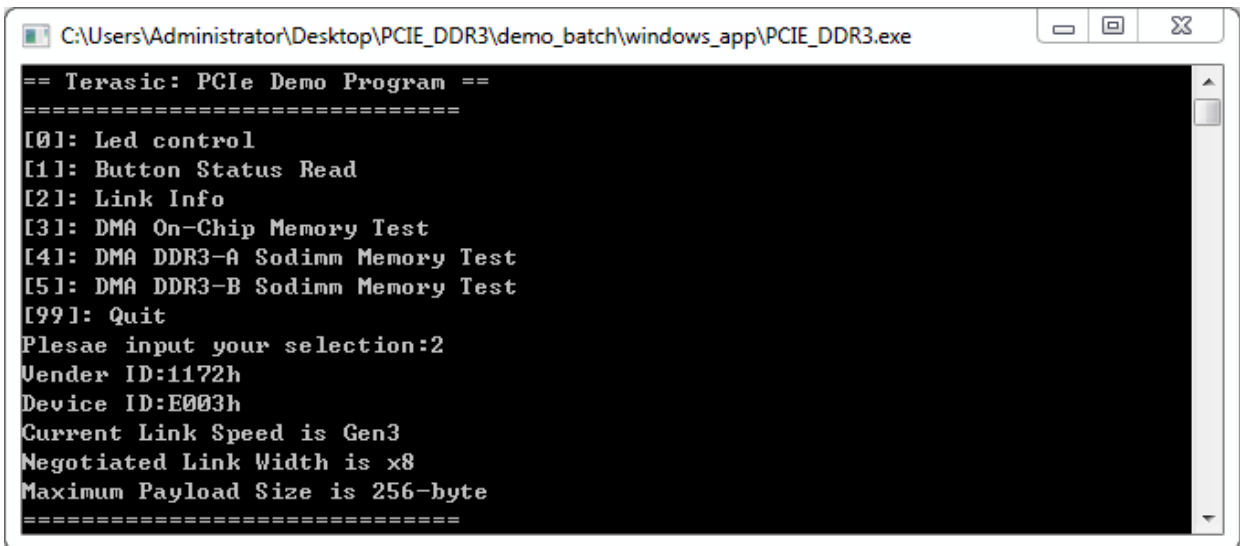
### ■ Demonstration Setup

1. Install both DDR3 1600 2GB SODIMM on the FPGA board.
2. Install the FPGA board on your PC.
3. Configure FPGA with PCIe\_DDR3.sof by executing the test.bat.
4. Install PCIe driver if necessary.
5. Restart Windows
6. Make sure the Windows has detected the FPGA Board by checking the Windows Control panel.
7. Goto windows\_app folder, execute PCIE\_DDR3.exe. A menu will appear as shown in **Figure 7-16**.



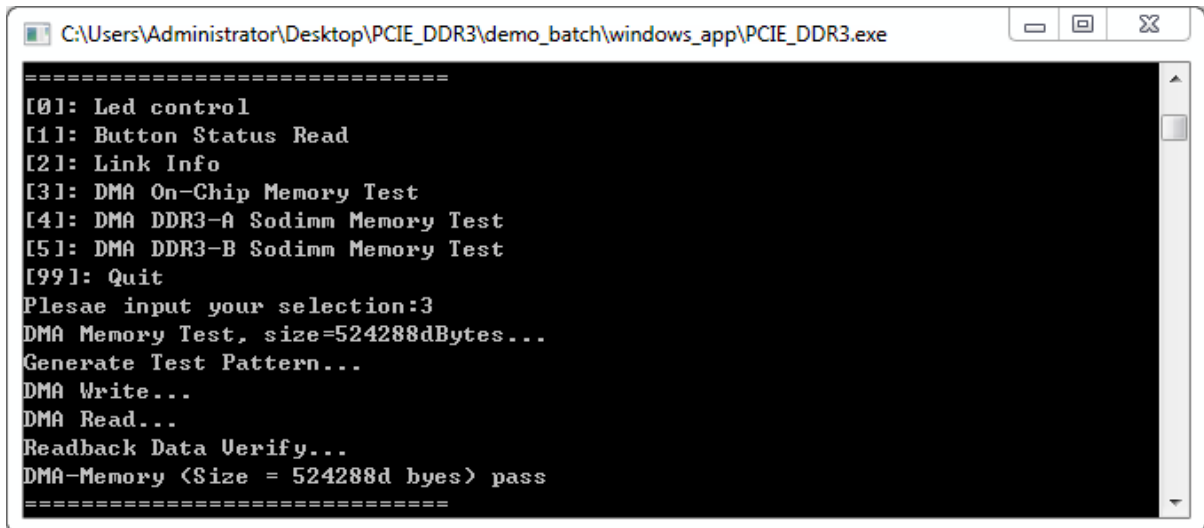
**Figure 7-16 Screenshot of Program Menu**

8. Type 2 followed by the ENTER key to select Link Info item. The PICE link information will be shown as in **Figure 7-17**. Gen3 link speed and x8 link width are expected.



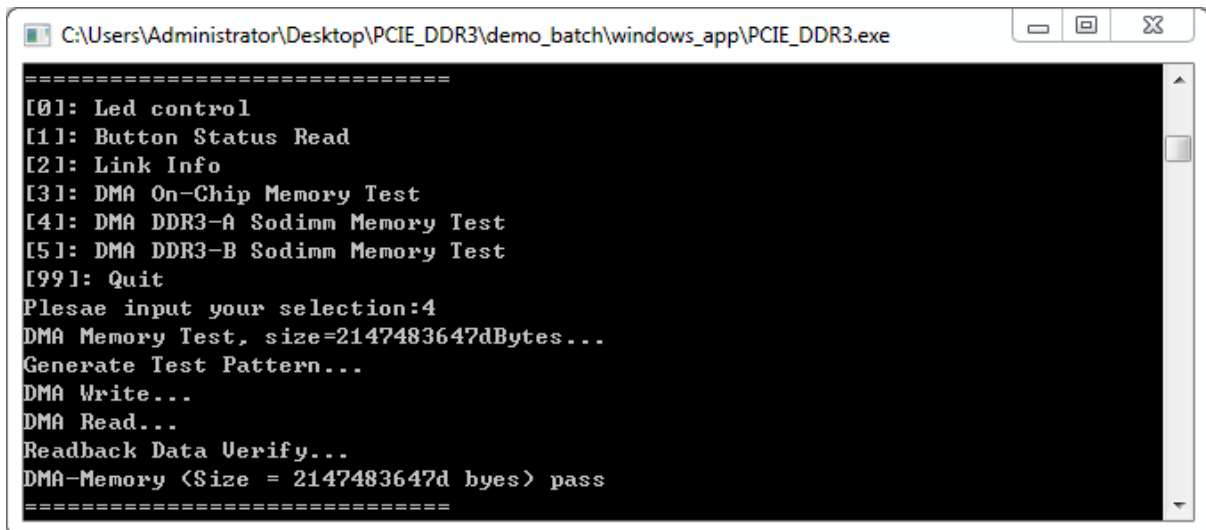
**Figure 7-17 Screenshot of Link Info**

9. Type 3 followed by the ENTER key to select DMA On-Chip Memory Test item. The DMA write and read test result will be reported as shown in **Figure 7-18**.



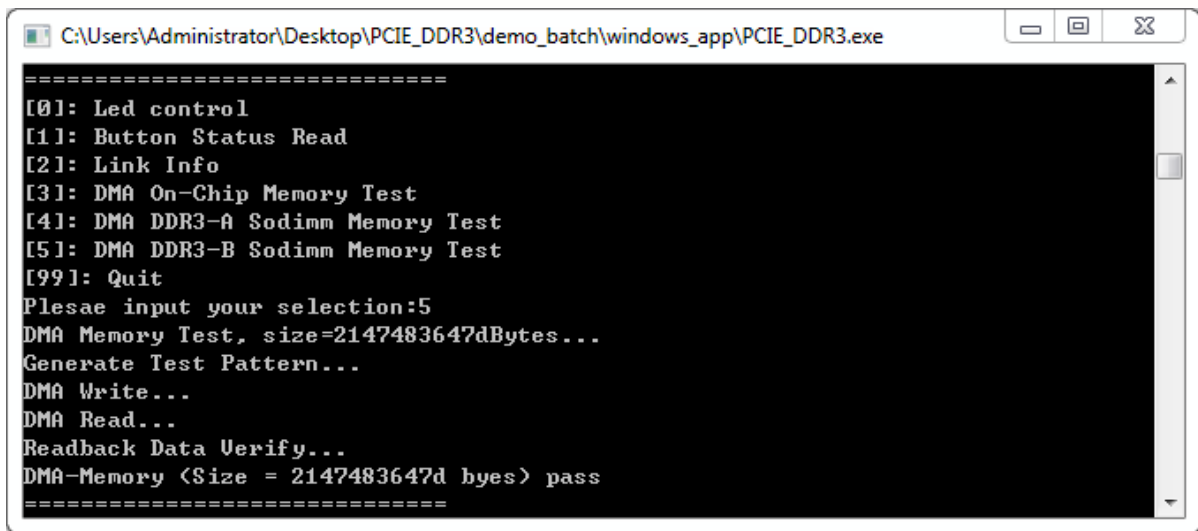
**Figure 7-18 Screenshot of On-Chip Memory DMA Test Result**

- Type-4 followed by the ENTER key to select DMA DDR3-A SODIMM Memory Test item. The DMA write and read test result will be report as shown in **Figure 7-19**.



**Figure 7-19 Screenshot of DDR3-A SODIMM Memory DMA Test Result**

- Type-5 followed by an ENTER key to select DMA DDR3-B SODIMM Memory Test item. The DMA write and read test result will be report as shown in **Figure 7-20**.



**Figure 7-20 Screenshot of DDR3-B SODIMM Memory DAM Test Result**

12. Type 99 followed by the ENTER key to exit this test program.

## ■ Development Tools

- Quartus Prime 16.1.2 Standard Edition
- Visual C++ 2012

## ■ Demonstration Source Code Location

- Quartus Project: Demonstrations\PCIE\_DDR3
- Visual C++ Project: Demonstrations\PCIE\_SW\_KIT\PCIE\_DDR3

## ■ FPGA Application Design

**Figure 7-21** shows the system block diagram in the FPGA system. In the Qsys, Altera PIO controller is used to control the LED and monitor the Button Status, and the On-Chip memory and DDR3 SODIMM Memory are used for performing DMA testing. The PIO controllers, the On-Chip memory and DDR3 SODIMM Memory are connected to the PCI Express Hard IP controller through the Memory-Mapped Interface.

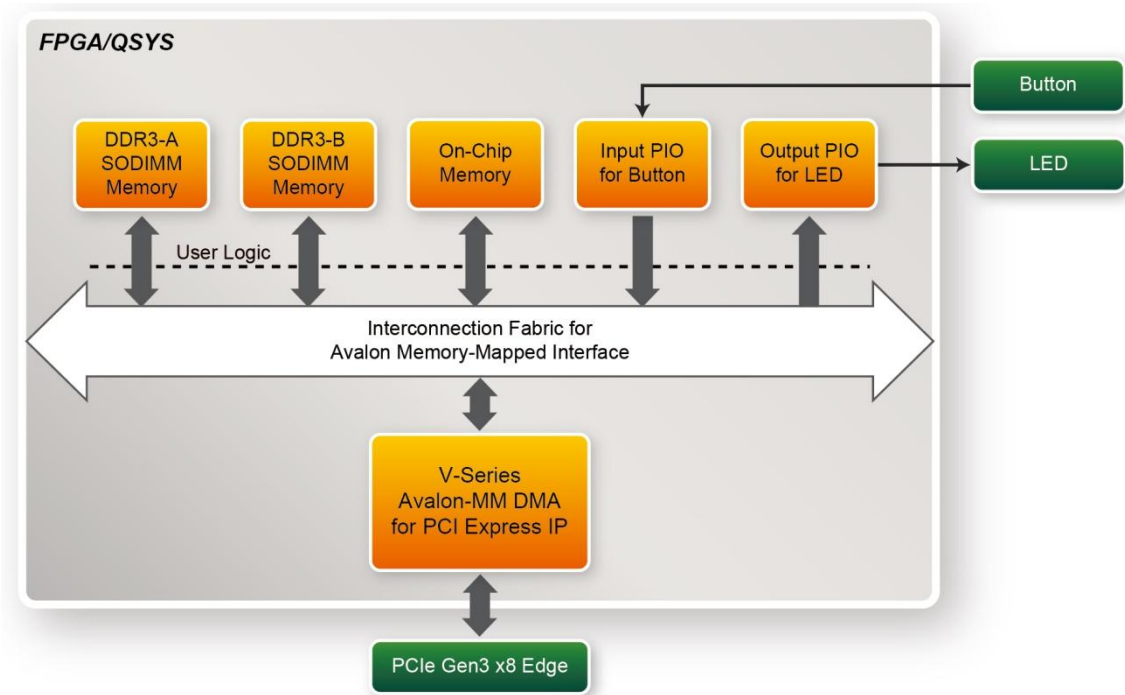


Figure 7-21 Hardware block diagram of the PCIe DDR3 reference design

## ■ Windows Based Application Software Design

The application software project is built by Visual C++ 2012. The project includes the following major files:

Name	Description
PCIE_DDR3.cpp	Main program
PCIE.c	Implement dynamically load for TERAISC_PCIE_AVMM.DLL
PCIE.h	
TERASIC_PCIE_AVMM.h	SDK library file, defines constant and data structure

The main program PCIE\_DDR3.cpp includes the header file "PCIE.h" and defines the controller address according to the FPGA design.

```

#define DEMO_PCIE_USER_BAR          PCIE_BAR4
#define DEMO_PCIE_IO_LED_ADDR       0x4000010
#define DEMO_PCIE_IO_BUTTON_ADDR    0x4000020
#define DEMO_PCIE_ONCHIP_MEM_ADDR    0x00000000
#define DEMO_PCIE_DDR3A_MEM_ADDR     0x100000000
#define DEMO_PCIE_DDR3B_MEM_ADDR     0x200000000

#define ONCHIP_MEM_TEST_SIZE         (512*1024) //512KB
#define DDR3A_MEM_TEST_SIZE          (2*1024*1024*1024) //2GB
#define DDR3B_MEM_TEST_SIZE          (2*1024*1024*1024) //2GB

```

The base address of BUTTON and LED controllers are 0x4000010 and 0x4000020 based on PCIE\_BAR4, respectively. The on-chip memory base address is 0x00000000 relative to the DMA controller. **The above definition is the same as those in the PCIe Fundamental demo.**

Before accessing the FPGA through PCI Express, the application first calls PCIE\_Load to dynamically load the Terasic\_PCIE\_AVMM.DLL. Then, it calls PCIE\_Open to open the PCI Express driver. The constant DEFAULT\_PCIE\_VID and DEFAULT\_PCIE\_DID used in PCIE\_Open are defined in Terasic\_PCIE\_AVMM.h. If the developer changes the Vendor ID, Device ID, and PCI Express IP, they also need to change the ID value defined in Terasic\_PCIE\_AVMM.h. If the return value of PCIE\_Open is zero, it means the driver cannot be accessed successfully. In this case, please make sure:

- The FPGA is configured with the associated bit-stream file and the host is rebooted.
- The PCI express driver is loaded successfully.

The LED control is implemented by calling PCIE\_Write32 API, as shown below:

```
bPass = PCIE_Write32(hPCIE, DEMO_PCIE_USER_BAR, DEMO_PCIE_IO_LED_ADDR, (DWORD)Mask);
```

The button status query is implemented by calling the PCIE\_Read32 API, as shown below:

```
PCIE_Read32(hPCIE, DEMO_PCIE_USER_BAR, DEMO_PCIE_IO_BUTTON_ADDR, &Status);
```

The memory-mapped memory read and write test is implemented by PCIE\_DmaWrite and PCIE\_DmaRead API, as shown below:

```
PCIE_DmaWrite(hPCIE, LocalAddr, pWrite, nTestSize);

PCIE_DmaWrite(hPCIE, LocalAddr, pWrite, nTestSize);
```

The pcie link information is implemented by PCIE\_ConfigRead32 API, as shown below:

```
// read config - link status
if (PCIE_ConfigRead32(hPCIE, 0x90, &Data32)){
    switch((Data32 >> 16) & 0x0F){
        case 1:
            printf("Current Link Speed is Gen1\r\n");
            break;
        case 2:
            printf("Current Link Speed is Gen2\r\n");
            break;
        case 3:
            printf("Current Link Speed is Gen3\r\n");
            break;
        default:
            printf("Current Link Speed is Unknown\r\n");
            break;
    }
    switch((Data32 >> 20) & 0x3F){
        case 1:
            printf("Negotiated Link Width is x1\r\n");
            break;
        case 2:
            printf("Negotiated Link Width is x2\r\n");
            break;
        case 4:
            printf("Negotiated Link Width is x4\r\n");
            break;
        case 8:
            printf("Negotiated Link Width is x8\r\n");
            break;
        case 16:
            printf("Negotiated Link Width is x16\r\n");
            break;
        default:
            printf("Negotiated Link Width is Unknown\r\n");
            break;
    }
}
else{
    bPass = false;
}
```

# Transceiver Verification

This chapter describes how to verify the FPGA transceivers using the test code provided in the DE5-Net system CD.

## 8.1 Test Code

The transceiver test code verifies the transceiver channels through an external loopback method. The following transceiver channels can be verified with different data rates:

- 10.3125 Gbps: SPF-A, SPF-B, SPF-C and SPF-D
  - 6.0 Gbps: SATA Host-0, SATA Host-1, SATA Device-0, and SATA Device-1
- Gbps: PCIe Channel 0~7

## 8.2 Loopback Fixture

To enable an external loopback of transceiver channels, specific loopback fixtures are required. Some fixtures may be proprietary to Terasic.

For SFP+ loopback, optical SFP+ loopback fixtures are required. **Figure 8-1** shows the optical SFP+ loopback fixture.



**Figure 8-1** Optical SFP+ Loopback Fixture



Figure 8-2 shows the SATA loopback fixture.



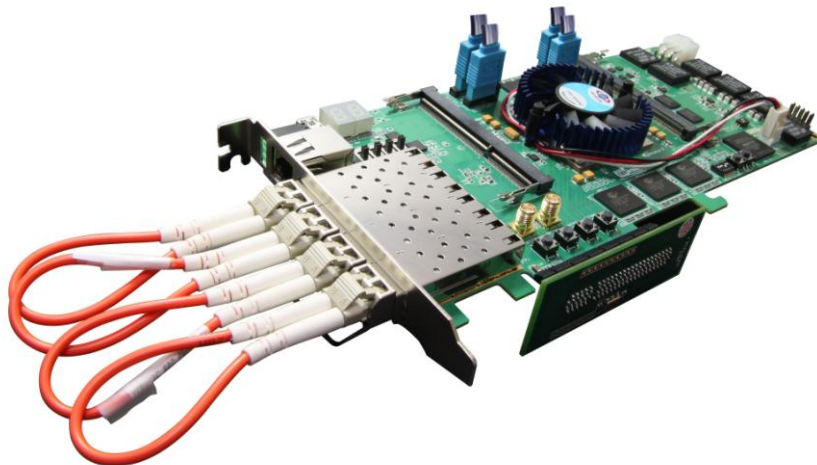
**Figure 8-2** SATA Loopback Fixture

Figure 8-3 shows the Terasic PCIe loopback fixture.



**Figure 8-3** PCIe Loopback Fixture

Figure 8-4 shows the FPGA board with all transceiver loopback fixtures installed.



**Figure 8-4** Transceiver Loopback Fixtures Installed

## 8.3 Testing

The transceiver test code is available in the folder System CD\Tool\Transceiver\_Test. Here are the procedures to perform transceiver channel test:

1. Copy **Transceiver\_Test** folder to your local disk.
2. Ensure that the FPGA board is NOT powered on.
3. Plug-in the SPF+ loopback fixtures if the SPF+ transceivers will be tested.
4. Plug-in the SATA loopback fixtures if the SATA transceivers will be tested.
5. Plug-in the PCIe loopback fixture if PCIe transceivers will be tested. Also, make sure PCIe Mode SW7 is switched to x8 mode.
6. Connect your FPGA board to your PC with a mini USB cable.
7. Power on the FPGA board
8. Execute 'xcvr\_test.bat" in the **Transceiver\_Test** folder under your local disk.
9. The batch file will download .sof and .elf files, and start the test immediately. The test result is shown in the Nios-Terminal, as shown in **Figure 8-5**.
10. To terminate the test, press one of the BUTTON0~3 buttons on the FPGA board. The loopback test will terminate, and the test summary will be shown in the Nios-Terminal, as shown in **Figure 8-6**.

```

C:\> Altera Nios II EDS 12.0sp2 [gcc4]
Info (209061): Ended Programmer operation at Tue Nov 06 09:03:36 2012
Info: Quartus II 32-bit Programmer was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 617 megabytes
Info: Processing ended: Tue Nov 06 09:03:36 2012
Info: Elapsed time: 00:00:22
Info: Total CPU time (on all processors): 00:00:11
Using cable "DE5 Standard [USB-1]", device 1, instance 0x00
Resetting and pausing target processor: OK
Initializing CPU cache (if present)
OK
Downloaded 105KB in 0.1s
Verified OK
Starting processor at address 0x000201B4
nios2-terminal: connected to hardware target using JTAG UART on cable
nios2-terminal: "DE5 Standard [USB-1]", device 1, instance 0
nios2-terminal: <Use the IDE stop button or Ctrl-C to terminate>

All Xcvr Channel Test...
[5]SFP-A=Pass, SFP-B=Pass, SFP-C=Pass, SFP-D=Pass, SATA HOST_0=Pass, SATA HOST_1
=Pass, SATA DEVICE_0=Pass, SATA DEVICE_1=Pass, PCIE_0=Pass, PCIE_1=Pass, PCIE_2=
Pass, PCIE_3=Pass, PCIE_4=Pass, PCIE_5=Pass, PCIE_6=Pass, PCIE_7=Pass,
[10]SFP-A=Pass, SFP-B=Pass, SFP-C=Pass, SFP-D=Pass, SATA HOST_0=Pass, SATA HOST_
1=Pass, SATA DEVICE_0=Pass, SATA DEVICE_1=Pass, PCIE_0=Pass, PCIE_1=Pass, PCIE_2
=Pass, PCIE_3=Pass, PCIE_4=Pass, PCIE_5=Pass, PCIE_6=Pass, PCIE_7=Pass,
[15]SFP-A=Pass, SFP-B=Pass, SFP-C=Pass, SFP-D=Pass, SATA HOST_0=Pass, SATA HOST_
1=Pass, SATA DEVICE_0=Pass, SATA DEVICE_1=Pass, PCIE_0=Pass, PCIE_1=Pass, PCIE_2
=Pass, PCIE_3=Pass, PCIE_4=Pass, PCIE_5=Pass, PCIE_6=Pass, PCIE_7=Pass,

```

Figure 8-5 Transceiver Loopback Test in Progress

```

C:\> Altera Nios II EDS 12.0sp2 [gcc4]
=Pass, PCIE_3=Pass, PCIE_4=Pass, PCIE_5=Pass, PCIE_6=Pass, PCIE_7=Pass,
[100]SFP-A=Pass, SFP-B=Pass, SFP-C=Pass, SFP-D=Pass, SATA HOST_0=Pass, SATA HOST_
1=Pass, SATA DEVICE_0=Pass, SATA DEVICE_1=Pass, PCIE_0=Pass, PCIE_1=Pass, PCIE_
2=Pass, PCIE_3=Pass, PCIE_4=Pass, PCIE_5=Pass, PCIE_6=Pass, PCIE_7=Pass,
[105]SFP-A=Pass, SFP-B=Pass, SFP-C=Pass, SFP-D=Pass, SATA HOST_0=Pass, SATA HOST_
1=Pass, SATA DEVICE_0=Pass, SATA DEVICE_1=Pass, PCIE_0=Pass, PCIE_1=Pass, PCIE_
2=Pass, PCIE_3=Pass, PCIE_4=Pass, PCIE_5=Pass, PCIE_6=Pass, PCIE_7=Pass,
===Test Report===
Test Result:PASS
Test Duration:106 seconds<1 Minutes>
SFP-A Pass
SFP-B Pass
SFP-C Pass
SFP-D Pass
SATA HOST_0 Pass
SATA HOST_1 Pass
SATA DEVICE_0 Pass
SATA DEVICE_1 Pass
PCIE_0 Pass
PCIE_1 Pass
PCIE_2 Pass
PCIE_3 Pass
PCIE_4 Pass
PCIE_5 Pass
PCIE_6 Pass
PCIE_7 Pass

```

Figure 8-6 Transceiver Loopback Test Result Summary