

Fixed Voltage Series - DO-214 (pxxx1s)



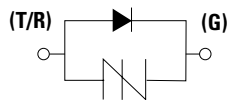
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

Fixed Voltage Series DO-214 (pxxx1s) are uni-directional SIDActo[®]r components designed to protect SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients. The series provides single line protection using a fixed voltage switching component for negative surges. All positive surges are routed through an internal diode to a ground reference.

Features and Benefits

- RoHS compliant, lead-free, and halogen-free
- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Integrated diode for positive voltage surges
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Intra-building*
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @ $I_{DRM}=5\mu A$	V_S @ 100V/ μs	I_H	I_S	I_T	V_T @ $I_T=2.2$ Amps	V_F	Capacitance @ 1MHz, -2V bias	
		V min	V max	mA min	mA max	A max	V max	V max	pF	
										pF min
P0181SALRP	P018A	18	40	100	800	2.2	4	5	30	90
P0641SALRP	P61A	58	77	120	800	2.2	4	5	50	90
P0721SALRP	P71A	65	88	120	800	2.2	4	5	45	85
P0901SALRP	P91A	75	98	120	800	2.2	4	5	45	80
P1101SALRP	P01A	95	130	120	800	2.2	4	5	40	70
P1301SALRP	P131A	120	160	120	800	2.2	4	5	40	70
P1701SALRP	P17A	160	200	120	800	2.2	4	5	30	55
P0641SCLRP	P61C	58	77	120	800	2.2	4	5	65	200
P0721SCLRP	P71C	65	88	120	800	2.2	4	5	60	190
P0901SCLRP	P91C	75	98	120	800	2.2	4	5	60	180
P1101SCLRP	P01C	95	130	120	800	2.2	4	5	50	160
P1201SCLRP	P121C	105	140	120	800	2.2	4	5	50	160
P1301SCLRP	P131C	120	160	120	800	2.2	4	5	50	160
P1701SCLRP	P17C	160	200	120	800	2.2	4	5	40	130
P0641SDLRP	P61D	58	77	120	800	2.2	4	5	65	200
P0721SDLRP	P71D	65	88	120	800	2.2	4	5	60	190
P0901SDLRP	P91D	75	98	120	800	2.2	4	5	60	180
P1101SDLRP	P01D	95	130	120	800	2.2	4	5	50	160
P1301SDLRP	P131D	120	160	120	800	2.2	4	5	50	160
P1701SDLRP	P17D	160	200	120	800	2.2	4	5	40	130

Notes:
 - Absolute maximum ratings measured at $T_J = 25^\circ C$ (unless otherwise noted).
 - Components are not appropriate for positive ringing systems.

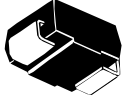
Surge Ratings

Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 ¹ 0.5/700 ²	2/10 ^{1,3} 2/10 ²	8/20 ¹ 1.2/50 ²	10/160 ¹ 10/160 ²	10/560 ¹ 10/560 ²	5/320 ¹ 9/720 ²	10/360 ¹ 10/360 ²	10/1000 ¹ 10/1000 ²	5/310 ¹ 10/700 ²		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/μs max
A	20	150	150	90	50	75	75	45	75	20	500
C	50	500	400	200	150	200	175	100	200	30	500
D	—	1000	800	—	—	—	—	200	350	50	1000

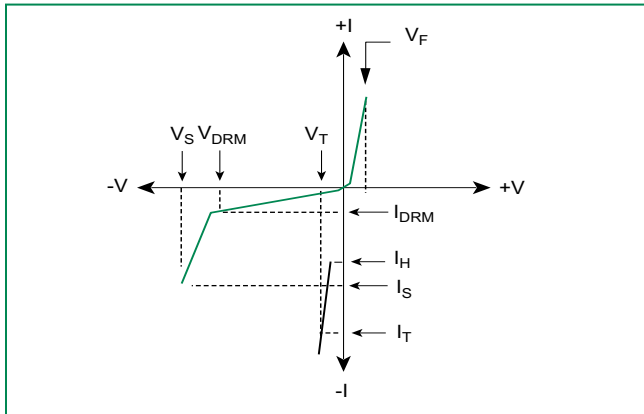
Notes:

- 1 Current waveform in μs
- 2 Voltage waveform in μs
- 3 2/10 of P0641SDLRP and P0721SDLRP is 800A min
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

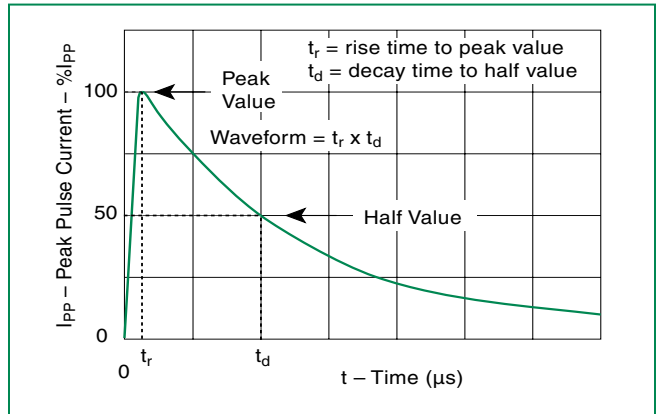
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-214AA 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{θJA}$	Thermal Resistance: Junction to Ambient	90	°C/W

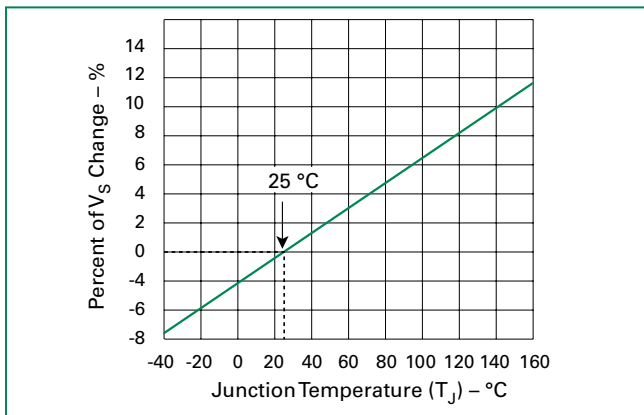
V-I Characteristics



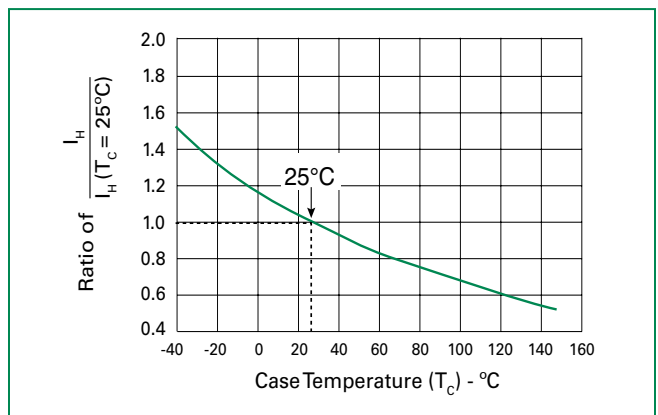
$t_r \times t_d$ Pulse Waveform



Normalized V_S Change vs. Junction Temperature

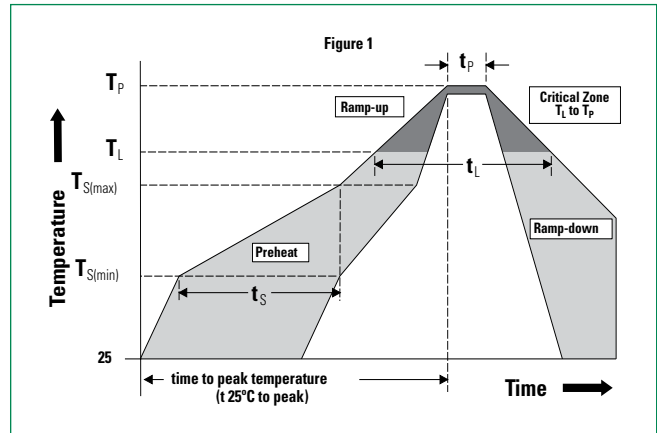


Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition	Pb-Free assembly (see Fig. 1)	
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)	3°C/sec. Max.	
$T_{s(max)}$ to T_L - Ramp-up Rate	3°C/sec. Max.	
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_p)	+260(+0/-5)°C	
Time within 5°C of actual PeakTemp (t_p)	30 secs. Max.	
Ramp-down Rate	6°C/sec. Max.	
Time 25°C to Peak Temp (T_p)	8 min. Max.	
Do not exceed	+260°C	



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Additional Information



Datasheet

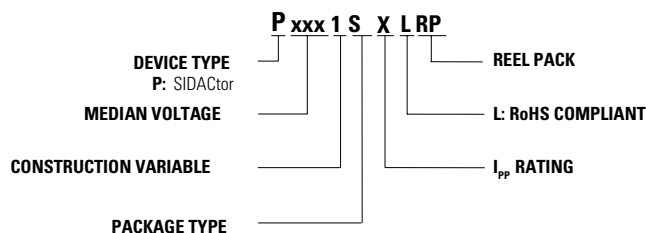


Resources



Samples

Part Numbering



Part Marking

