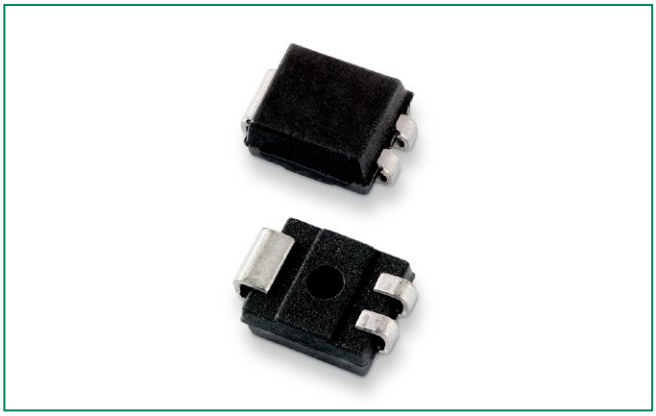
Littelfuse
Expertise Applied | Answers Delivered

Pxxx1Cx2L Series - Fixed Voltage TwinSLIC™ in Modified DO-214AA

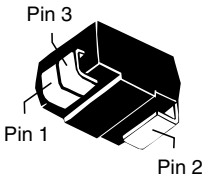
HF RoHS



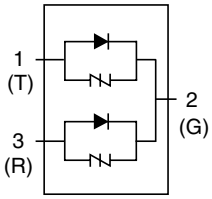
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

This fixed voltage, unidirectional, modified DO-214 SIDACtor thyristor series is designed to protect SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients.

These components provide single port protection implementing voltage switching characteristics for negative polarity surges and a clamping diode for positive polarity surges.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit
- Fails short circuit when surged in excess of ratings
- Integrated diodes for positive voltage surges
- Single-port protection
- RoHS Compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level*
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- Lightning, 150A (8/20 as defined in IEC 61000-4-5 2nd edition)
- YD/T 1082
- YD/T 993
- YD/T 950

* Series resistance required

Additional Information

Datasheet | **Resources** | **Samples**

© 2018 Littelfuse, Inc.
Specifications are subject to change without notice.
Revised: 05/08/18

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	V_F	Capacitance
		V min	V max	mA min	mA max	A max	V max	V max	
		Pin 1-2, 3-2							
P0641CA2LRP	P62A	58	77	120	800	2.2	4	5	See Capacitance Values table
P0721CA2LRP	P72A	65	88	120	800	2.2	4	5	
P0901CA2LRP	P92A	75	98	120	800	2.2	4	5	
P1101CA2LRP	P02A	95	130	120	800	2.2	4	5	
P1301CA2LRP	P131A	120	160	120	800	2.2	4	5	
P1501CA2LRP	P151A	140	185	120	800	2.2	4	5	
P1701CA2LRP	P17A	160	200	120	800	2.2	4	5	
P0641CB2LRP	P62B	58	77	120	800	2.2	4	5	
P0721CB2LRP	P72B	65	88	120	800	2.2	4	5	
P0901CB2LRP	P92B	75	98	120	800	2.2	4	5	
P1101CB2LRP	P02B	95	130	120	800	2.2	4	5	
P1301CB2LRP	P131B	120	160	120	800	2.2	4	5	
P1501CB2LRP	P151B	140	185	120	800	2.2	4	5	
P1701CB2LRP	P17B	160	200	120	800	2.2	4	5	

Notes:
- Absolute maximum ratings measured at T_A= 25ºC (unless otherwise noted).
- Components are not appropriate for positive ringing systems.

Capacitance Values

Part Number	pF Pin 1-2 / 3-2 Tip-Ground, Ring-Ground		pF Pin 1-3 Tip-Ring	
	MIN	MAX	MIN	MAX
P0641CA2LRP	40	70	20	45
P0721CA2LRP	35	70	20	45
P0901CA2LRP	30	65	20	40
P1101CA2LRP	25	55	15	35
P1301CA2LRP	25	45	15	30
P1701CA2LRP	25	40	15	25
P1501CA2LRP	25	45	15	30
P0641CB2LRP	40	70	20	45
P0721CB2LRP	35	70	20	45
P0901CB2LRP	30	65	20	40
P1101CB2LRP	25	55	15	35
P1301CB2LRP	25	45	15	30
P1501CB2LRP	25	45	15	30
P1701CB2LRP	25	40	15	25

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

© 2018 Littelfuse, Inc.
Specifications are subject to change without notice.
Revised: 05/08/18

Surge Ratings

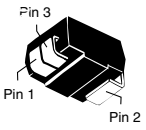
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
B	25	250	250	150	100	100	125	80	100	30	500

Notes:

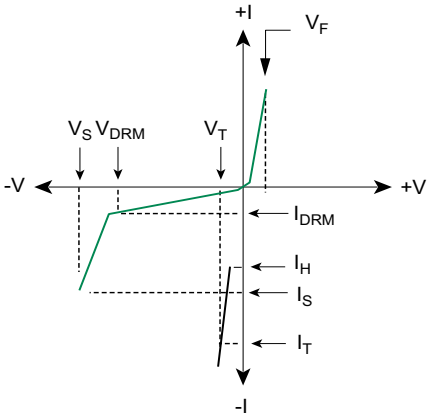
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

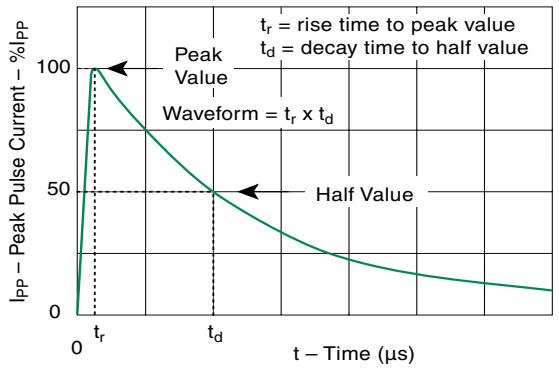
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified DO-214AA 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	85	°C/W

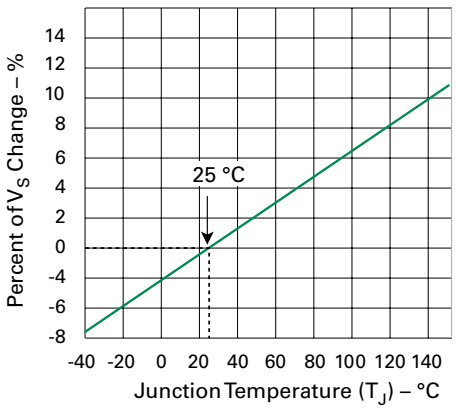
V-I Characteristics



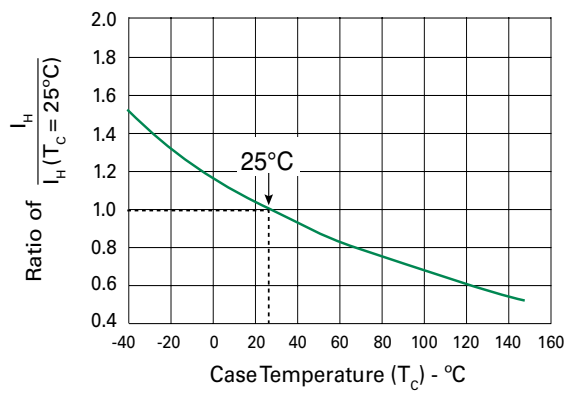
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



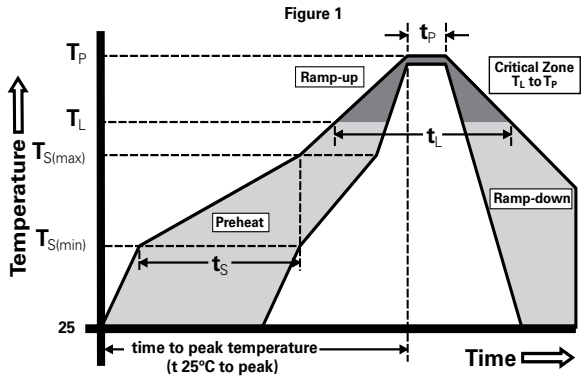
© 2018 Littelfuse, Inc.
Specifications are subject to change without notice.

Revised: 05/08/18

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



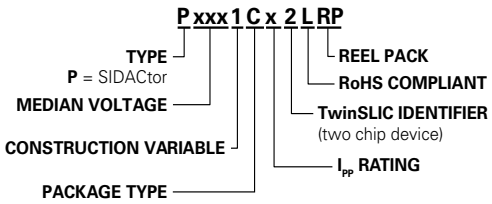
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized compound meeting flammability rating V-0.

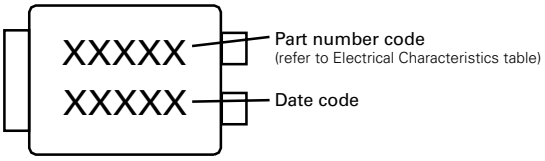
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C peak). JEDEC-J-STD-020, Level 1

Part Numbering



Part Marking



© 2018 Littelfuse, Inc.
Specifications are subject to change without notice.
Revised: 05/08/18