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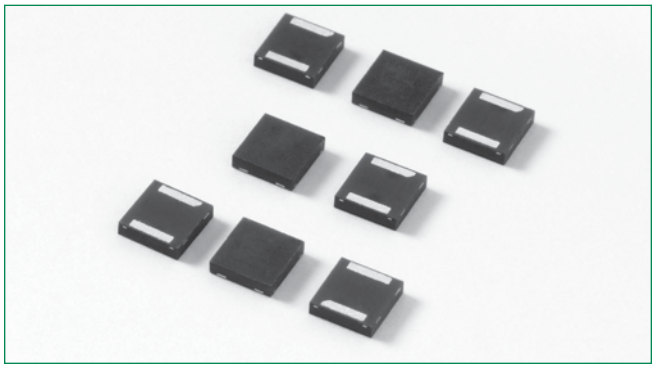
SIDACtor® Protection Thyristors
SLIC Protection

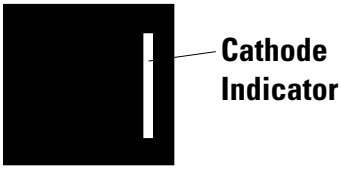
Fixed Voltage Q2L Series 3.3x3.3 QFN



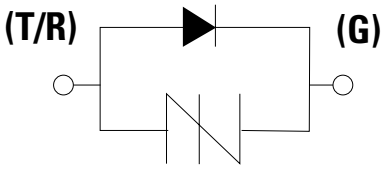
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

Fixed Voltage Q2L Series are uni-directional SIDACtor® thyristors designed to protect SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients.

The series provides single line protection using a fixed voltage switching component for negative surges. All positive surges are routed through an internal diode to a ground reference. The small size of the Q2L makes it ideal for high density applications.

Features and Benefits

- Integrated diode for positive voltage surges
- Low profile
- Small footprint QFN Package
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- RoHS Compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/Enhanced Level
- ITU K.20/21/Basic Level
- GR 1089 Inter-building
- GR-1089 Intra-building
- IEC 61000-4-5 2nd editin
- YD/T 950
- YD/T 993
- YD/T 1082

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	V_F	Capacitance @1MHz @ 2V bias	
		V min	V max	mA min	mA max	A max	V max	V max	pF min	pF max
P0641Q22CLRP	P61C	58	77	120	800	2.2	4	5	35	75
P0721Q22CLRP	P71C	65	88	120	800	2.2	4	5	25	45
P0901Q22CLRP	P91C	75	98	120	800	2.2	4	5	55	85
P1101Q22CLRP	P10C	95	130	120	800	2.2	4	5	50	75
P1301Q22CLRP	P13C	120	160	120	800	2.2	4	5	45	70
P1701Q22CLRP	P17C	160	200	120	800	2.2	4	5	45	70

Notes:
- Absolute maximum ratings measured at T_A= 25ºC (unless otherwise noted).
- Components are not appropriate for positive ringing systems.

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Surge Ratings

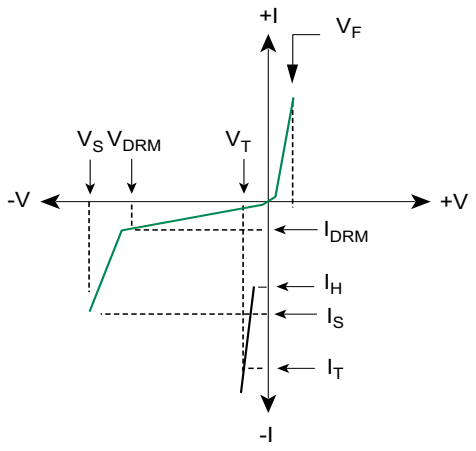
Series	I_{PP}					I_{TSM}	di/dt
	2/10µs	1.2/50µs/8/20µs	10/160µs	10/560µs	10/1000µs	50 / 60Hz	
	A min	A min	A min	A min	A min	A min	Amps/µs max
C	500	400	200	150	100	30	500

Notes:
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

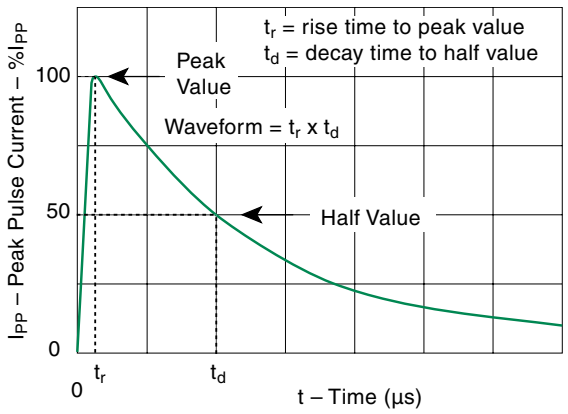
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
3.3x3.3 QFN 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

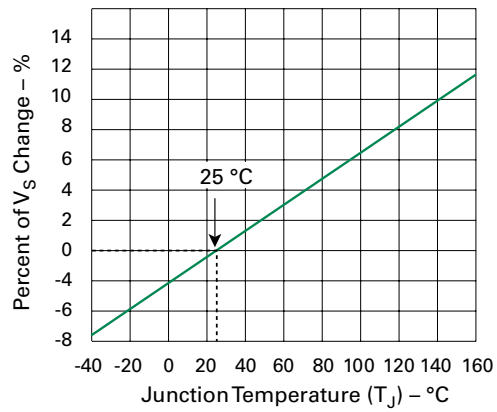
V-I Characteristics



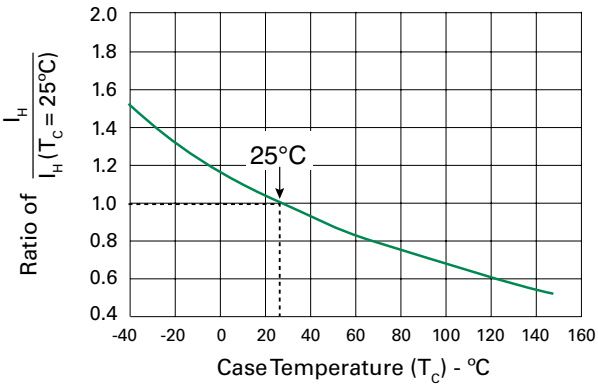
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



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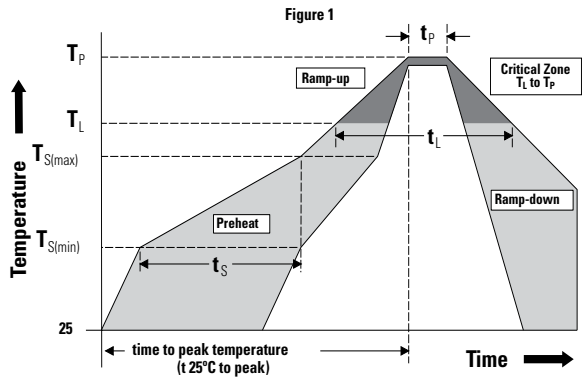
Soldering Parameters

Reflow Condition		Pb-Free assembly
Pre Heat	**- Temperature Min ($T_{s(min)}$)**	+150°C
	- Temperature Max ($T_{s(max)}$)	+200°C
	- Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	**- Temperature (T_L) (Liquidus)**	+217°C
	- Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



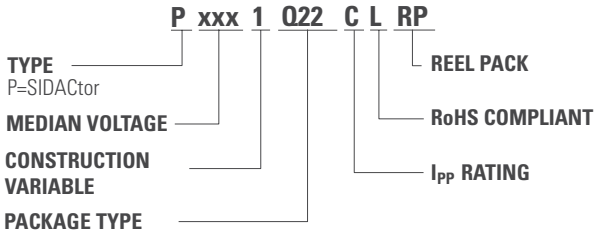
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

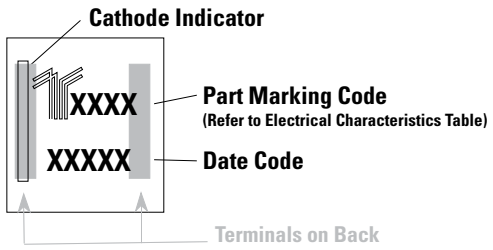
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{DC}) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering



Part Marking



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