

Fusion Family of Mixed Signal FPGAs

Features and Benefits

High-Performance Reprogrammable Flash Technology

- Advanced 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Nonvolatile, Retains Program when Powered Off
- Instant On Single-Chip Solution
- 350 MHz System Performance

Embedded Flash Memory

- User Flash Memory – 2 Mbits to 8 Mbits
 - Configurable 8-, 16-, or 32-Bit Datapath
 - 10 ns Access in Read-Ahead Mode
- 1 Kbit of Additional FlashROM

Integrated A/D Converter (ADC) and Analog I/O

- Up to 12-Bit Resolution and up to 600 Ksps
- Internal 2.56 V or External Reference Voltage
- ADC: Up to 30 Scalable Analog Input Channels
- High-Voltage Input Tolerance: –10.5 V to +12 V
- Current Monitor and Temperature Monitor Blocks
- Up to 10 MOSFET Gate Driver Outputs
 - P- and N-Channel Power MOSFET Support
 - Programmable 1, 3, 10, 30 μ A, and 20 mA Drive Strengths
- ADC Accuracy is Better than 1%

On-Chip Clocking Support

- Internal 100 MHz RC Oscillator (accurate to 1%)
- Crystal Oscillator Support (32 KHz to 20 MHz)
- Programmable Real-Time Counter (RTC)
- 6 Clock Conditioning Circuits (CCCs) with 1 or 2 Integrated PLLs
 - Phase Shift, Multiply/Divide, and Delay Capabilities
 - Frequency: Input 1.5–350 MHz, Output 0.75–350 MHz

Low Power Consumption

- Single 3.3 V Power Supply with On-Chip 1.5 V Regulator
- Sleep and Standby Low-Power Modes

In-System Programming (ISP) and Security

- ISP with 128-Bit AES via JTAG
- FlashLock® Designed to Protect FPGA Contents

Advanced Digital I/O

- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages – Up to 5 Banks per Chip
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, M-LVDS
 - Built-In I/O Registers
 - 700 Mbps DDR Operation
- Hot-Swappable I/Os
- Programmable Output Slew Rate, Drive Strength, and Weak Pull-Up/Down Resistor
- Pin-Compatible Packages across the Fusion® Family

SRAMs and FIFOs

- Variable-Aspect-Ratio 4,608-Bit SRAM Blocks ($\times 1$, $\times 2$, $\times 4$, $\times 9$, and $\times 18$ organizations available)
- True Dual-Port SRAM (except $\times 18$)
- Programmable Embedded FIFO Control Logic

Soft ARM Cortex-M1 Fusion Devices (M1)

- ARM® Cortex®-M1–Enabled

Pigeon Point ATCA IP Support (P1)

- Targeted to Pigeon Point® Board Management Reference (BMR) Starter Kits
- Designed in Partnership with Pigeon Point Systems
- ARM Cortex-M1 Enabled

MicroBlade Advanced Mezzanine Card Support (U1)

- Targeted to Advanced Mezzanine Card (AdvancedMC™ Designs)
- Designed in Partnership with MicroBlade
- 8051-Based Module Management Controller (MMC)

Table 1 • Fusion Family

| Fusion Devices | | AFS090 | AFS250 | AFS600 | AFS1500 |
|------------------------|-------------------------------|--------|----------|----------|-----------|
| ARM Cortex-M1* Devices | | | M1AFS250 | M1AFS600 | M1AFS1500 |
| Pigeon Point Devices | | | | P1AFS600 | P1AFS1500 |
| MicroBlade Devices | | | U1AFS250 | U1AFS600 | U1AFS1500 |
| General Information | System Gates | 90,000 | 250,000 | 600,000 | 1,500,000 |
| | Tiles (D-flip-flops) | 2,304 | 6,144 | 13,824 | 38,400 |
| | Secure (AES) ISP | Yes | Yes | Yes | Yes |
| | PLLs | 1 | 1 | 2 | 2 |
| | Globals | 18 | 18 | 18 | 18 |
| Memory | Flash Memory Blocks (2 Mbits) | 1 | 1 | 2 | 4 |
| | Total Flash Memory Bits | 2M | 2M | 4M | 8M |
| | FlashROM Bits | 1,024 | 1,024 | 1,024 | 1,024 |
| | RAM Blocks (4,608 bits) | 6 | 8 | 24 | 60 |
| | RAM kbits | 27 | 36 | 108 | 270 |
| Analog and I/Os | Analog Quads | 5 | 6 | 10 | 10 |
| | Analog Input Channels | 15 | 18 | 30 | 30 |
| | Gate Driver Outputs | 5 | 6 | 10 | 10 |
| | I/O Banks (+ JTAG) | 4 | 4 | 5 | 5 |
| | Maximum Digital I/Os | 75 | 114 | 172 | 252 |
| | Analog I/Os | 20 | 24 | 40 | 40 |

Note: *Refer to the Cortex-M1 product brief for more information.

Fusion Device Architecture Overview



Figure 1 • Fusion Device Architecture Overview (AFS600)

Package I/Os: Single-/Double-Ended (Analog)

| Fusion Devices | AFS090 | AFS250 | AFS600 | AFS1500 |
|-----------------------|------------|-----------------------|-----------------------|------------------------|
| ARM Cortex-M1 Devices | | M1AFS250 | M1AFS600 | M1AFS1500 |
| Pigeon Point Devices | | | P1AFS600 ¹ | P1AFS1500 ¹ |
| MicroBlade Devices | | U1AFS250 ² | U1AFS600 ² | U1AFS1500 ² |
| QN108 ³ | 37/9 (16) | | | |
| QN180 ³ | 60/16 (20) | 65/15 (24) | | |
| PQ208 ^{4, 5} | | 93/26 (24) | 95/46 (40) | |
| FG256 | 75/22 (20) | 114/37 (24) | 119/58 (40) | 119/58 (40) |
| FG484 | | | 172/86 (40) | 223/109 (40) |
| FG676 | | | | 252/126 (40) |

Notes:

1. Pigeon Point devices are only offered in FG484 and FG256.
2. MicroBlade devices are only offered in FG256.
3. Package not available.
4. Fusion devices in the same package are pin compatible with the exception of the PQ208 package (AFS250 and AFS600).
5. PQ208 package is discontinued.

Product Ordering Codes



Fusion Devices

AFS090 = 90,000 System Gates
 AFS250 = 250,000 System Gates
 AFS600 = 600,000 System Gates
 AFS1500 = 1,500,000 System Gates

ARM-Enabled Fusion Devices

M1AFS250 = 250,000 System Gates
 M1AFS600 = 600,000 System Gates
 M1AFS1500 = 1,500,000 System Gates

Pigeon Point Devices

P1AFS600 = 600,000 System Gates
 P1AFS1500 = 1,500,000 System Gates

MicroBlade Devices

U1AFS250 = 250,000 System Gates
 U1AFS600 = 600,000 System Gates
 U1AFS1500 = 1,500,000 System Gates

Notes:

- For Fusion devices, Quad Flat No Lead packages are only offered as RoHS compliant, QNG packages.
- MicroBlade and Pigeon Point devices only support FG packages.
- Package is discontinued.

Fusion Device Status

| Fusion | Status | Cortex-M1 | Status | Pigeon Point | Status | MicroBlade | Status |
|---------|------------|-----------|------------|--------------|------------|------------|------------|
| AFS090 | Production | | | | | | |
| AFS250 | Production | M1AFS250 | Production | | | U1AFS250 | Production |
| AFS600 | Production | M1AFS600 | Production | P1AFS600 | Production | U1AFS600 | Production |
| AFS1500 | Production | M1AFS1500 | Production | P1AFS1500 | Production | U1AFS1500 | Production |

Temperature Grade Offerings

| Fusion Devices | AFS090 | AFS250 | AFS600 | AFS1500 |
|-----------------------|--------|-----------------------|-----------------------|------------------------|
| ARM Cortex-M1 Devices | | M1AFS250 | M1AFS600 | M1AFS1500 |
| Pigeon Point Devices | | | P1AFS600 ³ | P1AFS1500 ³ |
| MicroBlade Devices | | U1AFS250 ⁴ | U1AFS600 ⁴ | U1AFS1500 ⁴ |
| QN108 ⁵ | C, I | – | – | – |
| QN180 ⁵ | C, I | C, I | – | – |
| PQ208 ⁶ | – | C, I | C, I | – |
| FG256 | C, I | C, I | C, I | C, I |
| FG484 | – | – | C, I | C, I |
| FG676 | – | – | – | C, I |

Notes:

1. C = Commercial Temperature Range: 0°C to 85°C Junction
2. I = Industrial Temperature Range: –40°C to 100°C Junction
3. Pigeon Point devices are only offered in FG484 and FG256.
4. MicroBlade devices are only offered in FG256.
5. Package not available.
6. Package is discontinued.

Speed Grade and Temperature Grade Matrix

| | Std. ¹ | –1 | –2 ² |
|----------------|-------------------|----|-----------------|
| C ³ | ✓ | ✓ | ✓ |
| I ⁴ | ✓ | ✓ | ✓ |

Notes:

1. MicroBlade devices are only offered in standard speed grade.
2. Pigeon Point devices are only offered in –2 speed grade.
3. C = Commercial Temperature Range: 0°C to 85°C Junction
4. I = Industrial Temperature Range: –40°C to 100°C Junction

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/index.php?option=com_content&id=137&lang=en&view=article.

Cortex-M1, Pigeon Point, and MicroBlade Fusion Device Information

This datasheet provides information for all Fusion (AFS), Cortex-M1 (M1), Pigeon Point (P1), and MicroBlade (U1) devices. The remainder of the document will only list the Fusion (AFS) devices. Please apply relevant information to M1, P1, and U1 devices when appropriate. Please note the following:

- Cortex-M1 devices are offered in the same speed grades and packages as basic Fusion devices.
- Pigeon Point devices are only offered in –2 speed grade and FG484 and FG256 packages.
- MicroBlade devices are only offered in standard speed grade and the FG256 package.

Table of Contents

Fusion Device Family Overview

| | |
|---------------------------------|------|
| Introduction | 1-1 |
| General Description | 1-1 |
| Unprecedented Integration | 1-4 |
| Related Documents | 1-10 |

Device Architecture

| | |
|---------------------------------|-------|
| Fusion Stack Architecture | 2-1 |
| Core Architecture | 2-2 |
| Clocking Resources | 2-18 |
| Real-Time Counter System | 2-31 |
| Embedded Memories | 2-39 |
| Analog Block | 2-76 |
| Analog Configuration MUX | 2-126 |
| User I/Os | 2-132 |
| Pin Descriptions | 2-223 |
| Security | 2-228 |

DC and Power Characteristics

| | |
|-------------------------------------|------|
| General Specifications | 3-1 |
| Calculating Power Dissipation | 3-10 |
| Power Consumption | 3-32 |

Package Pin Assignments

| | |
|-------------|------|
| QN108 | 4-1 |
| QN180 | 4-3 |
| PQ208 | 4-7 |
| FG256 | 4-11 |
| FG484 | 4-19 |
| FG676 | 4-27 |

Datasheet Information

| | |
|---|------|
| List of Changes | 5-1 |
| Datasheet Categories | 5-18 |
| Safety Critical, Life Support, and High-Reliability Applications Policy | 5-18 |

1 – Fusion Device Family Overview

Introduction

The Fusion mixed signal FPGA satisfies the demand from system architects for a device that simplifies design and unleashes their creativity. As the world's first mixed signal programmable logic family, Fusion integrates mixed signal analog, flash memory, and FPGA fabric in a monolithic device. Fusion devices enable designers to quickly move from concept to completed design and then deliver feature-rich systems to market. This new technology takes advantage of the unique properties of Microsemi flash-based FPGAs, including a high-isolation, triple-well process and the ability to support high-voltage transistors to meet the demanding requirements of mixed signal system design.

Fusion mixed signal FPGAs bring the benefits of programmable logic to many application areas, including power management, smart battery charging, clock generation and management, and motor control. Until now, these applications have only been implemented with costly and space-consuming discrete analog components or mixed signal ASIC solutions. Fusion mixed signal FPGAs present new capabilities for system development by allowing designers to integrate a wide range of functionality into a single device, while at the same time offering the flexibility of upgrades late in the manufacturing process or after the device is in the field. Fusion devices provide an excellent alternative to costly and time-consuming mixed signal ASIC designs. In addition, when used in conjunction with the ARM Cortex-M1 processor, Fusion technology represents the definitive mixed signal FPGA platform.

Flash-based Fusion devices are Instant On. As soon as system power is applied and within normal operating specifications, Fusion devices are working. Fusion devices have a 128-bit flash-based lock and industry-leading AES decryption, used to secure programmed intellectual property (IP) and configuration data. Fusion devices are the most comprehensive single-chip analog and digital programmable logic solution available today.

To support this new ground-breaking technology, Microsemi has developed a series of major tool innovations to help maximize designer productivity. Implemented as extensions to the popular Microsemi Libero® System-on-Chip (SoC) software, these new tools allow designers to easily instantiate and configure peripherals within a design, establish links between peripherals, create or import building blocks or reference designs, and perform hardware verification. This tool suite will also add comprehensive hardware/software debug capability as well as a suite of utilities to simplify development of embedded soft-processor-based solutions.

General Description

The Fusion family, based on the highly successful ProASIC®3 and ProASIC3E flash FPGA architecture, has been designed as a high-performance, programmable, mixed signal platform. By combining an advanced flash FPGA core with flash memory blocks and analog peripherals, Fusion devices dramatically simplify system design and, as a result, dramatically reduce overall system cost and board space.

The state-of-the-art flash memory technology offers high-density integrated flash memory blocks, enabling savings in cost, power, and board area relative to external flash solutions, while providing increased flexibility and performance. The flash memory blocks and integrated analog peripherals enable true mixed-mode programmable logic designs. Two examples are using an on-chip soft processor to implement a fully functional flash MCU and using high-speed FPGA logic to offer system and power supervisory capabilities. Instant On, and capable of operating from a single 3.3 V supply, the Fusion family is ideally suited for system management and control applications.

The devices in the Fusion family are categorized by FPGA core density. Each family member contains many peripherals, including flash memory blocks, an analog-to-digital-converter (ADC), high-drive outputs, both RC and crystal oscillators, and a real-time counter (RTC). This provides the user with a high level of flexibility and integration to support a wide variety of mixed signal applications. The flash memory block capacity ranges from 2 Mbits to 8 Mbits. The integrated 12-bit ADC supports up to 30 independently configurable input channels.

The on-chip crystal and RC oscillators work in conjunction with the integrated phase-locked loops (PLLs) to provide clocking support to the FPGA array and on-chip resources. In addition to supporting typical RTC uses such as watchdog timer, the Fusion RTC can control the on-chip voltage regulator to power down the device (FPGA fabric, flash memory block, and ADC), enabling a low power standby mode.

The Fusion family offers revolutionary features, never before available in an FPGA. The nonvolatile flash technology gives the Fusion solution the advantage of being a highly secure, low power, single-chip solution that is Instant On. Fusion is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based Fusion devices are Instant On and do not need to be loaded from an external boot PROM. On-board security mechanisms prevent access to the programming information and enable remote updates of the FPGA logic that are protected with high level security. Designers can perform remote in-system reprogramming to support future design iterations and field upgrades, with confidence that valuable IP is highly unlikely to be compromised or copied. ISP can be performed using the industry-standard AES algorithm with MAC data authentication on the device. The Fusion family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the Fusion family a cost-effective ASIC replacement solution for applications in the consumer, networking and communications, computing, and avionics markets.

Security

As the nonvolatile, flash-based Fusion family requires no boot PROM, there is no vulnerable external bitstream. Fusion devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Fusion devices utilize a 128-bit flash-based key lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the industry-leading AES-128 block cipher encryption standard (FIPS Publication 192). The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the DES standard, which was adopted in 1977. Fusion devices have a built-in AES decryption engine and a flash-based AES key that make Fusion devices the most comprehensive programmable logic device security solution available today. Fusion devices with AES-based security provide a high level of protection for remote field updates over public networks, such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the Fusion family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. Fusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. A Fusion device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Fusion FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Flash-based Fusion devices are Level 0 Instant On. Instant On Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for CPLDs. The Fusion Instant On clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of Instant On clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. Instant On from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design.

Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors is alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

Advanced Flash Technology

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary Fusion architecture provides granularity comparable to standard-cell ASICs. The Fusion device consists of several distinct and programmable architectural features, including the following (Figure 1-1 on page 1-5):

- Embedded memories
 - Flash memory blocks
 - FlashROM
 - SRAM and FIFO
- Clocking resources
 - PLL and CCC
 - RC oscillator
 - Crystal oscillator
 - No-Glitch MUX (NGMUX)
- Digital I/Os with advanced I/O standards
- FPGA VersaTiles
- Analog components
 - ADC
 - Analog I/Os supporting voltage, current, and temperature monitoring
 - 1.5 V on-board voltage regulator
 - Real-time counter

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic lookup table (LUT) equivalent or a D-flip-flop or latch (with or without enable) by programming the appropriate flash switch interconnections. This versatility allows efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi families of flash-based FPGAs. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid (3.3 V) single-voltage programming of Fusion devices via an IEEE 1532 JTAG interface.

Unprecedented Integration

Integrated Analog Blocks and Analog I/Os

Fusion devices offer robust and flexible analog mixed signal capability in addition to the high-performance flash FPGA fabric and flash memory block. The many built-in analog peripherals include a configurable 32:1 input analog MUX, up to 10 independent MOSFET gate driver outputs, and a configurable ADC. The ADC supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (Ksps), differential nonlinearity (DNL) < 1.0 LSB, and Total Unadjusted Error (TUE) of 0.72 LSB in 10-bit mode. The TUE is used for characterization of the conversion error and includes errors from all sources, such as offset and linearity. Internal bandgap circuitry offers 1% voltage reference accuracy with the flexibility of utilizing an external reference voltage. The ADC channel sampling sequence and sampling rate are programmable and implemented in the FPGA logic using Designer and Libero SoC software tool support.

Two channels of the 32-channel ADCMUX are dedicated. Channel 0 is connected internally to VCC and can be used to monitor core power supply. Channel 31 is connected to an internal temperature diode which can be used to monitor device temperature. The 30 remaining channels can be connected to external analog signals. The exact number of I/Os available for external connection signals is device-dependent (refer to the "Fusion Family" table on page I for details).

With Fusion, Microsemi also introduces the Analog Quad I/O structure (Figure 1-1). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three prescaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each prescaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. For more information, refer to the "Analog System Characteristics" section on page 2-117. Built-in operational amplifiers amplify small voltage signals for accurate current measurement. One analog input in each quad can be connected to an external temperature monitor diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADCMUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.



Figure 1-1 • Analog Quad

Embedded Memories

Flash Memory Blocks

The flash memory available in each Fusion device is composed of one to four flash blocks, each 2 Mbits in density. Each block operates independently with a dedicated flash controller and interface. Fusion flash memory blocks combine fast access times (60 ns random access and 10 ns access in Read-Ahead mode) with a configurable 8-, 16-, or 32-bit datapath, enabling high-speed flash operation without wait states. The memory block is organized in pages and sectors. Each page has 128 bytes, with 33 pages comprising one sector and 64 sectors per block. The flash block can support multiple partitions. The only constraint on size is that partition boundaries must coincide with page boundaries. The flexibility and granularity enable many use models and allow added granularity in programming updates.

Fusion devices support two methods of external access to the flash memory blocks. The first method is a serial interface that features a built-in JTAG-compliant port, which allows in-system programmability during user or monitor/test modes. This serial interface supports programming of an AES-encrypted stream. Data protected with security measures can be passed through the JTAG interface, decrypted, and then programmed in the flash block. The second method is a soft parallel interface.

FPGA logic or an on-chip soft microprocessor can access flash memory through the parallel interface. Since the flash parallel interface is implemented in the FPGA fabric, it can potentially be customized to meet special user requirements. For more information, refer to the [CoreCFI Handbook](#). The flash memory parallel interface provides configurable byte-wide ($\times 8$), word-wide ($\times 16$), or dual-word-wide ($\times 32$) data-port options. Through the programmable flash parallel interface, the on-chip and off-chip memories can be cascaded for wider or deeper configurations.

The flash memory has built-in security. The user can configure either the entire flash block or the small blocks to protect against unintentional or intrusive attempts to change or destroy the storage contents. Each on-chip flash memory block has a dedicated controller, enabling each block to operate independently.

The flash block logic consists of the following sub-blocks:

- Flash block – Contains all stored data. The flash block contains 64 sectors and each sector contains 33 pages of data.
- Page Buffer – Contains the contents of the current page being modified. A page contains 8 blocks of data.
- Block Buffer – Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic – The flash memory stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

User Nonvolatile FlashROM

In addition to the flash blocks, Fusion devices have 1 Kbit of user-accessible, nonvolatile FlashROM on-chip. The FlashROM is organized as 8×128 -bit pages. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for communications algorithms protected by security
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IEEE 1532 JTAG programming interface. Pages can be individually programmed (erased and written). On-chip AES decryption can be used selectively over public networks to load data such as security keys stored in the FlashROM for a user design.

The FlashROM can be programmed (erased and written) via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing.

The FlashPoint tool in the Fusion development software solutions, Libero SoC and Designer, has extensive support for flash memory blocks and FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be written through a 4-bit port and read as a single bitstream. The SRAM blocks can be initialized from the flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The SRAM/FIFO blocks can be cascaded to create larger configurations.

Clock Resources

PLLs and Clock Conditioning Circuits (CCCs)

Fusion devices provide designers with very flexible clock conditioning capabilities. Each member of the Fusion family contains six CCCs. In the two larger family members, two of these CCCs also include a PLL; the smaller devices support one PLL.

The inputs of the CCC blocks are accessible from the FPGA core or from one of several inputs with dedicated CCC block connections.

The CCC block has the following key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock phase adjustment via programmable and fixed delays from –6.275 ns to +8.75 ns
- Clock skew minimization (PLL)
- Clock frequency synthesis (PLL)
- On-chip analog clocking resources usable as inputs:
 - 100 MHz on-chip RC oscillator
 - Crystal oscillator

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°
- Output duty cycle = 50% ± 1.5%
- Low output jitter. Samples of peak-to-peak period jitter when a single global network is used:
 - 70 ps at 350 MHz
 - 90 ps at 100 MHz
 - 180 ps at 24 MHz
 - Worst case < 2.5% × clock period
- Maximum acquisition time = 150 μs
- Low power consumption of 5 mW

Global Clocking

Fusion devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there are on-chip oscillators as well as a comprehensive global clock distribution network.

The integrated RC oscillator generates a 100 MHz clock. It is used internally to provide a known clock source to the flash memory read and write control. It can also be used as a source for the PLLs.

The crystal oscillator supports the following operating modes:

- Crystal (32.768 KHz to 20 MHz)
- Ceramic (500 KHz to 8 MHz)
- RC (32.768 KHz to 4 MHz)

Each VersaTile input and output port has access to nine VersaNets: six main and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via MUXes. The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Digital I/Os with Advanced I/O Standards

The Fusion family of FPGAs features a flexible digital I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Fusion FPGAs support many different digital I/O standards, both single-ended and differential.

The I/Os are organized into banks, with four or five banks per device. The configuration of these banks determines the I/O standards supported. The banks along the east and west sides of the device support the full range of I/O standards (single-ended and differential). The south bank supports the Analog Quads (analog I/O). In the family's two smaller devices, the north bank supports multiple single-ended digital I/O standards. In the family's larger devices, the north bank is divided into two banks of digital Pro I/Os, supporting a wide variety of single-ended, differential, and voltage-referenced I/O standards.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following applications:

- Single-Data-Rate (SDR) applications
- Double-Data-Rate (DDR) applications—DDR LVDS I/O for chip-to-chip communications
- Fusion banks support LVPECL, LVDS, BLVDS, and M-LVDS with 20 multi-drop points.

VersaTiles

The Fusion core consists of VersaTiles, which are also used in the successful ProASIC3 family. The Fusion VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set and optional enable

Refer to [Figure 1-2](#) for the VersaTile configuration arrangement.



Figure 1-2 • VersaTile Configurations

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

The I/Os are controlled by the JTAG Boundary Scan register during programming, except for the analog pins (AC, AT and AV). The Boundary Scan register of the AG pin can be used to enable/disable the gate driver in Libero SoC.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click **PDB Configuration**. A FlashPoint – Programming File Generator window appears.
3. Click the **Specify I/O States During Programming** button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-3).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
 - 1 – I/O is set to drive out logic High
 - 0 – I/O is set to drive out logic Low
 - Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming
 - Z -Tri-State: I/O is tristated



Figure 1-3 • I/O States During Programming Window

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

Related Documents

Datasheet

Core8051

www.microsemi.com/soc/ipdocs/Core8051_DS.pdf

Application Notes

Fusion FlashROM

http://www.microsemi.com/soc/documents/Fusion_FROM_AN.pdf

Fusion SRAM/FIFO Blocks

http://www.microsemi.com/soc/documents/Fusion_RAM_FIFO_AN.pdf

Using DDR in Fusion Devices

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129938

Fusion Security

http://www.microsemi.com/soc/documents/Fusion_Security_AN.pdf

Using Fusion RAM as Multipliers

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129940

Handbook

Cortex-M1 Handbook

www.microsemi.com/soc/documents/CortexM1_HB.pdf

User Guides

Designer User Guide

http://www.microsemi.com/soc/documents/designer_UG.pdf

Fusion FPGA Fabric User Guide

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130817

IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide

http://www.microsemi.com/soc/documents/pa3_libguide_ug.pdf

SmartGen, FlashROM, Flash Memory System Builder, and Analog System Builder User Guide

http://www.microsemi.com/soc/documents/genguide_ug.pdf

White Papers

Fusion Technology

http://www.microsemi.com/soc/documents/Fusion_Tech_WP.pdf

2 – Device Architecture

Fusion Stack Architecture

To manage the unprecedented level of integration in Fusion devices, Microsemi developed the Fusion technology stack (Figure 2-1). This layered model offers a flexible design environment, enabling design at very high and very low levels of abstraction. Fusion peripherals include hard analog IP and hard and soft digital IP. Peripherals communicate across the FPGA fabric via a layer of soft gates—the Fusion backbone. Much more than a common bus interface, this Fusion backbone integrates a micro-sequencer within the FPGA fabric and configures the individual peripherals and supports low-level processing of peripheral data. Fusion applets are application building blocks that can control and respond to peripherals and other system signals. Applets can be rapidly combined to create large applications. The technology is scalable across devices, families, design types, and user expertise, and supports a well-defined interface for external IP and tool integration.

At the lowest level, Level 0, are Fusion peripherals. These are configurable functional blocks that can be hardwired structures such as a PLL or analog input channel, or soft (FPGA gate) blocks such as a UART or two-wire serial interface. The Fusion peripherals are configurable and support a standard interface to facilitate communication and implementation.

Connecting and controlling access to the peripherals is the Fusion backbone, Level 1. The backbone is a soft-gate structure, scalable to any number of peripherals. The backbone is a bus and much more; it manages peripheral configuration to ensure proper operation. Leveraging the common peripheral interface and a low-level state machine, the backbone efficiently offloads peripheral management from the system design. The backbone can set and clear flags based upon peripheral behavior and can define performance criteria. The flexibility of the stack enables a designer to configure the silicon, directly bypassing the backbone if that level of control is desired.

One step up from the backbone is the Fusion applet, Level 2. The applet is an application building block that implements a specific function in FPGA gates. It can react to stimuli and board-level events coming through the backbone or from other sources, and responds to these stimuli by accessing and manipulating peripherals via the backbone or initiating some other action. An applet controls or responds to the peripheral(s). Applets can be easily imported or exported from the design environment. The applet structure is open and well-defined, enabling users to import applets from Microsemi, system developers, third parties, and user groups.



Note: Levels 1, 2, and 3 are implemented in FPGA logic gates.

Figure 2-1 • Fusion Architecture Stack

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Core Architecture

VersaTile

Based upon successful ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

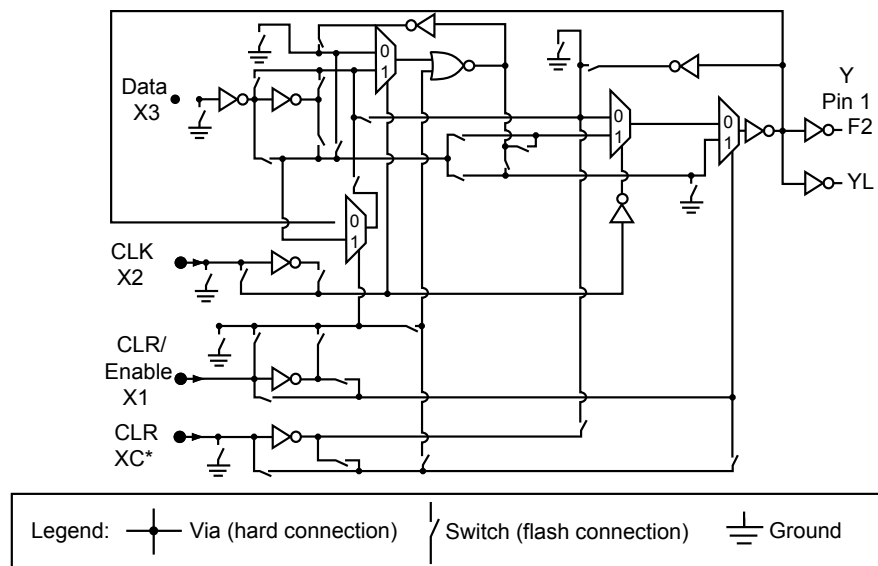
As illustrated in [Figure 2-2](#), there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the Versatile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources ([Figure 2-2](#)).



Note: *This input can only be connected to the global clock distribution network.

Figure 2-2 • Fusion Core VersaTile

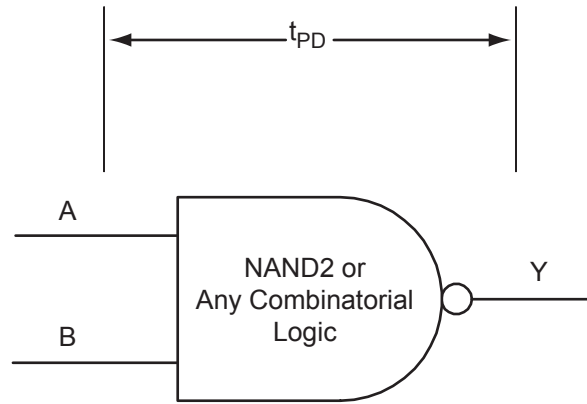
VersaTile Characteristics

Sample VersaTile Specifications—Combinatorial Module

The Fusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library (Figure 2-3). For more details, refer to the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide*.



Figure 2-3 • Sample of Combinatorial Cells



$$t_{PD} = \text{MAX}(t_{PD(RR)}, t_{PD(RF)}, t_{PD(FF)}, t_{PD(FR)})$$

where edges are applicable for the particular combinatorial cell

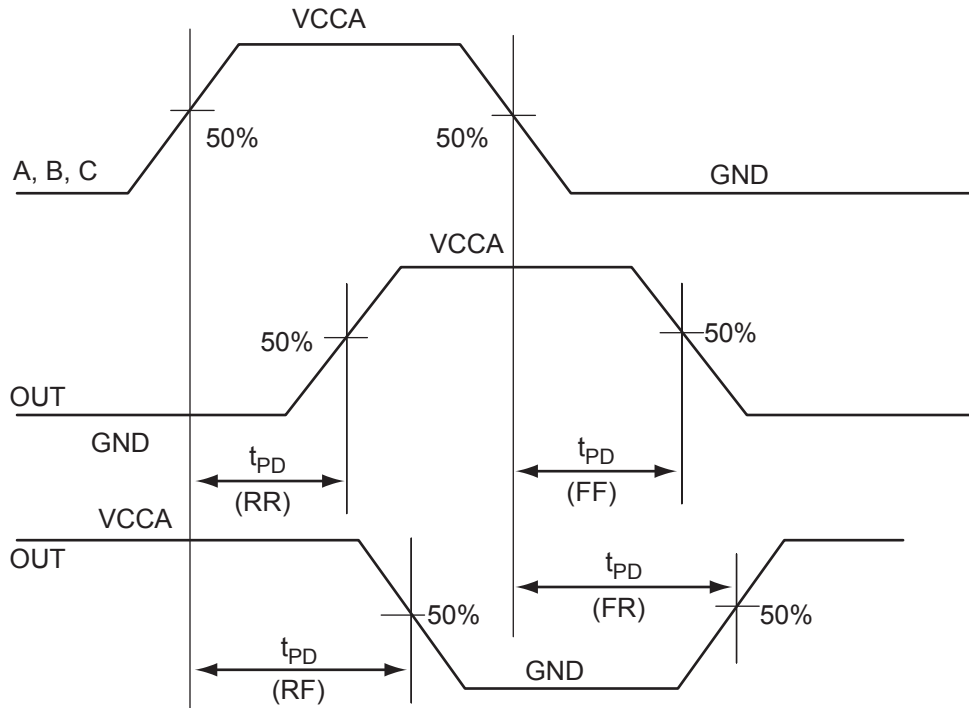


Figure 2-4 • Combinatorial Timing Model and Waveforms

Timing Characteristics

Table 2-1 • Combinatorial Cell Propagation Delays
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Combinatorial Cell | Equation | Parameter | -2 | -1 | Std. | Units |
|--------------------|-----------------------------------|-----------|------|------|------|-------|
| INV | $Y = !A$ | t_{PD} | 0.40 | 0.46 | 0.54 | ns |
| AND2 | $Y = A \cdot B$ | t_{PD} | 0.47 | 0.54 | 0.63 | ns |
| NAND2 | $Y = !(A \cdot B)$ | t_{PD} | 0.47 | 0.54 | 0.63 | ns |
| OR2 | $Y = A + B$ | t_{PD} | 0.49 | 0.55 | 0.65 | ns |
| NOR2 | $Y = !(A + B)$ | t_{PD} | 0.49 | 0.55 | 0.65 | ns |
| XOR2 | $Y = A \oplus B$ | t_{PD} | 0.74 | 0.84 | 0.99 | ns |
| MAJ3 | $Y = \text{MAJ}(A, B, C)$ | t_{PD} | 0.70 | 0.79 | 0.93 | ns |
| XOR3 | $Y = A \oplus B \oplus C$ | t_{PD} | 0.87 | 1.00 | 1.17 | ns |
| MUX2 | $Y = A \text{ IS } + B \text{ S}$ | t_{PD} | 0.51 | 0.58 | 0.68 | ns |
| AND3 | $Y = A \cdot B \cdot C$ | t_{PD} | 0.56 | 0.64 | 0.75 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

Sample VersaTile Specifications—Sequential Module

The Fusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library ([Figure 2-5](#)). For more details, refer to the *IGLOO*, *ProASIC3*, *SmartFusion* and *Fusion Macro Library Guide*.

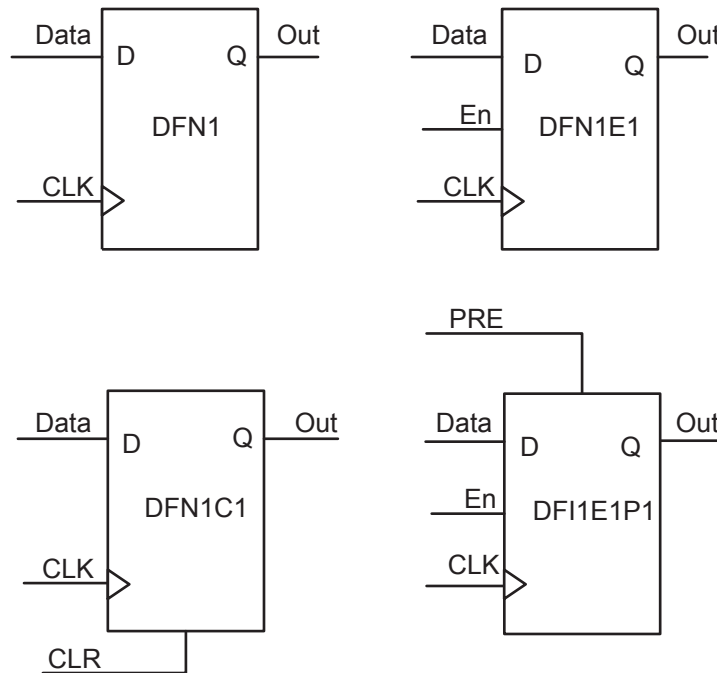
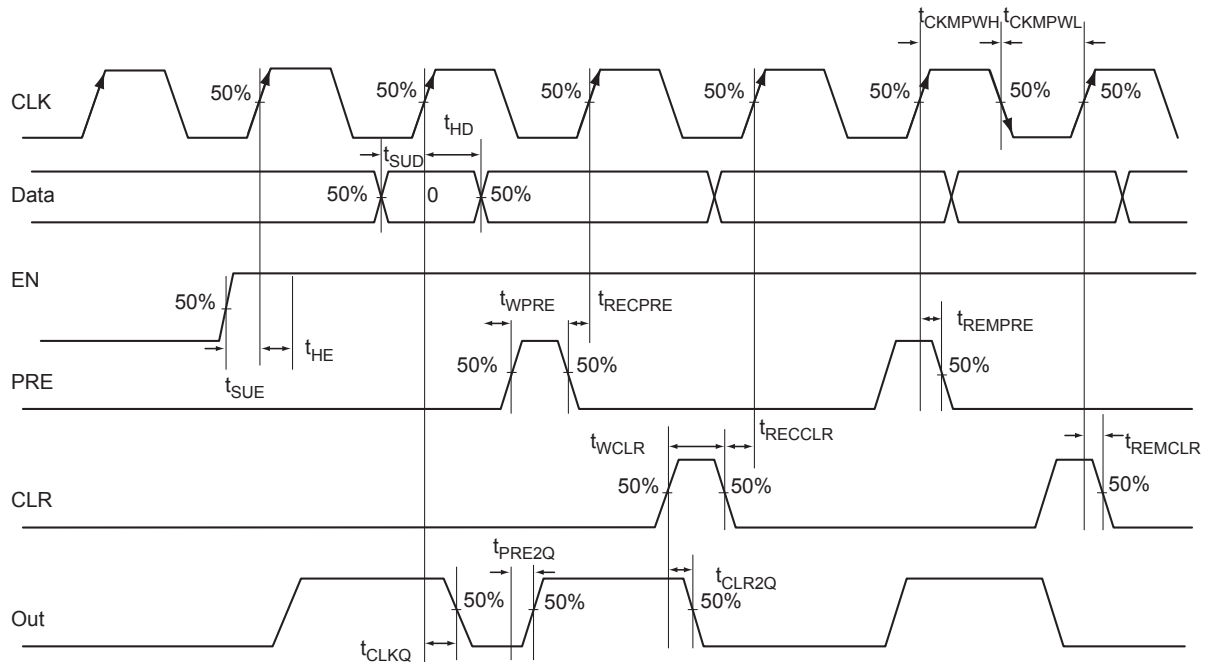


Figure 2-5 • Sample of Sequential Cells


Figure 2-6 • Sequential Timing Model and Waveforms

Sequential Timing Characteristics

Table 2-2 • Register Delays

 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|--------------|---|------|------|------|-------|
| t_{CLKQ} | Clock-to-Q of the Core Register | 0.55 | 0.63 | 0.74 | ns |
| t_{SUD} | Data Setup Time for the Core Register | 0.43 | 0.49 | 0.57 | ns |
| t_{HD} | Data Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{SUE} | Enable Setup Time for the Core Register | 0.45 | 0.52 | 0.61 | ns |
| t_{HE} | Enable Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{CLR2Q} | Asynchronous Clear-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| t_{PRE2Q} | Asynchronous Preset-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| t_{REMCLR} | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{RECCLR} | Asynchronous Clear Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{REMPRE} | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{RECPRE} | Asynchronous Preset Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{WCLR} | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{WPRE} | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{CKMPWH} | Clock Minimum Pulse Width High for the Core Register | 0.32 | 0.37 | 0.43 | ns |
| t_{CKMPWL} | Clock Minimum Pulse Width Low for the Core Register | 0.36 | 0.41 | 0.48 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Array Coordinates

During many place-and-route operations in the Microsemi Designer software tool, it is possible to set constraints that require array coordinates. Table 2-3 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wild card, and can contain core cells, memories, and I/Os.

Table 2-3 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-3. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-7 illustrates the array coordinates of an AFS600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for Fusion software tools.

Table 2-3 • Array Coordinates

| Device | VersaTiles | | | | Memory Rows | | All | |
|---------|------------|---|------|-----|-------------|----------|--------|------------|
| | Min. | | Max. | | Bottom | Top | Min. | Max. |
| | x | y | x | y | (x, y) | (x, y) | (x, y) | (x, y) |
| AFS090 | 3 | 2 | 98 | 25 | None | (3, 26) | (0, 0) | (101, 29) |
| AFS250 | 3 | 2 | 130 | 49 | None | (3, 50) | (0, 0) | (133, 53) |
| AFS600 | 3 | 4 | 194 | 75 | (3, 2) | (3, 76) | (0, 0) | (197, 79) |
| AFS1500 | 3 | 4 | 322 | 123 | (3, 2) | (3, 124) | (0, 0) | (325, 129) |



Note: The vertical I/O tile coordinates are not shown. West side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.

Figure 2-7 • Array Coordinates for AFS600

Routing Architecture

The routing structure of Fusion devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources; efficient long-line resources; high-speed very-long-line resources; and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-8). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaNet global network.

The efficient long-line resources provide routing for longer distances and higher-fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire Fusion device (Figure 2-9 on page 2-9). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit loading effects.

The high-speed very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length ± 12 VersaTiles in the vertical direction and length ± 16 in the horizontal direction from a given core VersaTile (Figure 2-10 on page 2-10). Very long lines in Fusion devices, like those in ProASIC3 devices, have been enhanced. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 2-11 on page 2-11). These nets are typically used to distribute clocks, reset signals, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all VersaTiles.



Note: Input to the core cell for the D-flip-flop set and reset is only available via the VersaNet global network connection.

Figure 2-8 • Ultra-Fast Local Lines Connected to the Eight Nearest Neighbors



Figure 2-9 • Efficient Long-Line Resources



Figure 2-10 • Very-Long-Line Resources

Global Resources (VersaNets)

Fusion devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has six CCCs. The west CCC also contains a PLL core. In the two larger devices (AFS600 and AFS1500), the west and the east CCCs each contain a PLL. The PLLs include delay lines, a phase shifter (0°, 90°, 180°, 270°), and clock multipliers/dividers. Each CCC has all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six lines total). The CCCs at the four corners each have access to three quadrant global lines on each quadrant of the chip.

Advantages of the VersaNet Approach

One of the architectural benefits of Fusion is the set of powerful and low-delay VersaNet global networks. Fusion offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 2-11). In addition, Fusion devices have three regional globals (quadrant globals) in each of the four chip quadrants. Each core VersaTile has access to nine global network resources: three quadrant and six chip (main) global networks. There are a total of 18 global networks on the device. Each of these networks contains spines and ribs that reach all VersaTiles in all quadrants (Figure 2-12 on page 2-12). This flexible VersaNet global network architecture allows users to map up to 180 different internal/external clocks in a Fusion device. Details on the VersaNet networks are given in Table 2-4 on page 2-12. The flexibility of the Fusion VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.

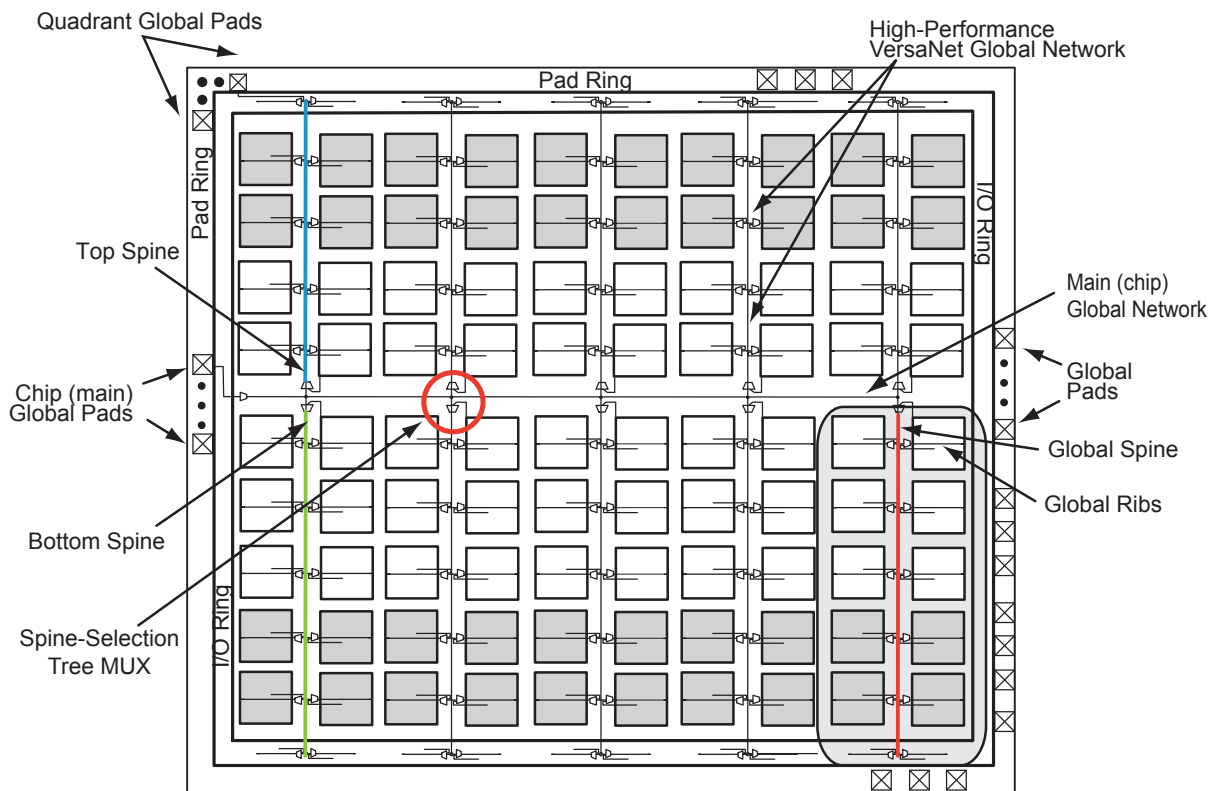


Figure 2-11 • Overview of Fusion VersaNet Global Network



Figure 2-12 • Global Network Architecture

Table 2-4 • Globals/Spines/Rows by Device

| | AFS090 | AFS250 | AFS600 | AFS1500 |
|--|---------------|---------------|---------------|----------------|
| Global VersaNets (trees)* | 9 | 9 | 9 | 9 |
| VersaNet Spines/Tree | 4 | 8 | 12 | 20 |
| Total Spines | 36 | 72 | 108 | 180 |
| VersaTiles in Each Top or Bottom Spine | 384 | 768 | 1,152 | 1,920 |
| Total VersaTiles | 2,304 | 6,144 | 13,824 | 38,400 |

Note: *There are six chip (main) globals and three globals per quadrant.

VersaNet Global Networks and Spine Access

The Fusion architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM, and I/O tiles on the Fusion device. There are 6 chip (main) global networks that access the entire device and 12 quadrant networks (3 in each quadrant). Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 180 internal/external clocks (in an AFS1500 device) or other high-fanout nets in Fusion devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on Fusion devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 2-12 on page 2-12).

The spines are the vertical branches of the global network tree, shown in Figure 2-11 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the Fusion device (the “scope” of the spine; see Figure 2-11 on page 2-11). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or another net defined by the user (Figure 2-13). Quadrant spines can be driven from user I/Os on the north and south sides of the die, via analog I/Os configured as direct digital inputs. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-13. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device. For details on using spines in Fusion devices, see the application note [Using Global Resources in Actel Fusion Devices](#).



Figure 2-13 • Spine-Selection MUX of Global Tree

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As [Figure 2-14](#) indicates, this access system is contiguous.

There is no break in the middle of the chip for north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib. Refer to the [Using Global Resources in Actel Fusion Devices](#) application note.



Figure 2-14 • Clock Aggregation Tree Architecture

Global Resource Characteristics

AFS600 VersaNet Topology

Clock delays are device-specific. Figure 2-15 is an example of a global tree used for clock routing. The global tree presented in Figure 2-15 is driven by a CCC located on the west side of the AFS600 device. It is used to drive all D-flip-flops in the device.



Figure 2-15 • Example of Global Tree Use in an AFS600 Device for Clock Routing

VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. [Table 2-5](#), [Table 2-6](#), [Table 2-7](#), and [Table 2-8](#) on [page 2-17](#) present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading, respectively.

Timing Characteristics

Table 2-5 • AFS1500 Global Resource Timing
 Commercial Temperature Range Conditions: $T_j = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|----------------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 1.53 | 1.75 | 1.74 | 1.99 | 2.05 | 2.34 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 1.53 | 1.79 | 1.75 | 2.04 | 2.05 | 2.40 | ns |
| t_{RCKMPWH} | Minimum Pulse Width High for Global Clock | | | | | | | ns |
| t_{RCKMPWL} | Minimum Pulse Width Low for Global Clock | | | | | | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | ns |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Table 2-6 • AFS600 Global Resource Timing
 Commercial Temperature Range Conditions: $T_j = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|----------------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 1.27 | 1.49 | 1.44 | 1.70 | 1.69 | 2.00 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 1.26 | 1.54 | 1.44 | 1.75 | 1.69 | 2.06 | ns |
| t_{RCKMPWH} | Minimum Pulse Width High for Global Clock | | | | | | | ns |
| t_{RCKMPWL} | Minimum Pulse Width Low for Global Clock | | | | | | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.27 | | 0.31 | | 0.36 | ns |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Table 2-7 • AFS250 Global Resource Timing
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 0.89 | 1.12 | 1.02 | 1.27 | 1.20 | 1.50 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 0.88 | 1.14 | 1.00 | 1.30 | 1.17 | 1.53 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | | | | | | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.26 | | 0.30 | | 0.35 | ns |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Table 2-8 • AFS090 Global Resource Timing
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|---------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 0.84 | 1.07 | 0.96 | 1.21 | 1.13 | 1.43 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 0.83 | 1.10 | 0.95 | 1.25 | 1.12 | 1.47 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | | | | | | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.27 | | 0.30 | | 0.36 | ns |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Clocking Resources

The Fusion family has a robust collection of clocking peripherals, as shown in the block diagram in [Figure 2-16](#). These on-chip resources enable the creation, manipulation, and distribution of many clock signals. The Fusion integrated RC oscillator produces a 100 MHz clock source with no external components. For systems requiring more precise clock signals, the Fusion family supports an on-chip crystal oscillator circuit. The integrated PLLs in each Fusion device can use the RC oscillator, crystal oscillator, or another on-chip clock signal as a source. These PLLs offer a variety of capabilities to modify the clock source (multiply, divide, synchronize, advance, or delay). Utilizing the CCC found in the popular ProASIC3 family, Fusion incorporates six CCC blocks. The CCCs allow access to Fusion global and local clock distribution nets, as described in the ["Global Resources \(VersaNets\)"](#) section on page 2-11.



Figure 2-16 • Fusion Clocking Options

RC Oscillator

The RC oscillator is an on-chip free-running clock source generating a 100 MHz clock. It can be used as a source clock for both on-chip and off-chip resources. When used in conjunction with the Fusion PLL and CCC circuits, the RC oscillator clock source can be used to generate clocks of varying frequency and phase.

The Fusion RC oscillator is very accurate at $\pm 1\%$ over commercial temperature ranges and $\pm 3\%$ over industrial temperature ranges. It is an automated clock, requiring no setup or configuration by the user. It requires only that the power and GNDOSC pins be connected; no external components are required. The RC oscillator can be used to drive either a PLL or another internal signal.

RC Oscillator Characteristics

Table 2-9 • Electrical Characteristics of RC Oscillator

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units | |
|--------------------|---------------------|---|------|------|------|-------|----|
| F _{RC} | Operating Frequency | | | 100 | | MHz | |
| | Accuracy | Temperature: 0°C to 85°C Voltage: 3.3 V \pm 5% | | 1 | | % | |
| | | Temperature: -40°C to 125°C Voltage: 3.3 V \pm 5% | | 3 | | % | |
| | Output Jitter | Period Jitter (at 5 k cycles) | | | 100 | | ps |
| | | Cycle–Cycle Jitter (at 5 k cycles) | | | 100 | | ps |
| | | Period Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply | | | 150 | | ps |
| | | Cycle–Cycle Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply | | | 150 | | ps |
| Output Duty Cycle | | | | 50 | | % | |
| I _{DYNRC} | Operating Current | | | 1 | | mA | |

Crystal Oscillator

The Crystal Oscillator (XTLOSC) is source that generates the clock from an external crystal. The output of XTLOSC CLKOUT signal can be selected as an input to the PLL. Refer to the "Clock Conditioning Circuits" section for more details. The XTLOSC can operate in normal operations and Standby mode (RTC is running and 1.5 V is not present).

In normal operation, the internal FPGA_EN signal is '1' as long as 1.5 V is present for VCC. As such, the internal enable signal, XTL_EN, for Crystal Oscillator is enabled since FPGA_EN is asserted. The XTL_MODE has the option of using MODE or RTC_MODE, depending on SELMODE.

During Standby, 1.5 V is not available, as such, and FPGA_EN is '0'. SELMODE must be asserted in order for XTL_EN to be enabled; hence XTL_MODE relies on RTC_MODE. SELMODE and RTC_MODE must be connected to RTCXTLSEL and RTCXTLMODE from the AB respectively for correct operation during Standby (refer to the "Real-Time Counter System" section on page 2-31 for a detailed description).

The Crystal Oscillator can be configured in one of four modes:

- RC network, 32 KHz to 4 MHz
- Low gain, 32 to 200 KHz
- Medium gain, 0.20 to 2.0 MHz
- High gain, 2.0 to 20.0 MHz

In RC network mode, the XTAL1 pin is connected to an RC circuit, as shown in Figure 2-16 on page 2-18. The XTAL2 pin should be left floating. The RC value can be chosen based on Figure 2-18 for any desired frequency between 32 KHz and 4 MHz. The RC network mode can also accommodate an external clock source on XTAL1 instead of an RC circuit.

In Low gain, Medium gain, and High gain, an external crystal component or ceramic resonator can be added onto XTAL1 and XTAL2, as shown in Figure 2-16 on page 2-18. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.



Note: *Internal signal—does not exist in macro.

Figure 2-17 • XTLOSC Macro



Figure 2-18 • Crystal Oscillator: RC Time Constant Values vs. Frequency (typical)

Table 2-10 • XTLOSC Signals Descriptions

| Signal Name | Width | Direction | Function | | |
|---------------|-------|-----------|---|---|-----------------|
| XTL_EN* | 1 | | Enables the crystal. Active high. | | |
| XTL_MODE* | 2 | | Settings for the crystal clock for different frequency. | | |
| | | | Value | Modes | Frequency Range |
| | | | b'00 | RC network | 32 KHz to 4 MHz |
| | | | b'01 | Low gain | 32 to 200 KHz |
| | | | b'10 | Medium gain | 0.20 to 2.0 MHz |
| | | | b'11 | High gain | 2.0 to 20.0 MHz |
| SELMODE | 1 | IN | Selects the source of XTL_MODE and also enables the XTL_EN. Connect from RTCXTLSEL from AB. | | |
| | | | 0 | For normal operation or sleep mode, XTL_EN depends on FPGA_EN, XTL_MODE depends on MODE | |
| | | | 1 | For Standby mode, XTL_EN is enabled, XTL_MODE depends on RTC_MODE | |
| RTC_MODE[1:0] | 2 | IN | Settings for the crystal clock for different frequency ranges. XTL_MODE uses RTC_MODE when SELMODE is '1'. | | |
| MODE[1:0] | 2 | IN | Settings for the crystal clock for different frequency ranges. XTL_MODE uses MODE when SELMODE is '0'. In Standby, MODE inputs will be 0's. | | |
| FPGA_EN* | 1 | IN | 0 when 1.5 V is not present for VCC 1 when 1.5 V is present for VCC | | |
| XTL | 1 | IN | Crystal Clock source | | |
| CLKOUT | 1 | OUT | Crystal Clock output | | |

Note: *Internal signal—does not exist in macro.

Clock Conditioning Circuits

In Fusion devices, the CCCs are used to implement frequency division, frequency multiplication, phase shifting, and delay operations.

The CCCs are available in six chip locations—each of the four chip corners and the middle of the east and west chip sides.

Each CCC can implement up to three independent global buffers (with or without programmable delay), or a PLL function (programmable frequency division/multiplication, phase shift, and delays) with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, and CLKC-GLC) of a given CCC.

A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and, optionally, the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global output cannot be reused if the YB (or YC) output is used (Figure 2-19). Refer to the "PLL Macro" section on page 2-27 for more information.

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core

The CCC block is fully configurable, either via flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous interface is dynamically accessible from inside the Fusion device to permit changes of parameters (such as divide ratios) during device operation. To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation. This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to the "UJTAG Applications in Micro-semi's Low-Power Flash Devices" chapter of the *Fusion FPGA Fabric User Guide* and the "CCC and PLL Characteristics" section on page 2-28 for more information.



Notes:

1. Visit the [Microsemi SoC Products Group website](#) for application notes concerning dynamic PLL reconfiguration. Refer to the "PLL Macro" section on page 2-27 for signal descriptions.
2. Many specific INBUF macros support the wide variety of single-ended and differential I/O standards for the Fusion family.
3. Refer to the [IGLOO](#), [ProASIC3](#), [SmartFusion](#) and [Fusion Macro Library Guide](#) for more information.

Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro

Table 2-11 • Available Selections of I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros

| CLKBUF Macros |
|------------------------------|
| CLKBUF_LVCMOS5 |
| CLKBUF_LVCMOS33 ¹ |
| CLKBUF_LVCMOS18 |
| CLKBUF_LVCMOS15 |
| CLKBUF_PCI |
| CLKBUF_LVDS ² |
| CLKBUF_LVPECL |

Notes:

1. This is the default macro. For more details, refer to the [IGLOO](#), [ProASIC3](#), [SmartFusion](#) and [Fusion Macro Library Guide](#).
2. The B-LVDS and M-LVDS standards are supported with CLKBUF_LVDS.

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS macros are composite macros that include an I/O macro driving a global buffer, hardwired together (Figure 2-20).

The CLKINT macro provides a global buffer function driven by the FPGA core.

The CLKBUF, CLKBUF_LVPECL/LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by Fusion devices. The available CLKBUF macros are described in the *IGLOO*, *ProASIC3*, *SmartFusion* and *Fusion Macro Library Guide*.



Figure 2-20 • Global Buffers with No Programmable Delay

Global Buffers with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay (Figure 2-21 on page 2-25). The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the Fusion family. The available INBUF macros are described in the *IGLOO*, *ProASIC3*, *SmartFusion* and *Fusion Macro Library Guide*.

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero SoC and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.



Figure 2-21 • Fusion CCC Options: Global Buffers with Programmable Delay

Global Input Selections

Each global buffer, as well as the PLL reference clock, can be driven from one of the following (Figure 2-22):

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core



GAA[0:2]: GA represents global in the northwest corner of the device. A[0:2]: designates specific A clock source.

Notes:

1. Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the "User I/O Naming Convention" section on page 2-158 for more information.
2. Instantiate the routed clock source input as follows:
 - a) Connect the output of a logic element to the clock input of the PLL, CLKDLY, or CLKINT macro.
 - b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS) in a relevant global pin location.
3. LVDS-based clock sources are available in the east and west banks on all Fusion devices.

Figure 2-22 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT

CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

Figure 2-23 • PLL Block

PLL Macro

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLK_A input of the CCC block, which is only accessible from the global A[2:0] package pins. Refer to [Figure 2-22 on page 2-25](#) for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL feedback loop can be driven either internally or externally. The PLL macro also provides power-down input and lock output signals. During power-up, POWERDOWN should be asserted Low until VCC is up. See [Figure 2-19 on page 2-23](#) for more information.

Inputs:

- CLK_A: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is power-down on (active low).

Outputs:

- LOCK (active high): indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. [Figure 2-23 on page 2-26](#) illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global networks, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate it from the hardwired I/O connection described earlier.

The visual PLL configuration in SmartGen, available with the Libero SoC and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLK_A) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select where the input clock is coming from. SmartGen automatically instantiates the special macro, PLLINT, when needed.

CCC and PLL Characteristics

Timing Characteristics

Table 2-12 • Fusion CCC/PLL Specification

| Parameter | Min. | Typ. | Max. | Unit |
|--|--------------------------------|------------------|------------------------|---------|
| Clock Conditioning Circuitry Input Frequency f_{IN_CCC} | 1.5 | | 350 | MHz |
| Clock Conditioning Circuitry Output Frequency f_{OUT_CCC} | 0.75 | | 350 | MHz |
| Delay Increments in Programmable Delay Blocks ^{1, 2} | | 160 ³ | | ps |
| Number of Programmable Values in Each Programmable Delay Block | | | 32 | |
| Input Period Jitter | | | 1.5 | ns |
| CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} | Max Peak-to-Peak Period Jitter | | | |
| | 1 Global Network Used | | 3 Global Networks Used | |
| 0.75 MHz to 24 MHz | 1.00% | | 1.00% | |
| 24 MHz to 100 MHz | 1.50% | | 1.50% | |
| 100 MHz to 250 MHz | 2.25% | | 2.25% | |
| 250 MHz to 350 MHz | 3.50% | | 3.50% | |
| Acquisition Time | LockControl = 0 | | 300 | μ s |
| | LockControl = 1 | | 6.0 | ms |
| Tracking Jitter ⁴ | LockControl = 0 | | 1.6 | ns |
| | LockControl = 1 | | 0.8 | ns |
| Output Duty Cycle | 48.5 | | 51.5 | % |
| Delay Range in Block: Programmable Delay 1 ^{1, 2} | 0.6 | | 5.56 | ns |
| Delay Range in Block: Programmable Delay 2 ^{1, 2} | 0.025 | | 5.56 | ns |
| Delay Range in Block: Fixed Delay ^{1, 2} | | 2.2 | | ns |

Notes:

1. This delay is a function of voltage and temperature. See [Table 3-7 on page 3-9](#) for deratings.
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the *Libero SoC Online Help* associated with the core for more information.
4. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.

No-Glitch MUX (NGMUX)

Positioned downstream from the PLL/CCC blocks, the NGMUX provides a special switching sequence between two asynchronous clock domains that prevents generating any unwanted narrow clock pulses. The NGMUX is used to switch the source of a global between three different clock sources. Allowable inputs are either two PLL/CCC outputs or a PLL/CCC output and a regular net, as shown in Figure 2-24. The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC). These are set by SmartGen during design but can also be changed by dynamically reconfiguring the PLL. The GLMUXSEL[1:0] bits control which clock source is passed through the NGMUX to the global network (GL). See Table 2-13.



Figure 2-24 • NGMUX

Table 2-13 • NGMUX Configuration and Selection Table

| GLMUXCFG[1:0] | GLMUXSEL[1:0] | | Selected Input Signal | MUX Type |
|---------------|---------------|---|-----------------------|--------------|
| 00 | X | 0 | GLA | 2-to-1 GLMUX |
| | X | 1 | GLC | |
| 01 | X | 0 | GLA | 2-to-1 GLMUX |
| | X | 1 | GLINT | |

The NGMUX macro is simplified to show the two clock options that have been selected by the GLMUXCFG[1:0] bits. Figure 2-25 illustrates the NGMUX macro. During design, the two clock sources are connected to CLK0 and CLK1 and are controlled by GLMUXSEL[1:0] to determine which signal is to be passed through the MUX.



Figure 2-25 • NGMUX Macro

The sequence of switching between two clock sources (from CLK0 to CLK1) is as follows (Figure 2-26):

- GLMUXSEL[1:0] transitions to initiate a switch.
- GL drives one last complete CLK0 positive pulse (i.e., one rising edge followed by one falling edge).
- From that point, GL stays Low until the second rising edge of CLK1 occurs.
- At the second CLK1 rising edge, GL will begin to continuously deliver the CLK1 signal.
- Minimum $t_{sw} = 0.05$ ns at 25°C (typical conditions)

For examples of NGMUX operation, refer to the *Fusion FPGA Fabric User Guide*.



Figure 2-26 • NGMUX Waveform

Real-Time Counter System

The RTC system enables Fusion devices to support standby and sleep modes of operation to reduce power consumption in many applications.

- Sleep mode, typical 10 μ A
- Standby mode (RTC running), typical 3 mA with 20 MHz

The RTC system is composed of five cores:

- RTC sub-block inside Analog Block (AB)
- Voltage Regulator and Power System Monitor (VRPSM)
- Crystal oscillator (XTLOSC); refer to the “Crystal Oscillator” section in the Fusion Clock Resources chapter of the *Fusion FPGA Fabric User Guide* for more detail.
- Crystal clock; does not require instantiation in RTL
- 1.5 V voltage regulator; does not require instantiation in RTL

All cores are powered by 3.3 V supplies, so the RTC system is operational without a 1.5 V supply during standby mode. [Figure 2-27](#) shows their connection.



Notes:

1. Signals are hardwired internally and do not exist in the macro core.
2. User is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off.

Figure 2-27 • Real-Time Counter System (not all the signals are shown for the AB macro)

Modes of Operation

Standby Mode

Standby mode allows periodic power-up and power-down of the FPGA fabric. In standby mode, the real-time counter and crystal block are ON. The FPGA is not powered by disabling the 1.5 V voltage regulator. The 1.5 V voltage regulator can be enabled when the preset count is matched. Refer to the "Real-Time Counter (part of AB macro)" section for details. To enter standby mode, the RTC must be first configured and enabled. Then VRPSM is shut off by deasserting the VRPU signal. The 1.5 V voltage regulator is then disabled, and shuts off the 1.5 V output.

Sleep Mode

In sleep mode, the real-time counter and crystal blocks are OFF. The 1.5 V voltage regulator inside the VRPSM can only be enabled by the PUB or TRST pin. Refer to the "Voltage Regulator and Power System Monitor (VRPSM)" section on page 2-36 for details on power-up and power-down of the 1.5 V voltage regulator.

Standby and Sleep Mode Circuit Implementation

For extra power savings, VJTAG and VPUMP should be at the same voltage as VCC, floated or ground, during standby and sleep modes. Note that when VJTAG is not powered, the 1.5 V voltage regulator cannot be enabled through TRST.

VPUMP and VJTAG can be controlled through an external switch. Microsemi recommends ADG839, ADG849, or ADG841 as possible switches. Figure 2-28 shows the implementation for controlling VPUMP. The IN signal of the switch can be connected to PTBASE of the Fusion device. VJTAG can be controlled in same manner.



Figure 2-28 • Implementation to Control VPUMP

Real-Time Counter (part of AB macro)

The RTC is a 40-bit loadable counter and used as the primary timekeeping element (Figure 2-29). The clock source, RTCCLK, must come from the CLKOUT signal of the crystal oscillator. The RTC can be configured to reset itself when a count value reaches the match value set in the Match Register.

The RTC is part of the Analog Block (AB) macro. The RTC is configured by the analog configuration MUX (ACM). Each address contains one byte of data. The circuitry in the RTC is powered by VCC33A, so the RTC can be used in standby mode when the 1.5 V supply is not present.

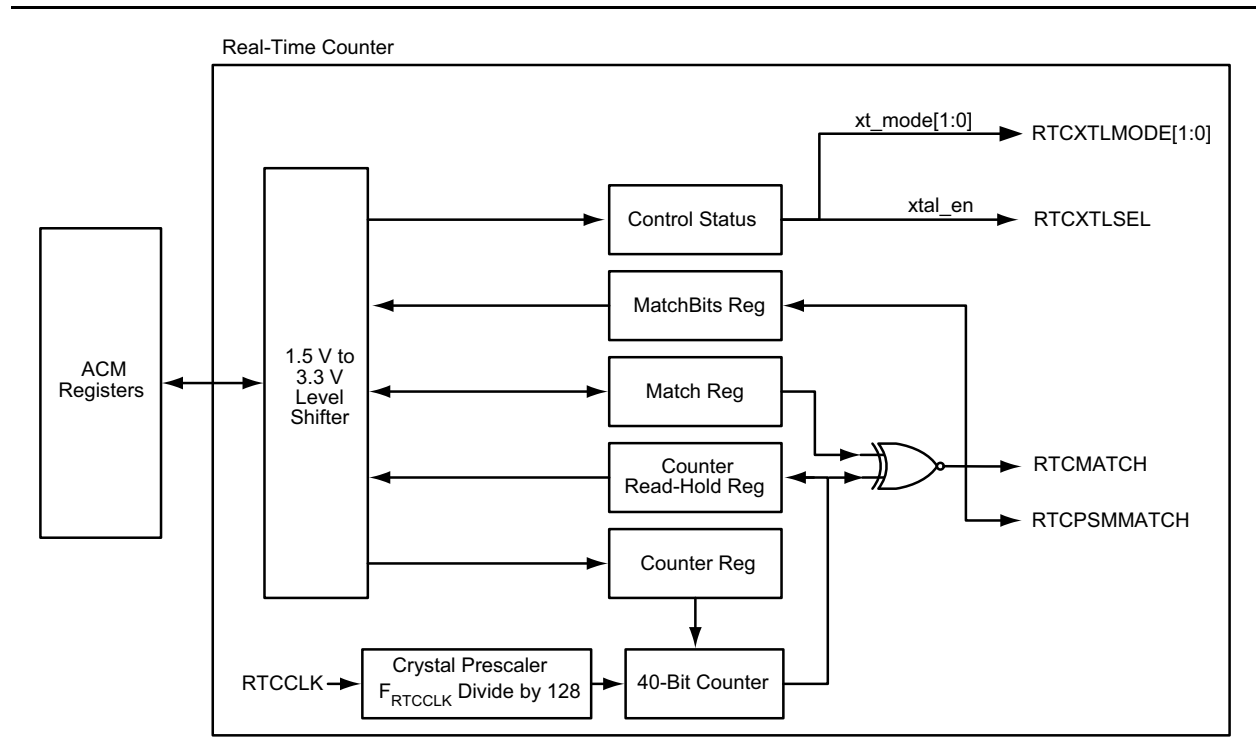


Figure 2-29 • RTC Block Diagram

Table 2-14 • RTC Signal Description

| Signal Name | Width | Direction | Function |
|-----------------|-------|-----------|---|
| RTCCLK | 1 | In | Must come from CLKOUT of XTLOSC. |
| RTCXTLMODE[1:0] | 2 | Out | Controlled by xt_mode in CTRL_STAT. Signal must connect to the RTC_MODE signal in XTLOSC, as shown in Figure 2-27. |
| RTCXTLSEL | 1 | Out | Controlled by xtal_en from CTRL_STAT register. Signal must connect to RTC_MODE signal in XTLOSC in Figure 2-27. |
| RTCMATCH | 1 | Out | Match signal for FPGA 0 – Counter value does not equal the Match Register value. 1 – Counter value equals the Match Register value. |
| RTCPSMMATCH | 1 | Out | Same signal as RTCMATCH. Signal must connect to RTCPSMMATCH in VRPSM, as shown in Figure 2-27. |

The 40-bit counter can be preloaded with an initial value as a starting point by the Counter Register. The count from the 40-bit counter can be read through the same set of address space. The count comes from a Read-Hold Register to avoid data changing during read. When the counter value equals the Match Register value, all Match Bits Register values will be 0xFFFFFFFF. The RTCMATCH and RTCPSMMATCH signals will assert. The 40-bit counter can be configured to automatically reset to 0x000000000 when the counter value equals the Match Register value. The automatic reset does not apply if the Match Register value is 0x000000000. The RTCCLK has a prescaler to divide the clock by 128 before it is used for the 40-bit counter. Below is an example of how to calculate the OFF time.

Example: Calculation for Match Count

To put the Fusion device on standby for one hour using an external crystal of 32.768 KHz:

The period of the crystal oscillator is T_{crystal} :

$$T_{\text{crystal}} = 1 / 32.768 \text{ KHz} = 30.518 \mu\text{s}$$

The period of the counter is T_{counter} :

$$T_{\text{counter}} = 30.518 \mu\text{s} \times 128 = 3.90625 \text{ ms}$$

The Match Count for 1 hour is Δtmatch :

$$\Delta\text{tmatch} / T_{\text{counter}} = (1 \text{ hr} \times 60 \text{ min/hr} \times 60 \text{ sec/min}) / 3.90625 \text{ ms} = 921600 \text{ or } 0xE1000$$

Using a 32.768 KHz crystal, the maximum standby time of the 40-bit counter is 4,294,967,296 seconds, which is 136 years.

Table 2-15 • Memory Map for RTC in ACM Register and Description

| ACMADDR | Register Name | Description | Use | Default Value |
|---------|---------------|---|--|---------------|
| 0x40 | COUNTER0 | Counter bits 7:0 | Used to preload the counter to a specified start point. | 0x00 |
| 0x41 | COUNTER1 | Counter bits 15:8 | | 0x00 |
| 0x42 | COUNTER2 | Counter bits 23:16 | | 0x00 |
| 0x43 | COUNTER3 | Counter bits 31:24 | | 0x00 |
| 0x44 | COUNTER4 | Counter bits 39:32 | | 0x00 |
| 0x48 | MATCHREG0 | Match register bits 7:0 | The RTC comparison bits | 0x00 |
| 0x49 | MATCHREG1 | Match register bits 15:8 | | 0x00 |
| 0x4A | MATCHREG2 | Match register bits 23:16 | | 0x00 |
| 0x4B | MATCHREG3 | Match register bits 31:24 | | 0x00 |
| 0x4C | MATCHREG4 | Match register bits 39:32 | | 0x00 |
| 0x50 | MATCHBIT0 | Individual match bits 7:0 | The output of the XNOR gates 0 – Not matched 1 – Matched | 0x00 |
| 0x51 | MATCHBIT1 | Individual match bits 15:8 | | 0x00 |
| 0x52 | MATCHBIT2 | Individual match bits 23:16 | | 0x00 |
| 0x53 | MATCHBIT3 | Individual match bits 31:24 | | 0x00 |
| 0x54 | MATCHBIT4 | Individual match bits 29:32 | | 0x00 |
| 0x58 | CTRL_STAT | Control (write/read) / Status (read only) register bits | Refer to Table 2-16 on page 2-35 for details. | 0x00 |

Table 2-16 • RTC Control/Status Register

| Bit | Name | Description | Default Value |
|-----|--------------|---|---------------|
| 7 | rtc_rst | RTC Reset 1 – Resets the RTC 0 – Deassert reset on after two ACM_CLK cycle. | |
| 6 | cntr_en | Counter Enable 1 – Enables the counter; rtc_rst must be deasserted as well. First counter increments after 64 RTCCLK positive edges. 0 – Disables the crystal prescaler but does not reset the counter value. Counter value can only be updated when the counter is disabled. | 0 |
| 5 | vr_en_mat | Voltage Regulator Enable on Match 1 – Enables RTCMATCH and RTCPSMMATCH to output 1 when the counter value equals the Match Register value. This enables the 1.5 V voltage regulator when RTCPSMMATCH connects to the RTCPSMMATCH signal in VRPSM. 0 – RTCMATCH and RTCPSMMATCH output 0 at all times. | 0 |
| 4:3 | xt_mode[1:0] | Crystal Mode Controls RTCXTLMODE[1:0]. Connects to RTC_MODE signal in XTLOSC. XTL_MODE uses this value when xtal_en is 1. See the " Crystal Oscillator " section on page 2-20 for mode configuration. | 00 |
| 2 | rst_cnt_omat | Reset Counter on Match 1 – Enables the sync clear of the counter when the counter value equals the Match Register value. The counter clears on the rising edge of the clock. If all the Match Registers are set to 0, the clear is disabled. 0 – Counter increments indefinitely | 0 |
| 1 | rstb_cnt | Counter Reset, active Low 0 - Resets the 40-bit counter value | 0 |
| 0 | xtal_en | Crystal Enable Controls RTCXTLSEL. Connects to SELMODE signal in XTLOSC. 0 – XTLOSC enables control by FPGA_EN; xt_mode is not used. Sleep mode requires this bit to equal 0. 1 – Enables XTLOSC, XTL_MODE control by xt_mode Standby mode requires this bit to be set to 1. See the " Crystal Oscillator " section on page 2-20 for further details on SELMODE configuration. | 0 |

Voltage Regulator and Power System Monitor (VRPSM)

The VRPSM macro controls the power-up state of the FPGA. The power-up bar (PUB) pin can turn on the voltage regulator when set to 0. TRST can enable the voltage regulator when deasserted, allowing the FPGA to power-up when user want access to JTAG ports. The inputs VRINITSTATE and RTCPSMMATCH come from the flash bits and RTC, and can also power up the FPGA.



Note: *Signals are hardwired internally and do not exist in the macro core.

Figure 2-30 • VRPSM Macro

Table 2-17 • VRPSM Signal Descriptions

| Signal Name | Width | Direction | Function |
|-------------|-------|-----------|--|
| VRPU | 1 | In | Voltage Regulator Power-Up 0 – Voltage regulator disabled. PUB must be floated or pulled up, and the TRST pin must be grounded to disable the voltage regulator. 1 – Voltage regulator enabled |
| VRINITSTATE | 1 | In | Voltage Regulator Initial State Defines the voltage Regulator status upon power-up of the 3.3 V. The signal is configured by Libero SoC when the VRPSM macro is generated. Tie off to 1 – Voltage regulator enables when 3.3 V is powered. Tie off to 0 – Voltage regulator disables when 3.3 V is powered. |
| RTCPSMMATCH | 1 | In | RTC Power System Management Match Connect from RTCPSMATCH signal from RTC in AB 0 transition to 1 turns on the voltage regulator |
| PUB | 1 | In | External pin, built-in weak pull-up Power-Up Bar 0 – Enables voltage regulator at all times |
| TRST* | 1 | In | External pin, JTAG Test Reset 1 – Enables voltage regulator at all times |
| FPGAGOOD | 1 | Out | Indicator that the FPGA is powered and functional No need to connect if it is not used. 1 – Indicates that the FPGA is powered up and functional. 0 – Not possible to read by FPGA since it has already powered off. |
| PUCORE | 1 | Out | Power-Up Core Inverted signal of PUB. No need to connect if it is not used. |
| VREN* | 1 | Out | Voltage Regulator Enable Connected to 1.5 V voltage regulator in Fusion device internally. 0 – Voltage regulator disables 1 – Voltage regulator enables |

Note: *Signals are hardwired internally and do not exist in the macro core.



Note: * To enter and exit standby mode without any external stimulus on PUB or TRST, the *vr_en_mat* in the CTRL_STAT register must also be set to 1, so that RTCPSMMATCH will assert when a match occurs; hence the device exits standby mode.

Figure 2-31 • State Diagram for All Different Power Modes

When TRST is 1 or PUB is 0, the 1.5 V voltage regulator is always ON, putting the Fusion device in normal operation at all times. Therefore, when the JTAG port is not in reset, the Fusion device cannot enter sleep mode or standby mode.

To enter standby mode, the Fusion device must first power-up into normal operation. The RTC is enabled through the RTC Control/Status Register described in the "Real-Time Counter (part of AB macro)" section on page 2-33. A match value corresponding to the wake-up time is loaded into the Match Register. The 1.5 V voltage regulator is disabled by setting VRPU to 0 to allow the Fusion device to enter standby mode, when the 1.5 V supply is off but the RTC remains on.

1.5 V Voltage Regulator

The 1.5 V voltage regulator uses an external pass transistor to generate 1.5 V from a 3.3 V supply. The base of the pass transistor is tied to PTBASE, the collector is tied to 3.3 V, and an emitter is tied to PTBASE and the 1.5 V supplies of the Fusion device. [Figure 2-27 on page 2-31](#) shows the hook-up of the 1.5 V voltage regulator to an external pass transistor.

Microsemi recommends using a PN2222A or 2N2222A transistor. The gain of such a transistor is approximately 25, with a maximum base current of 20 mA. The maximum current that can be supported is 0.5 A. Transistors with different gain can also be used for different current requirements.

Table 2-18 • Electrical Characteristics
VCC33A = 3.3 V

| Symbol | Parameter | Condition | | Min | Typical | Max | Units |
|---------|-------------------|-----------|---|-------|----------------|-------|----------------|
| VOUT | Output Voltage | Tj = 25°C | | 1.425 | 1.5 | 1.575 | V |
| ICC33A | Operation Current | Tj = 25°C | ILOAD = 1 mA ILOAD = 100 mA ILOAD = 0.5 A | | 11 11 30 | | mA mA mA |
| ΔVOUT | Load Regulation | Tj = 25°C | ILOAD = 1 mA to 0.5 A | | 90 | | mV |
| ΔVOUT | Line Regulation | Tj = 25°C | VCC33A = 2.97 V to 3.63 V ILOAD = 1 mA | | 10.6 | | mV/V |
| | | | VCC33A = 2.97 V to 3.63 V ILOAD = 100 mA | | 12.1 | | mV/V |
| | | | VCC33A = 2.97 V to 3.63 V ILOAD = 500 mA | | 10.6 | | mV/V |
| | Dropout Voltage* | Tj = 25°C | ILOAD = 1 mA | | 0.63 | | V |
| | | | ILOAD = 100 mA | | 0.84 | | V |
| | | | ILOAD = 0.5 A | | 1.35 | | V |
| IPTBASE | PTBase Current | Tj = 25°C | ILOAD = 1 mA | | 48 | | μA |
| | | | ILOAD = 100 mA | | 736 | | μA |
| | | | ILOAD = 0.5 A | | 12 | 20 | mA |

Note: *Data collected with 2N2222A.

Embedded Memories

Fusion devices include four types of embedded memory: flash block, FlashROM, SRAM, and FIFO.

Flash Memory Block

Fusion is the first FPGA that offers a flash memory block (FB). Each FB block stores 2 Mbits of data. The flash memory block macro is illustrated in [Figure 2-32](#). The port pin name and descriptions are detailed on [Table 2-19](#) on page 2-40. All flash memory block signals are active high, except for CLK and active low RESET. All flash memory operations are synchronous to the rising edge of CLK.



Figure 2-32 • Flash Memory Block

Flash Memory Block Pin Names

Table 2-19 • Flash Memory Block Pin Names

| Interface Name | Width | Direction | Description |
|------------------|-------|-----------|--|
| ADDR[17:0] | 18 | In | Byte offset into the FB. Byte-based address. |
| AUXBLOCK | 1 | In | When asserted, the page addressed is used to access the auxiliary block within that page. |
| BUSY | 1 | Out | When asserted, indicates that the FB is performing an operation. |
| CLK | 1 | In | User interface clock. All operations and status are synchronous to the rising edge of this clock. |
| DATAWIDTH[1:0] | 2 | In | Data width 00 = 1 byte in RD/WD[7:0] 01 = 2 bytes in RD/WD[15:0] 1x = 4 bytes in RD/WD[31:0] |
| DISCARDPAGE | 1 | In | When asserted, the contents of the Page Buffer are discarded so that a new page write can be started. |
| ERASEPAGE | 1 | In | When asserted, the address page is to be programmed with all zeros. ERASEPAGE must transition synchronously with the rising edge of CLK. |
| LOCKREQUEST | 1 | In | When asserted, indicates to the JTAG controller that the FPGA interface is accessing the FB. |
| OVERWRITEPAGE | 1 | In | When asserted, the page addressed is overwritten with the contents of the Page Buffer if the page is writable. |
| OVERWRITEPROTECT | 1 | In | When asserted, all program operations will set the overwrite protect bit of the page being programmed. |
| PAGESTATUS | 1 | In | When asserted with REN, initiates a read page status operation. |
| PAGELOSSPROTECT | 1 | In | When asserted, a modified Page Buffer must be programmed or discarded before accessing a new page. |
| PIPE | 1 | In | Adds a pipeline stage to the output for operation above 50 MHz. |
| PROGRAM | 1 | In | When asserted, writes the contents of the Page Buffer into the FB page addressed. |
| RD[31:0] | 32 | Out | Read data; data will be valid from the first non-busy cycle (BUSY = 0) after REN has been asserted. |
| READNEXT | 1 | In | When asserted with REN, initiates a read-next operation. |
| REN | 1 | In | When asserted, initiates a read operation. |
| RESET | 1 | In | When asserted, resets the state of the FB (active low). |
| SPAREPAGE | 1 | In | When asserted, the sector addressed is used to access the spare page within that sector. |

Table 2-19 • Flash Memory Block Pin Names (continued)

| Interface Name | Width | Direction | Description |
|----------------|-------|-----------|---|
| STATUS[1:0] | 2 | Out | Status of the last operation completed: 00: Successful completion 01: Read-/Unprotect-Page: single error detected and corrected Write: operation addressed a write-protected page Erase-Page: protection violation Program: Page Buffer is unmodified Protection violation 10: Read-/Unprotect-Page: two or more errors detected 11: Write: attempt to write to another page before programming current page Erase-Page/Program: page write count has exceeded the 10-year retention threshold |
| UNPROTECTPAGE | 1 | In | When asserted, the page addressed is copied into the Page Buffer and the Page Buffer is made writable. |
| WD[31:0] | 32 | In | Write data |
| WEN | 1 | In | When asserted, stores WD in the page buffer. |

All flash memory block input signals are active high, except for RESET.

Flash Memory Block Diagram

A simplified diagram of the flash memory block is shown in Figure 2-33.

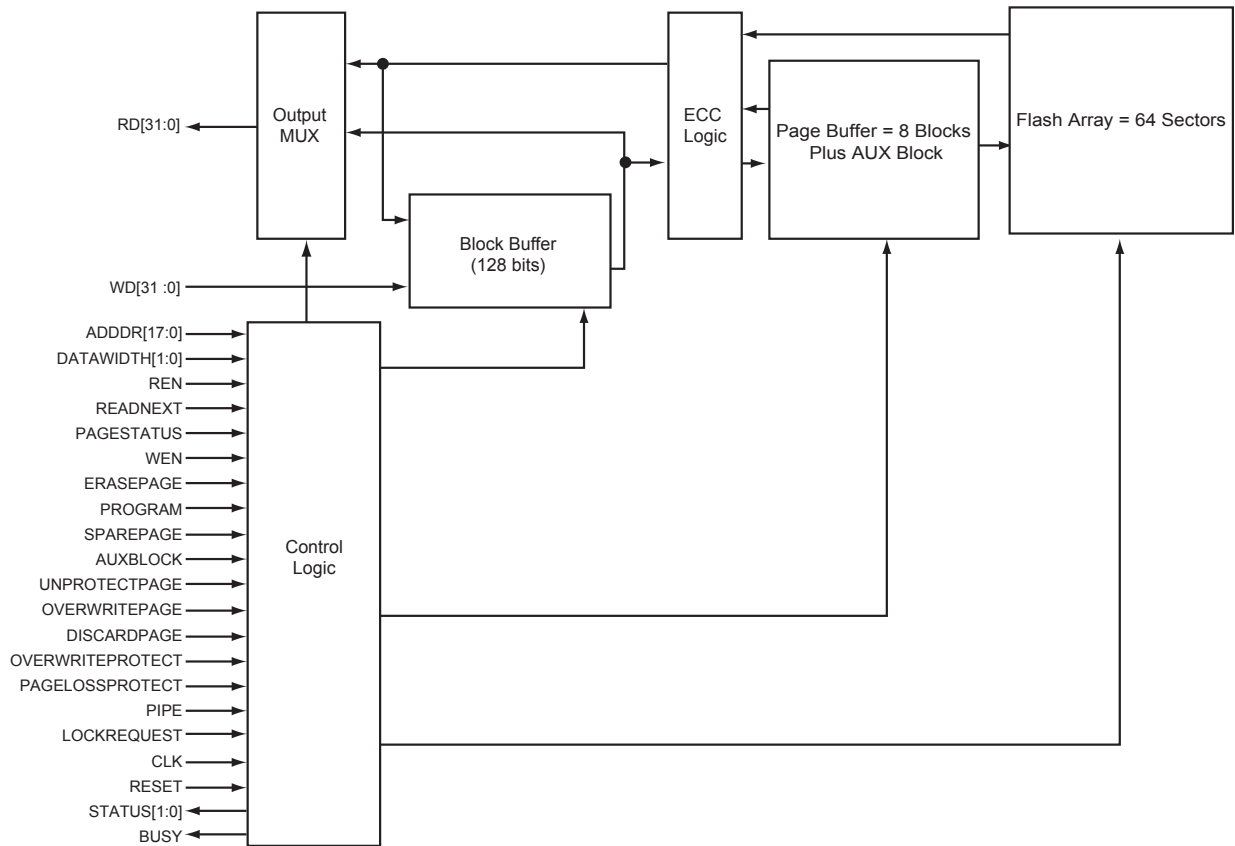


Figure 2-33 • Flash Memory Block Diagram

The logic consists of the following sub-blocks:

- Flash Array
Contains all stored data. The flash array contains 64 sectors, and each sector contains 33 pages of data.
- Page Buffer
A page-wide volatile register. A page contains 8 blocks of data and an AUX block.
- Block Buffer
Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic

The FB stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

Flash Memory Block Addressing

Figure 2-34 shows a graphical representation of the flash memory block.

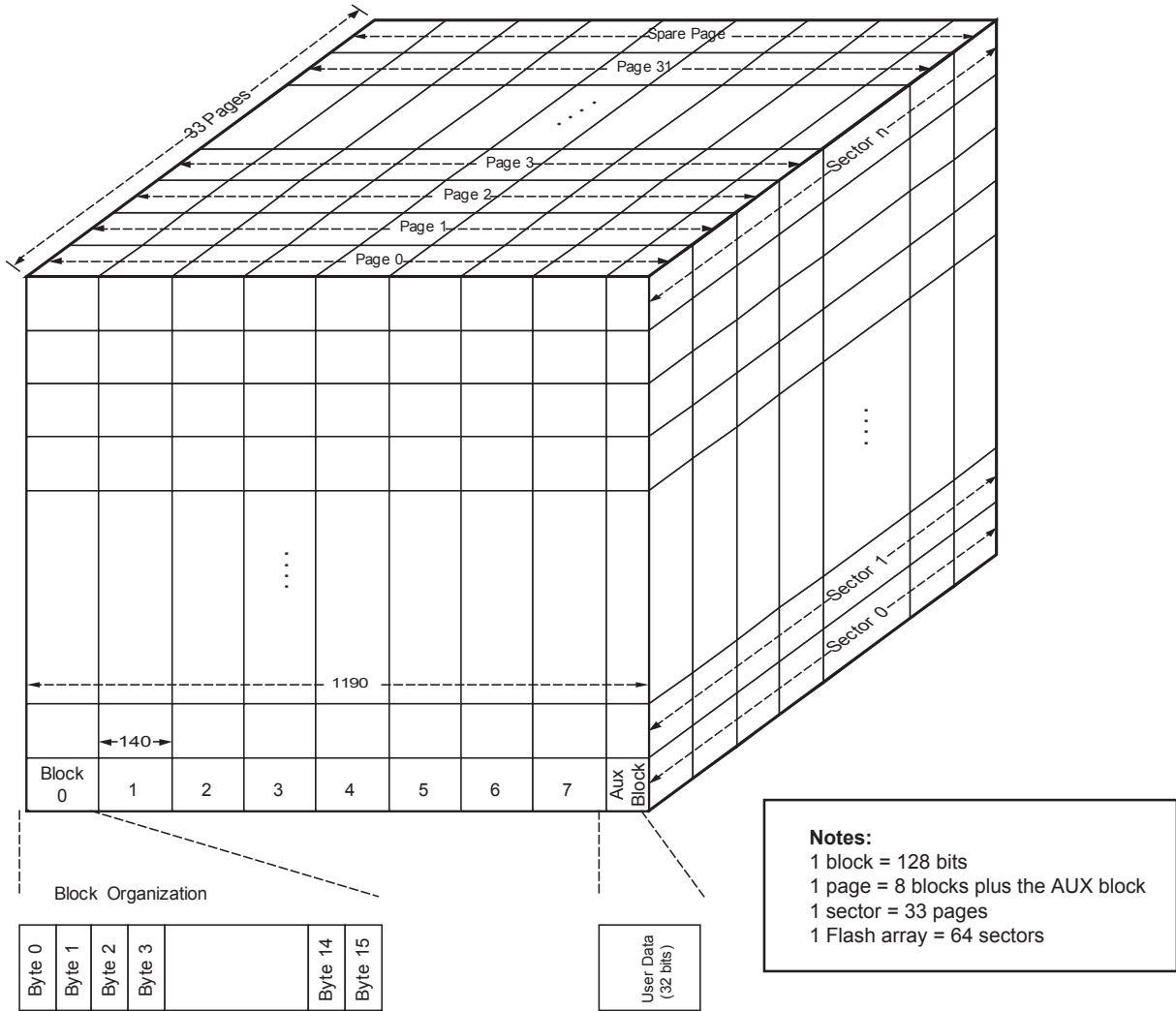


Figure 2-34 • Flash Memory Block Organization

Each FB is partitioned into sectors, pages, blocks, and bytes. There are 64 sectors in an FB, and each sector contains 32 pages and 1 spare page. Each page contains 8 data blocks and 1 auxiliary block. Each data block contains 16 bytes of user data, and the auxiliary block contains 4 bytes of user data. Addressing for the FB is shown in Table 2-20.

Table 2-20 • FB Address Bit Allocation ADDR[17:0]

| | | | | | | | |
|--------|----|------|---|-------|---|------|---|
| 17 | 12 | 11 | 7 | 6 | 4 | 3 | 0 |
| Sector | | Page | | Block | | Byte | |

When the spare page of a sector is addressed (SPAREPAGE active), ADDR[11:7] are ignored.

When the Auxiliary block is addressed (AUXBLOCK active), ADDR[6:2] are ignored.

Note: The spare page of sector 0 is unavailable for any user data. Writes to this page will return an error, and reads will return all zeroes.

Data operations are performed in widths of 1 to 4 bytes. A write to a location in a page that is not already in the Page Buffer will cause the page to be read from the FB Array and stored in the Page Buffer. The block that was addressed during the write will be put into the Block Buffer, and the data written by WD will overwrite the data in the Block Buffer. After the data is written to the Block Buffer, the Block Buffer is then written to the Page Buffer to keep both buffers in sync. Subsequent writes to the same block will overwrite the Block Buffer and the Page Buffer. A write to another block in the page will cause the addressed block to be loaded from the Page Buffer, and the write will be performed as described previously.

The data width can be selected dynamically via the DATAWIDTH input bus. The truth table for the data width settings is detailed in [Table 2-21](#). The minimum resolvable address is one 8-bit byte. For data widths greater than 8 bits, the corresponding address bits are ignored—when DATAWIDTH = 0 (2 bytes), ADDR[0] is ignored, and when DATAWIDTH = '10' or '11' (4 bytes), ADDR[1:0] are ignored. Data pins are LSB-oriented and unused WD data pins must be grounded.

Table 2-21 • Data Width Settings

| DATAWIDTH[1:0] | Data Width |
|----------------|----------------|
| 00 | 1 byte [7:0] |
| 01 | 2 byte [15:0] |
| 10, 11 | 4 bytes [31:0] |

Flash Memory Block Protection

Page Loss Protection

When the PAGELOSSPROTECT pin is set to logic 1, it prevents writes to any page other than the current page in the Page Buffer until the page is either discarded or programmed.

A write to another page while the current page is Page Loss Protected will return a STATUS of '11'.

Overwrite Protection

Any page that is Overwrite Protected will result in the STATUS being set to '01' when an attempt is made to either write, program, or erase it. To set the Overwrite Protection state for a page, set the OVERWRITEPROTECT pin when a Program operation is undertaken. To clear the Overwrite Protect state for a given page, an Unprotect Page operation must be performed on the page, and then the page must be programmed with the OVERWRITEPROTECT pin cleared to save the new page.

LOCKREQUEST

LOCKREQUEST indicates to the JTAG controller that the FPGA interface is accessing the Flash memory Block. For the JTAG master LOCKREQUEST check is optional and can be ignored.

Flash Memory Block Operations

FB Operation Priority

The FB provides for priority of operations when multiple actions are requested simultaneously. [Table 2-22](#) shows the priority order (priority 0 is the highest).

Table 2-22 • FB Operation Priority

| Operation | Priority |
|-----------------------|----------|
| System Initialization | 0 |
| FB Reset | 1 |
| Read | 2 |
| Write | 3 |
| Erase Page | 4 |
| Program | 5 |
| Unprotect Page | 6 |
| Discard Page | 7 |

Access to the FB is controlled by the BUSY signal. The BUSY output is synchronous to the CLK signal. FB operations are only accepted in cycles where BUSY is logic 0.

Write Operation

Write operations are initiated with the assertion of the WEN signal. Figure 2-35 on page 2-45 illustrates the multiple Write operations.

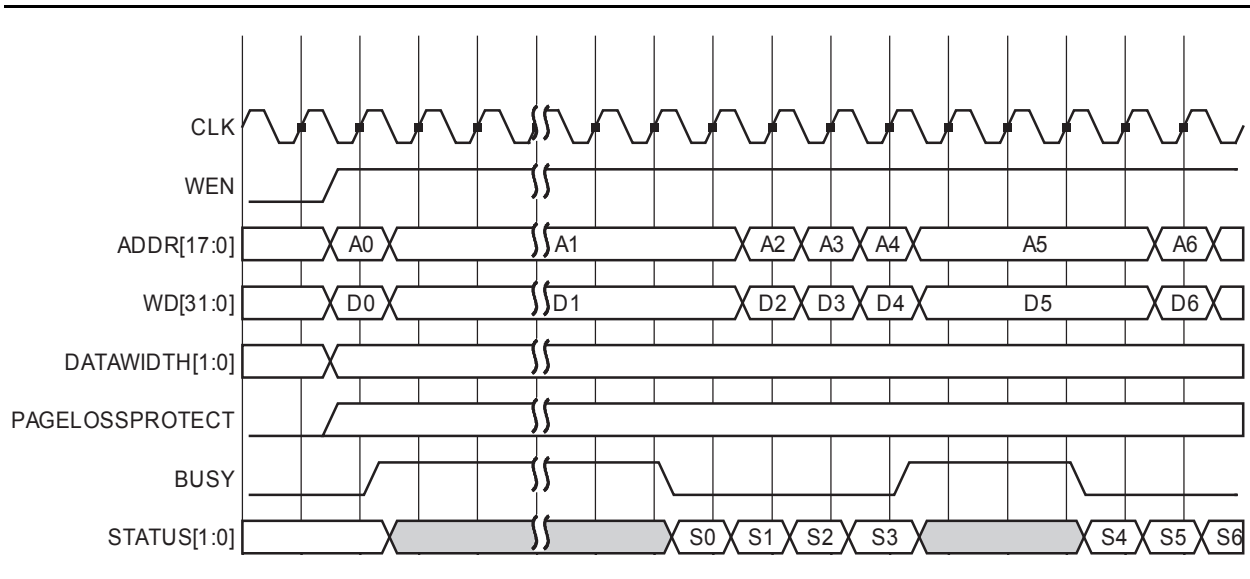


Figure 2-35 • FB Write Waveform

When a Write operation is initiated to a page that is currently not in the Page Buffer, the FB control logic will issue a BUSY signal to the user interface while the page is loaded from the FB Array into the Page Buffer. A Copy Page operation takes no less than 55 cycles and could take more if a Write or Unprotect Page operation is started while the NVM is busy pre-fetching a block. The basic operation is to read a block from the array into the block register (5 cycles) and then write the block register to the page buffer (1 cycle) and if necessary, when the copy is complete, reading the block being written from the page buffer into the block buffer (1 cycle). A page contains 9 blocks, so 9 blocks multiplied by 6 cycles to read/write each block, plus 1 is 55 cycles total. Subsequent writes to the same block of the page will incur no busy cycles. A write to another block in the page will assert BUSY for four cycles (five cycles when PIPE is asserted), to allow the data to be written to the Page Buffer and have the current block loaded into the Block Buffer.

Write operations are considered successful as long as the STATUS output is '00'. A non-zero STATUS indicates that an error was detected during the operation and the write was not performed. Note that the STATUS output is "sticky"; it is unchanged until another operation is started.

Only one word can be written at a time. Write word width is controlled by the DATAWIDTH bus. Users are responsible for keeping track of the contents of the Page Buffer and when to program it to the array. Just like a regular RAM, writing to random addresses is possible. Users can write into the Page Buffer in any order but will incur additional BUSY cycles. It is not necessary to modify the entire Page Buffer before saving it to nonvolatile memory.

Write errors include the following:

1. Attempting to write a page that is Overwrite Protected (STATUS = '01'). The write is not performed.
2. Attempting to write to a page that is not in the Page Buffer when Page Loss Protection is enabled (STATUS = '11'). The write is not performed.

Program Operation

A Program operation is initiated by asserting the PROGRAM signal on the interface. Program operations save the contents of the Page Buffer to the FB Array. Due to the technologies inherent in the FB, the total programming (including erase) time per page of the eNVM is 6.8 ms. While the FB is writing the data to the array, the BUSY signal will be asserted.

During a Program operation, the sector and page addresses on ADDR are compared with the stored address for the page (and sector) in the Page Buffer. If there is a mismatch between the two addresses, the Program operation will be aborted and an error will be reported on the STATUS output.

It is possible to write the Page Buffer to a different page in memory. When asserting the PROGRAM pin, if OVERWRITEPAGE is asserted as well, the FB will write the contents of the Page Buffer to the sector and page designated on the ADDR inputs if the destination page is not Overwrite Protected.

A Program operation can be utilized to either modify the contents of the page in the flash memory block or change the protections for the page. Setting the OVERWRITEPROTECT bit on the interface while asserting the PROGRAM pin will put the page addressed into Overwrite Protect Mode. Overwrite Protect Mode safeguards a page from being inadvertently overwritten during subsequent Program or Erase operations.

Program operations that result in a STATUS value of '01' do not modify the addressed page. For all other values of STATUS, the addressed page is modified. Program errors include the following:

1. Attempting to program a page that is Overwrite Protected (STATUS = '01')
2. Attempting to program a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection Mode (STATUS = '01')
3. Attempting to perform a program with OVERWRITEPAGE set when the page addressed has been Overwrite Protected (STATUS = '01')
4. The Write Count of the page programmed exceeding the Write Threshold defined in the part specification (STATUS = '11')
5. The ECC Logic determining that there is an uncorrectable error within the programmed page (STATUS = '10')
6. Attempting to program a page that is **not** in the Page Buffer when OVERWRITEPAGE is not set and the page in the Page Buffer is modified (STATUS = '01')
7. Attempting to program the page in the Page Buffer when the Page Buffer is **not** modified

The waveform for a Program operation is shown in [Figure 2-36](#).



Figure 2-36 • FB Program Waveform

Note: OVERWRITEPAGE is only sampled when the PROGRAM or ERASEPAGE pins are asserted. OVERWRITEPAGE is ignored in all other operations.

Erase Page Operation

The Erase Page operation is initiated when the ERASEPAGE pin is asserted. The Erase Page operation allows the user to erase (set user data to zero) any page within the FB.

The use of the OVERWRITEPAGE and PAGELOSSPROTECT pins is the same for erase as for a Program Page operation.

As with the Program Page operation, a STATUS of '01' indicates that the addressed page is not erased.

A waveform for an Erase Page operation is shown in Figure 2-37.

Erase errors include the following:

1. Attempting to erase a page that is Overwrite Protected (STATUS = '01')
2. Attempting to erase a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = '01')
3. The Write Count of the erased page exceeding the Write Threshold defined in the part specification (STATUS = '11')
4. The ECC Logic determining that there is an uncorrectable error within the erased page (STATUS = '10')

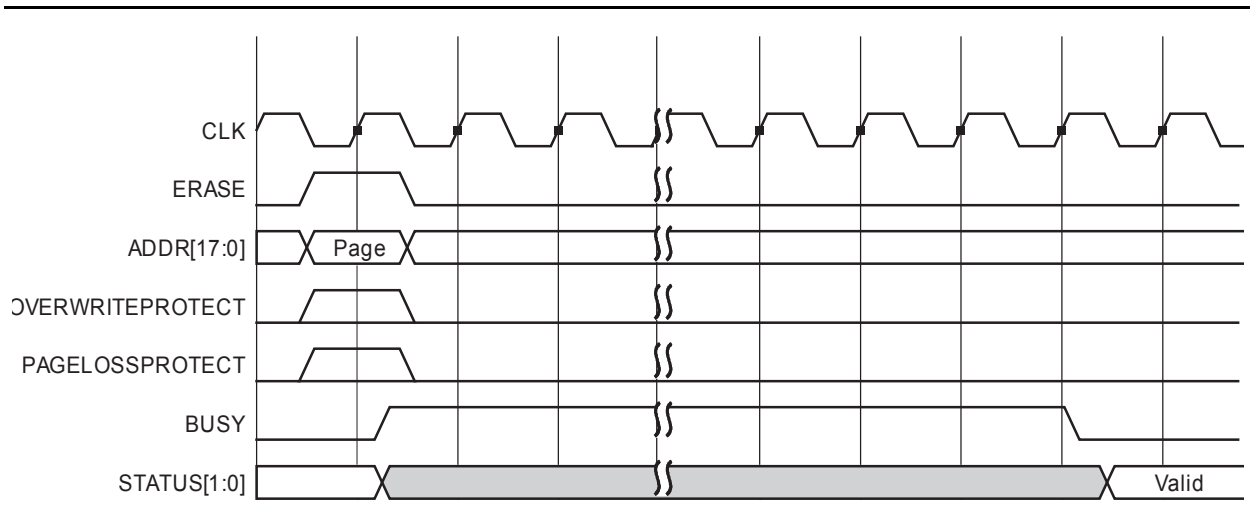


Figure 2-37 • FB Erase Page Waveform

Read Operation

Read operations are designed to read data from the FB Array, Page Buffer, Block Buffer, or status registers. Read operations support a normal read and a read-ahead mode (done by asserting READNEXT). Also, the timing for Read operations is dependent on the setting of PIPE.

The following diagrams illustrate representative timing for Non-Pipe Mode (Figure 2-38) and Pipe Mode (Figure 2-39) reads of the flash memory block interface.



Figure 2-38 • Read Waveform (Non-Pipe Mode, 32-bit access)



Figure 2-39 • Read Waveform (Pipe Mode, 32-bit access)

The following error indications are possible for Read operations:

1. STATUS = '01' when a single-bit data error was detected and corrected within the block addressed.
2. STATUS = '10' when a double-bit error was detected in the block addressed (note that the error is uncorrected).

In addition to data reads, users can read the status of any page in the FB by asserting PAGESTATUS along with REN. The format of the data returned by a page status read is shown in [Table 2-23](#), and the definition of the page status bits is shown in [Table 2-24](#).

Table 2-23 • Page Status Read Data Format

| | | | | | | | |
|-------------|---|----------|---|----------------|----------------|-----------------|---------------------|
| 31 | 8 | 7 | 4 | 3 | 2 | 1 | 0 |
| Write Count | | Reserved | | Over Threshold | Read Protected | Write Protected | Overwrite Protected |

Table 2-24 • Page Status Bit Definition

| Page Status Bit(s) | Definition |
|--------------------|---|
| 31–8 | The number of times the page addressed has been programmed/erased |
| 7–4 | Reserved; read as 0 |
| 3 | Over Threshold indicator (see the "Program Operation" section on page 2-46) |
| 2 | Read Protected; read protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value. |
| 1 | Write Protected; write protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value. |
| 0 | Overwrite Protected; designates that the user has set the OVERWRITEPROTECT bit on the interface while doing a Program operation. The page cannot be written without first performing an Unprotect Page operation. |

Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential Read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in [Figure 2-40](#) and [Figure 2-41](#).



Figure 2-40 • Read Next Waveform (Non-Pipe Mode, 32-bit access)



Figure 2-41 • Read Next WaveForm (Pipe Mode, 32-bit access)

Unprotect Page Operation

An Unprotect Page operation will clear the protection for a page addressed on the ADDR input. It is initiated by setting the UNPROTECTPAGE signal on the interface along with the page address on ADDR.

If the page is not in the Page Buffer, the Unprotect Page operation will copy the page into the Page Buffer. The Copy Page operation occurs only if the current page in the Page Buffer is not Page Loss Protected.

The waveform for an Unprotect Page operation is shown in Figure 2-42.



Figure 2-42 • FB Unprotected Page Waveform

The Unprotect Page operation can incur the following error conditions:

1. If the copy of the page to the Page Buffer determines that the page has a single-bit correctable error in the data, it will report a STATUS = '01'.
2. If the address on ADDR does not match the address of the Page Buffer, PAGELOSSPROTECT is asserted, and the Page Buffer has been modified, then STATUS = '11' and the addressed page is not loaded into the Page Buffer.
3. If the copy of the page to the Page Buffer determines that at least one block in the page has a double-bit uncorrectable error, STATUS = '10' and the Page Buffer will contain the corrupted data.

Discard Page Operation

If the contents of the modified Page Buffer have to be discarded, the DISCARDPAGE signal should be asserted. This command results in the Page Buffer being marked as unmodified.

The timing for the operation is shown in Figure 2-43. The BUSY signal will remain asserted until the operation has completed.



Figure 2-43 • FB Discard Page Waveform

Flash Memory Block Characteristics

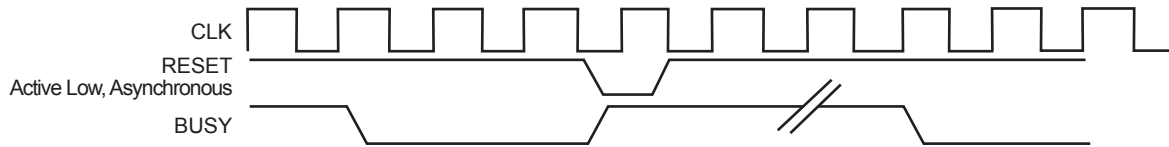


Figure 2-44 • Reset Timing Diagram

Table 2-25 • Flash Memory Block Timing
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------------------|--|-------|-------|-------|-------|
| t_{CLK2RD} | Clock-to-Q in 5-cycle read mode of the Read Data | 7.99 | 9.10 | 10.70 | ns |
| | Clock-to-Q in 6-cycle read mode of the Read Data | 5.03 | 5.73 | 6.74 | ns |
| t_{CLK2BUSY} | Clock-to-Q in 5-cycle read mode of BUSY | 4.95 | 5.63 | 6.62 | ns |
| | Clock-to-Q in 6-cycle read mode of BUSY | 4.45 | 5.07 | 5.96 | ns |
| $t_{\text{CLK2STATUS}}$ | Clock-to-Status in 5-cycle read mode | 11.24 | 12.81 | 15.06 | ns |
| | Clock-to-Status in 6-cycle read mode | 4.48 | 5.10 | 6.00 | ns |
| t_{DSUNVM} | Data Input Setup time for the Control Logic | 1.92 | 2.19 | 2.57 | ns |
| t_{DHNVM} | Data Input Hold time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| t_{ASUNVM} | Address Input Setup time for the Control Logic | 2.76 | 3.14 | 3.69 | ns |
| t_{AHNVM} | Address Input Hold time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| t_{SUDWNVM} | Data Width Setup time for the Control Logic | 1.85 | 2.11 | 2.48 | ns |
| t_{HDDWNVM} | Data Width Hold time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| t_{SURENVM} | Read Enable Setup time for the Control Logic | 3.85 | 4.39 | 5.16 | ns |
| t_{HDRENVM} | Read Enable Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| t_{SUWENVM} | Write Enable Setup time for the Control Logic | 2.37 | 2.69 | 3.17 | ns |
| t_{HDWENVM} | Write Enable Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{SUPROGNVM}}$ | Program Setup time for the Control Logic | 2.16 | 2.46 | 2.89 | ns |
| $t_{\text{HDPROGNVM}}$ | Program Hold time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{SUSPAREPAGE}}$ | SparePage Setup time for the Control Logic | 3.74 | 4.26 | 5.01 | ns |
| $t_{\text{HDSPAREPAGE}}$ | SparePage Hold time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| t_{SUAUXBLK} | Auxiliary Block Setup Time for the Control Logic | 3.74 | 4.26 | 5.00 | ns |
| t_{HDAUXBLK} | Auxiliary Block Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| t_{SURDNEXT} | ReadNext Setup Time for the Control Logic | 2.17 | 2.47 | 2.90 | ns |
| t_{HDRDNEXT} | ReadNext Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{SUERASEPG}}$ | Erase Page Setup Time for the Control Logic | 3.76 | 4.28 | 5.03 | ns |
| $t_{\text{HDERASEPG}}$ | Erase Page Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{SUUNPROTECTPG}}$ | Unprotect Page Setup Time for the Control Logic | 2.01 | 2.29 | 2.69 | ns |
| $t_{\text{HDUNPROTECTPG}}$ | Unprotect Page Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{SUDISCARDPG}}$ | Discard Page Setup Time for the Control Logic | 1.88 | 2.14 | 2.52 | ns |
| $t_{\text{HDDISCARDPG}}$ | Discard Page Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{SUOVERWRPRO}}$ | Overwrite Protect Setup Time for the Control Logic | 1.64 | 1.86 | 2.19 | ns |
| $t_{\text{HDOVERWRPRO}}$ | Overwrite Protect Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |

Table 2-25 • Flash Memory Block Timing (continued)
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------------------|--|--------|-------|-------|-------|
| $t_{\text{SUPGLOSSPRO}}$ | Page Loss Protect Setup Time for the Control Logic | 1.69 | 1.93 | 2.27 | ns |
| $t_{\text{HDPGLOSSPRO}}$ | Page Loss Protect Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| t_{SUPGSTAT} | Page Status Setup Time for the Control Logic | 2.49 | 2.83 | 3.33 | ns |
| t_{HDPGSTAT} | Page Status Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{SUOVERWRPG}}$ | Over Write Page Setup Time for the Control Logic | 1.88 | 2.14 | 2.52 | ns |
| $t_{\text{HDOVERWRPG}}$ | Over Write Page Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{SULOCKREQUEST}}$ | Lock Request Setup Time for the Control Logic | 0.87 | 0.99 | 1.16 | ns |
| $t_{\text{HDLOCKREQUEST}}$ | Lock Request Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| t_{REARNVM} | Reset Recovery Time | 0.94 | 1.07 | 1.25 | ns |
| t_{REARNVM} | Reset Removal Time | 0.00 | 0.00 | 0.00 | ns |
| t_{MPWARNVM} | Asynchronous Reset Minimum Pulse Width for the Control Logic | 10.00 | 12.50 | 12.50 | ns |
| $t_{\text{MPWCLKNVM}}$ | Clock Minimum Pulse Width for the Control Logic | 4.00 | 5.00 | 5.00 | ns |
| $t_{\text{FMAXCLKNVM}}$ | Maximum Frequency for Clock for the Control Logic – for AFS1500/AFS600 | 80.00 | 80.00 | 80.00 | MHz |
| | Maximum Frequency for Clock for the Control Logic – for AFS250/AFS090 | 100.00 | 80.00 | 80.00 | MHz |

FlashROM

Fusion devices have 1 kbit of on-chip nonvolatile flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in eight banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read-back of the FlashROM from the FPGA core (Figure 2-45).

The FlashROM can only be programmed via the IEEE 1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the eight 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports a synchronous read and can be read on byte boundaries. The upper three bits of the FlashROM address from the FPGA core define the bank that is being accessed. The lower four bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

The maximum FlashROM access clock is given in Table 2-26 on page 2-54. Figure 2-46 shows the timing behavior of the FlashROM access cycle—the address has to be set up on the rising edge of the clock for DOUT to be valid on the next falling edge of the clock.

If the address is unchanged for two cycles:

- D0 becomes invalid t_{CK2Q} ns after the second rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the second falling edge.

If the address is unchanged for three cycles:

- D0 becomes invalid t_{CK2Q} ns after the second rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the second falling edge.
- D0 becomes invalid t_{CK2Q} ns after the third rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the third falling edge.

| | | Byte Number in Bank | | | | | | | | | | | | | | | |
|-------------------------------------|---|----------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | 4 LSB of ADDR (READ) | | | | | | | | | | | | | | | |
| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Bank Number 3 MSB of ADDR (READ) | 7 | | | | | | | | | | | | | | | | |
| | 6 | | | | | | | | | | | | | | | | |
| | 5 | | | | | | | | | | | | | | | | |
| | 4 | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | |
| | 1 | | | | | | | | | | | | | | | | |
| | 0 | | | | | | | | | | | | | | | | |

Figure 2-45 • FlashROM Architecture

FlashROM Characteristics



Figure 2-46 • FlashROM Timing Diagram

Table 2-26 • FlashROM Access Time

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|------------|-------------------------|-------|-------|-------|-------|
| t_{SU} | Address Setup Time | 0.53 | 0.61 | 0.71 | ns |
| t_{HOLD} | Address Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t_{CK2Q} | Clock to Out | 21.42 | 24.40 | 28.68 | ns |
| F_{MAX} | Maximum Clock frequency | 15.00 | 15.00 | 15.00 | MHz |

SRAM and FIFO

All Fusion devices have SRAM blocks along the north side of the device. Additionally, AFS600 and AFS1500 devices have an SRAM block on the south side of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz. The following configurations are available:

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The Fusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to [Figure 2-47](#) for more information about the implementation of the embedded FIFO controller.

The Fusion architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. For example, the write size can be set to 256×18 and the read size to 512×9.

Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in [Table 2-27 on page 2-58](#).

When a width of one, two, or four is selected, the ninth bit is unused. For example, when writing 9-bit values and reading 4-bit values, only the first four bits and the second four bits of each 9-bit value are addressable for read operations. The ninth bit is not accessible.

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.



Figure 2-47 • Fusion RAM Block with Embedded FIFO Controller

RAM4K9 Description

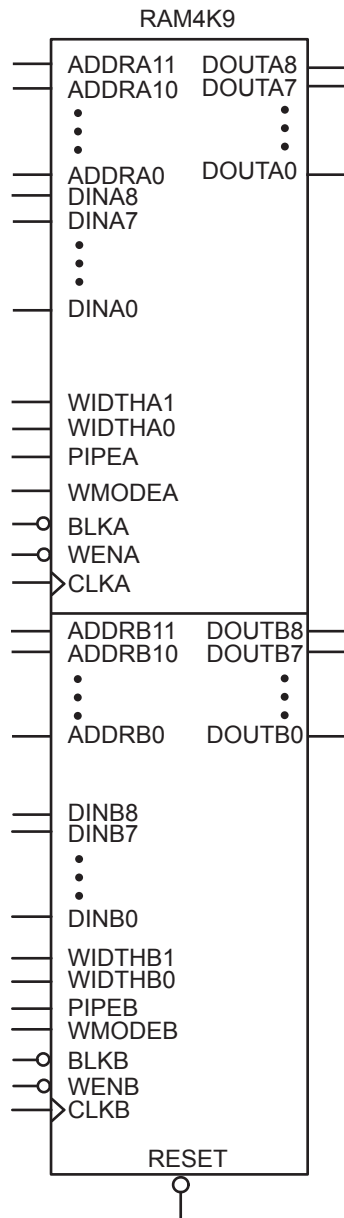


Figure 2-48 • RAM4K9

The following signals are used to configure the RAM4K9 memory element.

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-27).

Table 2-27 • Allowable Aspect Ratio Settings for WIDTHA[1:0]

| WIDTHA1, WIDTHA0 | WIDTHB1, WIDTHB0 | D×W |
|------------------|------------------|-------|
| 00 | 00 | 4k×1 |
| 01 | 01 | 2k×2 |
| 10 | 10 | 1k×4 |
| 11 | 11 | 512×9 |

Note: The aspect ratio settings are constant and cannot be changed on the fly.

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, the corresponding port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write mode for the respective ports. A Low on these signals indicates a write operation, and a High indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A Low on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A High indicates a pipelined, read and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when the RAM is in write mode. A Low on these signals makes the output retain data from the previous read. A High indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

RESET

This active low signal resets the output to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

ADDRA and ADDRb

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-28).

Table 2-28 • Address Pins Unused/Used for Various Supported Bus Widths

| D×W | ADDRx | |
|-------|---------|--------|
| | Unused | Used |
| 4k×1 | None | [11:0] |
| 2k×2 | [11] | [10:0] |
| 1k×4 | [11:10] | [9:0] |
| 512×9 | [11:9] | [8:0] |

Note: The "x" in ADDRx implies A or B.

DINA and DINB

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 2-29).

DOUTA and DOUTB

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 2-29). The output data on unused pins is undefined.

Table 2-29 • Unused/Used Input and Output Data Pins for Various Supported Bus Widths

| D×W | DINx/DOUTx | |
|------------|-------------------|-------------|
| | Unused | Used |
| 4k×1 | [8:1] | [0] |
| 2k×2 | [8:2] | [1:0] |
| 1k×4 | [8:4] | [3:0] |
| 512×9 | None | [8:0] |

Note: The "x" in DINx and DOUTx implies A or B.

RAM512X18 Description



Figure 2-49 • RAM512X18

RAM512X18 exhibits slightly different behavior from RAM4K9, as it has dedicated read and write ports.

WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 2-30).

Table 2-30 • Aspect Ratio Settings for WW[1:0]

| WW[1:0] | RW[1:0] | D×W |
|---------|---------|----------|
| 01 | 01 | 512×9 |
| 10 | 10 | 256×18 |
| 00, 11 | 00, 11 | Reserved |

WD and RD

These are the input and output data signals, and they are 18 bits wide. When a 512×9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, then RD[17:9] are undefined.

WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256×18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] are unused and must be grounded.

WCLK and RCLK

These signals are the write and read clocks, respectively. They are both active high.

WEN and REN

These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

RESET

This active low signal resets the output to zero, disables reads and/or writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

PIPE

This signal is used to specify pipelined read on the output. A Low on PIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

Clocking

The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge-triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge or by separate clocks, by port.

Fusion devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising edge or falling edge of WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the Fusion development tools, without performance penalty.

Note: Data in the SRAM block can be corrupted during a read operation, when the read address does not meet setup and hold requirements with respect to the clock for that port. The data corruption occurs when the read address (RADDR) changes almost simultaneously with read clock (RCLK) edge (that is, RADDR violates the timing requirement of the memory). Users must always meet the setup and hold time requirements on the RAM inputs; to have reliable and predictable results for reads and writes. To avoid data corruption due to asynchronous clocking for read address and read clock of the RAM, users must implement a proper synchronizer circuit. For more information, see, *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—1 clock edge): In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge, and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—2 clock edges): The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—1 clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is High. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "SRAM Characteristics" section on page 2-63 and the "FIFO Characteristics" section on page 2-72.

RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG IEEE 1532" section on page 2-229 and the *Fusion SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

SRAM Characteristics

Timing Waveforms



Figure 2-50 • RAM Read for Flow-Through Output. Applicable to both RAM4K9 and RAM512x18.



Figure 2-51 • RAM Read for Pipelined Output. Applicable to both RAM4K9 and RAM512x18.



Figure 2-52 • RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512x18.



Figure 2-53 • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.

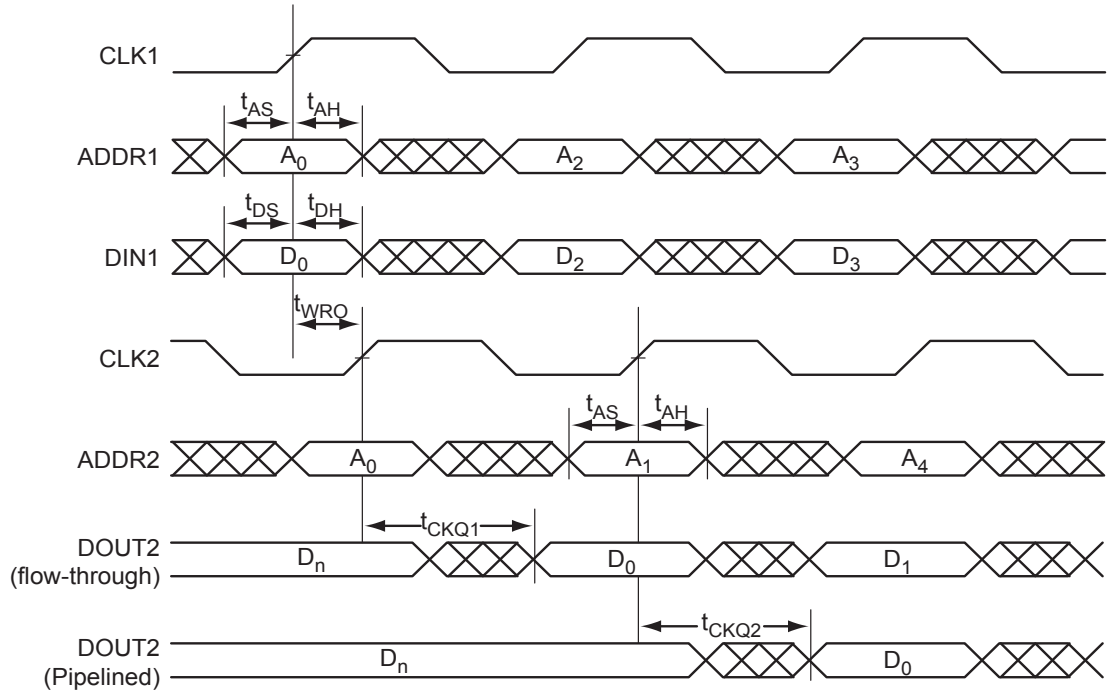


Figure 2-54 • One Port Write / Other Port Read Same

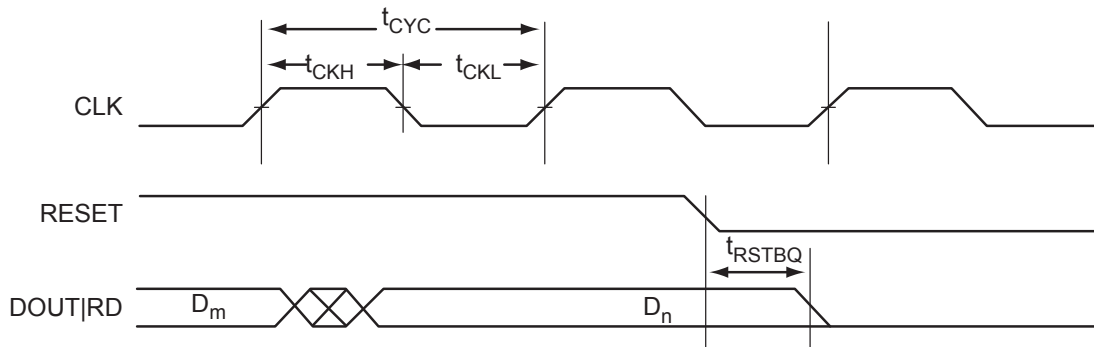


Figure 2-55 • RAM Reset. Applicable to both RAM4K9 and RAM512x18.

Timing Characteristics

Table 2-31 • RAM4K9

 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------|--|------|------|------|-------|
| t_{AS} | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| t_{AH} | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{ENS} | REN, WEN setup time | 0.14 | 0.16 | 0.19 | ns |
| t_{ENH} | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| t_{BKS} | BLK setup time | 0.23 | 0.27 | 0.31 | ns |
| t_{BKH} | BL hold time | 0.02 | 0.02 | 0.02 | ns |
| t_{DS} | Input data (DIN) setup time | 0.18 | 0.21 | 0.25 | ns |
| t_{DH} | Input data (DIN) hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 1.79 | 2.03 | 2.39 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 2.36 | 2.68 | 3.15 | ns |
| t_{CKQ2} | Clock High to new data valid on DOUT (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| t_{C2CWWH}^1 | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge | 0.30 | 0.26 | 0.23 | ns |
| t_{C2CRWH}^1 | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.45 | 0.38 | 0.34 | ns |
| t_{C2CWRH}^1 | Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge | 0.49 | 0.42 | 0.37 | ns |
| t_{RSTBQ} | RESET Low to data out Low on DOUT (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| t_{CYC} | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| F_{MAX} | Maximum frequency | 310 | 272 | 231 | MHz |

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Table 2-32 • RAM512X18Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------|--|------|------|------|-------|
| t_{AS} | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| t_{AH} | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{ENS} | REN, WEN setup time | 0.09 | 0.10 | 0.12 | ns |
| t_{ENH} | REN, WEN hold time | 0.06 | 0.07 | 0.08 | ns |
| t_{DS} | Input data (WD) setup time | 0.18 | 0.21 | 0.25 | ns |
| t_{DH} | Input data (WD) hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock High to new data valid on RD (output retained) | 2.16 | 2.46 | 2.89 | ns |
| t_{CKQ2} | Clock High to new data valid on RD (pipelined) | 0.90 | 1.02 | 1.20 | ns |
| t_{C2CRWH}^1 | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.50 | 0.43 | 0.38 | ns |
| t_{C2CWRH}^1 | Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge | 0.59 | 0.50 | 0.44 | ns |
| t_{RSTBQ}^1 | RESET Low to data out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to data out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| t_{CYC} | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| F_{MAX} | Maximum frequency | 310 | 272 | 231 | MHz |

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

FIFO4K18 Description



Figure 2-56 • FIFO4KX18

The following signals are used to configure the FIFO4K18 memory element.

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-33).

Table 2-33 • Aspect Ratio Settings for WW[2:0]

| WW2, WW1, WW0 | RW2, RW1, RW0 | D×W |
|---------------|---------------|----------|
| 000 | 000 | 4k×1 |
| 001 | 001 | 2k×2 |
| 010 | 010 | 1k×4 |
| 011 | 011 | 512×9 |
| 100 | 100 | 256×18 |
| 101, 110, 111 | 101, 110, 111 | Reserved |

WBLK and RBLK

These signals are active low and will enable the respective ports when Low. When the RBLK signal is High, the corresponding port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

RPIPE

This signal is used to specify pipelined read on the output. A Low on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

RESET

This active low signal resets the output to zero when asserted. It resets the FIFO counters. It also sets all the RD pins Low, the FULL and AFULL pins Low, and the EMPTY and AEMPTY pins High (Table 2-34).

Table 2-34 • Input Data Signal Usage for Different Aspect Ratios

| D×W | WD/RD Unused |
|--------|--------------------|
| 4k×1 | WD[17:1], RD[17:1] |
| 2k×2 | WD[17:2], RD[17:2] |
| 1k×4 | WD[17:4], RD[17:4] |
| 512×9 | WD[17:9], RD[17:9] |
| 256×18 | — |

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-34).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-34).

ESTOP, FSTOP

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the EMPTY flag goes High). A High on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the FULL flag goes High). A High on this signal inhibits the counting.

For more information on these signals, refer to the "[ESTOP and FSTOP Usage](#)" section on page 2-70.

FULL, EMPTY

When the FIFO is full and no more data can be written, the FULL flag asserts High. The FULL flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the FULL flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the EMPTY flag asserts High. The EMPTY flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent underflows. Since the read address is compared to a resynchronized (and thus time-delayed) version of the write address, the EMPTY flag will remain asserted until two RCLK active edges after a write operation removes the empty condition.

For more information on these signals, refer to the "[FIFO Flag Usage Considerations](#)" section on page 2-70.

AFULL, AEMPTY

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the AEMPTY output will go High. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go High.

AFVAL, AEVAL

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values, respectively. They are 12-bit signals. For more information on these signals, refer to "[FIFO Flag Usage Considerations](#)" section.

ESTOP and FSTOP Usage

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes High). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the FULL flag goes High).

The FIFO counters in the Fusion device start the count at 0, reach the maximum depth for the configuration (e.g., 511 for a 512×9 configuration), and then restart at 0. An example application for the ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over without doing another write.

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values, respectively. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

FIFO Characteristics
Timing Waveforms

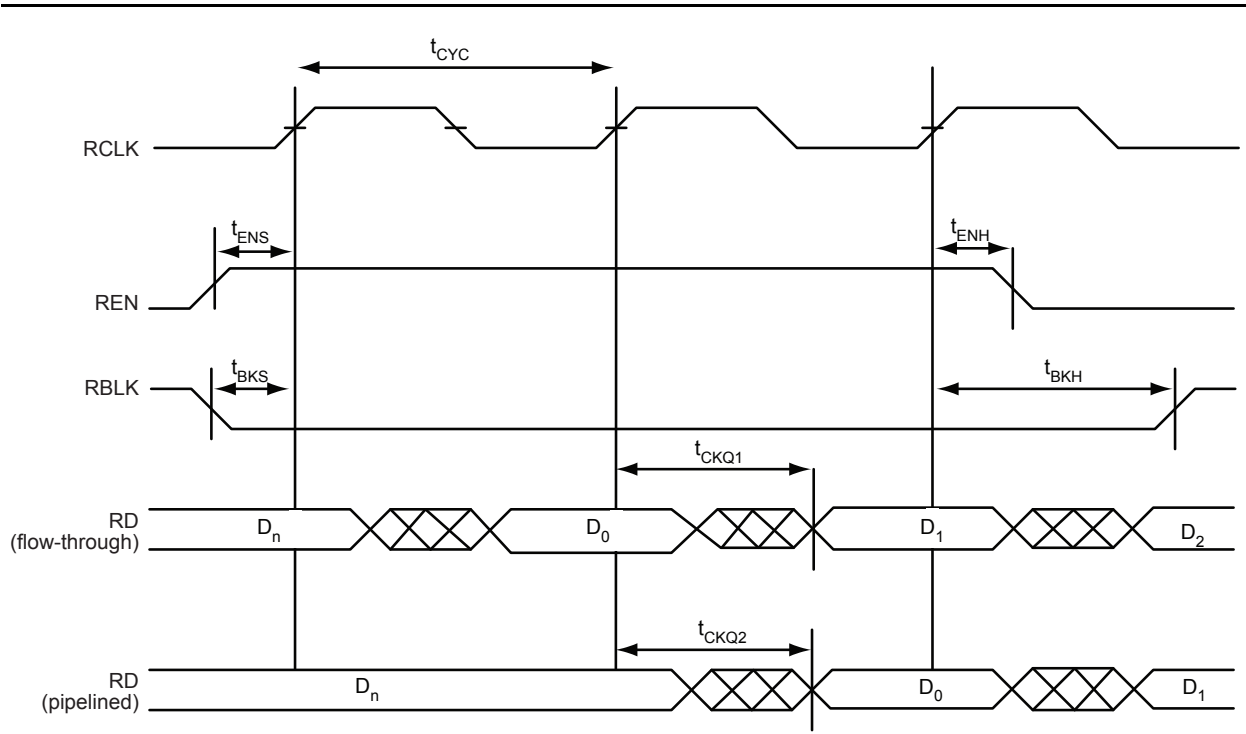


Figure 2-57 • FIFO Read



Figure 2-58 • FIFO Write

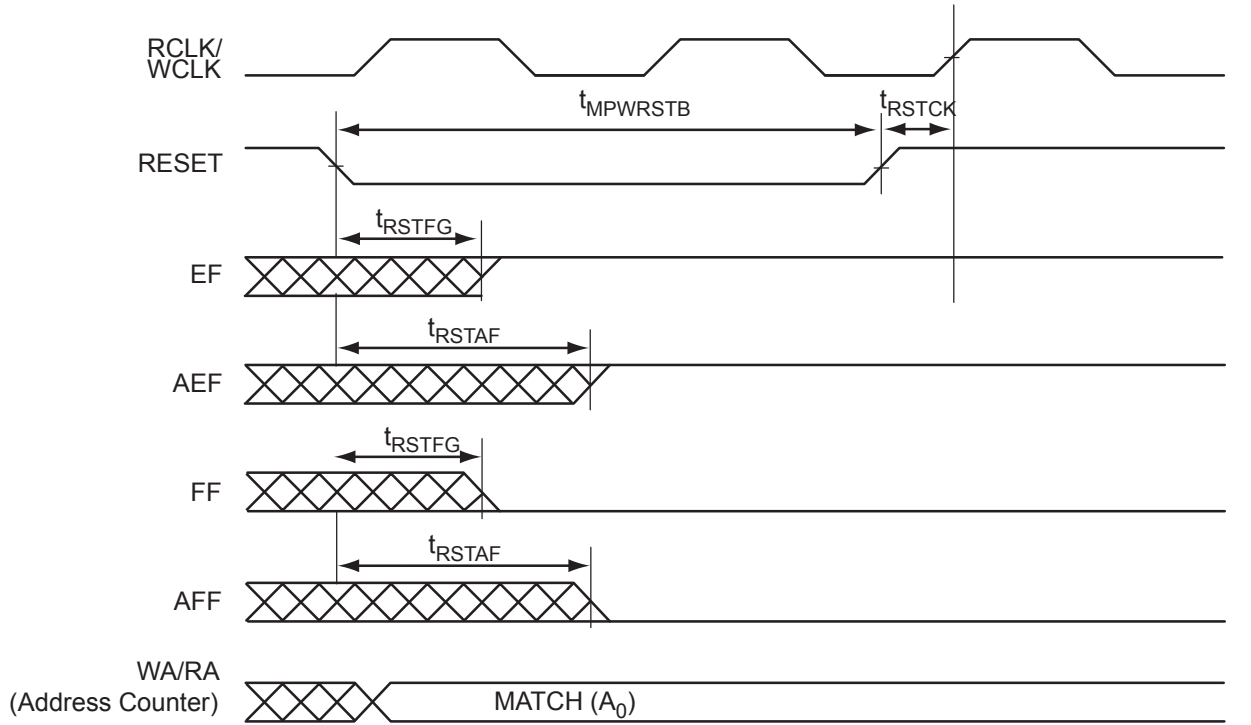


Figure 2-59 • FIFO Reset

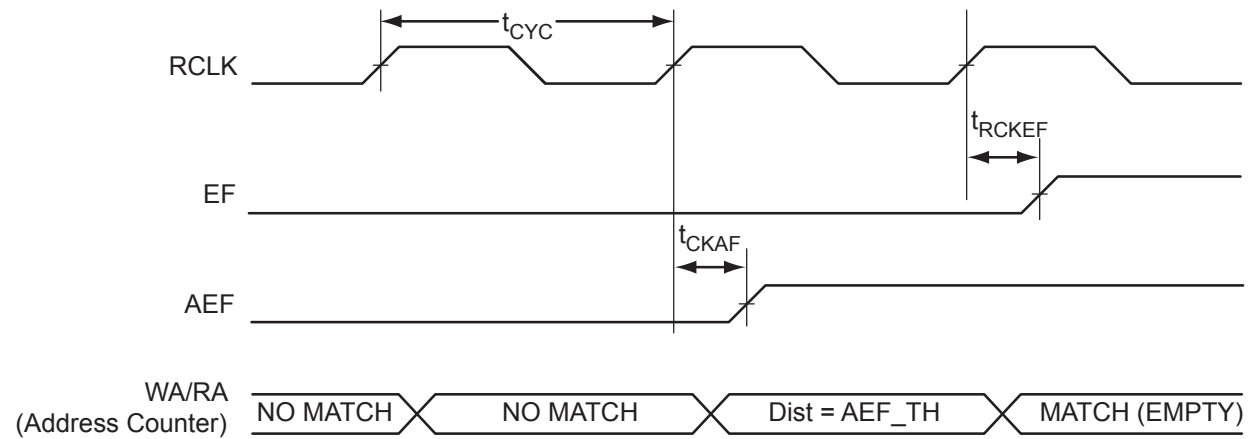


Figure 2-60 • FIFO EMPTY Flag and AEMPTY Flag Assertion



Figure 2-61 • FIFO FULL and AFULL Flag Assertion



Figure 2-62 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

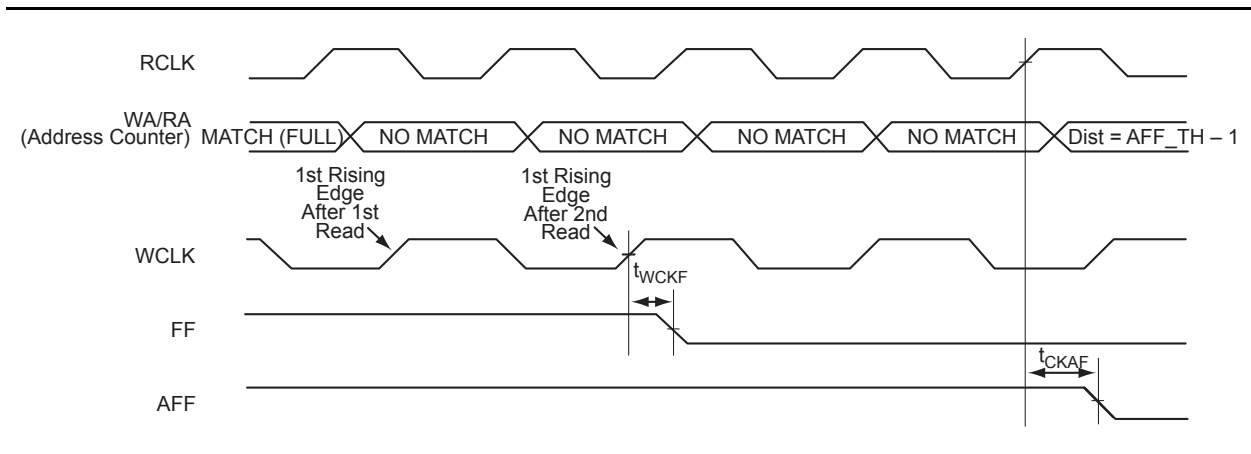


Figure 2-63 • FIFO FULL Flag and AFULL Flag Deassertion

Timing Characteristics

Table 2-35 • FIFO

 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------|---|------|------|------|-------|
| t_{ENS} | REN, WEN Setup time | 1.34 | 1.52 | 1.79 | ns |
| t_{ENH} | REN, WEN Hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{BKS} | BLK Setup time | 0.19 | 0.22 | 0.26 | ns |
| t_{BKH} | BLK Hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{DS} | Input data (WD) Setup time | 0.18 | 0.21 | 0.25 | ns |
| t_{DH} | Input data (WD) Hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock High to New Data Valid on RD (flow-through) | 2.17 | 2.47 | 2.90 | ns |
| t_{CKQ2} | Clock High to New Data Valid on RD (pipelined) | 0.94 | 1.07 | 1.26 | ns |
| t_{RCKEF} | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| t_{WCKFF} | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| t_{CKAF} | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| t_{RSTFG} | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| t_{RSTAF} | RESET Low to Almost-Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| t_{RSTBQ} | RESET Low to Data out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| t_{CYC} | Clock Cycle time | 3.23 | 3.68 | 4.32 | ns |
| F_{MAX} | Maximum Frequency for FIFO | 310 | 272 | 231 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Analog Block

With the Fusion family, Microsemi has introduced the world's first mixed-mode FPGA solution. Supporting a robust analog peripheral mix, Fusion devices will support a wide variety of applications. It is this Analog Block that separates Fusion from all other FPGA solutions on the market today.

By combining both flash and high-speed CMOS processes in a single chip, these devices offer the best of both worlds. The high-performance CMOS is used for building RAM resources. These high-performance structures support device operation up to 350 MHz. Additionally, the advanced Microsemi 0.13 μm flash process incorporates high-voltage transistors and a high-isolation, triple-well process. Both of these are suited for the flash-based programmable logic and nonvolatile memory structures.

High-voltage transistors support the integration of analog technology in several ways. They aid in noise immunity so that the analog portions of the chip can be better isolated from the digital portions, increasing analog accuracy. Because they support high voltages, Microsemi flash FPGAs can be connected directly to high-voltage input signals, eliminating the need for external resistor divider networks, reducing component count, and increasing accuracy. By supporting higher internal voltages, the Microsemi advanced flash process enables high dynamic range on analog circuitry, increasing precision and signal-noise ratio. Microsemi flash FPGAs also drive high-voltage outputs, eliminating the need for external level shifters and drivers.

The unique triple-well process enables the integration of high-performance analog features with increased noise immunity and better isolation. By increasing the efficiency of analog design, the triple-well process also enables a smaller overall design size, reducing die size and cost.

The Analog Block consists of the Analog Quad I/O structure, RTC (for details refer to the "[Real-Time Counter System](#)" section on page 2-31), ADC, and ACM. All of these elements are combined in the single Analog Block macro, with which the user implements this functionality ([Figure 2-64](#)).

The Analog Block needs to be reset/reinitialized after the core powers up or the device is programmed. An external reset/initialize signal, which can come from the internal voltage regulator when it powers up, must be applied.



Figure 2-64 • Analog Block Macro

Table 2-36 describes each pin in the Analog Block. Each function within the Analog Block will be explained in detail in the following sections.

Table 2-36 • Analog Block Pin Description

| Signal Name | Number of Bits | Direction | Function | Location of Details |
|------------------|----------------|--------------|---|---------------------|
| VAREF | 1 | Input/Output | Voltage reference for ADC | ADC |
| ADCGNDREF | 1 | Input | External ground reference | ADC |
| MODE[3:0] | 4 | Input | ADC operating mode | ADC |
| SYSCLK | 1 | Input | External system clock | |
| TVC[7:0] | 8 | Input | Clock divide control | ADC |
| STC[7:0] | 8 | Input | Sample time control | ADC |
| ADCSTART | 1 | Input | Start of conversion | ADC |
| PWRDWN | 1 | Input | ADC comparator power-down if 1. When asserted, the ADC will stop functioning, and the digital portion of the analog block will continue operating. This may result in invalid status flags from the analog block. Therefore, Microsemi does not recommend asserting the PWRDWN pin. | ADC |
| ADCRESET | 1 | Input | ADC resets and disables Analog Quad – active high | ADC |
| BUSY | 1 | Output | 1 – Running conversion | ADC |
| CALIBRATE | 1 | Output | 1 – Power-up calibration | ADC |
| DATAVALID | 1 | Output | 1 – Valid conversion result | ADC |
| RESULT[11:0] | 12 | Output | Conversion result | ADC |
| TMSTBINT | 1 | Input | Internal temp. monitor strobe | ADC |
| SAMPLE | 1 | Output | 1 – An analog signal is actively being sampled (stays high during signal acquisition only) 0 – No analog signal is being sampled | ADC |
| VAREFSEL | 1 | Input | 0 = Output internal voltage reference (2.56 V) to VAREF 1 = Input external voltage reference from VAREF and ADCGNDREF | ADC |
| CHNUMBER[4:0] | 5 | Input | Analog input channel select | Input multiplexer |
| ACMCLK | 1 | Input | ACM clock | ACM |
| ACMWEN | 1 | Input | ACM write enable – active high | ACM |
| ACMRESET | 1 | Input | ACM reset – active low | ACM |
| ACMWDATA[7:0] | 8 | Input | ACM write data | ACM |
| ACMRDATA[7:0] | 8 | Output | ACM read data | ACM |
| ACMADDR[7:0] | 8 | Input | ACM address | ACM |
| CMSTB0 to CMSTB9 | 10 | Input | Current monitor strobe – 1 per quad, active high | Analog Quad |

Table 2-36 • Analog Block Pin Description (continued)

| Signal Name | Number of Bits | Direction | Function | Location of Details |
|--|----------------|-----------|---|---------------------|
| GDON0 to GDON9 | 10 | Input | Control to power MOS – 1 per quad | Analog Quad |
| TMSTB0 to TMSTB9 | 10 | Input | Temperature monitor strobe – 1 per quad; active high | Analog Quad |
| DAVOUT0, DACOUT0, DATOUT0 to DAVOUT9, DACOUT9, DATOUT9 | 30 | Output | Digital outputs – 3 per quad | Analog Quad |
| DENAV0, DENAC0, DENAT0 to DENAV9, DENAC9, DENAT9 | 30 | Input | Digital input enables – 3 per quad | Analog Quad |
| AV0 | 1 | Input | Analog Quad 0 | Analog Quad |
| AC0 | 1 | Input | | Analog Quad |
| AG0 | 1 | Output | | Analog Quad |
| AT0 | 1 | Input | | Analog Quad |
| ATRETURN01 | 1 | Input | Temperature monitor return shared by Analog Quads 0 and 1 | Analog Quad |
| AV1 | 1 | Input | Analog Quad 1 | Analog Quad |
| AC1 | 1 | Input | | Analog Quad |
| AG1 | 1 | Output | | Analog Quad |
| AT1 | 1 | Input | | Analog Quad |
| AV2 | 1 | Input | Analog Quad 2 | Analog Quad |
| AC2 | 1 | Input | | Analog Quad |
| AG2 | 1 | Output | | Analog Quad |
| AT2 | 1 | Input | | Analog Quad |
| ATRETURN23 | 1 | Input | Temperature monitor return shared by Analog Quads 2 and 3 | Analog Quad |
| AV3 | 1 | Input | Analog Quad 3 | Analog Quad |
| AC3 | 1 | Input | | Analog Quad |
| AG3 | 1 | Output | | Analog Quad |
| AT3 | 1 | Input | | Analog Quad |
| AV4 | 1 | Input | Analog Quad 4 | Analog Quad |
| AC4 | 1 | Input | | Analog Quad |
| AG4 | 1 | Output | | Analog Quad |
| AT4 | 1 | Input | | Analog Quad |
| ATRETURN45 | 1 | Input | Temperature monitor return shared by Analog Quads 4 and 5 | Analog Quad |
| AV5 | 1 | Input | Analog Quad 5 | Analog Quad |
| AC5 | 1 | Input | | Analog Quad |
| AG5 | 1 | Output | | Analog Quad |
| AT5 | 1 | Input | | Analog Quad |
| AV6 | 1 | Input | Analog Quad 6 | Analog Quad |
| AC6 | 1 | Input | | Analog Quad |

Table 2-36 • Analog Block Pin Description (continued)

| Signal Name | Number of Bits | Direction | Function | Location of Details |
|-----------------|----------------|-----------|---|---------------------|
| AG6 | 1 | Output | | Analog Quad |
| AT6 | 1 | Input | | Analog Quad |
| ATRETURN67 | 1 | Input | Temperature monitor return shared by Analog Quads 6 and 7 | Analog Quad |
| AV7 | 1 | Input | Analog Quad 7 | Analog Quad |
| AC7 | 1 | Input | | Analog Quad |
| AG7 | 1 | Output | | Analog Quad |
| AT7 | 1 | Input | | Analog Quad |
| AV8 | 1 | Input | Analog Quad 8 | Analog Quad |
| AC8 | 1 | Input | | Analog Quad |
| AG8 | 1 | Output | | Analog Quad |
| AT8 | 1 | Input | | Analog Quad |
| ATRETURN89 | 1 | Input | Temperature monitor return shared by Analog Quads 8 and 9 | Analog Quad |
| AV9 | 1 | Input | Analog Quad 9 | Analog Quad |
| AC9 | 1 | Input | | Analog Quad |
| AG9 | 1 | Output | | Analog Quad |
| AT9 | 1 | Input | | Analog Quad |
| RTCMATCH | 1 | Output | MATCH | RTC |
| RTCPSMMATCH | 1 | Output | MATCH connected to VRPSM | RTC |
| RTCXTLMODE[1:0] | 2 | Output | Drives XTLOSC RTCMODE[1:0] pins | RTC |
| RTCXTLSEL | 1 | Output | Drives XTLOSC MODESEL pin | RTC |
| RTCCLK | 1 | Input | RTC clock input | RTC |

Analog Quad

With the Fusion family, Microsemi introduces the Analog Quad, shown in [Figure 2-65 on page 2-81](#), as the basic analog I/O structure. The Analog Quad is a four-channel system used to precondition a set of analog signals before sending it to the ADC for conversion into a digital signal. To maximize the usefulness of the Analog Quad, the analog input signals can also be configured as LVTTTL digital input signals. The Analog Quad is divided into four sections.

The first section is called the Voltage Monitor Block, and its input pin is named AV. It contains a two-channel analog multiplexer that allows an incoming analog signal to be routed directly to the ADC or allows the signal to be routed to a prescaler circuit before being sent to the ADC. The prescaler can be configured to accept analog signals between -12 V and 0 or between 0 and $+12\text{ V}$. The prescaler circuit scales the voltage applied to the ADC input pad such that it is compatible with the ADC input voltage range. The AV pin can also be used as a digital input pin.

The second section of the Analog Quad is called the Current Monitor Block. Its input pin is named AC. The Current Monitor Block contains all the same functions as the Voltage Monitor Block with one addition, which is a current monitoring function. A small external current sensing resistor (typically less than $1\ \Omega$) is connected between the AV and AC pins and is in series with a power source. The Current Monitor Block contains a current monitor circuit that converts the current through the external resistor to a voltage that can then be read using the ADC.

The third part of the Analog Quad is called the Gate Driver Block, and its output pin is named AG. This section is used to drive an external FET. There are two modes available: a High Current Drive mode and a Current Source Control mode. Both negative and positive voltage polarities are available, and in the current source control mode, four different current levels are available.

The fourth section of the Analog Quad is called the Temperature Monitor Block, and its input pin name is AT. This block is similar to the Voltage Monitor Block, except that it has an additional function: it can be used to monitor the temperature of an external diode-connected transistor. It has a modified prescaler and is limited to positive voltages only.

The Analog Quad can be configured during design time by Libero SoC; however, the ACM can be used to change the parameters of any of these I/Os during runtime. This type of change is referred to as a context switch. The Analog Quad is a modular structure that is replicated to generate the analog I/O resources. Each Fusion device supports between 5 and 10 Analog Quads.

The analog pads are numbered to clearly identify both the type of pad (voltage, current, gate driver, or temperature pad) and its corresponding Analog Quad (AV0, AC0, AG0, AT0, AV1, ..., AC9, AG9, and AT9). There are three types of input pads (AVx, ACx, and ATx) and one type of analog output pad (AGx). Since there can be up to 10 Analog Quads on a device, there can be a maximum of 30 analog input pads and 10 analog output pads.



Figure 2-65 • Analog Quad

Voltage Monitor

The Fusion Analog Quad offers a robust set of voltage-monitoring capabilities unique in the FPGA industry. The Analog Quad comprises three analog input pads— Analog Voltage (AV), Analog Current (AC), and Analog Temperature (AT)—and a single gate driver output pad, Analog Gate (AG). There are many common characteristics among the analog input pads. Each analog input can be configured to connect directly to the input MUX of the ADC. When configured in this manner (Figure 2-66), there will be no prescaling of the input signal. Care must be taken in this mode not to drive the ADC into saturation by applying an input voltage greater than the reference voltage. The internal reference voltage of the ADC is 2.56 V. Optionally, an external reference can be supplied by the user. The external reference can be a maximum of 3.3 V DC.



Figure 2-66 • Analog Quad Direct Connect

The Analog Quad offers a wide variety of prescaling options to enable the ADC to resolve the input signals. Figure 2-67 shows the path through the Analog Quad for a signal that is to be prescaled prior to conversion. The ADC internal reference voltage and the prescaler factors were selected to make both prescaling and postsaling of the signals easy binary calculations (refer to Table 2-57 on page 2-130 for details). When an analog input pad is configured with a prescaler, there will be a 1 M Ω resistor to ground. This occurs even when the device is in power-down mode. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, analog inputs are pulled down to ground through a 1 M Ω resistor. The gate driver output is floating (or tristated), and there is no extra current on VCC33A.

These scaling factors hold true whether the particular pad is configured to accept a positive or negative voltage. Note that whereas the AV and AC pads support the same prescaling factors, the AT pad supports a reduced set of prescaling factors and supports positive voltages only.

Typical scaling factors are given in Table 2-57 on page 2-130, and the gain error (which contributes to the minimum and maximum) is in Table 2-49 on page 2-117.



Figure 2-67 • Analog Quad Prescaler Input Configuration

Terminology

BW – Bandwidth

BW is a range of frequencies that a Channel can handle.

Channel

A channel is define as an analog input configured as one of the Prescaler range shown in Table 2-57 on page 2-130. The channel includes the Prescaler circuit and the ADC.

Channel Gain

Channel Gain is a measured of the deviation of the actual slope from the ideal slope. The slope is measured from the 20% and 80% point.

$$Gain = \frac{Gain_{actual}}{Gain_{ideal}}$$

EQ 1

Channel Gain Error

Channel Gain Error is a deviation from the ideal slope of the transfer function. The Prescaler Gain Error is expressed as the percent difference between the actual and ideal, as shown in EQ 2.

$$Error_{Gain} = (1-Gain) \times 100\%$$

EQ 2

Channel Input Offset Error

Channel Offset error is measured as the input voltage that causes the transition from zero to a count of one. An Ideal Prescaler will have offset equal to $\frac{1}{2}$ of LSB voltage. Offset error is a positive or negative when the first transition point is higher or lower than ideal. Offset error is expressed in LSB or input voltage.

Total Channel Error

Total Channel Error is defined as the total error measured compared to the ideal value. Total Channel Error is the sum of gain error and offset error combined. Figure 2-68 shows how Total Channel Error is measured.

Total Channel Error is defined as the difference between the actual ADC output and ideal ADC output. In the example shown in Figure 2-68, the Total Channel Error would be a negative number.



Figure 2-68 • Total Channel Error Example

Direct Digital Input

The AV, AC, and AT pads can also be configured as high-voltage digital inputs (Figure 2-69). As these pads are 12 V-tolerant, the digital input can also be up to 12 V. However, the frequency at which these pads can operate is limited to 10 MHz.

To enable one of these analog input pads to operate as a digital input, its corresponding Digital Input Enable (DENAx_y) pin on the Analog Block must be pulled High, where x is either V, C, or T (for AV, AC, or AT pads, respectively) and y is in the range 0 to 9, corresponding to the appropriate Analog Quad.

When the pad is configured as a digital input, the signal will come out of the Analog Block macro on the appropriate DAxOUT_y pin, where x represents the pad type (V for AV pad, C for AC pad, or T for AT pad) and y represents the appropriate Analog Quad number. Example: If the AT pad in Analog Quad 5 is configured as a digital input, it will come out on the DATOUT5 pin of the Analog Block macro.



Figure 2-69 • Analog Quad Direct Digital Input Configuration

Current Monitor

The Fusion Analog Quad is an excellent element for voltage- and current-monitoring applications. In addition to supporting the same functionality offered by the AV pad, the AC pad can be configured to monitor current across an external sense resistor (Figure 2-70). To support this current monitor function, a differential amplifier with 10x gain passes the amplified voltage drop between the AV and AC pads to the ADC. The amplifier enables the user to use very small resistor values, thereby limiting any impact on the circuit. This function of the AC pad does not limit AV pad operation. The AV pad can still be configured for use as a direct voltage input or scaled through the AV prescaler independently of its use as an input to the AC pad's differential amplifier.



Figure 2-70 • Analog Quad Current Monitor Configuration

To initiate a current measurement, the appropriate Current Monitor Strobe (CMSTB) signal on the AB macro must be asserted low for at least t_{CMSLO} in order to discharge the previous measurement. Then CMSTB must be asserted high for at least t_{CMSET} prior to asserting the ADCSTART signal. The CMSTB must remain high until after the SAMPLE signal is de-asserted by the AB macro. Note that the minimum sample time cannot be less than t_{CMSHI} . Figure 2-71 shows the timing diagram of CMSTB in relationship with the ADC control signals.



Figure 2-71 • Timing Diagram for Current Monitor Strobe

Figure 2-72 illustrates positive current monitor operation. The differential voltage between AV and AC goes into the 10× amplifier and is then converted by the ADC. For example, a current of 1.5 A is drawn from a 10 V supply and is measured by the voltage drop across a 0.050 Ω sense resistor. The voltage drop is amplified by ten times by the amplifier and then measured by the ADC. The 1.5 A current creates a differential voltage across the sense resistor of 75 mV. This becomes 750 mV after amplification. Thus, the ADC measures a current of 1.5 A as 750 mV. Using an ADC with 8-bit resolution and VAREF of 2.56 V, the ADC result is decimal 75. EQ 3 shows how to compute the current from the ADC result.

$$I = (ADC \times V_{AREF}) / (10 \times 2^N \times R_{sense})$$

EQ 3

where

- I is the current flowing through the sense resistor
- ADC is the result from the ADC
- VAREF is the Reference voltage
- N is the number of bits
- R_{sense} is the resistance of the sense resistor



Figure 2-72 • Positive Current Monitor

Care must be taken when choosing the right resistor for current measurement application. Note that because of the 10× amplification, the maximum measurable difference between the AV and AC pads is $V_{AREF} / 10$. A larger AV-to-AC voltage drop will result in ADC saturation; that is, the digital code put out by the ADC will stay fixed at the full scale value. Therefore, the user must select the external sense resistor appropriately. Table 2-38 shows recommended resistor values for different current measurement ranges. When choosing resistor values for a system, there is a trade-off between measurement accuracy and power consumption. Choosing a large resistor will increase the voltage drop and hence increase accuracy of the measurement; however the larger voltage drop dissipates more power ($P = I^2 \times R$).

The Current Monitor is a unipolar system, meaning that the differential voltage swing must be from 0 V to $V_{AREF}/10$. Therefore, the Current Monitor only supports differential voltage where $|V_{AV}-V_{AC}|$ is greater than 0 V. This results in the requirement that the potential of the AV pad must be larger than the potential of the AC pad. This is straightforward for positive voltage systems. For a negative voltage system, it means that the AV pad must be “more negative” than the AC pad. This is shown in Figure 2-73.

In this case, both the AV pad and the AC pad are configured for negative operations and the output of the differential amplifier still falls between 0 V and V_{AREF} as required.

Table 2-37 • Recommended Resistor for Different Current Range Measurement

| Current Range | Recommended Minimum Resistor Value (Ohms) |
|-------------------|---|
| > 5 mA – 10 mA | 10 – 20 |
| > 10 mA – 20 mA | 5 – 10 |
| > 20 mA – 50 mA | 2.5 – 5 |
| > 50 mA – 100 mA | 1 – 2 |
| > 100 mA – 200 mA | 0.5 – 1 |
| > 200 mA – 500 mA | 0.3 – 0.5 |
| > 500 mA – 1 A | 0.1 – 0.2 |
| > 1 A – 2 A | 0.05 – 0.1 |
| > 2 A – 4 A | 0.025 – 0.05 |
| > 4 A – 8 A | 0.0125 – 0.025 |
| > 8 A – 12 A | 0.00625 – 0.02 |



Figure 2-73 • Negative Current Monitor

Terminology

Accuracy

The accuracy of Fusion Current Monitor is ± 2 mV minimum plus 5% of the differential voltage at the input. The input accuracy can be translated to error at the ADC output by using EQ 4. The 10 V/V gain is the gain of the Current Monitor Circuit, as described in the "Current Monitor" section on page 2-86. For 8-bit mode, $N = 8$, $V_{AREF} = 2.56$ V, zero differential voltage between AV and AC, the Error (E_{ADC}) is equal to 2 LSBs.

$$E_{ADC} = (2mV + 0.05|V_{AV} - V_{AC}|) \times (10V) / V \times \frac{2^N}{V_{AREF}}$$

EQ 4

where

- N is the number of bits
- V_{AREF} is the Reference voltage
- V_{AV} is the voltage at AV pad
- V_{AC} is the voltage at AC pad

Gate Driver

The Fusion Analog Quad includes a Gate Driver connected to the Quad's AG pin (Figure 2-74). Designed to work with external p- or n-channel MOSFETs, the Gate driver is a configurable current sink or source and requires an external pull-up or pull-down resistor. The AG supports 4 selectable gate drive levels: 1 μ A, 3 μ A, 10 μ A, and 30 μ A (Figure 2-75 on page 2-91). The AG also supports a High Current Drive mode in which it can sink 20 mA; in this mode the switching rate is approximately 1.3 MHz with 100 ns turn-on time and 600 ns turn-off time. Modeled on an open-drain-style output, it does not output a voltage level without an appropriate pull-up or pull-down resistor. If 1 V is forced on the drain, the current sinking/sourcing will exceed the ability of the transistor, and the device could be damaged.

The AG pad is turned on via the corresponding GDONx pin in the Analog Block macro, where x is the number of the corresponding Analog Quad for the AG pad to be enabled (GDON0 to GDON9).



Figure 2-74 • Gate Driver

The gate-to-source voltage (V_{gs}) of the external MOSFET is limited to the programmable drive current times the external pull-up or pull-down resistor value (EQ 5).

$$V_{gs} \leq I_g \times (R_{pullup} \text{ or } R_{pulldown})$$

EQ 5

The rate at which the gate voltage of the external MOSFET slews is determined by the current, I_g , sourced or sunk by the AG pin and the gate-to-source capacitance, C_{GS} , of the external MOSFET. As an approximation, the slew rate is given by EQ 6.

$$dv/dt = I_g / C_{GS}$$

EQ 6

C_{GS} is not a fixed capacitance but, depending on the circuitry connected to its drain terminal, can vary significantly during the course of a turn-on or turn-off transient. Thus, EQ 6 on page 2-91 can only be used for a first-order estimate of the switching speed of the external MOSFET.



Figure 2-75 • Gate Driver Example

Temperature Monitor

The final pin in the Analog Quad is the Analog Temperature (AT) pin. The AT pin is used to implement an accurate temperature monitor in conjunction with an external diode-connected bipolar transistor (Figure 2-76). For improved temperature measurement accuracy, it is important to use the ATRTN pin for the return path of the current sourced by the AT pin. Each ATRTN pin is shared between two adjacent Analog Quads. Additionally, if not used for temperature monitoring, the AT pin can provide functionality similar to that of the AV pad. However, in this mode only positive voltages can be applied to the AT pin, and only two prescaler factors are available (16 V and 4 V ranges—refer to Table 2-57 on page 2-130).



Figure 2-76 • Temperature Monitor Quad

Fusion uses a remote diode as a temperature sensor. The Fusion Temperature Monitor uses a differential input; the AT pin and ATRTN (AT Return) pin are the differential inputs to the Temperature Monitor. There is one Temperature Monitor in each Quad. A simplified block diagram is shown in Figure 2-77.



Figure 2-77 • Block Diagram for Temperature Monitor Circuit

The Fusion approach to measuring temperature is forcing two different currents through the diode with a ratio of 10:1. The switch that controls the different currents is controlled by the Temperature Monitor Strobe signal, TMSTB. Setting TMSTB to '1' will initiate a Temperature reading. The TMSTB should remain '1' until the ADC finishes sampling the voltage from the Temperature Monitor. The minimum sample time for the Temperature Monitor cannot be less than the minimum strobe high time minus the setup time. Figure 2-78 shows the timing diagram.



Figure 2-78 • Timing Diagram for the Temperature Monitor Strobe Signal

Note: When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 µA sink into the Fusion device.

The diode's voltage is measured at each current level and the temperature is calculated based on EQ 7.

$$V_{TMSLO} - V_{TMSHI} = n \frac{kT}{q} \left(\ln \frac{I_{TMSLO}}{I_{TMSHI}} \right)$$

EQ 7

where

I_{TMSLO} is the current when the Temperature Strobe is Low, typically 100 μ A

I_{TMSHI} is the current when the Temperature Strobe is High, typically 10 μ A

V_{TMSLO} is diode voltage while Temperature Strobe is Low

V_{TMSHI} is diode voltage while Temperature Strobe is High

n is the non-ideality factor of the diode-connected transistor. It is typically 1.004 for the Microsemi-recommended transistor type 2N3904.

$K = 1.3806 \times 10^{-23}$ J/K is the Boltzman constant

$Q = 1.602 \times 10^{-19}$ C is the charge of a proton

When $I_{TMSLO} / I_{TMSHI} = 10$, the equation can be simplified as shown in EQ 8.

$$\Delta V = V_{TMSLO} - V_{TMSHI} = 1.986 \times 10^{-4} nT$$

EQ 8

In the Fusion TMB, the ideality factor n for 2N3904 is 1.004 and ΔV is amplified 12.5 times by an internal amplifier; hence the voltage before entering the ADC is as given in EQ 9.

$$V_{ADC} = \Delta V \times 12.5 = 2.5 \text{ mV} / (K \times T)$$

EQ 9

This means the temperature to voltage relationship is 2.5 mV per degree Kelvin. The unique design of Fusion has made the Temperature Monitor System simple for the user. When the 10-bit mode ADC is used, each LSB represents 1 degree Kelvin, as shown in EQ 10. That is, e. 25°C is equal to 293°K and is represented by decimal 293 counts from the ADC.

$$1K = 2.5 \text{ mV} \times \frac{2^{10}}{2.56 \text{ V}} = 1 \text{ LSB}$$

EQ 10

If 8-bit mode is used for the ADC resolution, each LSB represents 4 degrees Kelvin; however, the resolution remains as 1 degree Kelvin per LSB, even for 12-bit mode, due to the Temperature Monitor design. An example of the temperature data format for 10-bit mode is shown in Table 2-38.

Table 2-38 • Temperature Data Format

| Temperature | Temperature (K) | Digital Output (ADC 10-bit mode) |
|-------------|-----------------|----------------------------------|
| -40°C | 233 | 00 1110 1001 |
| -20°C | 253 | 00 1111 1101 |
| 0°C | 273 | 01 0001 0001 |
| 1°C | 274 | 01 0001 0010 |
| 10 °C | 283 | 01 0001 1011 |
| 25°C | 298 | 01 0010 1010 |
| 50 °C | 323 | 01 0100 0011 |
| 85 °C | 358 | 01 0110 0110 |

Terminology

Resolution

Resolution defines the smallest temperature change Fusion Temperature Monitor can resolve. For ADC configured as 8-bit mode, each LSB represents 4°C, and 1°C per LSB for 10-bit mode. With 12-bit mode, the Temperature Monitor can still only resolve 1°C due to Temperature Monitor design.

Offset

The Fusion Temperature Monitor has a systematic offset ([Table 2-49 on page 2-117](#)), excluding error due to board resistance and ideality factor of the external diode. Microsemi provides an IP block (CalibIP) that is required in order to mitigate the systematic temperature offset. For further details on CalibIP, refer to the “*Temperature, Voltage, and Current Calibration in Fusion FPGAs*” chapter of the [Fusion FPGA Fabric User Guide](#).

Analog-to-Digital Converter Block

At the heart of the Fusion analog system is a programmable Successive Approximation Register (SAR) ADC. The ADC can support 8-, 10-, or 12-bit modes of operation. In 12-bit mode, the ADC can resolve 500 kbps. All results are MSB-justified in the ADC. The input to the ADC is a large 32:1 analog input multiplexer. A simplified block diagram of the Analog Quads, analog input multiplexer, and ADC is shown in Figure 2-79. The ADC offers multiple self-calibrating modes to ensure consistent high performance both at power-up and during runtime.



Figure 2-79 • ADC Block Diagram

ADC Description

The Fusion ADC is a 12-bit SAR ADC. It offers a wide variety of features for different use models. Figure 2-80 shows a block diagram of the Fusion ADC.

- Configurable resolution: 8-bit, 10-bit, and 12-bit mode
- DNL: 0.6 LSB for 10-bit mode
- INL: 0.4 LSB for 10-bit mode
- No missing code
- Internal VAREF = 2.56 V
- Maximum Sample Rate = 600 Ksps
- Power-up calibration and dynamic calibration after every sample to compensate for temperature drift over time

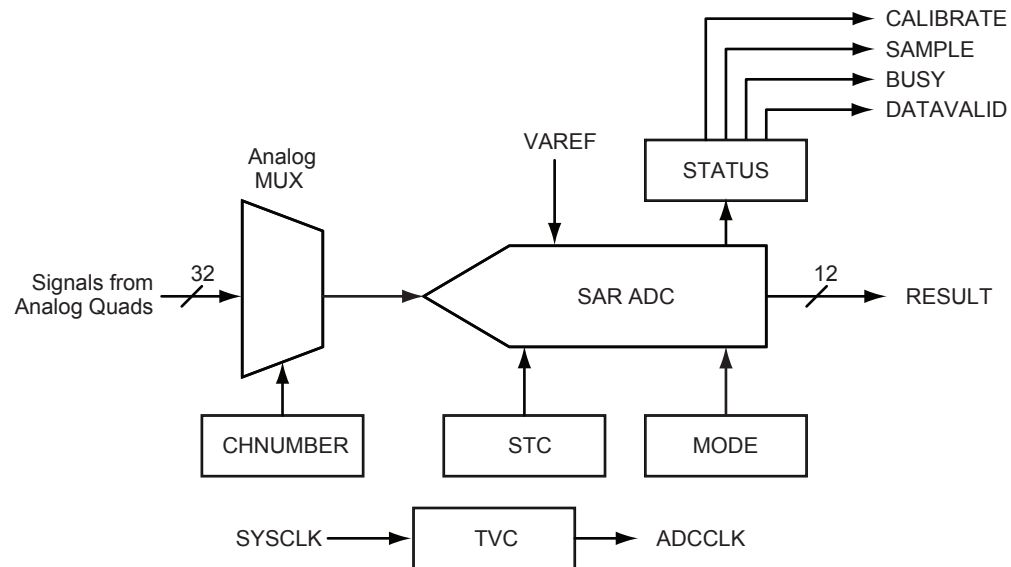


Figure 2-80 • ADC Simplified Block Diagram

ADC Theory of Operation

An analog-to-digital converter is used to capture discrete samples of a continuous analog voltage and provide a discrete binary representation of the signal. Analog-to-digital converters are generally characterized in three ways:

- Input voltage range
- Resolution
- Bandwidth or conversion rate

The input voltage range of an ADC is determined by its reference voltage (VREF). Fusion devices include an internal 2.56 V reference, or the user can supply an external reference of up to 3.3 V. The following examples use the internal 2.56 V reference, so the full-scale input range of the ADC is 0 to 2.56 V.

The resolution (LSB) of the ADC is a function of the number of binary bits in the converter. The ADC approximates the value of the input voltage using 2^n steps, where n is the number of bits in the converter. Each step therefore represents $VREF / 2^n$ volts. In the case of the Fusion ADC configured for 12-bit operation, the LSB is $2.56 \text{ V} / 4096 = 0.625 \text{ mV}$.

Finally, bandwidth is an indication of the maximum number of conversions the ADC can perform each second. The bandwidth of an ADC is constrained by its architecture and several key performance characteristics.

There are several popular ADC architectures, each with advantages and limitations. The analog-to-digital converter in Fusion devices is a switched-capacitor Successive Approximation Register (SAR) ADC. It supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (ksp/s). Built-in bandgap circuitry offers 1% internal voltage reference accuracy or an external reference voltage can be used.

As shown in Figure 2-81, a SAR ADC contains N capacitors with binary-weighted values.

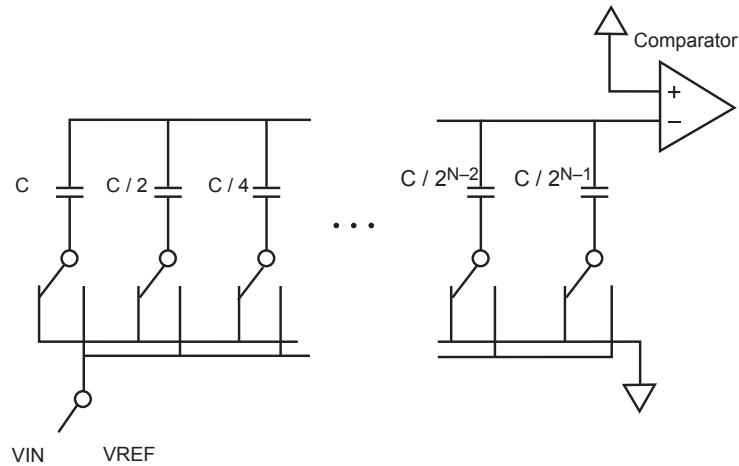


Figure 2-81 • Example SAR ADC Architecture

To begin a conversion, all of the capacitors are quickly discharged. Then VIN is applied to all the capacitors for a period of time (acquisition time) during which the capacitors are charged to a value very close to VIN. Then all of the capacitors are switched to ground, and thus $-VIN$ is applied across the comparator. Now the conversion process begins. First, C is switched to VREF. Because of the binary weighting of the capacitors, the voltage at the input of the comparator is then shown by EQ 11.

$$\text{Voltage at input of comparator} = -VIN + VREF / 2$$

EQ 11

If VIN is greater than $VREF / 2$, the output of the comparator is 1; otherwise, the comparator output is 0. A register is clocked to retain this value as the MSB of the result. Next, if the MSB is 0, C is switched back to ground; otherwise, it remains connected to VREF, and C / 2 is connected to VREF. The result at the comparator input is now either $-VIN + VREF / 4$ or $-VIN + 3 VREF / 4$ (depending on the state of the MSB), and the comparator output now indicates the value of the next most significant bit. This bit is likewise registered, and the process continues for each subsequent bit until a conversion is completed. The conversion process requires some acquisition time plus N + 1 ADC clock cycles to complete.

This process results in a binary approximation of VIN. Generally, there is a fixed interval T, the sampling period, between the samples. The inverse of the sampling period is often referred to as the sampling frequency $f_S = 1 / T$. The combined effect is illustrated in Figure 2-82.



Figure 2-82 • Conversion Example

Figure 2-82 demonstrates that if the signal changes faster than the sampling rate can accommodate, or if the actual value of VIN falls between counts in the result, this information is lost during the conversion. There are several techniques that can be used to address these issues.

First, the sampling rate must be chosen to provide enough samples to adequately represent the input signal. Based on the Nyquist-Shannon Sampling Theorem, the minimum sampling rate must be at least twice the frequency of the highest frequency component in the target signal (Nyquist Frequency). For example, to recreate the frequency content of an audio signal with up to 22 KHz bandwidth, the user must sample it at a minimum of 44 ksps. However, as shown in Figure 2-82, significant post-processing of the data is required to interpolate the value of the waveform during the time between each sample.

Similarly, to re-create the amplitude variation of a signal, the signal must be sampled with adequate resolution. Continuing with the audio example, the dynamic range of the human ear (the ratio of the amplitude of the threshold of hearing to the threshold of pain) is generally accepted to be 135 dB, and the dynamic range of a typical symphony orchestra performance is around 85 dB. Most commercial recording media provide about 96 dB of dynamic range using 16-bit sample resolution. But 16-bit fidelity does not necessarily mean that you need a 16-bit ADC. As long as the input is sampled at or above the Nyquist Frequency, post-processing techniques can be used to interpolate intermediate values and reconstruct the original input signal to within desired tolerances.

If sophisticated digital signal processing (DSP) capabilities are available, the best results are obtained by implementing a reconstruction filter, which is used to interpolate many intermediate values with higher resolution than the original data. Interpolating many intermediate values increases the effective number of samples, and higher resolution increases the effective number of bits in the sample. In many cases, however, it is not cost-effective or necessary to implement such a sophisticated reconstruction algorithm. For applications that do not require extremely fine reproduction of the input signal, alternative methods can enhance digital sampling results with relatively simple post-processing. The details of such techniques are out of the scope of this chapter; refer to the [Improving ADC Results through Oversampling and Post-Processing of Data](#) white paper for more information.

ADC Terminology

Conversion Time

Conversion time is the interval between the release of the hold state (imposed by the input circuitry of a track-and-hold) and the instant at which the voltage on the sampling capacitor settles to within one LSB of a new input value.

DNL – Differential Non-Linearity

For an ideal ADC, the analog-input levels that trigger any two successive output codes should differ by one LSB (DNL = 0). Any deviation from one LSB is defined as DNL (Figure 2-83).

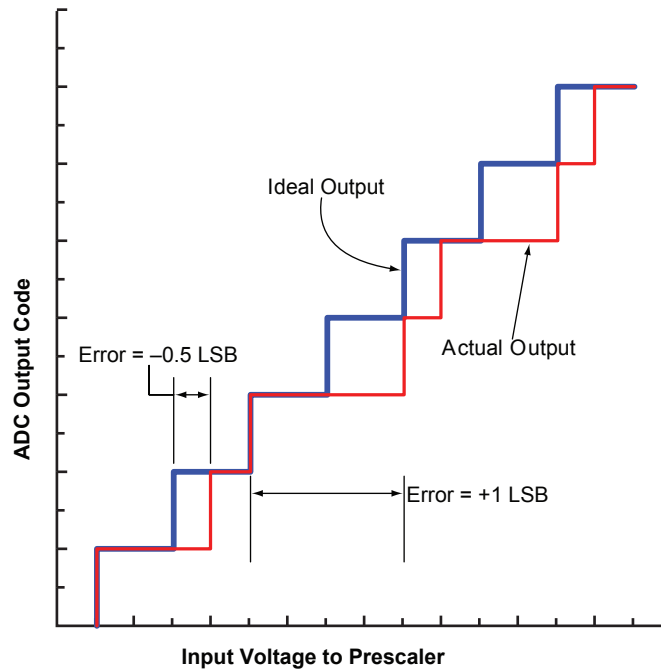


Figure 2-83 • Differential Non-Linearity (DNL)

ENOB – Effective Number of Bits

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists only of quantization of noise. As the input frequency increases, the overall noise (particularly in the distortion components) also increases, thereby reducing the ENOB and SINAD (also see "Signal-to-Noise and Distortion Ratio (SINAD)"). ENOB for a full-scale, sinusoidal input waveform is computed using EQ 12.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

EQ 12

FS Error – Full-Scale Error

Full-scale error is the difference between the actual value that triggers that transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error.

Gain Error

The gain error of an ADC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale (%FSR). Gain error is the full-scale error minus the offset error (Figure 2-84).



Figure 2-84 • Gain Error

Gain Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.

INL – Integral Non-Linearity

INL is the deviation of an actual transfer function from a straight line. After nullifying offset and gain errors, the straight line is either a best-fit straight line or a line drawn between the end points of the transfer function (Figure 2-85).



Figure 2-85 • Integral Non-Linearity (INL)

LSB – Least Significant Bit

In a binary number, the LSB is the least weighted bit in the group. Typically, the LSB is the furthest right bit. For an ADC, the weight of an LSB equals the full-scale voltage range of the converter divided by 2^N , where N is the converter's resolution.

EQ 13 shows the calculation for a 10-bit ADC with a unipolar full-scale voltage of 2.56 V:

$$1 \text{ LSB} = (2.56 \text{ V} / 2^{10}) = 2.5 \text{ mV}$$

EQ 13

No Missing Codes

An ADC has no missing codes if it produces all possible digital codes in response to a ramp signal applied to the analog input.

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. For an ideal ADC, the first transition occurs at 0.5 LSB above zero. The offset voltage is measured by applying an analog input such that the ADC outputs all zeroes and increases until the first transition occurs (Figure 2-86).



Figure 2-86 • Offset Error

Resolution

ADC resolution is the number of bits used to represent an analog input signal. To more accurately replicate the analog signal, resolution needs to be increased.

Sampling Rate

Sampling rate or sample frequency, specified in samples per second (sps), is the rate at which an ADC acquires (samples) the analog input.

SNR – Signal-to-Noise Ratio

SNR is the ratio of the amplitude of the desired signal to the amplitude of the noise signals at a given point in time. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR (EQ 14) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum ADC noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[Max]} = 6.02_{dB} \times N + 1.76_{dB}$$

EQ 14

SINAD – Signal-to-Noise and Distortion

SINAD is the ratio of the rms amplitude to the mean value of the root-sum-square of the all other spectral components, including harmonics, but excluding DC. SINAD is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion.

Total Harmonic Distortion

THD measures the distortion content of a signal, and is specified in decibels relative to the carrier (dBc). THD is the ratio of the RMS sum of the selected harmonics of the input signal to the fundamental itself. Only harmonics within the Nyquist limit are included in the measurement.

TUE – Total Unadjusted Error

TUE is a comprehensive specification that includes linearity errors, gain error, and offset error. It is the worst-case deviation from the ideal device performance. TUE is a static specification (Figure 2-87).



Figure 2-87 • Total Unadjusted Error (TUE)

ADC Operation

Once the ADC has powered up and been released from reset, ADCRESET, the ADC will initiate a calibration routine designed to provide optimal ADC performance. The Fusion ADC offers a robust calibration scheme to reduce integrated offset and linearity errors. The offset and linearity errors of the main capacitor array are compensated for with an 8-bit calibration capacitor array. The offset/linearity error calibration is carried out in two ways. First, a power-up calibration is carried out when the ADC comes out of reset. This is initiated by the CALIBRATE output of the Analog Block macro and is a fixed number of ADC_CLK cycles (3,840 cycles), as shown in Figure 2-89 on page 2-111. In this mode, the linearity and offset errors of the capacitors are calibrated.

To further compensate for drift and temperature-dependent effects, every conversion is followed by post-calibration of either the offset or a bit of the main capacitor array. The post-calibration ensures that, over time and with temperature, the ADC remains consistent.

After both calibration and the setting of the appropriate configurations, as explained above, the ADC is ready for operation. Setting the ADCSTART signal high for one clock period will initiate the sample and conversion of the analog signal on the channel as configured by CHNUMBER[4:0]. The status signals SAMPLE and BUSY will show when the ADC is sampling and converting (Figure 2-91 on page 2-112). Both SAMPLE and BUSY will initially go high. After the ADC has sampled and held the analog signal, SAMPLE will go low. After the entire operation has completed and the analog signal is converted, BUSY will go low and DATAVALID will go high. This indicates that the digital result is available on the RESULT[11:0] pins.

DATAVALID will remain high until a subsequent ADCSTART is issued. The DATAVALID goes low on the rising edge of SYSCLK as shown in Figure 2-90 on page 2-112. The RESULT signals will be kept constant until the ADC finishes the subsequent sample. The next sampled RESULT will be available when DATAVALID goes high again. It is ideal to read the RESULT when DATAVALID is '1'. The RESULT is latched and remains unchanged until the next DATAVALID rising edge.

ADC Input Multiplexer

At the input to the Fusion ADC is a 32:1 multiplexer. Of the 32 input channels, up to 30 are user definable. Two of these channels are hardwired internally. Channel 31 connects to an internal temperature diode so the temperature of the Fusion device itself can be monitored. Channel 0 is wired to the FPGA's 1.5 V VCC supply, enabling the Fusion device to monitor its own power supply. Doing this internally makes it unnecessary to use an analog I/O to support these functions. The balance of the MUX inputs are connected to Analog Quads (see the "Analog Quad" section on page 2-80). Table 2-40 defines which Analog Quad inputs are associated with which specific analog MUX channels. The number of Analog Quads present is device-dependent; refer to the family list in the "Fusion Family" table on page 1 of this datasheet for the number of quads per device. Regardless of the number of quads populated in a device, the internal connections to both VCC and the internal temperature diode remain on Channels 0 and 31, respectively. To sample the internal temperature monitor, it must be strobed (similar to the AT pads). The TMSTBINT pin on the Analog Block macro is the control for strobing the internal temperature measurement diode.

To determine which channel is selected for conversion, there is a five-pin interface on the Analog Block, CHNUMBER[4:0], defined in Table 2-39.

Table 2-39 • Channel Selection

| Channel Number | CHNUMBER[4:0] |
|----------------|---------------|
| 0 | 00000 |
| 1 | 00001 |
| 2 | 00010 |
| 3 | 00011 |
| · | · |
| · | · |
| · | · |
| 30 | 11110 |
| 31 | 11111 |

Table 2-40 shows the correlation between the analog MUX input channels and the analog input pins.

Table 2-40 • Analog MUX Channels

| Analog MUX Channel | Signal | Analog Quad Number |
|--------------------|------------|--------------------|
| 0 | Vcc_analog | |
| 1 | AV0 | Analog Quad 0 |
| 2 | AC0 | |
| 3 | AT0 | |
| 4 | AV1 | Analog Quad 1 |
| 5 | AC1 | |
| 6 | AT1 | |
| 7 | AV2 | Analog Quad 2 |
| 8 | AC2 | |
| 9 | AT2 | |
| 10 | AV3 | Analog Quad 3 |
| 11 | AC3 | |
| 12 | AT3 | |
| 13 | AV4 | Analog Quad 4 |
| 14 | AC4 | |
| 15 | AT4 | |

Table 2-40 • Analog MUX Channels (continued)

| Analog MUX Channel | Signal | Analog Quad Number |
|--------------------|------------------------------|--------------------|
| 16 | AV5 | Analog Quad 5 |
| 17 | AC5 | |
| 18 | AT5 | |
| 19 | AV6 | Analog Quad 6 |
| 20 | AC6 | |
| 21 | AT6 | |
| 22 | AV7 | Analog Quad 7 |
| 23 | AC7 | |
| 24 | AT7 | |
| 25 | AV8 | Analog Quad 8 |
| 26 | AC8 | |
| 27 | AT8 | |
| 28 | AV9 | Analog Quad 9 |
| 29 | AC9 | |
| 30 | AT9 | |
| 31 | Internal temperature monitor | |

The ADC can be powered down independently of the FPGA core, as an additional control or for power-saving considerations, via the PWRDWN pin of the Analog Block. The PWRDWN pin controls only the comparators in the ADC.

ADC Modes

The Fusion ADC can be configured to operate in 8-, 10-, or 12-bit modes, power-down after conversion, and dynamic calibration. This is controlled by MODE[3:0], as defined in [Table 2-41 on page 2-106](#).

The output of the ADC is the RESULT[11:0] signal. In 8-bit mode, the Most Significant 8 Bits RESULT[11:4] are used as the ADC value and the Least Significant 4 Bits RESULT[3:0] are logical '0's. In 10-bit mode, RESULT[11:2] are used the ADC value and RESULT[1:0] are logical 0s.

Table 2-41 • Mode Bits Function

| Name | Bits | Function |
|------|------|--|
| MODE | 3 | 0 – Internal calibration after every conversion; two ADCCLK cycles are used after the conversion. 1 – No calibration after every conversion |
| MODE | 2 | 0 – Power-down after conversion 1 – No Power-down after conversion |
| MODE | 1:0 | 00 – 10-bit 01 – 12-bit 10 – 8-bit 11 – Unused |

Integrated Voltage Reference

The Fusion device has an integrated on-chip 2.56 V reference voltage for the ADC. The value of this reference voltage was chosen to make the prescaling and postsaling factors for the prescaler blocks change in a binary fashion. However, if desired, an external reference voltage of up to 3.3 V can be connected between the VAREF and ADCGNDREF pins. The VAREFSEL control pin is used to select the reference voltage.

Table 2-42 • VAREF Bit Function

| Name | Bit | Function |
|-------|-----|--|
| VAREF | 0 | Reference voltage selection 0 – Internal voltage reference selected. VAREF pin outputs 2.56 V. 1 – Input external voltage reference from VAREF and ADCGNDREF |

ADC Clock

The speed of the ADC depends on its internal clock, ADCCLK, which is not accessible to users. The ADCCLK is derived from SYSCLK. Input signal TVC[7:0], Time Divider Control, determines the speed of the ADCCLK in relationship to SYSCLK, based on EQ 15.

$$t_{\text{ADCCLK}} = 4 \times (1 + \text{TVC}) \times t_{\text{SYSCLK}}$$

EQ 15

TVC: Time Divider Control (0–255)

t_{ADCCLK} is the period of ADCCLK, and must be between 0.5 MHz and 10 MHz

t_{SYSCLK} is the period of SYSCLK

Table 2-43 • TVC Bits Function

| Name | Bits | Function |
|------|-------|------------------------|
| TVC | [7:0] | SYSCLK divider control |

The frequency of ADCCLK, f_{ADCCLK} , must be within 0.5 Hz to 10 MHz.

The inputs to the ADC are synchronized to SYSCLK. A conversion is initiated by asserting the ADCSTART signal on a rising edge of SYSCLK. Figure 2-90 on page 2-112 and Figure 2-91 on page 2-112 show the timing diagram for the ADC.

Acquisition Time or Sample Time Control

Acquisition time (t_{SAMPLE}) specifies how long an analog input signal has to charge the internal capacitor array. Figure 2-88 shows a simplified internal input sampling mechanism of a SAR ADC.

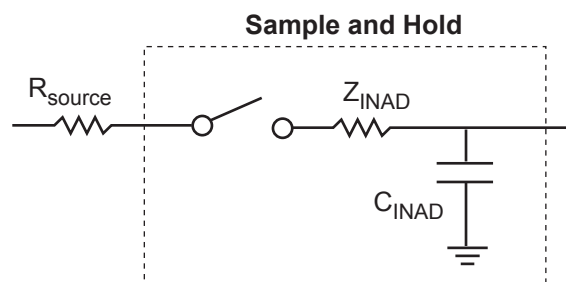


Figure 2-88 • Simplified Sample and Hold Circuitry

The internal impedance (Z_{INAD}), external source resistance (R_{SOURCE}), and sample capacitor (C_{INAD}) form a simple RC network. As a result, the accuracy of the ADC can be affected if the ADC is given insufficient time to charge the capacitor. To resolve this problem, you can either reduce the source resistance or increase the sampling time by changing the acquisition time using the STC signal.

EQ 16 through EQ 18 can be used to calculate the acquisition time required for a given input. The STC signal gives the number of sample periods in ADCCLK for the acquisition time of the desired signal. If the actual acquisition time is higher than the STC value, the settling time error can affect the accuracy of the ADC, because the sampling capacitor is only partially charged within the given sampling cycle. Example acquisition times are given in Table 2-44 and Table 2-45. When controlling the sample time for the ADC along with the use of the active bipolar prescaler, current monitor, or temperature monitor, the minimum sample time(s) for each must be obeyed. EQ 19 can be used to determine the appropriate value of STC.

You can calculate the minimum actual acquisition time by using EQ 16:

$$V_{OUT} = V_{IN}(1 - e^{-t/RC})$$

EQ 16

For 0.5 LSB gain error, V_{OUT} should be replaced with $(V_{IN} - (0.5 \times \text{LSB Value}))$:

$$(V_{IN} - 0.5 \times \text{LSB Value}) = V_{IN}(1 - e^{-t/RC})$$

EQ 17

where V_{IN} is the ADC reference voltage (V_{REF})

Solving EQ 17:

$$t = RC \times \ln(V_{IN} / (0.5 \times \text{LSB Value}))$$

EQ 18

where $R = Z_{INAD} + R_{SOURCE}$ and $C = C_{INAD}$.

Calculate the value of STC by using EQ 19.

$$t_{SAMPLE} = (2 + \text{STC}) \times (1 / \text{ADCCLK}) \text{ or } t_{SAMPLE} = (2 + \text{STC}) \times (\text{ADC Clock Period})$$

EQ 19

where ADCCLK = ADC clock frequency in MHz.

$t_{SAMPLE} = 0.449 \mu\text{s}$ from bit resolution in Table 2-44.

ADC Clock frequency = 10 MHz or a 100 ns period.

$\text{STC} = (t_{SAMPLE} / (1 / 10 \text{ MHz})) - 2 = 4.49 - 2 = 2.49$.

You must round up to 3 to accommodate the minimum sample time.

Table 2-44 • Acquisition Time Example with $V_{AREF} = 2.56 \text{ V}$

| VIN = 2.56V, R = 4K (R _{SOURCE} ~ 0), C = 18 pF | | |
|--|----------------|--|
| Resolution | LSB Value (mV) | Min. Sample/Hold Time for 0.5 LSB (μs) |
| 8 | 10 | 0.449 |
| 10 | 2.5 | 0.549 |
| 12 | 0.625 | 0.649 |

Table 2-45 • Acquisition Time Example with $V_{AREF} = 3.3 \text{ V}$

| VIN = 3.3V, R = 4K (R _{SOURCE} ~ 0), C = 18 pF | | |
|---|----------------|--|
| Resolution | LSB Value (mV) | Min. Sample/Hold time for 0.5 LSB (μs) |
| 8 | 12.891 | 0.449 |
| 10 | 3.223 | 0.549 |
| 12 | 0.806 | 0.649 |

Sample Phase

A conversion is performed in three phases. In the first phase, the analog input voltage is sampled on the input capacitor. This phase is called sample phase. During the sample phase, the output signals BUSY and SAMPLE change from '0' to '1', indicating the ADC is busy and sampling the analog signal. The sample time can be controlled by input signals STC[7:0]. The sample time can be calculated by EQ 20. When controlling the sample time for the ADC along with the use of Prescaler or Current Monitor or Temperature Monitor, the minimum sample time for each must be obeyed.

Refer to [Table 2-46](#) on [page 2-109](#) and the "Acquisition Time or Sample Time Control" section on [page 2-107](#)

$$t_{\text{sample}} = (2 + \text{STC}) \times t_{\text{ADCCLK}}$$

EQ 20

STC: Sample Time Control value (0–255)

t_{SAMPLE} is the sample time

Table 2-46 • STC Bits Function

| Name | Bits | Function |
|------|-------|---------------------|
| STC | [7:0] | Sample time control |

Sample time is computed based on the period of ADCCLK.

Distribution Phase

The second phase is called the distribution phase. During distribution phase, the ADC computes the equivalent digital value from the value stored in the input capacitor. In this phase, the output signal SAMPLE goes back to '0', indicating the sample is completed; but the BUSY signal remains '1', indicating the ADC is still busy for distribution. The distribution time depends strictly on the number of bits. If the ADC is configured as a 10-bit ADC, then 10 ADCCLK cycles are needed. [EQ 8](#) describes the distribution time.

$$t_{\text{distrib}} = N \times t_{\text{ADCCLK}}$$

EQ 21

N: Number of bits

Post-Calibration Phase

The last phase is the post-calibration phase. This is an optional phase. The post-calibration phase takes two ADCCLK cycles. The output BUSY signal will remain '1' until the post-calibration phase is completed. If the post-calibration phase is skipped, then the BUSY signal goes to '0' after distribution phase. As soon as BUSY signal goes to '0', the DATAVALID signal goes to '1', indicating the digital result is available on the RESULT output signals. DATAVALID will remain '1' until the next ADCSTART is asserted. Microsemi recommends enabling post-calibration to compensate for drift and temperature-dependent effects. This ensures that the ADC remains consistent over time and with temperature. The post-calibration phase is enabled by bit 3 of the Mode register. [EQ 9](#) describes the post-calibration time.

$$t_{\text{post-cal}} = \text{MODE}[3] \times (2 \times t_{\text{ADCCLK}})$$

EQ 22

MODE[3]: Bit 3 of the Mode register, described in [Table 2-41](#) on [page 2-106](#).

The calculation for the conversion time for the ADC is summarized in [EQ 23](#).

$$t_{\text{conv}} = t_{\text{sync_read}} + t_{\text{sample}} + t_{\text{distrib}} + t_{\text{post-cal}} + t_{\text{sync_write}}$$

EQ 23

t_{conv} : conversion time

$t_{\text{sync_read}}$: maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, t_{SYSCLK} .

t_{sample} : Sample time

t_{distrib} : Distribution time

$t_{\text{post-cal}}$: Post-calibration time

$t_{\text{sync_write}}$: Maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, t_{SYSCLK} .

Intra-Conversion

Performing a conversion during power-up calibration is possible but should be avoided, since the performance is not guaranteed, as shown in [Table 2-49 on page 2-117](#). This is described as intra-conversion. [Figure 2-92 on page 2-113](#) shows intra-conversion, (conversion that starts during power-up calibration).

Injected Conversion

A conversion can be interrupted by another conversion. Before the current conversion is finished, a second conversion can be started by issuing a pulse on signal ADCSTART. When a second conversion is issued before the current conversion is completed, the current conversion would be dropped and the ADC would start the second conversion on the rising edge of the SYSCLK. This is known as injected conversion. Since the ADC is synchronous, the minimum time to issue a second conversion is two clock cycles of SYSCLK after the previous one. [Figure 2-93 on page 2-113](#) shows injected conversion, (conversion that starts before a previously started conversion is finished). The total time for calibration still remains 3,840 ADCCLK cycles.

ADC Example

This example shows how to choose the correct settings to achieve the fastest sample time in 10-bit mode for a system that runs at 66 MHz. Assume the acquisition times defined in [Table 2-44 on page 2-108](#) for 10-bit mode, which gives 0.549 μs as a minimum hold time.

The period of SYSCLK: $t_{\text{SYSCLK}} = 1/66 \text{ MHz} = 0.015 \mu\text{s}$

Choosing TVC between 1 and 33 will meet the maximum and minimum period for the ADCCLK requirement. A higher TVC leads to a higher ADCCLK period.

The minimum TVC is chosen so that t_{distrib} and $t_{\text{post-cal}}$ can be run faster. The period of ADCCLK with a TVC of 1 can be computed by [EQ 24](#).

$$t_{\text{ADCCLK}} = 4 \times (1 + \text{TVC}) \times t_{\text{SYSCLK}} = 4 \times (1 + 1) \times 0.015 \mu\text{s} = 0.12 \mu\text{s}$$

EQ 24

The STC value can now be computed by using the minimum sample/hold time from [Table 2-44 on page 2-108](#), as shown in [EQ 25](#).

$$\text{STC} = \frac{t_{\text{sample}}}{t_{\text{ADCCLK}}} - 2 = \frac{0.549 \mu\text{s}}{0.12 \mu\text{s}} - 2 = 4.575 - 2 = 2.575$$

EQ 25

You must round up to 3 to accommodate the minimum sample time requirement. The actual sample time, t_{sample} , with an STC of 3, is now equal to 0.6 μs , as shown in [EQ 26](#)

$$t_{\text{sample}} = (2 + \text{STC}) \times t_{\text{ADCCLK}} = (2 + 3) \times t_{\text{ADCCLK}} = 5 \times 0.12 \mu\text{s} = 0.6 \mu\text{s}$$

EQ 26

Microsemi recommends post-calibration for temperature drift over time, so post-calibration is enabled.

The post-calibration time, $t_{\text{post-cal}}$, can be computed by [EQ 27](#). The post-calibration time is 0.24 μs .

$$t_{\text{post-cal}} = 2 \times t_{\text{ADCCLK}} = 0.24 \mu\text{s}$$

EQ 27

The distribution time, t_{distrib} , is equal to 1.2 μs and can be computed as shown in [EQ 28](#) (N is number of bits, referring back to [EQ 8 on page 2-94](#)).

$$t_{\text{distrib}} = N \times t_{\text{ADCCLK}} = 10 \times 0.12 = 1.2 \mu\text{s}$$

EQ 28

The total conversion time can now be summated, as shown in [EQ 29](#) (referring to [EQ 23 on page 2-109](#)).

$$t_{\text{sync_read}} + t_{\text{sample}} + t_{\text{distrib}} + t_{\text{post-cal}} + t_{\text{sync_write}} = (0.015 + 0.60 + 1.2 + 0.24 + 0.015) \mu\text{s} = 2.07 \mu\text{s}$$

EQ 29

The optimal setting for the system running at 66 MHz with an ADC for 10-bit mode chosen is shown in Table 2-47:

Table 2-47 • Optimal Setting at 66 MHz in 10-Bit Mode

| | | |
|-----------|----------|--------|
| TVC[7:0] | = 1 | = 0x01 |
| STC[7:0] | = 3 | = 0x03 |
| MODE[3:0] | = b'0100 | = 0x4* |

Note: No power-down after every conversion is chosen in this case; however, if the application is power-sensitive, the MODE[2] can be set to '0', as described above, and it will not affect any performance.

Timing Diagrams



Note: *Refer to EQ 15 on page 2-107 for the calculation on the period of ADCCLK, t_{ADCCLK} .

Figure 2-89 • Power-Up Calibration Status Signal Timing Diagram



Figure 2-90 • Input Setup Time

Standard Conversion



Notes:

1. Refer to EQ 20 on page 2-109 for the calculation on the sample time, t_{SAMPLE} .
2. See EQ 23 on page 2-109 for calculation of the conversion time, t_{CONV} .
3. Minimum time to issue an ADCSTART after DATAVALID is 1 SYSCLK period

Figure 2-91 • Standard Conversion Status Signal Timing Diagram

Intra-Conversion



Note: t_{CONV}^* represents the conversion time of the second conversion. See EQ 23 on page 2-109 for calculation of the conversion time, t_{CONV} .

Figure 2-92 • Intra-Conversion Timing Diagram

Injected Conversion



Note: *See EQ 23 on page 2-109 for calculation on the conversion time, t_{CONV} .

Figure 2-93 • Injected Conversion Timing Diagram

ADC Interface Timing

Table 2-48 • ADC Interface Timing
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|-------------------|--|--------|--------|--------|-------|
| t_{SUMODE} | Mode Pin Setup Time | 0.56 | 0.64 | 0.75 | ns |
| t_{HDMODE} | Mode Pin Hold Time | 0.26 | 0.29 | 0.34 | ns |
| t_{SUTVC} | Clock Divide Control (TVC) Setup Time | 0.68 | 0.77 | 0.90 | ns |
| t_{HDTVC} | Clock Divide Control (TVC) Hold Time | 0.32 | 0.36 | 0.43 | ns |
| t_{SUSTC} | Sample Time Control (STC) Setup Time | 1.58 | 1.79 | 2.11 | ns |
| t_{HDSTC} | Sample Time Control (STC) Hold Time | 1.27 | 1.45 | 1.71 | ns |
| $t_{SUVAREFSEL}$ | Voltage Reference Select (VAREFSEL) Setup Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{HDVAREFSEL}$ | Voltage Reference Select (VAREFSEL) Hold Time | 0.67 | 0.76 | 0.89 | ns |
| $t_{SUCHNUM}$ | Channel Select (CHNUMBER) Setup Time | 0.90 | 1.03 | 1.21 | ns |
| $t_{HDCHNUM}$ | Channel Select (CHNUMBER) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUADCSTART}$ | Start of Conversion (ADCSTART) Setup Time | 0.75 | 0.85 | 1.00 | ns |
| $t_{HDADCSTART}$ | Start of Conversion (ADCSTART) Hold Time | 0.43 | 0.49 | 0.57 | ns |
| $t_{CK2QBUSY}$ | Busy Clock-to-Q | 1.33 | 1.51 | 1.78 | ns |
| $t_{CK2QCAL}$ | Power-Up Calibration Clock-to-Q | 0.63 | 0.71 | 0.84 | ns |
| $t_{CK2QVAL}$ | Valid Conversion Result Clock-to-Q | 3.12 | 3.55 | 4.17 | ns |
| $t_{CK2QSAMPLE}$ | Sample Clock-to-Q | 0.22 | 0.25 | 0.30 | ns |
| $t_{CK2QRESULT}$ | Conversion Result Clock-to-Q | 2.53 | 2.89 | 3.39 | ns |
| $t_{CLR2QBUSY}$ | Busy Clear-to-Q | 2.06 | 2.35 | 2.76 | ns |
| $t_{CLR2QCAL}$ | Power-Up Calibration Clear-to-Q | 2.15 | 2.45 | 2.88 | ns |
| $t_{CLR2QVAL}$ | Valid Conversion Result Clear-to-Q | 2.41 | 2.74 | 3.22 | ns |
| $t_{CLR2QSAMPLE}$ | Sample Clear-to-Q | 2.17 | 2.48 | 2.91 | ns |
| $t_{CLR2QRESULT}$ | Conversion result Clear-to-Q | 2.25 | 2.56 | 3.01 | ns |
| t_{RECCLR} | Recovery Time of Clear | 0.00 | 0.00 | 0.00 | ns |
| t_{REMCLR} | Removal Time of Clear | 0.63 | 0.72 | 0.84 | ns |
| $t_{MPWSYSCLK}$ | Clock Minimum Pulse Width for the ADC | 4.00 | 4.00 | 4.00 | ns |
| $t_{FMAXSYSCLK}$ | Clock Maximum Frequency for the ADC | 100.00 | 100.00 | 100.00 | MHz |

Typical Performance Characteristics

Temperature Error vs. Die Temperature



Figure 2-94 • Temperature Error

Temperature Error vs. Interconnect Capacitance



Figure 2-95 • Effect of External Sensor Capacitance



Figure 2-96 • Temperature Reading Noise When Averaging is Used

Analog System Characteristics

Table 2-49 • Analog Channel Specifications
 Commercial Temperature Range Conditions, $T_J = 85^\circ\text{C}$ (unless noted otherwise),
 Typical: $V_{CC33A} = 3.3\text{ V}$, $V_{CC} = 1.5\text{ V}$

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|--|-------------------------------------|--|----------------|------|---|---------------|
| Voltage Monitor Using Analog Pads AV, AC and AT (using prescaler) | | | | | | |
| | Input Voltage (Prescaler) | Refer to Table 3-2 on page 3-3 | | | | |
| VINAP | Uncalibrated Gain and Offset Errors | Refer to Table 2-51 on page 2-122 | | | | |
| | Calibrated Gain and Offset Errors | Refer to Table 2-52 on page 2-123 | | | | |
| | Bandwidth ¹ | | | | 100 | KHz |
| | Input Resistance | Refer to Table 3-3 on page 3-4 | | | | |
| | Scaling Factor | Prescaler modes (Table 2-57 on page 2-130) | | | | |
| | Sample Time | | 10 | | | μs |
| Current Monitor Using Analog Pads AV and AC | | | | | | |
| VRSM ¹ | Maximum Differential Input Voltage | | | | VAREF / 10 | mV |
| | Resolution | Refer to "Current Monitor" section | | | | |
| | Common Mode Range | | | | - 10.5 to +12 | V |
| CMRR | Common Mode Rejection Ratio | DC – 1 KHz | | 60 | | dB |
| | | 1 KHz - 10 KHz | | 50 | | dB |
| | | > 10 KHz | | 30 | | dB |
| t_{CMSHI} | Strobe High time | | ADC conv. time | | 200 | μs |
| t_{CMSHI} | Strobe Low time | | 5 | | | μs |
| t_{CMSHI} | Settling time | | 0.02 | | | μs |
| | Accuracy | Input differential voltage > 50 mV | | | -2 –(0.05 x VRSM) to +2 + (0.05 x VRSM) | mV |

Notes:

1. VRSM is the maximum voltage drop across the current sense resistor.
2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.
3. VIND is limited to $V_{CC33A} + 0.2$ to allow reaching 10 MHz input frequency.
4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.
5. The temperature offset is a fixed positive value.
6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.

Table 2-49 • Analog Channel Specifications (continued)
 Commercial Temperature Range Conditions, $T_J = 85^\circ\text{C}$ (unless noted otherwise),
 Typical: $V_{CC33A} = 3.3\text{ V}$, $V_{CC} = 1.5\text{ V}$

| Parameter | Description | Condition | Min. | Typ. | Max. | Units | |
|--|--------------------------------|--|------|---------|---------|------------------|---------------|
| Temperature Monitor Using Analog Pad AT | | | | | | | |
| External Temperature Monitor (external diode 2N3904, $T_J = 25^\circ\text{C}$) ⁴ | Resolution | 8-bit ADC | | 4 | | $^\circ\text{C}$ | |
| | | 10-bit ADC | | 1 | | $^\circ\text{C}$ | |
| | | 12-bit ADC | | 0.25 | | $^\circ\text{C}$ | |
| | Systematic Offset ⁵ | AFS090, AFS250, AFS600, AFS1500, uncalibrated ⁷ | | 5 | | $^\circ\text{C}$ | |
| | | AFS090, AFS250, AFS600, AFS1500, calibrated ⁷ | | ± 5 | | $^\circ\text{C}$ | |
| | Accuracy | | | ± 3 | ± 5 | $^\circ\text{C}$ | |
| | External Sensor Source Current | High level, TMSTBx = 0 | | | 10 | | μA |
| | | Low level, TMSTBx = 1 | | | 100 | | μA |
| Max Capacitance on AT pad | | | | | 1.3 | nF | |
| Internal Temperature Monitor | Resolution | 8-bit ADC | 4 | | | $^\circ\text{C}$ | |
| | | 10-bit ADC | 1 | | | $^\circ\text{C}$ | |
| | | 12-bit ADC | 0.25 | | | $^\circ\text{C}$ | |
| | Systematic Offset ⁵ | AFS090 ⁷ | | 5 | | $^\circ\text{C}$ | |
| | | AFS250, AFS600, AFS1500 ⁷ | | 11 | | $^\circ\text{C}$ | |
| | Accuracy | | | ± 3 | ± 5 | $^\circ\text{C}$ | |
| t_{TMSHI} | Strobe High time | | 10 | | 105 | μs | |
| t_{TMSLO} | Strobe Low time | | 5 | | | μs | |
| t_{TMSSET} | Settling time | | 5 | | | μs | |

Notes:

1. V_{RSM} is the maximum voltage drop across the current sense resistor.
2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as V_{IND} does not exceed these limits.
3. V_{IND} is limited to $V_{\text{CC33A}} + 0.2$ to allow reaching 10 MHz input frequency.
4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.
5. The temperature offset is a fixed positive value.
6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the [Fusion FPGA Fabric User Guide](#).

Table 2-49 • Analog Channel Specifications (continued)
 Commercial Temperature Range Conditions, $T_J = 85^\circ\text{C}$ (unless noted otherwise),
 Typical: $V_{CC33A} = 3.3\text{ V}$, $V_{CC} = 1.5\text{ V}$

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|--|------------------------|--|------|------|------|-------|
| Digital Input using Analog Pads AV, AC and AT | | | | | | |
| VIND ^{2,3} | Input Voltage | Refer to Table 3-2 on page 3-3 | | | | |
| VHYSIN | Hysteresis | | | 0.3 | | V |
| VIHDIN | Input High | | | 1.2 | | V |
| VILDIN | Input Low | | | 0.9 | | V |
| VMPWDIN | Minimum Pulse Width | | 50 | | | ns |
| F _{DIN} | Maximum Frequency | | | | 10 | MHz |
| ISTBDIN | Input Leakage Current | | | 2 | | μA |
| IDYNDIN | Dynamic Current | | | 20 | | μA |
| t _{INDIN} | Input Delay | | | 10 | | ns |
| Gate Driver Output Using Analog Pad AG | | | | | | |
| VG | Voltage Range | Refer to Table 3-2 on page 3-3 | | | | |
| IG | Output Current Drive | High Current Mode ⁶ at 1.0 V | | | ±20 | mA |
| | | Low Current Mode: ±1 μA | 0.8 | 1.0 | 1.3 | μA |
| | | Low Current Mode: ±3 μA | 2.0 | 2.7 | 3.3 | μA |
| | | Low Current Mode: ±10 μA | 7.4 | 9.0 | 11.5 | μA |
| | | Low Current Mode: ±30 μA | 21.0 | 27.0 | 32.0 | μA |
| IOFFG | Maximum Off Current | | | | 100 | nA |
| F _G | Maximum switching rate | High Current Mode ⁶ at 1.0 V, 1 kΩ resistive load | | 1.3 | | MHz |
| | | Low Current Mode: ±1 μA, 3 MΩ resistive load | | 3 | | KHz |
| | | Low Current Mode: ±3 μA, 1 MΩ resistive load | | 7 | | KHz |
| | | Low Current Mode: ±10 μA, 300 kΩ resistive load | | 25 | | KHz |
| | | Low Current Mode: ±30 μA, 105 kΩ resistive load | | 78 | | KHz |

Notes:

1. *V_{RSM}* is the maximum voltage drop across the current sense resistor.
2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as *V_{IND}* does not exceed these limits.
3. *V_{IND}* is limited to $V_{CC33A} + 0.2$ to allow reaching 10 MHz input frequency.
4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.
5. The temperature offset is a fixed positive value.
6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the “Temperature, Voltage, and Current Calibration in Fusion FPGAs” chapter of the [Fusion FPGA Fabric User Guide](#).

Table 2-50 • ADC Characteristics in Direct Input Mode
 Commercial Temperature Range Conditions, $T_J = 85^\circ\text{C}$ (unless noted otherwise),
 Typical: $V_{CC33A} = 3.3\text{ V}$, $V_{CC} = 1.5\text{ V}$

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|--|--|-------|--------|--------------------|------------------------|
| Direct Input using Analog Pad AV, AC, AT | | | | | | |
| VINADC | Input Voltage (Direct Input) | Refer to Table 3-2 on page 3-3 | | | | |
| CINADC | Input Capacitance | Channel not selected | | 7 | | pF |
| | | Channel selected but not sampling | | 8 | | pF |
| | | Channel selected and sampling | | 18 | | pF |
| ZINADC | Input Impedance | 8-bit mode | | 2 | | k Ω |
| | | 10-bit mode | | 2 | | k Ω |
| | | 12-bit mode | | 2 | | k Ω |
| Analog Reference Voltage VAREF | | | | | | |
| VAREF | Accuracy | $T_J = 25^\circ\text{C}$ | 2.537 | 2.56 | 2.583 | V |
| | Temperature Drift of Internal Reference | | | 65 | | ppm / $^\circ\text{C}$ |
| | External Reference | | 2.527 | | $V_{CC33A} + 0.05$ | V |
| ADC Accuracy (using external reference) ^{1,2} | | | | | | |
| DC Accuracy | | | | | | |
| TUE | Total Unadjusted Error | 8-bit mode | | 0.29 | | LSB |
| | | 10-bit mode | | 0.72 | | LSB |
| | | 12-bit mode | | 1.8 | | LSB |
| INL | Integral Non-Linearity | 8-bit mode | | 0.20 | 0.25 | LSB |
| | | 10-bit mode | | 0.32 | 0.43 | LSB |
| | | 12-bit mode | | 1.71 | 1.80 | LSB |
| DNL | Differential Non-Linearity (no missing code) | 8-bit mode | | 0.20 | 0.24 | LSB |
| | | 10-bit mode | | 0.60 | 0.65 | LSB |
| | | 12-bit mode | | 2.40 | 2.48 | LSB |
| | Offset Error | 8-bit mode | | 0.01 | 0.17 | LSB |
| | | 10-bit mode | | 0.05 | 0.20 | LSB |
| | | 12-bit mode | | 0.20 | 0.40 | LSB |
| | Gain Error | 8-bit mode | | 0.0004 | 0.003 | LSB |
| | | 10-bit mode | | 0.002 | 0.011 | LSB |
| | | 12-bit mode | | 0.007 | 0.044 | LSB |
| | Gain Error (with internal reference) | All modes | | 2 | | % FSR |

Notes:

1. Accuracy of the external reference is $2.56\text{ V} \pm 4.6\text{ mV}$.
2. Data is based on characterization.
3. The sample rate is time-shared among active analog inputs.

Table 2-50 • ADC Characteristics in Direct Input Mode (continued)
 Commercial Temperature Range Conditions, $T_J = 85^\circ\text{C}$ (unless noted otherwise),
 Typical: $V_{CC33A} = 3.3\text{ V}$, $V_{CC} = 1.5\text{ V}$

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|----------------------------|----------------------------|-------------|------|-------|-------|---------------|
| Dynamic Performance | | | | | | |
| SNR | Signal-to-Noise Ratio | 8-bit mode | 48.0 | 49.5 | | dB |
| | | 10-bit mode | 58.0 | 60.0 | | dB |
| | | 12-bit mode | 62.9 | 64.5 | | dB |
| SINAD | Signal-to-Noise Distortion | 8-bit mode | 47.6 | 49.5 | | dB |
| | | 10-bit mode | 57.4 | 59.8 | | dB |
| | | 12-bit mode | 62.0 | 64.2 | | dB |
| THD | Total Harmonic Distortion | 8-bit mode | | -74.4 | -63.0 | dBc |
| | | 10-bit mode | | -78.3 | -63.0 | dBc |
| | | 12-bit mode | | -77.9 | -64.4 | dBc |
| ENOB | Effective Number of Bits | 8-bit mode | 7.6 | 7.9 | | bits |
| | | 10-bit mode | 9.5 | 9.6 | | bits |
| | | 12-bit mode | 10.0 | 10.4 | | bits |
| Conversion Rate | | | | | | |
| | Conversion Time | 8-bit mode | 1.7 | | | μs |
| | | 10-bit mode | 1.8 | | | μs |
| | | 12-bit mode | 2 | | | μs |
| | Sample Rate | 8-bit mode | | | 600 | Ksps |
| | | 10-bit mode | | | 550 | Ksps |
| | | 12-bit mode | | | 500 | Ksps |

Notes:

1. Accuracy of the external reference is $2.56\text{ V} \pm 4.6\text{ mV}$.
2. Data is based on characterization.
3. The sample rate is time-shared among active analog inputs.

Table 2-51 • Uncalibrated Analog Channel Accuracy*
Worst-Case Industrial Conditions, T_J = 85°C

| | | Total Channel Error (LSB) | | | Channel Input Offset Error (LSB) | | | Channel Input Offset Error (mV) | | | Channel Gain Error (%FSR) | | |
|-----------------------|---------------------|---------------------------|------|-----------|----------------------------------|------|-----------|---------------------------------|------|-----------|---------------------------|------|------|
| Analog Pad | Prescaler Range (V) | Neg. Max. | Med. | Pos. Max. | Neg. Max | Med. | Pos. Max. | Neg. Max. | Med. | Pos. Max. | Min. | Typ. | Max. |
| Positive Range | | ADC in 10-Bit Mode | | | | | | | | | | | |
| AV, AC | 16 | -22 | -2 | 12 | -11 | -2 | 14 | -169 | -32 | 224 | 3 | 0 | -3 |
| | 8 | -40 | -5 | 17 | -11 | -5 | 21 | -87 | -40 | 166 | 2 | 0 | -4 |
| | 4 | -45 | -9 | 24 | -16 | -11 | 36 | -63 | -43 | 144 | 2 | 0 | -4 |
| | 2 | -70 | -19 | 33 | -33 | -20 | 66 | -66 | -39 | 131 | 2 | 0 | -4 |
| | 1 | -25 | -7 | 5 | -11 | -3 | 26 | -11 | -3 | 26 | 3 | -1 | -3 |
| | 0.5 | -41 | -12 | 8 | -12 | -7 | 38 | -6 | -4 | 19 | 3 | -1 | -3 |
| | 0.25 | -53 | -14 | 19 | -20 | -14 | 40 | -5 | -3 | 10 | 5 | 0 | -4 |
| | 0.125 | -89 | -29 | 24 | -40 | -28 | 88 | -5 | -4 | 11 | 7 | 0 | -5 |
| AT | 16 | -3 | 9 | 15 | -4 | 0 | 4 | -64 | 5 | 64 | 1 | 0 | -1 |
| | 4 | -10 | 2 | 15 | -11 | -2 | 11 | -44 | -8 | 44 | 1 | 0 | -1 |
| Negative Range | | ADC in 10-Bit Mode | | | | | | | | | | | |
| AV, AC | 16 | -35 | -10 | 9 | -24 | -6 | 9 | -383 | -96 | 148 | 5 | -1 | -6 |
| | 8 | -65 | -19 | 12 | -34 | -12 | 9 | -268 | -99 | 75 | 5 | -1 | -5 |
| | 4 | -86 | -28 | 21 | -64 | -24 | 19 | -254 | -96 | 76 | 5 | -1 | -6 |
| | 2 | -136 | -53 | 37 | -115 | -42 | 39 | -230 | -83 | 78 | 6 | -2 | -7 |
| | 1 | -98 | -35 | 8 | -39 | -8 | 15 | -39 | -8 | 15 | 10 | -3 | -10 |
| | 0.5 | -121 | -46 | 7 | -54 | -14 | 18 | -27 | -7 | 9 | 10 | -4 | -11 |
| | 0.25 | -149 | -49 | 19 | -72 | -16 | 40 | -18 | -4 | 10 | 14 | -4 | -12 |
| | 0.125 | -188 | -67 | 38 | -112 | -27 | 56 | -14 | -3 | 7 | 16 | -5 | -14 |

Note: *Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Gain remains the same.

Table 2-52 • Calibrated Analog Channel Accuracy ^{1,2,3}
Worst-Case Industrial Conditions, T_J = 85°C

| | | Condition | Total Channel Error (LSB) | | |
|-----------------------|---------------------|--------------------------------|---------------------------|--------|---------------|
| Analog Pad | Prescaler Range (V) | Input Voltage ⁴ (V) | Negative Max. | Median | Positive Max. |
| Positive Range | | | ADC in 10-Bit Mode | | |
| AV, AC | 16 | 0.300 to 12.0 | -6 | 1 | 6 |
| | 8 | 0.250 to 8.00 | -6 | 0 | 6 |
| | 4 | 0.200 to 4.00 | -7 | -1 | 7 |
| | 2 | 0.150 to 2.00 | -7 | 0 | 7 |
| | 1 | 0.050 to 1.00 | -6 | -1 | 6 |
| AT | 16 | 0.300 to 16.0 | -5 | 0 | 5 |
| | 4 | 0.100 to 4.00 | -7 | -1 | 7 |
| Negative Range | | | ADC in 10-Bit Mode | | |
| AV, AC | 16 | -0.400 to -10.5 | -7 | 1 | 9 |
| | 8 | -0.350 to -8.00 | -7 | -1 | 7 |
| | 4 | -0.300 to -4.00 | -7 | -2 | 9 |
| | 2 | -0.250 to -2.00 | -7 | -2 | 7 |
| | 1 | -0.050 to -1.00 | -16 | -1 | 20 |

Notes:

1. Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Overall accuracy remains the same.
2. Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the [Fusion FPGA Fabric User Guide](#).
3. Calibrated with two-point calibration methodology, using 20% and 80% full-scale points.
4. The lower limit of the input voltage is determined by the prescaler input offset.

Table 2-53 • Analog Channel Accuracy: Monitoring Standard Positive Voltages
 Typical Conditions, T_A = 25°C

| Input Voltage (V) | Calibrated Typical Error per Positive Prescaler Setting ¹ (%FSR) | | | | | | | Direct ADC ^{2,3} (%FSR) |
|-------------------|---|---------------------|-------------|----------|-------------|-------------|-------------|----------------------------------|
| | 16 V (AT) | 16 V (12 V) (AV/AC) | 8 V (AV/AC) | 4 V (AT) | 4 V (AV/AC) | 2 V (AV/AC) | 1 V (AV/AC) | VAREF = 2.56 V |
| 15 | 1 | | | | | | | |
| 14 | 1 | | | | | | | |
| 12 | 1 | 1 | | | | | | |
| 5 | 2 | 2 | 1 | | | | | |
| 3.3 | 2 | 2 | 1 | 1 | 1 | | | |
| 2.5 | 3 | 2 | 1 | 1 | 1 | | | 1 |
| 1.8 | 4 | 4 | 1 | 1 | 1 | 1 | | 1 |
| 1.5 | 5 | 5 | 2 | 2 | 2 | 1 | | 1 |
| 1.2 | 7 | 6 | 2 | 2 | 2 | 1 | | 1 |
| 0.9 | 9 | 9 | 4 | 3 | 3 | 1 | 1 | 1 |

Notes:

1. Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.
2. Direct ADC mode using an external VAREF of 2.56V±4.6mV, without Analog Calibration macro.
3. For input greater than 2.56 V, the ADC output will saturate. A higher VAREF or prescaler usage is recommended.

Examples

Calculating Accuracy for an Uncalibrated Analog Channel

Formula

For a given prescaler range, EQ 30 gives the output voltage.

$$\text{Output Voltage} = (\text{Channel Output Offset in V}) + (\text{Input Voltage} \times \text{Channel Gain})$$

EQ 30

where

Channel Output offset in V = Channel Input offset in LSBs x Equivalent voltage per LSB

Channel Gain Factor = 1 + (% Channel Gain / 100)

Example

Input Voltage = 5 V

Chosen Prescaler range = 8 V range

Refer to Table 2-51 on page 2-122.

Max. Output Voltage = (Max Positive input offset) + (Input Voltage x Max Positive Channel Gain)

Max. Positive input offset = (21 LSB) x (8 mV per LSB in 10-bit mode)

Max. Positive input offset = 166 mV

Max. Positive Gain Error = +3%

Max. Positive Channel Gain = 1 + (+3% / 100)

Max. Positive Channel Gain = 1.03

Max. Output Voltage = (166 mV) + (5 V x 1.03)

Max. Output Voltage = **5.316 V**

Similarly,

$$\begin{aligned} \text{Min. Output Voltage} &= (\text{Max. Negative input offset}) + (\text{Input Voltage} \times \text{Max. Negative Channel Gain}) \\ &= (-88 \text{ mV}) + (5 \text{ V} \times 0.96) = \mathbf{4.712 \text{ V}} \end{aligned}$$

Calculating Accuracy for a Calibrated Analog Channel

Formula

For a given prescaler range, [EQ 31](#) gives the output voltage.

$$\text{Output Voltage} = \text{Channel Error in V} + \text{Input Voltage}$$

EQ 31

where

$$\text{Channel Error in V} = \text{Total Channel Error in LSBs} \times \text{Equivalent voltage per LSB}$$

Example

Input Voltage = 5 V

Chosen Prescaler range = 8 V range

Refer to [Table 2-52 on page 2-123](#).

Max. Output Voltage = Max. Positive Channel Error in V + Input Voltage

Max. Positive Channel Error in V = (6 LSB) × (8 mV per LSB in 10-bit mode) = 48 mV

Max. Output Voltage = 48 mV + 5 V = **5.048 V**

Similarly,

Min. Output Voltage = Max. Negative Channel Error in V + Input Voltage = (-48 mV) + 5 V = **4.952 V**

Calculating LSBs from a Given Error Budget

Formula

For a given prescaler range,

$$\text{LSB count} = \pm (\text{Input Voltage} \times \text{Required\% error}) / (\text{Equivalent voltage per LSB})$$

Example

Input Voltage = 3.3 V

Required error margin = 1%

Refer to [Table 2-52 on page 2-123](#).

Equivalent voltage per LSB = 16 mV for a 16V prescaler, with ADC in 10-bit mode

LSB Count = $\pm (5.0 \text{ V} \times 1\%) / (0.016)$

LSB Count = **± 3.125**

Equivalent voltage per LSB = **8 mV** for an 8 V prescaler, with ADC in 10-bit mode

LSB Count = $\pm (5.0 \text{ V} \times 1\%) / (0.008)$

LSB Count = **± 6.25**

The 8 V prescaler satisfies the calculated LSB count accuracy requirement (see [Table 2-52 on page 2-123](#)).

Analog Configuration MUX

The ACM is the interface between the FPGA, the Analog Block configurations, and the real-time counter. Microsemi Libero SoC will generate IP that will load and configure the Analog Block via the ACM. However, users are not limited to using the Libero SoC IP. This section provides a detailed description of the ACM's register map, truth tables for proper configuration of the Analog Block and RTC, as well as timing waveforms so users can access and control the ACM directly from their designs.

The Analog Block contains four 8-bit latches per Analog Quad that are initialized through the ACM. These latches act as configuration bits for Analog Quads. The ACM block runs from the core voltage supply (1.5 V).

Access to the ACM is achieved via 8-bit address and data busses with enables. The pin list is provided in [Table 2-36 on page 2-78](#). The ACM clock speed is limited to a maximum of 10 MHz, more than sufficient to handle the low-bandwidth requirements of configuring the Analog Block and the RTC (sub-block of the Analog Block).

[Table 2-54](#) decodes the ACM address space and maps it to the corresponding Analog Quad and configuration byte for that quad.

Table 2-54 • ACM Address Decode Table for Analog Quad

| ACMADDR [7:0] in Decimal | Name | Description | Associated Peripheral |
|--------------------------|-----------|-------------------------|-----------------------|
| 0 | – | – | Analog Quad |
| 1 | AQ0 | Byte 0 | Analog Quad |
| 2 | AQ0 | Byte 1 | Analog Quad |
| 3 | AQ0 | Byte 2 | Analog Quad |
| 4 | AQ0 | Byte 3 | Analog Quad |
| 5 | AQ1 | Byte 0 | Analog Quad |
| . | . | . | Analog Quad |
| . | . | . | |
| . | . | . | |
| 36 | AQ8 | Byte 3 | Analog Quad |
| 37 | AQ9 | Byte 0 | Analog Quad |
| 38 | AQ9 | Byte 1 | Analog Quad |
| 39 | AQ9 | Byte 2 | Analog Quad |
| 40 | AQ9 | Byte 3 | Analog Quad |
| 41 | | Undefined | Analog Quad |
| . | . | Undefined | Analog Quad |
| . | . | | |
| . | . | | |
| 63 | | Undefined | RTC |
| 64 | COUNTER0 | Counter bits 7:0 | RTC |
| 65 | COUNTER1 | Counter bits 15:8 | RTC |
| 66 | COUNTER2 | Counter bits 23:16 | RTC |
| 67 | COUNTER3 | Counter bits 31:24 | RTC |
| 68 | COUNTER4 | Counter bits 39:32 | RTC |
| 72 | MATCHREG0 | Match register bits 7:0 | RTC |

Table 2-54 • ACM Address Decode Table for Analog Quad (continued)

| ACMADDR [7:0] in Decimal | Name | Description | Associated Peripheral |
|--------------------------|------------|---|-----------------------|
| 73 | MATCHREG1 | Match register bits 15:8 | RTC |
| 74 | MATCHREG2 | Match register bits 23:16 | RTC |
| 75 | MATCHREG3 | Match register bits 31:24 | RTC |
| 76 | MATCHREG4 | Match register bits 39:32 | RTC |
| 80 | MATCHBITS0 | Individual match bits 7:0 | RTC |
| 81 | MATCHBITS1 | Individual match bits 15:8 | RTC |
| 82 | MATCHBITS2 | Individual match bits 23:16 | RTC |
| 83 | MATCHBITS3 | Individual match bits 31:24 | RTC |
| 84 | MATCHBITS4 | Individual match bits 39:32 | RTC |
| 88 | CTRL_STAT | Control (write) / Status (read) register bits 7:0 | RTC |

Note: ACMADDR bytes 1 to 40 pertain to the Analog Quads; bytes 64 to 89 pertain to the RTC.

ACM Characteristics¹



Figure 2-97 • ACM Write Waveform



Figure 2-98 • ACM Read Waveform

1. When addressing the RTC addresses (i.e., ACMADDR 64 to 89), there is no timing generator, and the rc_osc, byte_en, and aq_wen signals have no impact.

Timing Characteristics

Table 2-55 • Analog Configuration Multiplexer (ACM) Timing
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|-------------------------|--|-------|-------|-------|-------|
| t_{CLKQACM} | Clock-to-Q of the ACM | 19.73 | 22.48 | 26.42 | ns |
| t_{SUDACM} | Data Setup time for the ACM | 4.39 | 5.00 | 5.88 | ns |
| t_{HDACM} | Data Hold time for the ACM | 0.00 | 0.00 | 0.00 | ns |
| t_{SUAACM} | Address Setup time for the ACM | 4.73 | 5.38 | 6.33 | ns |
| t_{HAACM} | Address Hold time for the ACM | 0.00 | 0.00 | 0.00 | ns |
| t_{SUEACM} | Enable Setup time for the ACM | 3.93 | 4.48 | 5.27 | ns |
| t_{HEACM} | Enable Hold time for the ACM | 0.00 | 0.00 | 0.00 | ns |
| t_{MPWARACM} | Asynchronous Reset Minimum Pulse Width for the ACM | 10.00 | 10.00 | 10.00 | ns |
| t_{REMARACM} | Asynchronous Reset Removal time for the ACM | 12.98 | 14.79 | 17.38 | ns |
| t_{RECARACM} | Asynchronous Reset Recovery time for the ACM | 12.98 | 14.79 | 17.38 | ns |
| $t_{\text{MPWCLKACM}}$ | Clock Minimum Pulse Width for the ACM | 45.00 | 45.00 | 45.00 | ns |
| $t_{\text{FMAXCLKACM}}$ | lock Maximum Frequency for the ACM | 10.00 | 10.00 | 10.00 | MHz |

Analog Quad ACM Description

Table 2-56 maps out the ACM space associated with configuration of the Analog Quads within the Analog Block. Table 2-56 shows the byte assignment within each quad and the function of each bit within each byte. Subsequent tables will explain each bit setting and how it corresponds to a particular configuration. After 3.3 V and 1.5 V are applied to Fusion, Analog Quad configuration registers are loaded with default settings until the initialization and configuration state machine changes them to user-defined settings.

Table 2-56 • Analog Quad ACM Byte Assignment

| Byte | Bit | Signal (Bx) | Function | Default Setting |
|----------------|-----|-------------|-------------------------------------|-----------------------|
| Byte 0 (AV) | 0 | B0[0] | Scaling factor control – prescaler | Highest voltage range |
| | 1 | B0[1] | | |
| | 2 | B0[2] | | |
| | 3 | B0[3] | Analog MUX select | Prescaler |
| | 4 | B0[4] | Current monitor switch | Off |
| | 5 | B0[5] | Direct analog input switch | Off |
| | 6 | B0[6] | Selects V-pad polarity | Positive |
| | 7 | B0[7] | Prescaler op amp mode | Power-down |
| Byte 1 (AC) | 0 | B1[0] | Scaling factor control – prescaler | Highest voltage range |
| | 1 | B1[1] | | |
| | 2 | B1[2] | | |
| | 3 | B1[3] | Analog MUX select | Prescaler |
| | 4 | B1[4] | | |
| | 5 | B1[5] | Direct analog input switch | Off |
| | 6 | B1[6] | Selects C-pad polarity | Positive |
| | 7 | B1[7] | Prescaler op amp mode | Power-down |
| Byte 2 (AG) | 0 | B2[0] | Internal chip temperature monitor * | Off |
| | 1 | B2[1] | Spare | – |
| | 2 | B2[2] | Current drive control | Lowest current |
| | 3 | B2[3] | | |
| | 4 | B2[4] | Spare | – |
| | 5 | B2[5] | Spare | – |
| | 6 | B2[6] | Selects G-pad polarity | Positive |
| | 7 | B2[7] | Selects low/high drive | Low drive |
| Byte 3 (AT) | 0 | B3[0] | Scaling factor control – prescaler | Highest voltage range |
| | 1 | B3[1] | | |
| | 2 | B3[2] | | |
| | 3 | B3[3] | Analog MUX select | Prescaler |
| | 4 | B3[4] | | |
| | 5 | B3[5] | Direct analog input switch | Off |
| | 6 | B3[6] | – | – |
| | 7 | B3[7] | Prescaler op amp mode | Power-down |

Note: *For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

Table 2-57 details the settings available to control the prescaler values of the AV, AC, and AT pins. Note that the AT pin has a reduced number of available prescaler values.

Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

| Control Lines Bx[2:0] | Scaling Factor, Pad to ADC Input | LSB for an 8-Bit Conversion ¹ (mV) | LSB for a 10-Bit Conversion ¹ (mV) | LSB for a 12-Bit Conversion ¹ (mV) | Full-Scale Voltage in 10-Bit Mode ² | Range Name |
|-----------------------|----------------------------------|---|---|---|--|------------|
| 000 ³ | 0.15625 | 64 | 16 | 4 | 16.368 V | 16 V |
| 001 | 0.3125 | 32 | 8 | 2 | 8.184 V | 8 V |
| 010 ³ | 0.625 | 16 | 4 | 1 | 4.092 V | 4 V |
| 011 | 1.25 | 8 | 2 | 0.5 | 2.046 V | 2 V |
| 100 | 2.5 | 4 | 1 | 0.25 | 1.023 V | 1 V |
| 101 | 5.0 | 2 | 0.5 | 0.125 | 0.5115 V | 0.5 V |
| 110 | 10.0 | 1 | 0.25 | 0.0625 | 0.25575 V | 0.25 V |
| 111 | 20.0 | 0.5 | 0.125 | 0.03125 | 0.127875 V | 0.125 V |

Notes:

1. LSB voltage equivalences assume $V_{AREF} = 2.56 V$.
2. Full Scale voltage for n -bit mode: $((2^n) - 1) \times (\text{LSB for a } n\text{-bit Conversion})$
3. These are the only valid ranges for the Temperature Monitor Block Prescaler.

Table 2-58 details the settings available to control the MUX within each of the AV, AC, and AT circuits. This MUX determines whether the signal routed to the ADC is the direct analog input, prescaled signal, or output of either the Current Monitor Block or the Temperature Monitor Block.

Table 2-58 • Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

| Control Lines Bx[4] | Control Lines Bx[3] | ADC Connected To |
|---------------------|---------------------|---------------------------------------|
| 0 | 0 | Prescaler |
| 0 | 1 | Direct input |
| 1 | 0 | Current amplifier temperature monitor |
| 1 | 1 | Not valid |

Table 2-59 details the settings available to control the Direct Analog Input switch for the AV, AC, and AT pins.

Table 2-59 • Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

| Control Lines Bx[5] | Direct Input Switch |
|---------------------|---------------------|
| 0 | Off |
| 1 | On |

Table 2-60 details the settings available to control the polarity of the signals coming to the AV, AC, and AT pins. Note that the only valid setting for the AT pin is logic 0 to support positive voltages.

Table 2-60 • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)*

| Control Lines Bx[6] | Input Signal Polarity |
|---------------------|-----------------------|
| 0 | Positive |
| 1 | Negative |

Note: *The B3[6] signal for the AT pad should be kept at logic 0 to accept only positive voltages.

Table 2-61 details the settings available to either power down or enable the prescaler associated with the analog inputs AV, AC, and AT.

Table 2-61 • Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

| Control Lines Bx[7] | Prescaler Op Amp |
|---------------------|------------------|
| 0 | Power-down |
| 1 | Operational |

Table 2-62 details the settings available to enable the Current Monitor Block associated with the AC pin.

Table 2-62 • Current Monitor Input Switch Control Truth Table—AV (x = 0)

| Control Lines B0[4] | Current Monitor Input Switch |
|---------------------|------------------------------|
| 0 | Off |
| 1 | On |

Table 2-63 details the settings available to configure the drive strength of the gate drive when not in high-drive mode.

Table 2-63 • Low-Drive Gate Driver Current Truth Table (AG)

| Control Lines B2[3] | Control Lines B2[2] | Current (μA) |
|---------------------|---------------------|--------------|
| 0 | 0 | 1 |
| 0 | 1 | 3 |
| 1 | 0 | 10 |
| 1 | 1 | 30 |

Table 2-64 details the settings available to set the polarity of the gate driver (either p-channel- or n-channel-type devices).

Table 2-64 • Gate Driver Polarity Truth Table (AG)

| Control Lines B2[6] | Gate Driver Polarity |
|---------------------|----------------------|
| 0 | Positive |
| 1 | Negative |

Table 2-65 details the settings available to turn on the Gate Driver and set whether high-drive mode is on or off.

Table 2-65 • Gate Driver Control Truth Table (AG)

| Control Lines B2[7] | GDON | Gate Driver |
|---------------------|------|---------------|
| 0 | 0 | Off |
| 0 | 1 | Low drive on |
| 1 | 0 | Off |
| 1 | 1 | High drive on |

Table 2-66 details the settings available to turn on and off the chip internal temperature monitor.

Note: For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

Table 2-66 • Internal Temperature Monitor Control Truth Table

| Control Lines B2[0] | PDTMB | Chip Internal Temperature Monitor |
|---------------------|-------|-----------------------------------|
| 0 | 0 | Off |
| 1 | 1 | On |

User I/Os

Introduction

Fusion devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. [Table 2-68](#), [Table 2-69](#), [Table 2-70](#), and [Table 2-71 on page 2-135](#) show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V-tolerant. See the ["5 V Input Tolerance" section on page 2-144](#) for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up, and any power-up sequence is allowed without current impact. Refer to the ["I/O Power-Up and Supply Voltage Thresholds for Power-On Reset \(Commercial and Industrial\)" section on page 3-5](#) for more information. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, digital inputs are tristated, digital outputs are tristated, and digital buffers (input/output) are tristated.

I/O Tile

The Fusion I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile in selected I/O banks can be used to support high-performance register inputs and outputs, with register enable if desired ([Figure 2-99 on page 2-133](#)). The registers can also be used to support the JESD-79C DDR standard within the I/O structure (see the ["Double Data Rate \(DDR\) Support" section on page 2-139](#) for more information).

As depicted in [Figure 2-100 on page 2-138](#), all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the ["I/O Registers" section on page 2-138](#) for more information.

I/O Banks and I/O Standards Compatibility

The digital I/Os are grouped into I/O voltage banks. There are three digital I/O banks on the AFS090 and AFS250 devices and four digital I/O banks on the AFS600 and AFS1500 devices. [Figure 2-113 on page 2-158](#) and [Figure 2-114 on page 2-159](#) show the bank configuration by device. The north side of the I/O in the AFS600 and AFS1500 devices comprises two banks of Pro I/Os. The Pro I/Os support a wide number of voltage-referenced I/O standards in addition to the multitude of single-ended and differential I/O standards common throughout all Microsemi digital I/Os. Each I/O voltage bank has dedicated I/O supply and ground voltages (VCCI/GNDQ for input buffers and VCCI/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. [Table 2-69](#) and [Table 2-70 on page 2-134](#) show the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the ["Package Pin Assignments" on page 4-1](#) and the ["User I/O Naming Convention" section on page 2-158](#).

Each Pro I/O bank is divided into minibanks. Any user I/O in a VREF minibank (a minibank is the region of scope of a VREF pin) can be configured as a VREF pin ([Figure 2-99 on page 2-133](#)). Only one VREF pin is needed to control the entire VREF minibank. The location and scope of the VREF minibanks can be determined by the I/O name. For details, see the ["User I/O Naming Convention" section on page 2-158](#).

[Table 2-70 on page 2-134](#) shows the I/O standards supported by Fusion devices and the corresponding voltage levels.

I/O standards are compatible if the following are true:

- Their VCCI values are identical.
- If both of the standards need a VREF, their VREF values must be identical (Pro I/O only).



Figure 2-99 • Fusion Pro I/O Bank Detail Showing VREF Minibanks (north side of AFS600 and AFS1500)

Table 2-67 • I/O Standards Supported by Bank Type

| I/O Bank | Single-Ended I/O Standards | Differential I/O Standards | Voltage-Referenced | Hot-Swap |
|--------------|---|----------------------------|--|----------|
| Standard I/O | LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V | – | – | Yes |
| Advanced I/O | LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X | LVPECL and LVDS | – | – |
| Pro I/O | LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X | LVPECL and LVDS | GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II | Yes |

Table 2-68 • I/O Bank Support by Device

| I/O Bank | AFS090 | AFS250 | AFS600 | AFS1500 |
|--------------|--------|--------|--------|---------|
| Standard I/O | N | N | – | – |
| Advanced I/O | E, W | E, W | E, W | E, W |
| Pro I/O | – | – | N | N |
| Analog Quad | S | S | S | S |

Note: E = East side of the device
 W = West side of the device
 N = North side of the device
 S = South side of the device

Table 2-69 • Fusion VCCI Voltages and Compatible Standards

| VCCI (typical) | Compatible Standards |
|----------------|---|
| 3.3 V | LVTTTL/LVCMOS 3.3, PCI 3.3, SSTL3 (Class I and II),* GTL+ 3.3, GTL 3.3,* LVPECL |
| 2.5 V | LVCMOS 2.5, LVCMOS 2.5/5.0, SSTL2 (Class I and II),* GTL+ 2.5,* GTL 2.5,* LVDS, BLVDS, M-LVDS |
| 1.8 V | LVCMOS 1.8 |
| 1.5 V | LVCMOS 1.5, HSTL (Class I),* HSTL (Class II)* |

Note: *I/O standard supported by Pro I/O banks.

Table 2-70 • Fusion VREF Voltages and Compatible Standards*

| VREF (typical) | Compatible Standards |
|----------------|---------------------------------|
| 1.5 V | SSTL3 (Class I and II) |
| 1.25 V | SSTL2 (Class I and II) |
| 1.0 V | GTL+ 2.5, GTL+ 3.3 |
| 0.8 V | GTL 2.5, GTL 3.3 |
| 0.75 V | HSTL (Class I), HSTL (Class II) |

Note: *I/O standards supported by Pro I/O banks.

Table 2-71 • Fusion Standard and Advanced I/O Features

| I/O Bank Voltage (typical) | Minibank Voltage (typical) | LVTTL/LVCMOS 3.3 V | LVC MOS 2.5 V | LVC MOS 1.8 V | LVC MOS 1.5 V | 3.3 V PCI / PCI-X | GTL + (3.3 V) | GTL + (2.5 V) | GTL (3.3 V) | GTL (2.5 V) | HSTL Class I and II (1.5 V) | SSTL2 Class I and II (2.5 V) | SSTL3 Class I and II (3.3 V) | LVDS (2.5 V ± 5%) | LVPECL (3.3 V) |
|----------------------------|----------------------------|--------------------|---------------|---------------|---------------|-------------------|---------------|---------------|-------------|-------------|-----------------------------|------------------------------|------------------------------|-------------------|----------------|
| 3.3 V | - | | | | | | | | | | | | | | |
| | 0.80 V | | | | | | | | | | | | | | |
| | 1.00 V | | | | | | | | | | | | | | |
| | 1.50 V | | | | | | | | | | | | | | |
| 2.5 V | - | | | | | | | | | | | | | | |
| | 0.80 V | | | | | | | | | | | | | | |
| | 1.00 V | | | | | | | | | | | | | | |
| | 1.25 V | | | | | | | | | | | | | | |
| 1.8 V | - | | | | | | | | | | | | | | |
| 1.5 V | - | | | | | | | | | | | | | | |
| | 0.75 V | | | | | | | | | | | | | | |

Note: White box: Allowable I/O standard combinations
 Gray box: Illegal I/O standard combinations

Features Supported on Pro I/Os

Table 2-72 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

Table 2-72 • Fusion Pro I/O Features

| Feature | Description |
|--|--|
| Single-ended and voltage-referenced transmitter features | • Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion) |
| | • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os. |
| | • Weak pull-up and pull-down |
| | • Two slew rates |
| | • Skew between output buffer enable/disable time: 2 ns delay (rising edge) and 0 ns delay (falling edge); see "Selectable Skew between Output Buffer Enable/Disable Time" on page 2-149 for more information |
| | • Five drive strengths |
| | • 5 V–tolerant receiver ("5 V Input Tolerance" section on page 2-144) |
| | • LVTTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-148) |
| | • High performance (Table 2-76 on page 2-143) |
| Single-ended receiver features | • Schmitt trigger option |
| | • ESD protection |
| | • Programmable delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V) |
| | • High performance (Table 2-76 on page 2-143) |
| | • Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry |
| Voltage-referenced differential receiver features | • Programmable Delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V) |
| | • High performance (Table 2-76 on page 2-143) |
| | • Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry |
| CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL transmitter | • Two I/Os and external resistors are used to provide a CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL transmitter solution. |
| | • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os. |
| | • Weak pull-up and pull-down |
| | • Fast slew rate |
| LVDS/LVPECL differential receiver features | • ESD protection |
| | • High performance (Table 2-76 on page 2-143) |
| | • Programmable delay: 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V) |
| | • Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry |

**Table 2-73 • Maximum I/O Frequency for Single-Ended, Voltage-Referenced, and Differential I/Os;
 All I/O Bank Types (maximum drive strength and high slew selected)**

| Specification | Performance Up To |
|---------------------|-------------------|
| LVTTTL/LVCMOS 3.3 V | 200 MHz |
| LVCMOS 2.5 V | 250 MHz |
| LVCMOS 1.8 V | 200 MHz |
| LVCMOS 1.5 V | 130 MHz |
| PCI | 200 MHz |
| PCI-X | 200 MHz |
| HSTL-I | 300 MHz |
| HSTL-II | 300 MHz |
| SSTL2-I | 300 MHz |
| SSTL2-II | 300 MHz |
| SSTL3-I | 300 MHz |
| SSTL3-II | 300 MHz |
| GTL+ 3.3 V | 300 MHz |
| GTL+ 2.5 V | 300 MHz |
| GTL 3.3 V | 300 MHz |
| GTL 2.5 V | 300 MHz |
| LVDS | 350 MHz |
| LVPECL | 300 MHz |

I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-100 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-100) between registers to implement single or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation. The I/O register combining must satisfy some rules.



Note: Fusion I/Os have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-139 for more information).

Figure 2-100 • I/O Block Logical Representation

Double Data Rate (DDR) Support

Fusion Pro I/Os support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making it very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using HSTL, SSTL, LVDS, and LVPECL I/O standards. In addition, high-speed DDR interfaces can be implemented using LVDS I/O.

Input Support for DDR

The basic structure to support a DDR input is shown in [Figure 2-101](#). Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on Fusion devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in [Figure 2-102 on page 2-140](#). New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the application note [Using DDR for Fusion Devices](#) for more information.



Figure 2-101 • DDR Input Register Support in Fusion Devices

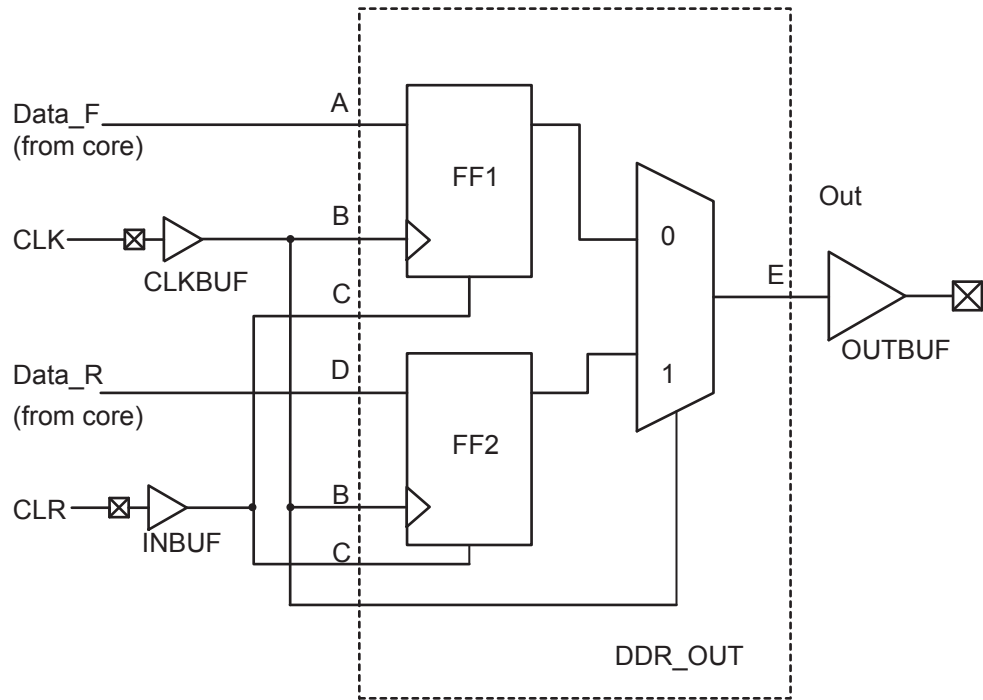


Figure 2-102 • DDR Output Support in Fusion Devices

Hot-Swap Support

Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The levels of hot-swap support and examples of related applications are described in [Table 2-74](#). The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required.

Table 2-74 • Levels of Hot-Swap Support

| Hot Swapping Level | Description | Power Applied to Device | Bus State | Card Ground Connection | Device Circuitry Connected to Bus Pins | Example of Application with Cards that Contain Fusion Devices | Compliance of Fusion Devices |
|--------------------|---------------------------|-------------------------|---|--|---|--|---|
| 1 | Cold-swap | No | – | – | – | System and card with Microsemi FPGA chip are powered down, then card gets plugged into system, then power supplies are turned on for system but not for FPGA on card. | Compliant I/Os can but do not have to be set to hot insertion mode. |
| 2 | Hot-swap while reset | Yes | Held in reset state | Must be made and maintained for 1 ms before, during, and after insertion/removal | – | In PCI hot plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable. | Compliant I/Os can but do not have to be set to hot insertion mode. |
| 3 | Hot-swap while bus idle | Yes | Held idle (no ongoing I/O processes during insertion/removal) | Same as Level 2 | Must remain glitch-free during power-up or power-down | Board bus shared with card bus is "frozen," and there is no toggling activity on bus. It is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal. | Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode. |
| 4 | Hot-swap on an active bus | Yes | Bus may have active I/O processes ongoing, but device being inserted or removed must be idle. | Same as Level 2 | Same as Level 3 | There is activity on the system bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal. | Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode. |

For Fusion devices requiring Level 3 and/or Level 4 compliance, the board drivers connected to Fusion I/Os need to have 10 k Ω (or lower) output drive resistance at hot insertion, and 1 k Ω (or lower) output drive resistance at hot removal. This is the resistance of the transmitter sending a signal to the Fusion I/O, and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet Level 3 and/or Level 4 compliance. Cards with two levels of staging should have the following sequence:

1. Grounds
2. Powers, I/Os, other pins

Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

Pro I/O banks and standard I/O banks fully support cold-sparing.

For Pro I/O banks, standards such as PCI that require I/O clamp diodes, can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

For Advanced I/O banks, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each advanced I/O pin to 0 V.

If Standard I/O banks are used in applications requiring cold-sparing, a discharge path from the power supply to ground should be provided. This can be done with a discharge resistor or a switched resistor. This is necessary because the standard I/O buffers do not have built-in I/O clamp diodes.

If a resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

I/O cold-sparing may add additional current if the pin is configured with either a pull-up or pull down resistor and driven in the opposite direction. A small static current is induced on each IO pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Please refer to [Table 2-95 on page 2-169](#), [Table 2-96 on page 2-169](#), and [Table 2-97 on page 2-171](#) for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTTL 3.3 V input pin is configured with a weak Pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven low. For an LVTTTL 3.3 V, pull-up resistor is ~45 k Ω and the resulting current is equal to $3.3 \text{ V} / 45 \text{ k}\Omega = 73 \mu\text{A}$ for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven high. Avoiding this current can be done by driving the input low when a weak pull-down resistor is used, and driving it high when a weak pull-up resistor is used.

In Active and Static modes, this current draw can occur in the following cases:

- Input buffers with pull-up, driven low
- Input buffers with pull-down, driven high
- Bidirectional buffers with pull-up, driven low
- Bidirectional buffers with pull-down, driven high
- Output buffers with pull-up, driven low
- Output buffers with pull-down, driven high
- Tristate buffers with pull-up, driven low
- Tristate buffers with pull-down, driven high

Electrostatic Discharge (ESD) Protection

Fusion devices are tested per JEDEC Standard JESD22-A114-B.

Fusion devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to VCCI. The second diode has its P side connected to GND and its N side connected to the pad. During operation, these diodes are normally biased in the Off state, except when transient voltage is significantly above VCCI or below GND levels.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to [Table 2-75](#) and [Table 2-76 on page 2-143](#) for more information about I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

Table 2-75 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities

| I/O Assignment | Clamp Diode | | Hot Insertion | | 5 V Input Tolerance ¹ | | Input Buffer | Output Buffer |
|--|--------------|--------------|---------------|--------------|----------------------------------|------------------|------------------|---------------|
| | Standard I/O | Advanced I/O | Standard I/O | Advanced I/O | Standard I/O | Advanced I/O | | |
| 3.3 V LVTTTL/LVCMOS | No | Yes | Yes | No | Yes ¹ | Yes ¹ | Enabled/Disabled | |
| 3.3 V PCI, 3.3 V PCI-X | N/A | Yes | N/A | No | N/A | Yes ¹ | Enabled/Disabled | |
| LVCMOS 2.5 V | No | Yes | Yes | No | No | No | Enabled/Disabled | |
| LVCMOS 2.5 V / 5.0 V | N/A | Yes | N/A | No | N/A | Yes ² | Enabled/Disabled | |
| LVCMOS 1.8 V | No | Yes | Yes | No | No | No | Enabled/Disabled | |
| LVCMOS 1.5 V | No | Yes | Yes | No | No | No | Enabled/Disabled | |
| Differential, LVDS/BLVDS/M-LVDS/ LVPECL ³ | N/A | Yes | N/A | No | N/A | No | Enabled/Disabled | |

Notes:

1. Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.
2. Can be implemented with an external resistor and an internal clamp diode.
3. Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.

Table 2-76 • Fusion Pro I/O – Hot-Swap and 5 V Input Tolerance Capabilities

| I/O Assignment | Clamp Diode | Hot Insertion | 5 V Input Tolerance | Input Buffer | Output Buffer |
|---|-------------|---------------|---------------------|------------------|---------------|
| 3.3 V LVTTTL/LVCMOS | No | Yes | Yes ¹ | Enabled/Disabled | |
| 3.3 V PCI, 3.3 V PCI-X | Yes | No | Yes ¹ | Enabled/Disabled | |
| LVCMOS 2.5 V ³ | No | Yes | No | Enabled/Disabled | |
| LVCMOS 2.5 V / 5.0 V ³ | Yes | No | Yes ² | Enabled/Disabled | |
| LVCMOS 1.8 V | No | Yes | No | Enabled/Disabled | |
| LVCMOS 1.5 V | No | Yes | No | Enabled/Disabled | |
| Voltage-Referenced Input Buffer | No | Yes | No | Enabled/Disabled | |
| Differential, LVDS/BLVDS/M-LVDS/LVPECL ⁴ | No | Yes | No | Enabled/Disabled | |

Notes:

1. Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.
2. Can be implemented with an external resistor and an internal clamp diode.
3. In the [SmartGen](#), [FlashROM](#), [Flash Memory System Builder](#), and [Analog System Builder User Guide](#), select the LVCMOS5 macro for the LVCMOS 2.5 V / 5.0 V I/O standard or the LVCMOS25 macro for the LVCMOS 2.5 V I/O standard.
4. Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.

5 V Input Tolerance

I/Os can support 5 V input tolerance when LVTTTL 3.3 V, LVCMOS 3.3 V, LVCMOS 2.5 V / 5 V, and LVCMOS 2.5 V configurations are used (see [Table 2-77 on page 2-147](#) for more details). There are four recommended solutions (see [Figure 2-103 to Figure 2-106 on page 2-146](#) for details of board and macro setups) to achieve 5 V receiver tolerance. All the solutions meet a common requirement of limiting the voltage at the input to 3.6 V or less. In fact, the I/O absolute maximum voltage rating is 3.6 V, and any voltage above 3.6 V may cause long-term gate oxide failures.

Solution 1

The board-level design needs to ensure that the reflected waveform at the pad does not exceed the limits provided in [Table 3-4 on page 3-4](#). This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI / PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the two external resistors, as explained below. Relying on the diode clamping would create an excessive pad DC voltage of $3.3\text{ V} + 0.7\text{ V} = 4\text{ V}$.

The following are some examples of possible resistor values (based on a simplified simulation model with no line effects and $10\ \Omega$ transmitter output resistance, where $R_{tx_out_high} = (V_{CCI} - V_{OH}) / I_{OH}$, $R_{tx_out_low} = V_{OL} / I_{OL}$).

Example 1 (high speed, high current):

$$R_{tx_out_high} = R_{tx_out_low} = 10\ \Omega$$

$$R1 = 36\ \Omega (\pm 5\%), P(r1)_{min} = 0.069\ \Omega$$

$$R2 = 82\ \Omega (\pm 5\%), P(r2)_{min} = 0.158\ \Omega$$

$$I_{max_tx} = 5.5\text{ V} / (82 * 0.95 + 36 * 0.95 + 10) = 45.04\text{ mA}$$

$$t_{RISE} = t_{FALL} = 0.85\text{ ns at } C_{pad_load} = 10\text{ pF (includes up to 25\% safety margin)}$$

$$t_{RISE} = t_{FALL} = 4\text{ ns at } C_{pad_load} = 50\text{ pF (includes up to 25\% safety margin)}$$

Example 2 (low-medium speed, medium current):

$$R_{tx_out_high} = R_{tx_out_low} = 10\ \Omega$$

$$R1 = 220\ \Omega (\pm 5\%), P(r1)_{min} = 0.018\ \Omega$$

$$R2 = 390\ \Omega (\pm 5\%), P(r2)_{min} = 0.032\ \Omega$$

$$I_{max_tx} = 5.5\text{ V} / (220 * 0.95 + 390 * 0.95 + 10) = 9.17\text{ mA}$$

$$t_{RISE} = t_{FALL} = 4\text{ ns at } C_{pad_load} = 10\text{ pF (includes up to 25\% safety margin)}$$

$$t_{RISE} = t_{FALL} = 20\text{ ns at } C_{pad_load} = 50\text{ pF (includes up to 25\% safety margin)}$$

Other values of resistors are also allowed as long as the resistors are sized appropriately to limit the voltage at the receiving end to $2.5\text{ V} < V_{in}(rx) < 3.6\text{ V}$ when the transmitter sends a logic 1. This range of $V_{in_dc}(rx)$ must be assured for any combination of transmitter supply ($5\text{ V} \pm 0.5\text{ V}$), transmitter output resistance, and board resistor tolerances.

Temporary overshoots are allowed according to [Table 3-4 on page 3-4](#).

Solution 1



Figure 2-103 • Solution 1

Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in [Table 3-4 on page 3-4](#). This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in [Figure 2-104](#). Relying on the diode clamping would create an excessive pad DC voltage of $3.3\text{ V} + 0.7\text{ V} = 4\text{ V}$.

Solution 2



Figure 2-104 • Solution 2

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in [Table 3-4 on page 3-4](#). This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in [Figure 2-105](#). Relying on the diode clamping would create an excessive pad DC voltage of $3.3\text{ V} + 0.7\text{ V} = 4\text{ V}$.



Figure 2-105 • Solution 3

Solution 4



Figure 2-106 • Solution 4

Table 2-77 • Comparison Table for 5 V–Compliant Receiver Scheme

| Scheme | Board Components | Speed | Current Limitations |
|--------|---|--------------------------|---|
| 1 | Two resistors | Low to high ¹ | Limited by transmitter's drive strength |
| 2 | Resistor and Zener 3.3 V | Medium | Limited by transmitter's drive strength |
| 3 | Bus switch | High | N/A |
| 4 | Minimum resistor value ² $R = 47 \Omega$ at $T_J = 70^\circ\text{C}$ $R = 150 \Omega$ at $T_J = 85^\circ\text{C}$ $R = 420 \Omega$ at $T_J = 100^\circ\text{C}$ | Medium | Maximum diode current at 100% duty cycle, signal constantly at '1' 52.7 mA at $T_J = 70^\circ\text{C}$ / 10-year lifetime 16.5 mA at $T_J = 85^\circ\text{C}$ / 10-year lifetime 5.9 mA at $T_J = 100^\circ\text{C}$ / 10-year lifetime For duty cycles other than 100%, the currents can be increased by a factor = $1 / (\text{duty cycle})$. Example: 20% duty cycle at 70°C Maximum current = $(1 / 0.2) * 52.7 \text{ mA} = 5 * 52.7 \text{ mA} = 263.5 \text{ mA}$ |

Notes:

1. Speed and current consumption increase as the board resistance values decrease.
2. Resistor values ensure I/O diode long-term reliability.

5 V Output Tolerance

Fusion I/Os must be set to 3.3 V LVTTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to 3.3 V LVTTTL or 3.3 V LVCMOS mode, Fusion I/Os can directly drive signals into 5 V TTL receivers. In fact, $V_{OL} = 0.4$ V and $V_{OH} = 2.4$ V in both 3.3 V LVTTTL and 3.3 V LVCMOS modes exceed the $V_{IL} = 0.8$ V and $V_{IH} = 2$ V level requirements of 5 V TTL receivers. Therefore, level '1' and level '0' will be recognized correctly by 5 V TTL receivers.

Simultaneously Switching Outputs and PCB Layout

- Simultaneously switching outputs (SSOs) can produce signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and VCCI dip noise. These two noise types are caused by rapidly changing currents through GND and VCCI package pin inductances during switching activities:
- Ground bounce noise voltage = $L(\text{GND}) * di/dt$
- VCCI dip noise voltage = $L(\text{VCCI}) * di/dt$

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to SSO bus are LVTTTL/LVCMOS inputs, LVTTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to be considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

Selectable Skew between Output Buffer Enable/Disable Time

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.



Figure 2-107 • Block Diagram of Output Enable Path



Figure 2-108 • Timing Diagram (option1: bypasses skew circuit)



Figure 2-109 • Timing Diagram (option 2: enables skew circuit)

At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss or transmitter over-stress due to transmitter-to-transmitter current shorts. [Figure 2-110](#) presents an example of the skew circuit implementation in a bidirectional communication system. [Figure 2-111](#) shows how bus contention is created, and [Figure 2-112](#) on [page 2-151](#) shows how it can be avoided with the skew circuit.



Figure 2-110 • Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using Fusion Devices

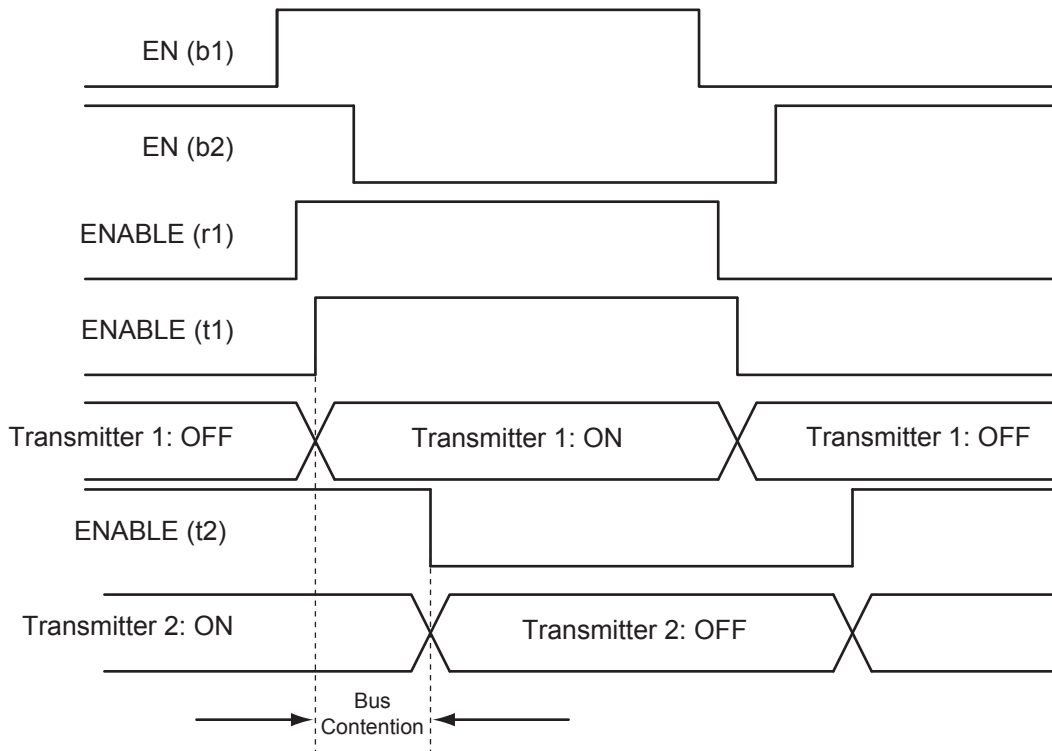


Figure 2-111 • Timing Diagram (bypasses skew circuit)



Figure 2-112 • Timing Diagram (with skew circuit selected)

Weak Pull-Up and Weak Pull-Down Resistors

Fusion devices support optional weak pull-up and pull-down resistors for each I/O pin. When the I/O is pulled up, it is connected to the VCCI of its corresponding I/O bank. When it is pulled down, it is connected to GND. Refer to [Table 2-97 on page 2-171](#) for more information.

Slew Rate Control and Drive Strength

Fusion devices support output slew rate control: high and low. The high slew rate option is recommended to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V / 5.0 V input, LVCMOS 1.8 V, and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

For Fusion slew rate and drive strength specifications, refer to the appropriate I/O bank table:

- Fusion Standard I/O ([Table 2-78 on page 2-152](#))
- Fusion Advanced I/O ([Table 2-79 on page 2-152](#))
- Fusion Pro I/O ([Table 2-80 on page 2-152](#))

[Table 2-83 on page 2-155](#) lists the default values for the above selectable I/O attributes as well as those that are preset for each I/O standard.

Refer to [Table 2-78](#), [Table 2-79](#), and [Table 2-80 on page 2-152](#) for SLEW and OUT_DRIVE settings. [Table 2-81 on page 2-153](#) and [Table 2-82 on page 2-154](#) list the I/O default attributes. [Table 2-83 on page 2-155](#) lists the voltages for the supported I/O standards.

Table 2-78 • Fusion Standard I/O Standards—OUT_DRIVE Settings

| I/O Standards | OUT_DRIVE (mA) | | | | | |
|---------------------|----------------|---|---|---|------|-----|
| | 2 | 4 | 6 | 8 | Slew | |
| LVTTTL/LVCMOS 3.3 V | ✓ | ✓ | ✓ | ✓ | High | Low |
| LVCMOS 2.5 V | ✓ | ✓ | ✓ | ✓ | High | Low |
| LVCMOS 1.8 V | ✓ | ✓ | – | – | High | Low |
| LVCMOS 1.5 V | ✓ | – | – | – | High | Low |

Table 2-79 • Fusion Advanced I/O Standards—SLEW and OUT_DRIVE Settings

| I/O Standards | OUT_DRIVE (mA) | | | | | | | Slew | |
|---------------------|----------------|---|---|---|----|----|------|------|--|
| | 2 | 4 | 6 | 8 | 12 | 16 | | | |
| LVTTTL/LVCMOS 3.3 V | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | High | Low | |
| LVCMOS 2.5 V | ✓ | ✓ | ✓ | ✓ | ✓ | – | High | Low | |
| LVCMOS 1.8 V | ✓ | ✓ | ✓ | ✓ | – | – | High | Low | |
| LVCMOS 1.5 V | ✓ | ✓ | – | – | – | – | High | Low | |

Table 2-80 • Fusion Pro I/O Standards—SLEW and OUT_DRIVE Settings

| I/O Standards | OUT_DRIVE (mA) | | | | | | | Slew | |
|---------------------|----------------|---|---|---|----|----|----|------|-----|
| | 2 | 4 | 6 | 8 | 12 | 16 | 24 | | |
| LVTTTL/LVCMOS 3.3 V | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | High | Low |
| LVCMOS 2.5 V | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | High | Low |
| LVCMOS 2.5 V/5.0 V | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | High | Low |
| LVCMOS 1.8 V | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | – | High | Low |
| LVCMOS 1.5 V | ✓ | ✓ | ✓ | ✓ | ✓ | – | – | High | Low |

Table 2-81 • Fusion Pro I/O Default Attributes

| I/O Standards | SLEW (output only) | OUT_DRIVE (output only) | SKEW (tribuf and bibuf only) | RES_PULL | OUT_LOAD (output only) | COMBINE_REGISTER | IN_DELAY (input only) | IN_DELAY_VAL (input only) | SCHMITT_TRIGGER (input only) |
|----------------------|---|---|------------------------------|----------|------------------------|------------------|-----------------------|---------------------------|------------------------------|
| LVTTTL/LVCMOS 3.3 V | Refer to the following tables for more information: Table 2-78 on page 2-152 Table 2-79 on page 2-152 Table 2-80 on page 2-152 | Refer to the following tables for more information: Table 2-78 on page 2-152 Table 2-79 on page 2-152 Table 2-80 on page 2-152 | Off | None | 35 pF | – | Off | 0 | Off |
| LVC MOS 2.5 V | | | Off | None | 35 pF | – | Off | 0 | Off |
| LVC MOS 2.5/5.0 V | | | Off | None | 35 pF | – | Off | 0 | Off |
| LVC MOS 1.8 V | | | Off | None | 35 pF | – | Off | 0 | Off |
| LVC MOS 1.5 V | | | Off | None | 35 pF | – | Off | 0 | Off |
| PCI (3.3 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| PCI-X (3.3 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| GTL+ (3.3 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| GTL+ (2.5 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| GTL (3.3 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| GTL (2.5 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| HSTL Class I | | | Off | None | 20 pF | – | Off | 0 | Off |
| HSTL Class II | | | Off | None | 20 pF | – | Off | 0 | Off |
| SSTL2 Class I and II | | | Off | None | 30 pF | – | Off | 0 | Off |
| SSTL3 Class I and II | | | Off | None | 30 pF | – | Off | 0 | Off |
| LVDS, BLVDS, M-LVDS | Off | None | 0 pF | – | Off | 0 | Off | | |
| LVPECL | Off | None | 0 pF | – | Off | 0 | Off | | |

Table 2-82 • Advanced I/O Default Attributes

| I/O Standards | SLEW (output only) | OUT_DRIVE (output only) | SKEW (tribuf and bibuf only) | RES_PULL | OUT_LOAD (output only) | COMBINE_REGISTER |
|----------------------|---|---|-------------------------------------|-----------------|-------------------------------|-------------------------|
| LVTTTL/LVCMOS 3.3 V | Refer to the following tables for more information: Table 2-78 on page 2-152 Table 2-79 on page 2-152 Table 2-80 on page 2-152 | Refer to the following tables for more information: Table 2-78 on page 2-152 Table 2-79 on page 2-152 Table 2-80 on page 2-152 | Off | None | 35 pF | – |
| LVCMOS 2.5 V | | | Off | None | 35 pF | – |
| LVCMOS 2.5/5.0 V | | | Off | None | 35 pF | – |
| LVCMOS 1.8 V | | | Off | None | 35 pF | – |
| LVCMOS 1.5 V | | | Off | None | 35 pF | – |
| PCI (3.3 V) | | | Off | None | 10 pF | – |
| PCI-X (3.3 V) | | | Off | None | 10 pF | – |
| LVDS, BLVDS, M-LVDS | | | Off | None | – | – |
| LVPECL | | | Off | None | – | – |

Table 2-83 • Fusion Pro I/O Supported Standards and Corresponding VREF and VTT Voltages

| I/O Standard | Input/Output Supply Voltage (VCCI_TYP) | Input Reference Voltage (VREF_TYP) | Board Termination Voltage (VTT_TYP) |
|-----------------------------|--|------------------------------------|-------------------------------------|
| LVTTTL/LVCMOS 3.3 V | 3.30 V | – | – |
| LVC MOS 2.5 V | 2.50 V | – | – |
| LVC MOS 2.5 V / 5.0 V Input | 2.50 V | – | – |
| LVC MOS 1.8 V | 1.80 V | – | – |
| LVC MOS 1.5 V | 1.50 V | – | – |
| PCI 3.3 V | 3.30 V | – | – |
| PCI-X 3.3 V | 3.30 V | – | – |
| GTL+ 3.3 V | 3.30 V | 1.00 V | 1.50 V |
| GTL+ 2.5 V | 2.50 V | 1.00 V | 1.50 V |
| GTL 3.3 V | 3.30 V | 0.80 V | 1.20 V |
| GTL 2.5 V | 2.50 V | 0.80 V | 1.20 V |
| HSTL Class I | 1.50 V | 0.75 V | 0.75 V |
| HSTL Class II | 1.50 V | 0.75 V | 0.75 V |
| SSTL3 Class I | 3.30 V | 1.50 V | 1.50 V |
| SSTL3 Class II | 3.30 V | 1.50 V | 1.50 V |
| SSTL2 Class I | 2.50 V | 1.25 V | 1.25 V |
| SSTL2 Class II | 2.50 V | 1.25 V | 1.25 V |
| LVDS, BLVDS, M-LVDS | 2.50 V | – | – |
| LVPECL | 3.30 V | – | – |

I/O Software Support

In the Fusion development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. [Table 2-84](#) and [Table 2-85](#) list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in Fusion support up to five different drive strengths.

Table 2-84 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications

| I/O Standards | SLEW (output only) | OUT_DRIVE (output only) | SKEW (all macros with OE)* | RES_PULL | OUT_LOAD (output only) | COMBINE_REGISTER |
|---------------------|-----------------------|----------------------------|-------------------------------|----------|---------------------------|------------------|
| LVTTTL/LVCMOS 3.3 V | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 2.5 V | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 2.5/5.0 V | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 1.8 V | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 1.5 V | 3 | 3 | 3 | 3 | 3 | 3 |
| PCI (3.3 V) | | | 3 | | 3 | 3 |
| PCI-X (3.3 V) | 3 | | 3 | | 3 | 3 |
| LVDS, BLVDS, M-LVDS | | | 3 | | | 3 |
| LVPECL | | | | | | 3 |

Note: * This feature does not apply to the standard I/O banks, which are the north I/O banks of AFS090 and AFS250 devices

Table 2-85 • Fusion Pro I/O Attributes vs. I/O Standard Applications

| I/O Standards | SLEW (output only) | OUT_DRIVE (output only) | SKREW (all macros with OE) | RES_PULL | OUT_LOAD (output only) | COMBINE_REGISTER | IN_DELAY (input only) | IN_DELAY_VAL (input only) | SCHMITT_TRIGGER (input only) | HOT_SWAPPABLE |
|----------------------|--------------------|-------------------------|----------------------------|----------|------------------------|------------------|-----------------------|---------------------------|------------------------------|---------------|
| LVTTTL/LVCMOS 3.3 V | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 2.5 V | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 2.5/5.0 V | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 1.8 V | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 1.5 V | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| PCI (3.3 V) | | | 3 | | 3 | 3 | 3 | 3 | | |
| PCI-X (3.3 V) | 3 | | 3 | | 3 | 3 | 3 | 3 | | |
| GTL+ (3.3 V) | | | 3 | | 3 | 3 | 3 | 3 | | 3 |
| GTL+ (2.5 V) | | | 3 | | 3 | 3 | 3 | 3 | | 3 |
| GTL (3.3 V) | | | 3 | | 3 | 3 | 3 | 3 | | 3 |
| GTL (2.5 V) | | | 3 | | 3 | 3 | 3 | 3 | | 3 |
| HSTL Class I | | | 3 | | 3 | 3 | 3 | 3 | | 3 |
| HSTL Class II | | | 3 | | 3 | 3 | 3 | 3 | | 3 |
| SSTL2 Class I and II | | | 3 | | 3 | 3 | 3 | 3 | | 3 |
| SSTL3 Class I and II | | | 3 | | 3 | 3 | 3 | 3 | | 3 |
| LVDS, BLVDS, M-LVDS | | | 3 | | | 3 | 3 | 3 | | 3 |
| LVPECL | | | | | | 3 | 3 | 3 | | 3 |

User I/O Naming Convention

Due to the comprehensive and flexible nature of Fusion device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-113 on page 2-158 and Figure 2-114 on page 2-159). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwByVz

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle).

n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Figure 2-22 on page 2-25 shows the three input pins per clock source MUX at CCC location m.

u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.

x = P (Positive) or N (Negative) for differential pairs, or R (Regular – single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive-LVDS only) or V (Negative-LVDS only) restrict the I/O differential pair from being selected as an LVPECL pair.

w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number (0–3). The Bank number starts at 0 from the northwest I/O bank and proceeds in a clockwise direction.

V = Reference voltage

z = Minibank number



Figure 2-113 • Naming Conventions of Fusion Devices with Three Digital I/O Banks

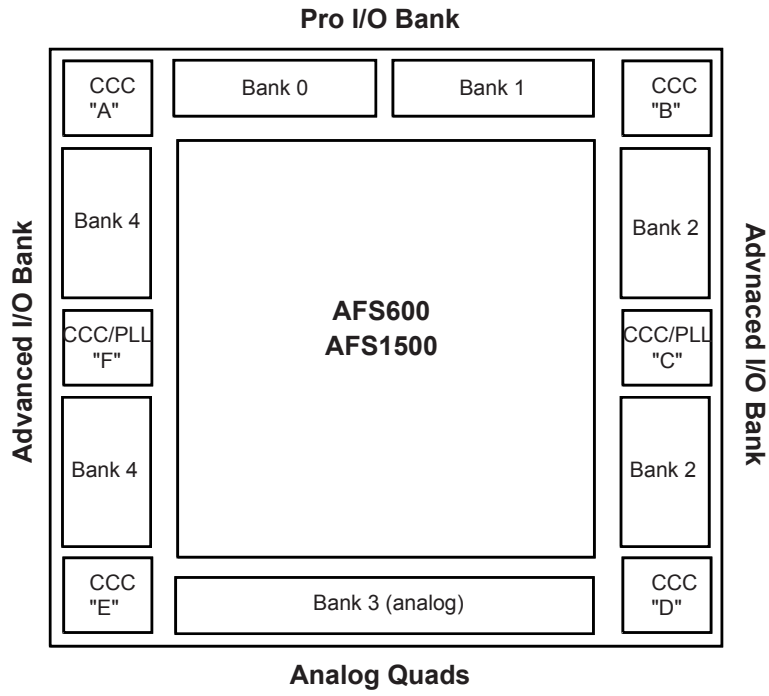


Figure 2-114 • Naming Conventions of Fusion Devices with Four I/O Banks

User I/O Characteristics

Timing Model

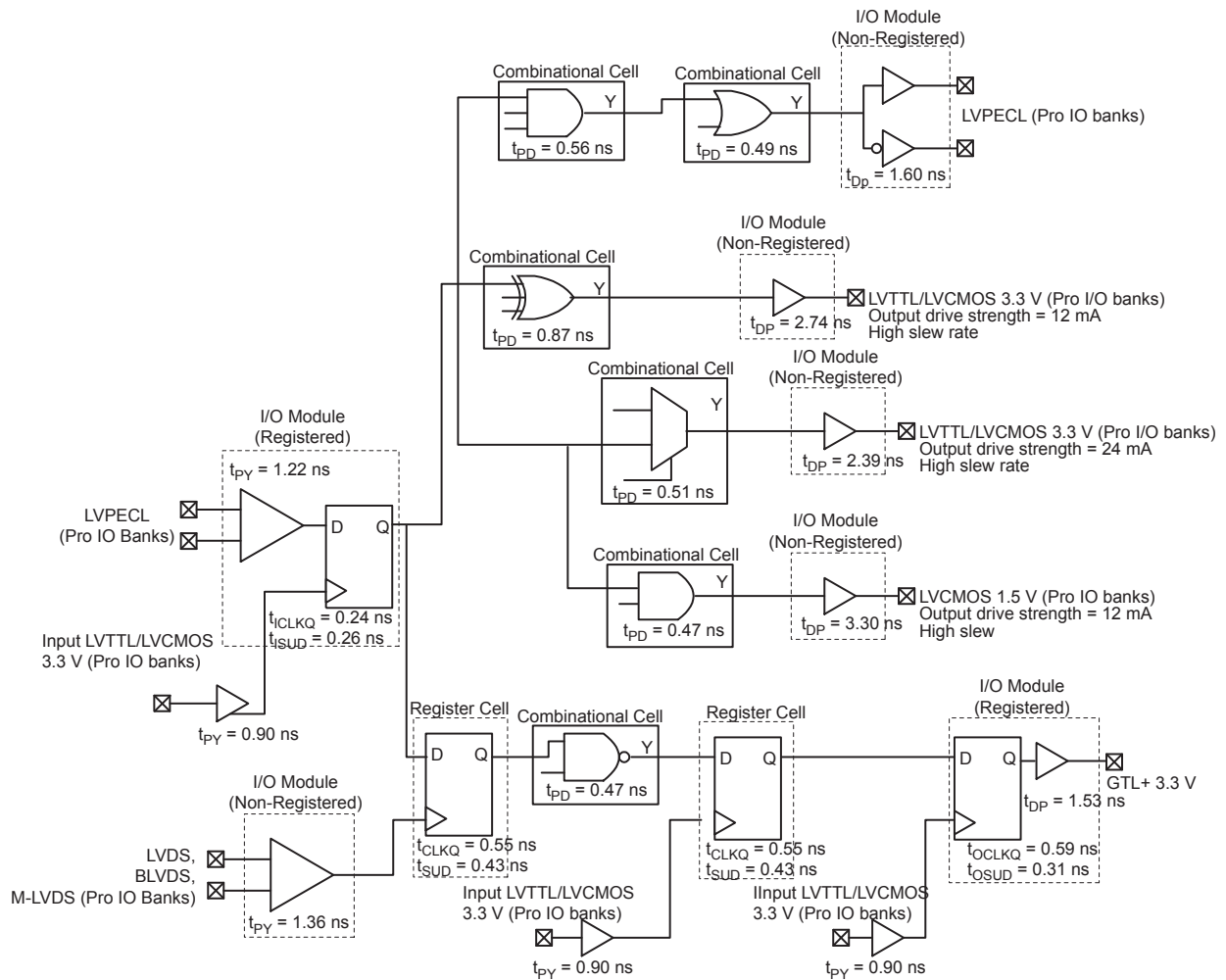
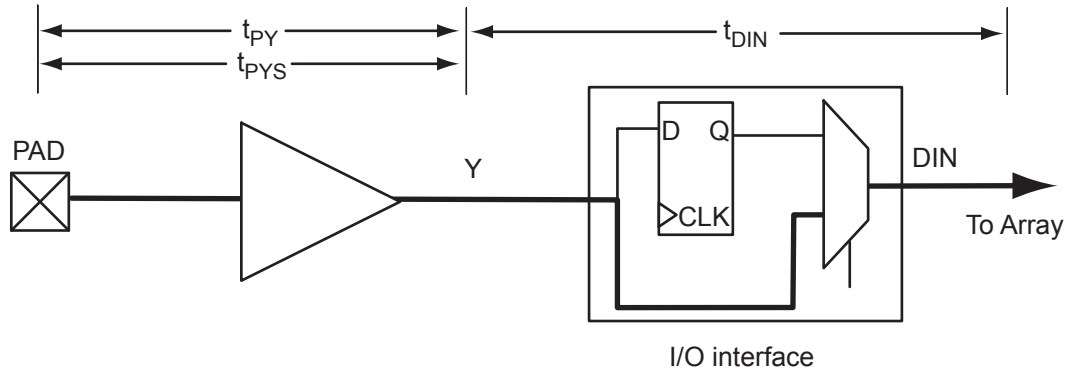


Figure 2-115 • Timing Model

**Operating Conditions: -2 Speed, Commercial Temperature Range ($T_J = 70^\circ\text{C}$),
Worst-Case VCC = 1.425 V**



$$t_{PY} = \text{MAX}(t_{PY} (R), t_{PY} (F))$$

$$t_{PYS} = \text{MAX}(t_{PYS} (R), t_{PYS} (F))$$

$$t_{DIN} = \text{MAX}(t_{DIN} (R), t_{DIN} (F))$$

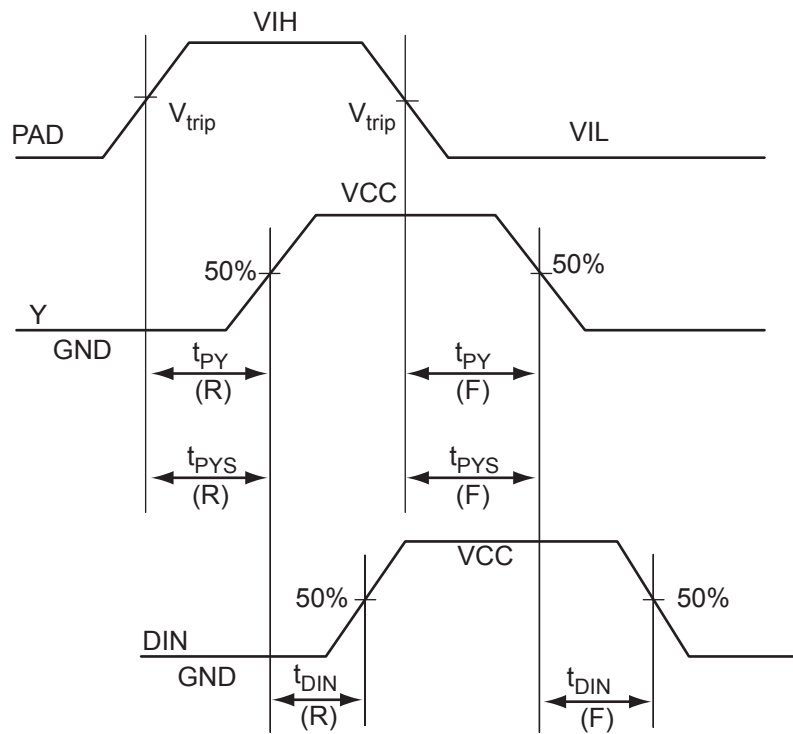


Figure 2-116 • Input Buffer Timing Model and Delays (example)



Figure 2-117 • Output Buffer Model and Delays (example)



Figure 2-118 • Tristate Output Buffer Timing Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions
Applicable to Pro I/Os**

| I/O Standard | Drive Strength | Slew Rate | VIL | | VIH | | VOL | VOH | IOL | IOH |
|--------------------------------|-------------------------|-----------|--------|-------------|-------------|--------|-------------|-------------|-----|-----|
| | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 12 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 2.5 V LVCMOS | 12 mA | High | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 3.3 V PCI | Per PCI Specification | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X Specification | | | | | | | | | |
| 3.3 V GTL | 20 mA ² | High | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 |
| 2.5 V GTL | 20 mA ² | High | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 |
| 3.3 V GTL+ | 35 mA | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 35 | 35 |
| 2.5 V GTL+ | 33 mA | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 33 | 33 |
| HSTL (I) | 8 mA | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 8 | 8 |
| HSTL (II) | 15 mA ² | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 15 | 15 |
| SSTL2 (I) | 15 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.54 | VCCI - 0.62 | 15 | 15 |
| SSTL2 (II) | 18 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI - 0.43 | 18 | 18 |
| SSTL3 (I) | 14 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.7 | VCCI - 1.1 | 14 | 14 |
| SSTL3 (II) | 21 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.5 | VCCI - 0.9 | 21 | 21 |

Notes:

1. Currents are measured at 85°C junction temperature.
2. Output drive strength is below JEDEC specification.
3. Output slew rate can be extracted by the IBIS models.

**Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions
Applicable to Advanced I/Os**

| I/O Standard | Drive Strength | Slew Rate | VIL | | VIH | | VOL | VOH | IOL | IOH |
|--------------------------------|--------------------------|-----------|--------|-------------|-------------|--------|-------------|-------------|-----|-----|
| | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 12 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 2.5 V LVCMOS | 12 mA | High | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 3.3 V PCI | Per PCI specifications | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X specifications | | | | | | | | | |

Note: Currents are measured at 85°C junction temperature.

Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions
Applicable to Standard I/Os

| I/O Standard | Drive Strength | Slew Rate | VIL | | VIH | | VOL | VOH | IOL | IOH |
|-----------------------------|----------------|-----------|--------|-------------|-------------|--------|-------------|-------------|-----|-----|
| | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 8 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 |
| 2.5 V LVCMOS | 8 mA | High | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 |
| 1.8 V LVCMOS | 4 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 4 | 4 |
| 1.5 V LVCMOS | 2 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 |

Note: Currents are measured at 85°C junction temperature.

Table 2-89 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions
Applicable to All I/O Bank Types

| DC I/O Standards | Commercial ¹ | | Industrial ² | |
|-----------------------------|-------------------------|------------------|-------------------------|------------------|
| | IIL ³ | IIH ⁴ | IIL ³ | IIH ⁴ |
| | µA | µA | µA | µA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 10 | 10 | 15 | 15 |
| 2.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.8 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3 V PCI | 10 | 10 | 15 | 15 |
| 3.3 V PCI-X | 10 | 10 | 15 | 15 |
| 3.3 V GTL | 10 | 10 | 15 | 15 |
| 2.5 V GTL | 10 | 10 | 15 | 15 |
| 3.3 V GTL+ | 10 | 10 | 15 | 15 |
| 2.5 V GTL+ | 10 | 10 | 15 | 15 |
| HSTL (I) | 10 | 10 | 15 | 15 |
| HSTL (II) | 10 | 10 | 15 | 15 |
| SSTL2 (I) | 10 | 10 | 15 | 15 |
| SSTL2 (II) | 10 | 10 | 15 | 15 |
| SSTL3 (I) | 10 | 10 | 15 | 15 |
| SSTL3 (II) | 10 | 10 | 15 | 15 |

Notes:

1. Commercial range ($0^{\circ}\text{C} < T_j < 85^{\circ}\text{C}$)
2. Industrial range ($-40^{\circ}\text{C} < T_j < 100^{\circ}\text{C}$)
3. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
4. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-90 • Summary of AC Measuring Points
 Applicable to All I/O Bank Types

| Standard | Input Reference Voltage (VREF_TYP) | Board Termination Voltage (VTT_REF) | Measuring Trip Point (Vtrip) |
|-----------------------------|------------------------------------|-------------------------------------|---|
| 3.3 V LVTTTL / 3.3 V LVCMOS | – | – | 1.4 V |
| 2.5 V LVCMOS | – | – | 1.2 V |
| 1.8 V LVCMOS | – | – | 0.90 V |
| 1.5 V LVCMOS | – | – | 0.75 V |
| 3.3 V PCI | – | – | 0.285 * VCCI (RR) 0.615 * VCCI (FF)) |
| 3.3 V PCI-X | – | – | 0.285 * VCCI (RR) 0.615 * VCCI (FF) |
| 3.3 V GTL | 0.8 V | 1.2 V | VREF |
| 2.5 V GTL | 0.8 V | 1.2 V | VREF |
| 3.3 V GTL+ | 1.0 V | 1.5 V | VREF |
| 2.5 V GTL+ | 1.0 V | 1.5 V | VREF |
| HSTL (I) | 0.75 V | 0.75 V | VREF |
| HSTL (II) | 0.75 V | 0.75 V | VREF |
| SSTL2 (I) | 1.25 V | 1.25 V | VREF |
| SSTL2 (II) | 1.25 V | 1.25 V | VREF |
| SSTL3 (I) | 1.5 V | 1.485 V | VREF |
| SSTL3 (II) | 1.5 V | 1.485 V | VREF |
| LVDS | – | – | Cross point |
| LVPECL | – | – | Cross point |

Table 2-91 • I/O AC Parameter Definitions

| Parameter | Definition |
|-------------------|---|
| t _{DP} | Data to Pad delay through the Output Buffer |
| t _{PY} | Pad to Data delay through the Input Buffer with Schmitt trigger disabled |
| t _{DOUT} | Data to Output Buffer delay through the I/O interface |
| t _{EOUT} | Enable to Output Buffer Tristate Control delay through the I/O interface |
| t _{DIN} | Input Buffer to Data delay through the I/O interface |
| t _{PYS} | Pad to Data delay through the Input Buffer with Schmitt trigger enabled |
| t _{HZ} | Enable to Pad delay through the Output Buffer—High to Z |
| t _{ZH} | Enable to Pad delay through the Output Buffer—Z to High |
| t _{LZ} | Enable to Pad delay through the Output Buffer—Low to Z |
| t _{ZL} | Enable to Pad delay through the Output Buffer—Z to Low |
| t _{ZHS} | Enable to Pad delay through the Output Buffer with delayed enable—Z to High |
| t _{ZLS} | Enable to Pad delay through the Output Buffer with delayed enable—Z to Low |

Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = I/O Standard Dependent
Applicable to Pro I/Os

| I/O Standard | Drive Strength (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ohm) | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{PYS} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------------------------|----------------------|-----------|----------------------|-------------------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 3.3 V LVTTTL/ 3.3 V LVCMOS | 12 mA | High | 35 | – | 0.49 | 2.74 | 0.03 | 0.90 | 1.17 | 0.32 | 2.79 | 2.14 | 2.45 | 2.70 | 4.46 | 3.81 | ns |
| 2.5 V LVCMOS | 12 mA | High | 35 | – | 0.49 | 2.80 | 0.03 | 1.13 | 1.24 | 0.32 | 2.85 | 2.61 | 2.51 | 2.61 | 4.52 | 4.28 | ns |
| 1.8 V LVCMOS | 12 mA | High | 35 | – | 0.49 | 2.83 | 0.03 | 1.08 | 1.42 | 0.32 | 2.89 | 2.31 | 2.79 | 3.16 | 4.56 | 3.98 | ns |
| 1.5 V LVCMOS | 12 mA | High | 35 | – | 0.49 | 3.30 | 0.03 | 1.27 | 1.60 | 0.32 | 3.36 | 2.70 | 2.96 | 3.27 | 5.03 | 4.37 | ns |
| 3.3 V PCI | Per PCI spec | High | 10 | 25 ² | 0.49 | 2.09 | 0.03 | 0.78 | 1.25 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 | ns |
| 3.3 V PCI-X | Per PCI-X spec | High | 10 | 25 ² | 0.49 | 2.09 | 0.03 | 0.77 | 1.17 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 | ns |
| 3.3 V GTL | 20 mA | High | 10 | 25 | 0.49 | 1.55 | 0.03 | 2.19 | – | 0.32 | 1.52 | 1.55 | 0.00 | 0.00 | 3.19 | 3.22 | ns |
| 2.5 V GTL | 20 mA | High | 10 | 25 | 0.49 | 1.59 | 0.03 | 1.83 | – | 0.32 | 1.61 | 1.59 | 0.00 | 0.00 | 3.28 | 3.26 | ns |
| 3.3 V GTL+ | 35 mA | High | 10 | 25 | 0.49 | 1.53 | 0.03 | 1.19 | – | 0.32 | 1.56 | 1.53 | 0.00 | 0.00 | 3.23 | 3.20 | ns |
| 2.5 V GTL+ | 33 mA | High | 10 | 25 | 0.49 | 1.65 | 0.03 | 1.13 | – | 0.32 | 1.68 | 1.57 | 0.00 | 0.00 | 3.35 | 3.24 | ns |
| HSTL (I) | 8 mA | High | 20 | 50 | 0.49 | 2.37 | 0.03 | 1.59 | – | 0.32 | 2.42 | 2.35 | 0.00 | 0.00 | 4.09 | 4.02 | ns |
| HSTL (II) | 15 mA | High | 20 | 25 | 0.49 | 2.26 | 0.03 | 1.59 | – | 0.32 | 2.30 | 2.03 | 0.00 | 0.00 | 3.97 | 3.70 | ns |
| SSTL2 (I) | 17 mA | High | 30 | 50 | 0.49 | 1.59 | 0.03 | 1.00 | – | 0.32 | 1.62 | 1.38 | 0.00 | 0.00 | 3.29 | 3.05 | ns |
| SSTL2 (II) | 21 mA | High | 30 | 25 | 0.49 | 1.62 | 0.03 | 1.00 | – | 0.32 | 1.65 | 1.32 | 0.00 | 0.00 | 3.32 | 2.99 | ns |
| SSTL3 (I) | 16 mA | High | 30 | 50 | 0.49 | 1.72 | 0.03 | 0.93 | – | 0.32 | 1.75 | 1.37 | 0.00 | 0.00 | 3.42 | 3.04 | ns |
| SSTL3 (II) | 24 mA | High | 30 | 25 | 0.49 | 1.54 | 0.03 | 0.93 | – | 0.32 | 1.57 | 1.25 | 0.00 | 0.00 | 3.24 | 2.92 | ns |
| LVDS | 24 mA | High | – | – | 0.49 | 1.57 | 0.03 | 1.36 | – | – | – | – | – | – | – | – | ns |
| LVPECL | 24 mA | High | – | – | 0.49 | 1.60 | 0.03 | 1.22 | – | – | – | – | – | – | – | – | ns |

Notes:

1. For specific junction temperature and voltage-supply levels, refer to [Table 3-6 on page 3-7](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-123 on page 2-197](#) for connectivity. This resistor is not required during normal operation.

Table 2-93 • Summary of I/O Timing Characteristics – Software Default Settings
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = I/O Standard Dependent
 Applicable to Advanced I/Os

| I/O Standard | Drive Strength (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ohm) | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------------------------|---------------------|-----------|----------------------|-------------------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 3.3 V LVTTTL/ 3.3 V LVCMOS | 12 mA | High | 35 pF | – | 0.49 | 2.64 | 0.03 | 0.90 | 0.32 | 2.69 | 2.11 | 2.40 | 2.68 | 4.36 | 3.78 | ns |
| 2.5 V LVCMOS | 12 mA | High | 35 pF | – | 0.49 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |
| 1.8 V LVCMOS | 12 mA | High | 35 pF | – | 0.49 | 2.64 | 0.03 | 0.91 | 0.32 | 2.69 | 2.27 | 2.76 | 3.05 | 4.36 | 3.94 | ns |
| 1.5 V LVCMOS | 12 mA | High | 35 pF | – | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |
| 3.3 V PCI | Per PCI spec | High | 10 pF | 25 ² | 0.49 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |
| 3.3 V PCI-X | Per PCI-X spec | High | 10 pF | 25 ² | 0.49 | 2.00 | 0.03 | 0.62 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |
| LVDS | 24 mA | High | – | – | 0.49 | 1.37 | 0.03 | 1.20 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| LVPECL | 24 mA | High | – | – | 0.49 | 1.34 | 0.03 | 1.05 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | ns |

Notes:

1. For specific junction temperature and voltage-supply levels, refer to [Table 3-6 on page 3-7](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-123 on page 2-197](#) for connectivity. This resistor is not required during normal operation.

Table 2-94 • Summary of I/O Timing Characteristics – Software Default Settings
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = I/O Standard Dependent
 Applicable to Standard I/Os

| I/O Standard | Drive Strength (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ohm) | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|-------------------------------|---------------------|-----------|----------------------|-------------------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 3.3 V LVTTTL/ 3.3 V LVCMOS | 8 mA | High | 35 pF | – | 0.49 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |
| 2.5 V LVCMOS | 8 mA | High | 35pF | – | 0.49 | 3.56 | 0.03 | 0.96 | 0.32 | 3.40 | 3.56 | 1.78 | 1.91 | ns |
| 1.8 V LVCMOS | 4 mA | High | 35pF | – | 0.49 | 4.74 | 0.03 | 0.90 | 0.32 | 4.02 | 4.74 | 1.80 | 1.85 | ns |
| 1.5 V LVCMOS | 2 mA | High | 35pF | – | 0.49 | 5.71 | 0.03 | 1.06 | 0.32 | 4.71 | 5.71 | 1.83 | 1.83 | ns |

Note: For specific junction temperature and voltage-supply levels, refer to [Table 3-6 on page 3-7](#) for derating values.

Detailed I/O DC Characteristics

Table 2-95 • Input Capacitance

| Symbol | Definition | Conditions | Min. | Max. | Units |
|-------------|------------------------------------|----------------------|------|------|-------|
| C_{IN} | Input capacitance | VIN = 0, f = 1.0 MHz | | 8 | pF |
| C_{INCLK} | Input capacitance on the clock pin | VIN = 0, f = 1.0 MHz | | 8 | pF |

Table 2-96 • I/O Output Buffer Maximum Resistances ¹

| Standard | Drive Strength | $R_{PULL-DOWN}$ (ohms) ² | $R_{PULL-UP}$ (ohms) ³ |
|------------------------------------|-----------------------------|--|--------------------------------------|
| Applicable to Pro I/O Banks | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 4 mA | 100 | 300 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 2.5 V LVCMOS | 4 mA | 100 | 200 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |
| 3.3 V GTL | 20 mA | 11 | – |
| 2.5 V GTL | 20 mA | 14 | – |
| 3.3 V GTL+ | 35 mA | 12 | – |
| 2.5 V GTL+ | 33 mA | 15 | – |

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/techdocs/models/ibis.html>.
2. $R_{(PULL-DOWN-MAX)} = VOL_{spec} / I_{OL_{spec}}$
3. $R_{(PULL-UP-MAX)} = (VCC_{lmax} - VOH_{spec}) / IOH_{spec}$

Table 2-96 • I/O Output Buffer Maximum Resistances ¹ (continued)

| Standard | Drive Strength | R _{PULL-DOWN} (ohms) ² | R _{PULL-UP} (ohms) ³ |
|---|-----------------------------|---|---|
| HSTL (I) | 8 mA | 50 | 50 |
| HSTL (II) | 15 mA | 25 | 25 |
| SSTL2 (I) | 17 mA | 27 | 31 |
| SSTL2 (II) | 21 mA | 13 | 15 |
| SSTL3 (I) | 16 mA | 44 | 69 |
| SSTL3 (II) | 24 mA | 18 | 32 |
| Applicable to Advanced I/O Banks | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/techdocs/models/ibis.html>.
2. $R_{(PULL-DOWN-MAX)} = V_{OLspec} / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-96 • I/O Output Buffer Maximum Resistances¹ (continued)

| Standard | Drive Strength | R _{PULL-DOWN} (ohms) ² | R _{PULL-UP} (ohms) ³ |
|---|----------------|---|---|
| Applicable to Standard I/O Banks | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/techdocs/models/ibis.html>.
2. $R_{(PULL-DOWN-MAX)} = VOL_{spec} / I_{OL_{spec}}$
3. $R_{(PULL-UP-MAX)} = (VCCImax - VOH_{spec}) / IOH_{spec}$

**Table 2-97 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

| VCCI | R _(WEAK PULL-UP) ¹ (ohms) | | R _(WEAK PULL-DOWN) ² (ohms) | |
|-------|--|------|--|-------|
| | Min. | Max. | Min. | Max. |
| 3.3 V | 10 k | 45 k | 10 k | 45 k |
| 2.5 V | 11 k | 55 k | 12 k | 74 k |
| 1.8 V | 18 k | 70 k | 17 k | 110 k |
| 1.5 V | 19 k | 90 k | 19 k | 140 k |

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCImax - VOH_{spec}) / I_{WEAK PULL-UP-MIN}$
2. $R_{(WEAK PULL-DOWN-MAX)} = VOL_{spec} / I_{WEAK PULL-DOWN-MIN}$

Table 2-98 • I/O Short Currents IOSH/IOSL

| | Drive Strength | IOSH (mA)* | IOSL (mA)* |
|---|----------------|------------|------------|
| Applicable to Pro I/O Banks | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 4 mA | 25 | 27 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 2.5 V LVCMOS | 4 mA | 16 | 18 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| | 16 mA | 83 | 87 |
| | 24 mA | 169 | 124 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 45 | 51 |
| | 12 mA | 91 | 74 |
| | 16 mA | 91 | 74 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| | 6 mA | 32 | 39 |
| | 8 mA | 66 | 55 |
| | 12 mA | 66 | 55 |
| Applicable to Advanced I/O Banks | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |

 Note: * $T_J = 100^{\circ}\text{C}$

Table 2-98 • I/O Short Currents IOSH/IOSL (continued)

| | Drive Strength | IOSH (mA)* | IOSL (mA)* |
|---|-----------------------------|------------|------------|
| 2.5 V LVCMOS | 2 mA | 16 | 18 |
| | 4 mA | 16 | 18 |
| | 6 mA | 32 | 37 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| | 16 mA | 83 | 87 |
| | 24 mA | 169 | 124 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 45 | 51 |
| | 12 mA | 91 | 74 |
| | 16 mA | 91 | 74 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| | 6 mA | 32 | 39 |
| | 8 mA | 66 | 55 |
| | 12 mA | 66 | 55 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 103 | 109 |
| Applicable to Standard I/O Banks | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| 2.5 V LVCMOS | 2 mA | 16 | 18 |
| | 4 mA | 16 | 18 |
| | 6 mA | 32 | 37 |
| | 8 mA | 32 | 37 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |

Note: * $T_J = 100^\circ\text{C}$

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-99 • Short Current Event Duration before Failure

| Temperature | Time Before Failure |
|-------------|---------------------|
| -40°C | >20 years |
| 0°C | >20 years |
| 25°C | >20 years |
| 70°C | 5 years |
| 85°C | 2 years |
| 100°C | 6 months |

**Table 2-100 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers**

| Input Buffer Configuration | Hysteresis Value (typ.) |
|--|-------------------------|
| 3.3 V LVTTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode) | 240 mV |
| 2.5 V LVCMOS (Schmitt trigger mode) | 140 mV |
| 1.8 V LVCMOS (Schmitt trigger mode) | 80 mV |
| 1.5 V LVCMOS (Schmitt trigger mode) | 60 mV |

Table 2-101 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|--|-----------------------------|--|------------------|
| LVTTTL/LVCMOS (Schmitt trigger disabled) | No requirement | 10 ns* | 20 years (100°C) |
| LVTTTL/LVCMOS (Schmitt trigger enabled) | No requirement | No requirement, but input noise voltage cannot exceed Schmitt hysteresis | 20 years (100°C) |
| HSTL/SSTL/GTL | No requirement | 10 ns* | 10 years (100°C) |
| LVDS/BLVDS/M-LVDS/LVPECL | No requirement | 10 ns* | 10 years (100°C) |

Note: * The maximum input rise/fall time is related only to the noise induced into the input buffer trace. If the noise is low, the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure there is no excessive noise coupling into input signals.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTTL support.

Table 2-102 • Minimum and Maximum DC Input and Output Levels

| 3.3 V LVTTTL / 3.3 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|---|-----------|-----------|-----------|-----------|-----------|-----------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| Applicable to Pro I/O Banks | | | | | | | | | | | | |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 10 | 10 |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 10 | 10 |
| 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 109 | 103 | 10 | 10 |
| 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 127 | 132 | 10 | 10 |
| 24 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 24 | 24 | 181 | 268 | 10 | 10 |
| Applicable to Advanced I/O Banks | | | | | | | | | | | | |
| 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 27 | 25 | 10 | 10 |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 54 | 51 | 10 | 10 |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 10 | 10 |
| 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 109 | 103 | 10 | 10 |
| 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 127 | 132 | 10 | 10 |
| 24 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 24 | 24 | 181 | 268 | 10 | 10 |
| Applicable to Standard I/O Banks | | | | | | | | | | | | |
| 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 27 | 25 | 10 | 10 |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 54 | 51 | 10 | 10 |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



Figure 2-119 • AC Loading

Table 2-103 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 3.3 | 1.4 | – | 35 |

Note: *Measuring point = V_{trip}. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics
Table 2-104 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,

Worst-Case VCCI = 3.0 V

Applicable to Pro I/Os

| Drive Strength | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{PYS} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|----------------|-------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 4 mA | Std. | 0.66 | 11.01 | 0.04 | 1.20 | 1.57 | 0.43 | 11.21 | 9.05 | 2.69 | 2.44 | 13.45 | 11.29 | ns |
| | –1 | 0.56 | 9.36 | 0.04 | 1.02 | 1.33 | 0.36 | 9.54 | 7.70 | 2.29 | 2.08 | 11.44 | 9.60 | ns |
| | –2 | 0.49 | 8.22 | 0.03 | 0.90 | 1.17 | 0.32 | 8.37 | 6.76 | 2.01 | 1.82 | 10.04 | 8.43 | ns |
| 8 mA | Std. | 0.66 | 7.86 | 0.04 | 1.20 | 1.57 | 0.43 | 8.01 | 6.44 | 3.04 | 3.06 | 10.24 | 8.68 | ns |
| | –1 | 0.56 | 6.69 | 0.04 | 1.02 | 1.33 | 0.36 | 6.81 | 5.48 | 2.58 | 2.61 | 8.71 | 7.38 | ns |
| | –2 | 0.49 | 5.87 | 0.03 | 0.90 | 1.17 | 0.32 | 5.98 | 4.81 | 2.27 | 2.29 | 7.65 | 6.48 | ns |
| 12 mA | Std. | 0.66 | 6.03 | 0.04 | 1.20 | 1.57 | 0.43 | 6.14 | 5.02 | 3.28 | 3.47 | 8.37 | 7.26 | ns |
| | –1 | 0.56 | 5.13 | 0.04 | 1.02 | 1.33 | 0.36 | 5.22 | 4.27 | 2.79 | 2.95 | 7.12 | 6.17 | ns |
| | –2 | 0.49 | 4.50 | 0.03 | 0.90 | 1.17 | 0.32 | 4.58 | 3.75 | 2.45 | 2.59 | 6.25 | 5.42 | ns |
| 16 mA | Std. | 0.66 | 5.62 | 0.04 | 1.20 | 1.57 | 0.43 | 5.72 | 4.72 | 3.32 | 3.58 | 7.96 | 6.96 | ns |
| | –1 | 0.56 | 4.78 | 0.04 | 1.02 | 1.33 | 0.36 | 4.87 | 4.02 | 2.83 | 3.04 | 6.77 | 5.92 | ns |
| | –2 | 0.49 | 4.20 | 0.03 | 0.90 | 1.17 | 0.32 | 4.27 | 3.53 | 2.48 | 2.67 | 5.94 | 5.20 | ns |
| 24 mA | Std. | 0.66 | 5.24 | 0.04 | 1.20 | 1.57 | 0.43 | 5.34 | 4.69 | 3.39 | 3.96 | 7.58 | 6.93 | ns |
| | –1 | 0.56 | 4.46 | 0.04 | 1.02 | 1.33 | 0.36 | 4.54 | 3.99 | 2.88 | 3.37 | 6.44 | 5.89 | ns |
| | –2 | 0.49 | 3.92 | 0.03 | 0.90 | 1.17 | 0.32 | 3.99 | 3.50 | 2.53 | 2.96 | 5.66 | 5.17 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-105 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Pro I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOU_T} | t_{zL} | t_{zH} | t_{LZ} | t_{HZ} | t_{zLS} | t_{zHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|-------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.66 | 7.88 | 0.04 | 1.20 | 1.57 | 0.43 | 8.03 | 6.70 | 2.69 | 2.59 | 10.26 | 8.94 | ns |
| | -1 | 0.56 | 6.71 | 0.04 | 1.02 | 1.33 | 0.36 | 6.83 | 5.70 | 2.29 | 2.20 | 8.73 | 7.60 | ns |
| | -2 | 0.49 | 5.89 | 0.03 | 0.90 | 1.17 | 0.32 | 6.00 | 5.01 | 2.01 | 1.93 | 7.67 | 6.67 | ns |
| 8 mA | Std. | 0.66 | 5.08 | 0.04 | 1.20 | 1.57 | 0.43 | 5.17 | 4.14 | 3.05 | 3.21 | 7.41 | 6.38 | ns |
| | -1 | 0.56 | 4.32 | 0.04 | 1.02 | 1.33 | 0.36 | 4.40 | 3.52 | 2.59 | 2.73 | 6.30 | 5.43 | ns |
| | -2 | 0.49 | 3.79 | 0.03 | 0.90 | 1.17 | 0.32 | 3.86 | 3.09 | 2.28 | 2.40 | 5.53 | 4.76 | ns |
| 12 mA | Std. | 0.66 | 3.67 | 0.04 | 1.20 | 1.57 | 0.43 | 3.74 | 2.87 | 3.28 | 3.61 | 5.97 | 5.11 | ns |
| | -1 | 0.56 | 3.12 | 0.04 | 1.02 | 1.33 | 0.36 | 3.18 | 2.44 | 2.79 | 3.07 | 5.08 | 4.34 | ns |
| | -2 | 0.49 | 2.74 | 0.03 | 0.90 | 1.17 | 0.32 | 2.79 | 2.14 | 2.45 | 2.70 | 4.46 | 3.81 | ns |
| 16 mA | Std. | 0.66 | 3.46 | 0.04 | 1.20 | 1.57 | 0.43 | 3.53 | 2.61 | 3.33 | 3.72 | 5.76 | 4.84 | ns |
| | -1 | 0.56 | 2.95 | 0.04 | 1.02 | 1.33 | 0.36 | 3.00 | 2.22 | 2.83 | 3.17 | 4.90 | 4.12 | ns |
| | -2 | 0.49 | 2.59 | 0.03 | 0.90 | 1.17 | 0.32 | 2.63 | 1.95 | 2.49 | 2.78 | 4.30 | 3.62 | ns |
| 24 mA | Std. | 0.66 | 3.21 | 0.04 | 1.20 | 1.57 | 0.43 | 3.27 | 2.16 | 3.39 | 4.13 | 5.50 | 4.39 | ns |
| | -1 | 0.56 | 2.73 | 0.04 | 1.02 | 1.33 | 0.36 | 2.78 | 1.83 | 2.88 | 3.51 | 4.68 | 3.74 | ns |
| | -2 | 0.49 | 2.39 | 0.03 | 0.90 | 1.17 | 0.32 | 2.44 | 1.61 | 2.53 | 3.08 | 4.11 | 3.28 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Table 2-106 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.66 | 10.26 | 0.04 | 1.20 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | -1 | 0.56 | 8.72 | 0.04 | 1.02 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | -2 | 0.49 | 7.66 | 0.03 | 0.90 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 8 mA | Std. | 0.66 | 7.27 | 0.04 | 1.20 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | -1 | 0.56 | 6.19 | 0.04 | 1.02 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | -2 | 0.49 | 5.43 | 0.03 | 0.90 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 12 mA | Std. | 0.66 | 5.58 | 0.04 | 1.20 | 0.43 | 5.68 | 4.87 | 3.21 | 3.42 | 7.92 | 7.11 | ns |
| | -1 | 0.56 | 4.75 | 0.04 | 1.02 | 0.36 | 4.84 | 4.14 | 2.73 | 2.91 | 6.74 | 6.05 | ns |
| | -2 | 0.49 | 4.17 | 0.03 | 0.90 | 0.32 | 4.24 | 3.64 | 2.39 | 2.55 | 5.91 | 5.31 | ns |
| 16 mA | Std. | 0.66 | 5.21 | 0.04 | 1.20 | 0.43 | 5.30 | 4.56 | 3.26 | 3.51 | 7.54 | 6.80 | ns |
| | -1 | 0.56 | 4.43 | 0.04 | 1.02 | 0.36 | 4.51 | 3.88 | 2.77 | 2.99 | 6.41 | 5.79 | ns |
| | -2 | 0.49 | 3.89 | 0.03 | 0.90 | 0.32 | 3.96 | 3.41 | 2.43 | 2.62 | 5.63 | 5.08 | ns |
| 24 mA | Std. | 0.66 | 4.85 | 0.04 | 1.20 | 0.43 | 4.94 | 4.54 | 3.32 | 3.88 | 7.18 | 6.78 | ns |
| | -1 | 0.56 | 4.13 | 0.04 | 1.02 | 0.36 | 4.20 | 3.87 | 2.82 | 3.30 | 6.10 | 5.77 | ns |
| | -2 | 0.49 | 3.62 | 0.03 | 0.90 | 0.32 | 3.69 | 3.39 | 2.48 | 2.90 | 5.36 | 5.06 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Table 2-107 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Advanced I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.66 | 7.66 | 0.04 | 1.20 | 0.43 | 7.80 | 6.59 | 2.65 | 2.61 | 10.03 | 8.82 | ns |
| | -1 | 0.56 | 6.51 | 0.04 | 1.02 | 0.36 | 6.63 | 5.60 | 2.25 | 2.22 | 8.54 | 7.51 | ns |
| | -2 | 0.49 | 5.72 | 0.03 | 0.90 | 0.32 | 5.82 | 4.92 | 1.98 | 1.95 | 7.49 | 6.59 | ns |
| 8 mA | Std. | 0.66 | 4.91 | 0.04 | 1.20 | 0.43 | 5.00 | 4.07 | 2.99 | 3.20 | 7.23 | 6.31 | ns |
| | -1 | 0.56 | 4.17 | 0.04 | 1.02 | 0.36 | 4.25 | 3.46 | 2.54 | 2.73 | 6.15 | 5.36 | ns |
| | -2 | 0.49 | 3.66 | 0.03 | 0.90 | 0.32 | 3.73 | 3.04 | 2.23 | 2.39 | 5.40 | 4.71 | ns |
| 12 mA | Std. | 0.66 | 3.53 | 0.04 | 1.20 | 0.43 | 3.60 | 2.82 | 3.21 | 3.58 | 5.83 | 5.06 | ns |
| | -1 | 0.56 | 3.00 | 0.04 | 1.02 | 0.36 | 3.06 | 2.40 | 2.73 | 3.05 | 4.96 | 4.30 | ns |
| | -2 | 0.49 | 2.64 | 0.03 | 0.90 | 0.32 | 2.69 | 2.11 | 2.40 | 2.68 | 4.36 | 3.78 | ns |
| 16 mA | Std. | 0.66 | 3.33 | 0.04 | 1.20 | 0.43 | 3.39 | 2.56 | 3.26 | 3.68 | 5.63 | 4.80 | ns |
| | -1 | 0.56 | 2.83 | 0.04 | 1.02 | 0.36 | 2.89 | 2.18 | 2.77 | 3.13 | 4.79 | 4.08 | ns |
| | -2 | 0.49 | 2.49 | 0.03 | 0.90 | 0.32 | 2.53 | 1.91 | 2.44 | 2.75 | 4.20 | 3.58 | ns |
| 24 mA | Std. | 0.66 | 3.08 | 0.04 | 1.20 | 0.43 | 3.13 | 2.12 | 3.32 | 4.06 | 5.37 | 4.35 | ns |
| | -1 | 0.56 | 2.62 | 0.04 | 1.02 | 0.36 | 2.66 | 1.80 | 2.83 | 3.45 | 4.57 | 3.70 | ns |
| | -2 | 0.49 | 2.30 | 0.03 | 0.90 | 0.32 | 2.34 | 1.58 | 2.48 | 3.03 | 4.01 | 3.25 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-108 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 9.46 | 0.04 | 1.00 | 0.43 | 9.64 | 8.54 | 2.07 | 2.04 | ns |
| | -1 | 0.56 | 8.05 | 0.04 | 0.85 | 0.36 | 8.20 | 7.27 | 1.76 | 1.73 | ns |
| | -2 | 0.49 | 7.07 | 0.03 | 0.75 | 0.32 | 7.20 | 6.38 | 1.55 | 1.52 | ns |
| 4 mA | Std. | 0.66 | 9.46 | 0.04 | 1.00 | 0.43 | 9.64 | 8.54 | 2.07 | 2.04 | ns |
| | -1 | 0.56 | 8.05 | 0.04 | 0.85 | 0.36 | 8.20 | 7.27 | 1.76 | 1.73 | ns |
| | -2 | 0.49 | 7.07 | 0.03 | 0.75 | 0.32 | 7.20 | 6.38 | 1.55 | 1.52 | ns |
| 6 mA | Std. | 0.66 | 6.57 | 0.04 | 1.00 | 0.43 | 6.69 | 5.98 | 2.40 | 2.57 | ns |
| | -1 | 0.56 | 5.59 | 0.04 | 0.85 | 0.36 | 5.69 | 5.09 | 2.04 | 2.19 | ns |
| | -2 | 0.49 | 4.91 | 0.03 | 0.75 | 0.32 | 5.00 | 4.47 | 1.79 | 1.92 | ns |
| 8 mA | Std. | 0.66 | 6.57 | 0.04 | 1.00 | 0.43 | 6.69 | 5.98 | 2.40 | 2.57 | ns |
| | -1 | 0.56 | 5.59 | 0.04 | 0.85 | 0.36 | 5.69 | 5.09 | 2.04 | 2.19 | ns |
| | -2 | 0.49 | 4.91 | 0.03 | 0.75 | 0.32 | 5.00 | 4.47 | 1.79 | 1.92 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-109 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-----------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 7.07 | 0.04 | 1.00 | 0.43 | 7.20 | 6.23 | 2.07 | 2.15 | ns |
| | -1 | 0.56 | 6.01 | 0.04 | 0.85 | 0.36 | 6.12 | 5.30 | 1.76 | 1.83 | ns |
| | -2 ² | 0.49 | 5.28 | 0.03 | 0.75 | 0.32 | 5.37 | 4.65 | 1.55 | 1.60 | ns |
| 4 mA | Std. | 0.66 | 7.07 | 0.04 | 1.00 | 0.43 | 7.20 | 6.23 | 2.07 | 2.15 | ns |
| | -1 | 0.56 | 6.01 | 0.04 | 0.85 | 0.36 | 6.12 | 5.30 | 1.76 | 1.83 | ns |
| | -2 | 0.49 | 5.28 | 0.03 | 0.75 | 0.32 | 5.37 | 4.65 | 1.55 | 1.60 | ns |
| 6 mA | Std. | 0.66 | 4.41 | 0.04 | 1.00 | 0.43 | 4.49 | 3.75 | 2.39 | 2.69 | ns |
| | -1 | 0.56 | 3.75 | 0.04 | 0.85 | 0.36 | 3.82 | 3.19 | 2.04 | 2.29 | ns |
| | -2 | 0.49 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |
| 8 mA | Std. | 0.66 | 4.41 | 0.04 | 1.00 | 0.43 | 4.49 | 3.75 | 2.39 | 2.69 | ns |
| | -1 | 0.56 | 3.75 | 0.04 | 0.85 | 0.36 | 3.82 | 3.19 | 2.04 | 2.29 | ns |
| | -2 | 0.49 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-110 • Minimum and Maximum DC Input and Output Levels

| 2.5 V LVCMOS Drive Strength | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|---|--------|--------|--------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| Applicable to Pro I/O Banks | | | | | | | | | | | | |
| 4 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |
| 12 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 10 | 10 |
| 16 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 16 | 16 | 87 | 83 | 10 | 10 |
| 24 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 24 | 24 | 124 | 169 | 10 | 10 |
| Applicable to Advanced I/O Banks | | | | | | | | | | | | |
| 2 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 2 | 2 | 18 | 16 | 10 | 10 |
| 4 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 6 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 6 | 6 | 37 | 32 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |
| 12 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 10 | 10 |
| 16 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 16 | 16 | 87 | 83 | 10 | 10 |
| 24 mA | -0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 24 | 24 | 124 | 169 | 10 | 10 |
| Applicable to Standard I/O Banks | | | | | | | | | | | | |
| 2 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 2 | 2 | 18 | 16 | 10 | 10 |
| 4 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 6 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 6 | 6 | 37 | 32 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



Figure 2-120 • AC Loading

Table 2-111 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 2.5 | 1.2 | – | 35 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-112 • 2.5 V LVCMOS Low Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Pro I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.60 | 12.00 | 0.04 | 1.51 | 1.66 | 0.43 | 12.23 | 11.61 | 2.72 | 2.20 | 14.46 | 13.85 | ns |
| | -1 | 0.51 | 10.21 | 0.04 | 1.29 | 1.41 | 0.36 | 10.40 | 9.88 | 2.31 | 1.87 | 12.30 | 11.78 | ns |
| | -2 | 0.45 | 8.96 | 0.03 | 1.13 | 1.24 | 0.32 | 9.13 | 8.67 | 2.03 | 1.64 | 10.80 | 10.34 | ns |
| 8 mA | Std. | 0.60 | 8.73 | 0.04 | 1.51 | 1.66 | 0.43 | 8.89 | 8.01 | 3.10 | 2.93 | 11.13 | 10.25 | ns |
| | -1 | 0.51 | 7.43 | 0.04 | 1.29 | 1.41 | 0.36 | 7.57 | 6.82 | 2.64 | 2.49 | 9.47 | 8.72 | ns |
| | -2 | 0.45 | 6.52 | 0.03 | 1.13 | 1.24 | 0.32 | 6.64 | 5.98 | 2.32 | 2.19 | 8.31 | 7.65 | ns |
| 12 mA | Std. | 0.66 | 6.77 | 0.04 | 1.51 | 1.66 | 0.43 | 6.90 | 6.11 | 3.37 | 3.39 | 9.14 | 8.34 | ns |
| | -1 | 0.56 | 5.76 | 0.04 | 1.29 | 1.41 | 0.36 | 5.87 | 5.20 | 2.86 | 2.89 | 7.77 | 7.10 | ns |
| | -2 | 0.49 | 5.06 | 0.03 | 1.13 | 1.24 | 0.32 | 5.15 | 4.56 | 2.51 | 2.53 | 6.82 | 6.23 | ns |
| 16 mA | Std. | 0.66 | 6.31 | 0.04 | 1.51 | 1.66 | 0.43 | 6.42 | 5.73 | 3.42 | 3.52 | 8.66 | 7.96 | ns |
| | -1 | 0.56 | 5.37 | 0.04 | 1.29 | 1.41 | 0.36 | 5.46 | 4.87 | 2.91 | 3.00 | 7.37 | 6.77 | ns |
| | -2 | 0.49 | 4.71 | 0.03 | 1.13 | 1.24 | 0.32 | 4.80 | 4.28 | 2.56 | 2.63 | 6.47 | 5.95 | ns |
| 24 mA | Std. | 0.66 | 5.93 | 0.04 | 1.51 | 1.66 | 0.43 | 6.04 | 5.70 | 3.49 | 4.00 | 8.28 | 7.94 | ns |
| | -1 | 0.56 | 5.05 | 0.04 | 1.29 | 1.41 | 0.36 | 5.14 | 4.85 | 2.97 | 3.40 | 7.04 | 6.75 | ns |
| | -2 | 0.49 | 4.43 | 0.03 | 1.13 | 1.24 | 0.32 | 4.51 | 4.26 | 2.61 | 2.99 | 6.18 | 5.93 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Table 2-113 • 2.5 V LVCMOS High Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Pro I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.60 | 8.82 | 0.04 | 1.51 | 1.66 | 0.43 | 8.13 | 8.82 | 2.72 | 2.29 | 10.37 | 11.05 | ns |
| | -1 | 0.51 | 7.50 | 0.04 | 1.29 | 1.41 | 0.36 | 6.92 | 7.50 | 2.31 | 1.95 | 8.82 | 9.40 | ns |
| | -2 | 0.45 | 6.58 | 0.03 | 1.13 | 1.24 | 0.32 | 6.07 | 6.58 | 2.03 | 1.71 | 7.74 | 8.25 | ns |
| 8 mA | Std. | 0.60 | 5.27 | 0.04 | 1.51 | 1.66 | 0.43 | 5.27 | 5.27 | 3.10 | 3.03 | 7.50 | 7.51 | ns |
| | -1 | 0.51 | 4.48 | 0.04 | 1.29 | 1.41 | 0.36 | 4.48 | 4.48 | 2.64 | 2.58 | 6.38 | 6.38 | ns |
| | -2 | 0.45 | 3.94 | 0.03 | 1.13 | 1.24 | 0.32 | 3.93 | 3.94 | 2.32 | 2.26 | 5.60 | 5.61 | ns |
| 12 mA | Std. | 0.66 | 3.74 | 0.04 | 1.51 | 1.66 | 0.43 | 3.81 | 3.49 | 3.37 | 3.49 | 6.05 | 5.73 | ns |
| | -1 | 0.56 | 3.18 | 0.04 | 1.29 | 1.41 | 0.36 | 3.24 | 2.97 | 2.86 | 2.97 | 5.15 | 4.87 | ns |
| | -2 | 0.49 | 2.80 | 0.03 | 1.13 | 1.24 | 0.32 | 2.85 | 2.61 | 2.51 | 2.61 | 4.52 | 4.28 | ns |
| 16 mA | Std. | 0.66 | 3.53 | 0.04 | 1.51 | 1.66 | 0.43 | 3.59 | 3.12 | 3.42 | 3.62 | 5.83 | 5.35 | ns |
| | -1 | 0.56 | 3.00 | 0.04 | 1.29 | 1.41 | 0.36 | 3.06 | 2.65 | 2.91 | 3.08 | 4.96 | 4.55 | ns |
| | -2 | 0.49 | 2.63 | 0.03 | 1.13 | 1.24 | 0.32 | 2.68 | 2.33 | 2.56 | 2.71 | 4.35 | 4.00 | ns |
| 24 mA | Std. | 0.66 | 3.26 | 0.04 | 1.51 | 1.66 | 0.43 | 3.32 | 2.48 | 3.49 | 4.11 | 5.56 | 4.72 | ns |
| | -1 | 0.56 | 2.77 | 0.04 | 1.29 | 1.41 | 0.36 | 2.83 | 2.11 | 2.97 | 3.49 | 4.73 | 4.01 | ns |
| | -2 | 0.49 | 2.44 | 0.03 | 1.13 | 1.24 | 0.32 | 2.48 | 1.85 | 2.61 | 3.07 | 4.15 | 3.52 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Table 2-114 • 2.5 V LVCMOS Low Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Advanced I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.66 | 11.40 | 0.04 | 1.31 | 0.43 | 11.22 | 11.40 | 2.68 | 2.20 | 13.45 | 13.63 | ns |
| | -1 | 0.56 | 9.69 | 0.04 | 1.11 | 0.36 | 9.54 | 9.69 | 2.28 | 1.88 | 11.44 | 11.60 | ns |
| | -2 | 0.49 | 8.51 | 0.03 | 0.98 | 0.32 | 8.38 | 8.51 | 2.00 | 1.65 | 10.05 | 10.18 | ns |
| 8 mA | Std. | 0.66 | 7.96 | 0.04 | 1.31 | 0.43 | 8.11 | 7.81 | 3.05 | 2.89 | 10.34 | 10.05 | ns |
| | -1 | 0.56 | 6.77 | 0.04 | 1.11 | 0.36 | 6.90 | 6.65 | 2.59 | 2.46 | 8.80 | 8.55 | ns |
| | -2 | 0.49 | 5.94 | 0.03 | 0.98 | 0.32 | 6.05 | 5.84 | 2.28 | 2.16 | 7.72 | 7.50 | ns |
| 12 mA | Std. | 0.66 | 6.18 | 0.04 | 1.31 | 0.43 | 6.29 | 5.92 | 3.30 | 3.32 | 8.53 | 8.15 | ns |
| | -1 | 0.56 | 5.26 | 0.04 | 1.11 | 0.36 | 5.35 | 5.03 | 2.81 | 2.83 | 7.26 | 6.94 | ns |
| | -2 | 0.49 | 4.61 | 0.03 | 0.98 | 0.32 | 4.70 | 4.42 | 2.47 | 2.48 | 6.37 | 6.09 | ns |
| 16 mA | Std. | 0.66 | 6.18 | 0.04 | 1.31 | 0.43 | 6.29 | 5.92 | 3.30 | 3.32 | 8.53 | 8.15 | ns |
| | -1 | 0.56 | 5.26 | 0.04 | 1.11 | 0.36 | 5.35 | 5.03 | 2.81 | 2.83 | 7.26 | 6.94 | ns |
| | -2 | 0.49 | 4.61 | 0.03 | 0.98 | 0.32 | 4.70 | 4.42 | 2.47 | 2.48 | 6.37 | 6.09 | ns |
| 24 mA | Std. | 0.66 | 6.18 | 0.04 | 1.31 | 0.43 | 6.29 | 5.92 | 3.30 | 3.32 | 8.53 | 8.15 | ns |
| | -1 | 0.56 | 5.26 | 0.04 | 1.11 | 0.36 | 5.35 | 5.03 | 2.81 | 2.83 | 7.26 | 6.94 | ns |
| | -2 | 0.49 | 4.61 | 0.03 | 0.98 | 0.32 | 4.70 | 4.42 | 2.47 | 2.48 | 6.37 | 6.09 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Table 2-115 • 2.5 V LVC MOS High Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Advanced I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.66 | 8.66 | 0.04 | 1.31 | 0.43 | 7.83 | 8.66 | 2.68 | 2.30 | 10.07 | 10.90 | ns |
| | -1 | 0.56 | 7.37 | 0.04 | 1.11 | 0.36 | 6.66 | 7.37 | 2.28 | 1.96 | 8.56 | 9.27 | ns |
| | -2 | 0.49 | 6.47 | 0.03 | 0.98 | 0.32 | 5.85 | 6.47 | 2.00 | 1.72 | 7.52 | 8.14 | ns |
| 8 mA | Std. | 0.66 | 5.17 | 0.04 | 1.31 | 0.43 | 5.04 | 5.17 | 3.05 | 3.00 | 7.27 | 7.40 | ns |
| | -1 | 0.56 | 4.39 | 0.04 | 1.11 | 0.36 | 4.28 | 4.39 | 2.59 | 2.55 | 6.19 | 6.30 | ns |
| | -2 | 0.49 | 3.86 | 0.03 | 0.98 | 0.32 | 3.76 | 3.86 | 2.28 | 2.24 | 5.43 | 5.53 | ns |
| 12 mA | Std. | 0.66 | 3.56 | 0.04 | 1.31 | 0.43 | 3.63 | 3.43 | 3.30 | 3.44 | 5.86 | 5.67 | ns |
| | -1 | 0.56 | 3.03 | 0.04 | 1.11 | 0.36 | 3.08 | 2.92 | 2.81 | 2.92 | 4.99 | 4.82 | ns |
| | -2 | 0.49 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |
| 16 mA | Std. | 0.66 | 3.35 | 0.04 | 1.31 | 0.43 | 3.41 | 3.06 | 3.36 | 3.55 | 5.65 | 5.30 | ns |
| | -1 | 0.56 | 2.85 | 0.04 | 1.11 | 0.36 | 2.90 | 2.60 | 2.86 | 3.02 | 4.81 | 4.51 | ns |
| | -2 | 0.49 | 2.50 | 0.03 | 0.98 | 0.32 | 2.55 | 2.29 | 2.51 | 2.65 | 4.22 | 3.96 | ns |
| 24 mA | Std. | 0.66 | 3.56 | 0.04 | 1.31 | 0.43 | 3.63 | 3.43 | 3.30 | 3.44 | 5.86 | 5.67 | ns |
| | -1 | 0.56 | 3.03 | 0.04 | 1.11 | 0.36 | 3.08 | 2.92 | 2.81 | 2.92 | 4.99 | 4.82 | ns |
| | -2 | 0.49 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Table 2-116 • 2.5 V LVC MOS Low Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Standard I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 11.00 | 0.04 | 1.29 | 0.43 | 10.37 | 11.00 | 2.03 | 1.83 | ns |
| | -1 | 0.56 | 9.35 | 0.04 | 1.10 | 0.36 | 8.83 | 9.35 | 1.73 | 1.56 | ns |
| | -2 | 0.49 | 8.21 | 0.03 | 0.96 | 0.32 | 7.75 | 8.21 | 1.52 | 1.37 | ns |
| 4 mA | Std. | 0.66 | 11.00 | 0.04 | 1.29 | 0.43 | 10.37 | 11.00 | 2.03 | 1.83 | ns |
| | -1 | 0.56 | 9.35 | 0.04 | 1.10 | 0.36 | 8.83 | 9.35 | 1.73 | 1.56 | ns |
| | -2 | 0.49 | 8.21 | 0.03 | 0.96 | 0.32 | 7.75 | 8.21 | 1.52 | 1.37 | ns |
| 6 mA | Std. | 0.66 | 7.50 | 0.04 | 1.29 | 0.43 | 7.36 | 7.50 | 2.39 | 2.46 | ns |
| | -1 | 0.56 | 6.38 | 0.04 | 1.10 | 0.36 | 6.26 | 6.38 | 2.03 | 2.10 | ns |
| | -2 | 0.49 | 5.60 | 0.03 | 0.96 | 0.32 | 5.49 | 5.60 | 1.78 | 1.84 | ns |
| 8 mA | Std. | 0.66 | 7.50 | 0.04 | 1.29 | 0.43 | 7.36 | 7.50 | 2.39 | 2.46 | ns |
| | -1 | 0.56 | 6.38 | 0.04 | 1.10 | 0.36 | 6.26 | 6.38 | 2.03 | 2.10 | ns |
| | -2 | 0.49 | 5.60 | 0.03 | 0.96 | 0.32 | 5.49 | 5.60 | 1.78 | 1.84 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Table 2-117 • 2.5 V LVCMOS High Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 8.20 | 0.04 | 1.29 | 0.43 | 7.24 | 8.20 | 2.03 | 1.91 | ns |
| | -1 | 0.56 | 6.98 | 0.04 | 1.10 | 0.36 | 6.16 | 6.98 | 1.73 | 1.62 | ns |
| | -2 | 0.49 | 6.13 | 0.03 | 0.96 | 0.32 | 5.41 | 6.13 | 1.52 | 1.43 | ns |
| 4 mA | Std. | 0.66 | 8.20 | 0.04 | 1.29 | 0.43 | 7.24 | 8.20 | 2.03 | 1.91 | ns |
| | -1 | 0.56 | 6.98 | 0.04 | 1.10 | 0.36 | 6.16 | 6.98 | 1.73 | 1.62 | ns |
| | -2 | 0.49 | 6.13 | 0.03 | 0.96 | 0.32 | 5.41 | 6.13 | 1.52 | 1.43 | ns |
| 6 mA | Std. | 0.66 | 4.77 | 0.04 | 1.29 | 0.43 | 4.55 | 4.77 | 2.38 | 2.55 | ns |
| | -1 | 0.56 | 4.05 | 0.04 | 1.10 | 0.36 | 3.87 | 4.05 | 2.03 | 2.17 | ns |
| | -2 | 0.49 | 3.56 | 0.03 | 0.96 | 0.32 | 3.40 | 3.56 | 1.78 | 1.91 | ns |
| 8 mA | Std. | 0.66 | 4.77 | 0.04 | 1.29 | 0.43 | 4.55 | 4.77 | 2.38 | 2.55 | ns |
| | -1 | 0.56 | 4.05 | 0.04 | 1.10 | 0.36 | 3.87 | 4.05 | 2.03 | 2.17 | ns |
| | -2 | 0.49 | 3.56 | 0.03 | 0.96 | 0.32 | 3.40 | 3.56 | 1.78 | 1.91 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and push-pull output buffer.

Table 2-118 • Minimum and Maximum DC Input and Output Levels

| 1.8 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|---|--------|-------------|-------------|--------|--------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| Applicable to Pro I/O Banks | | | | | | | | | | | | |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 8 | 8 | 51 | 45 | 10 | 10 |
| 12 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 12 | 12 | 74 | 91 | 10 | 10 |
| 16 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 16 | 16 | 74 | 91 | 10 | 10 |
| Applicable to Advanced I/O Banks | | | | | | | | | | | | |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 8 | 8 | 51 | 45 | 10 | 10 |
| 12 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 12 | 12 | 74 | 91 | 10 | 10 |
| 16 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI - 0.45 | 16 | 16 | 74 | 91 | 10 | 10 |
| Applicable to Standard I/O Banks | | | | | | | | | | | | |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

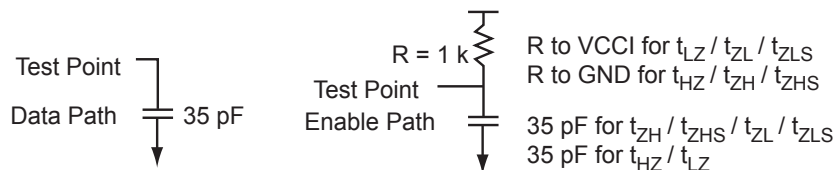


Figure 2-121 • AC Loading

Table 2-119 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input Low (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|---------------|----------------------|-----------------|------------------------|
| 0 | 1.8 | 0.9 | - | 35 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics
Table 2-120 • 1.8 V LVCMOS Low Slew

 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,

 Worst-Case $V_{CCI} = 1.7\text{ V}$

Applicable to Pro I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 15.84 | 0.04 | 1.45 | 1.91 | 0.43 | 15.65 | 15.84 | 2.78 | 1.58 | 17.89 | 18.07 | ns |
| | -1 | 0.56 | 13.47 | 0.04 | 1.23 | 1.62 | 0.36 | 13.31 | 13.47 | 2.37 | 1.35 | 15.22 | 15.37 | ns |
| | -2 | 0.49 | 11.83 | 0.03 | 1.08 | 1.42 | 0.32 | 11.69 | 11.83 | 2.08 | 1.18 | 13.36 | 13.50 | ns |
| 4 mA | Std. | 0.66 | 11.39 | 0.04 | 1.45 | 1.91 | 0.43 | 11.60 | 10.76 | 3.26 | 2.77 | 13.84 | 12.99 | ns |
| | -1 | 0.56 | 9.69 | 0.04 | 1.23 | 1.62 | 0.36 | 9.87 | 9.15 | 2.77 | 2.36 | 11.77 | 11.05 | ns |
| | -2 | 0.49 | 8.51 | 0.03 | 1.08 | 1.42 | 0.32 | 8.66 | 8.03 | 2.43 | 2.07 | 10.33 | 9.70 | ns |
| 8 mA | Std. | 0.66 | 8.97 | 0.04 | 1.45 | 1.91 | 0.43 | 9.14 | 8.10 | 3.57 | 3.36 | 11.37 | 10.33 | ns |
| | -1 | 0.56 | 7.63 | 0.04 | 1.23 | 1.62 | 0.36 | 7.77 | 6.89 | 3.04 | 2.86 | 9.67 | 8.79 | ns |
| | -2 | 0.49 | 6.70 | 0.03 | 1.08 | 1.42 | 0.32 | 6.82 | 6.05 | 2.66 | 2.51 | 8.49 | 7.72 | ns |
| 12 mA | Std. | 0.66 | 8.35 | 0.04 | 1.45 | 1.91 | 0.43 | 8.50 | 7.59 | 3.64 | 3.52 | 10.74 | 9.82 | ns |
| | -1 | 0.56 | 7.10 | 0.04 | 1.23 | 1.62 | 0.36 | 7.23 | 6.45 | 3.10 | 3.00 | 9.14 | 8.35 | ns |
| | -2 | 0.49 | 6.24 | 0.03 | 1.08 | 1.42 | 0.32 | 6.35 | 5.66 | 2.72 | 2.63 | 8.02 | 7.33 | ns |
| 16 mA | Std. | 0.66 | 7.94 | 0.04 | 1.45 | 1.91 | 0.43 | 8.09 | 7.56 | 3.74 | 4.11 | 10.32 | 9.80 | ns |
| | -1 | 0.56 | 6.75 | 0.04 | 1.23 | 1.62 | 0.36 | 6.88 | 6.43 | 3.18 | 3.49 | 8.78 | 8.33 | ns |
| | -2 | 0.49 | 5.93 | 0.03 | 1.08 | 1.42 | 0.32 | 6.04 | 5.65 | 2.79 | 3.07 | 7.71 | 7.32 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Table 2-121 • 1.8 V LVC MOS High Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 1.7\text{ V}$
Applicable to Pro I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 12.10 | 0.04 | 1.45 | 1.91 | 0.43 | 9.59 | 12.10 | 2.78 | 1.64 | 11.83 | 14.34 | ns |
| | -1 | 0.56 | 10.30 | 0.04 | 1.23 | 1.62 | 0.36 | 8.16 | 10.30 | 2.37 | 1.39 | 10.06 | 12.20 | ns |
| | -2 | 0.49 | 9.04 | 0.03 | 1.08 | 1.42 | 0.32 | 7.16 | 9.04 | 2.08 | 1.22 | 8.83 | 10.71 | ns |
| 4 mA | Std. | 0.66 | 7.05 | 0.04 | 1.45 | 1.91 | 0.43 | 6.20 | 7.05 | 3.25 | 2.86 | 8.44 | 9.29 | ns |
| | -1 | 0.56 | 6.00 | 0.04 | 1.23 | 1.62 | 0.36 | 5.28 | 6.00 | 2.76 | 2.44 | 7.18 | 7.90 | ns |
| | -2 | 0.49 | 5.27 | 0.03 | 1.08 | 1.42 | 0.32 | 4.63 | 5.27 | 2.43 | 2.14 | 6.30 | 6.94 | ns |
| 8 mA | Std. | 0.66 | 4.52 | 0.04 | 1.45 | 1.91 | 0.43 | 4.47 | 4.52 | 3.57 | 3.47 | 6.70 | 6.76 | ns |
| | -1 | 0.56 | 3.85 | 0.04 | 1.23 | 1.62 | 0.36 | 3.80 | 3.85 | 3.04 | 2.95 | 5.70 | 5.75 | ns |
| | -2 | 0.49 | 3.38 | 0.03 | 1.08 | 1.42 | 0.32 | 3.33 | 3.38 | 2.66 | 2.59 | 5.00 | 5.05 | ns |
| 12 mA | Std. | 0.66 | 4.12 | 0.04 | 1.45 | 1.91 | 0.43 | 4.20 | 3.99 | 3.63 | 3.62 | 6.43 | 6.23 | ns |
| | -1 | 0.56 | 3.51 | 0.04 | 1.23 | 1.62 | 0.36 | 3.57 | 3.40 | 3.09 | 3.08 | 5.47 | 5.30 | ns |
| | -2 | 0.49 | 3.08 | 0.03 | 1.08 | 1.42 | 0.32 | 3.14 | 2.98 | 2.71 | 2.71 | 4.81 | 4.65 | ns |
| 16 mA | Std. | 0.66 | 3.80 | 0.04 | 1.45 | 1.91 | 0.43 | 3.87 | 3.09 | 3.73 | 4.24 | 6.10 | 5.32 | ns |
| | -1 | 0.56 | 3.23 | 0.04 | 1.23 | 1.62 | 0.36 | 3.29 | 2.63 | 3.18 | 3.60 | 5.19 | 4.53 | ns |
| | -2 | 0.49 | 2.83 | 0.03 | 1.08 | 1.42 | 0.32 | 2.89 | 2.31 | 2.79 | 3.16 | 4.56 | 3.98 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

Table 2-122 • 1.8 V LVCMOS Low Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Advanced I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-----------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 15.53 | 0.04 | 1.31 | 0.43 | 14.11 | 15.53 | 2.78 | 1.60 | 16.35 | 17.77 | ns |
| | -1 | 0.56 | 13.21 | 0.04 | 1.11 | 0.36 | 12.01 | 13.21 | 2.36 | 1.36 | 13.91 | 15.11 | ns |
| | -2 ² | 0.49 | 11.60 | 0.03 | 0.98 | 0.32 | 10.54 | 11.60 | 2.07 | 1.19 | 12.21 | 13.27 | ns |
| 4 mA | Std. | 0.66 | 10.48 | 0.04 | 1.31 | 0.43 | 10.41 | 10.48 | 3.23 | 2.73 | 12.65 | 12.71 | ns |
| | -1 | 0.56 | 8.91 | 0.04 | 1.11 | 0.36 | 8.86 | 8.91 | 2.75 | 2.33 | 10.76 | 10.81 | ns |
| | -2 | 0.49 | 7.82 | 0.03 | 0.98 | 0.32 | 7.77 | 7.82 | 2.41 | 2.04 | 9.44 | 9.49 | ns |
| 8 mA | Std. | 0.66 | 8.05 | 0.04 | 1.31 | 0.43 | 8.20 | 7.84 | 3.54 | 3.27 | 10.43 | 10.08 | ns |
| | -1 | 0.56 | 6.85 | 0.04 | 1.11 | 0.36 | 6.97 | 6.67 | 3.01 | 2.78 | 8.88 | 8.57 | ns |
| | -2 | 0.49 | 6.01 | 0.03 | 0.98 | 0.32 | 6.12 | 5.86 | 2.64 | 2.44 | 7.79 | 7.53 | ns |
| 12 mA | Std. | 0.66 | 7.50 | 0.04 | 1.31 | 0.43 | 7.64 | 7.30 | 3.61 | 3.41 | 9.88 | 9.53 | ns |
| | -1 | 0.56 | 6.38 | 0.04 | 1.11 | 0.36 | 6.50 | 6.21 | 3.07 | 2.90 | 8.40 | 8.11 | ns |
| | -2 | 0.49 | 5.60 | 0.03 | 0.98 | 0.32 | 5.71 | 5.45 | 2.69 | 2.55 | 7.38 | 7.12 | ns |
| 16 mA | Std. | 0.66 | 7.29 | 0.04 | 1.31 | 0.43 | 7.23 | 7.29 | 3.71 | 3.95 | 9.47 | 9.53 | ns |
| | -1 | 0.56 | 6.20 | 0.04 | 1.11 | 0.36 | 6.15 | 6.20 | 3.15 | 3.36 | 8.06 | 8.11 | ns |
| | -2 | 0.49 | 5.45 | 0.03 | 0.98 | 0.32 | 5.40 | 5.45 | 2.77 | 2.95 | 7.07 | 7.12 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Table 2-123 • 1.8 V LVC MOS High Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Advanced I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 11.86 | 0.04 | 1.22 | 0.43 | 9.14 | 11.86 | 2.77 | 1.66 | 11.37 | 14.10 | ns |
| | -1 | 0.56 | 10.09 | 0.04 | 1.04 | 0.36 | 7.77 | 10.09 | 2.36 | 1.41 | 9.67 | 11.99 | ns |
| | -2 | 0.49 | 8.86 | 0.03 | 0.91 | 0.32 | 6.82 | 8.86 | 2.07 | 1.24 | 8.49 | 10.53 | ns |
| 4 mA | Std. | 0.66 | 6.91 | 0.04 | 1.22 | 0.43 | 5.86 | 6.91 | 3.22 | 2.84 | 8.10 | 9.15 | ns |
| | -1 | 0.56 | 5.88 | 0.04 | 1.04 | 0.36 | 4.99 | 5.88 | 2.74 | 2.41 | 6.89 | 7.78 | ns |
| | -2 | 0.49 | 5.16 | 0.03 | 0.91 | 0.32 | 4.38 | 5.16 | 2.41 | 2.12 | 6.05 | 6.83 | ns |
| 8 mA | Std. | 0.66 | 4.45 | 0.04 | 1.22 | 0.43 | 4.18 | 4.45 | 3.53 | 3.38 | 6.42 | 6.68 | ns |
| | -1 | 0.56 | 3.78 | 0.04 | 1.04 | 0.36 | 3.56 | 3.78 | 3.00 | 2.88 | 5.46 | 5.69 | ns |
| | -2 | 0.49 | 3.32 | 0.03 | 0.91 | 0.32 | 3.12 | 3.32 | 2.64 | 2.53 | 4.79 | 4.99 | ns |
| 12 mA | Std. | 0.66 | 3.92 | 0.04 | 1.22 | 0.43 | 3.93 | 3.92 | 3.60 | 3.52 | 6.16 | 6.16 | ns |
| | -1 | 0.56 | 3.34 | 0.04 | 1.04 | 0.36 | 3.34 | 3.34 | 3.06 | 3.00 | 5.24 | 5.24 | ns |
| | -2 | 0.49 | 2.93 | 0.03 | 0.91 | 0.32 | 2.93 | 2.93 | 2.69 | 2.63 | 4.60 | 4.60 | ns |
| 16 mA | Std. | 0.66 | 3.53 | 0.04 | 1.22 | 0.43 | 3.60 | 3.04 | 3.70 | 4.08 | 5.84 | 5.28 | ns |
| | -1 | 0.56 | 3.01 | 0.04 | 1.04 | 0.36 | 3.06 | 2.59 | 3.15 | 3.47 | 4.96 | 4.49 | ns |
| | -2 | 0.49 | 2.64 | 0.03 | 0.91 | 0.32 | 2.69 | 2.27 | 2.76 | 3.05 | 4.36 | 3.94 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

Table 2-124 • 1.8 V LVC MOS Low Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Standard I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 15.01 | 0.04 | 1.20 | 0.43 | 13.15 | 15.01 | 1.99 | 1.99 | ns |
| | -1 | 0.56 | 12.77 | 0.04 | 1.02 | 0.36 | 11.19 | 12.77 | 1.70 | 1.70 | ns |
| | -2 | 0.49 | 11.21 | 0.03 | 0.90 | 0.32 | 9.82 | 11.21 | 1.49 | 1.49 | ns |
| 4 mA | Std. | 0.66 | 10.10 | 0.04 | 1.20 | 0.43 | 9.55 | 10.10 | 2.41 | 2.37 | ns |
| | -1 | 0.56 | 8.59 | 0.04 | 1.02 | 0.36 | 8.13 | 8.59 | 2.05 | 2.02 | ns |
| | -2 | 0.49 | 7.54 | 0.03 | 0.90 | 0.32 | 7.13 | 7.54 | 1.80 | 1.77 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

Table 2-125 • 1.8 V LVC MOS High Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 1.7\text{ V}$
Applicable to Standard I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 11.21 | 0.04 | 1.20 | 0.43 | 8.53 | 11.21 | 1.99 | 1.21 | ns |
| | -1 | 0.56 | 9.54 | 0.04 | 1.02 | 0.36 | 7.26 | 9.54 | 1.69 | 1.03 | ns |
| | -2 | 0.49 | 8.37 | 0.03 | 0.90 | 0.32 | 6.37 | 8.37 | 1.49 | 0.90 | ns |
| 4 mA | Std. | 0.66 | 6.34 | 0.04 | 1.20 | 0.43 | 5.38 | 6.34 | 2.41 | 2.48 | ns |
| | -1 | 0.56 | 5.40 | 0.04 | 1.02 | 0.36 | 4.58 | 5.40 | 2.05 | 2.11 | ns |
| | -2 | 0.49 | 4.74 | 0.03 | 0.90 | 0.32 | 4.02 | 4.74 | 1.80 | 1.85 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and push-pull output buffer.

Table 2-126 • Minimum and Maximum DC Input and Output Levels

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|---|--------|-------------|-------------|--------|-------------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| Applicable to Pro I/O Banks | | | | | | | | | | | | |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 16 | 13 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 33 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 6 | 6 | 39 | 32 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 8 | 8 | 55 | 66 | 10 | 10 |
| 12 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 | 55 | 66 | 10 | 10 |
| Applicable to Advanced I/O Banks | | | | | | | | | | | | |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 16 | 13 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 33 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 6 | 6 | 39 | 32 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 8 | 8 | 55 | 66 | 10 | 10 |
| 12 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 | 55 | 66 | 10 | 10 |
| Applicable to Pro I/O Banks | | | | | | | | | | | | |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 16 | 13 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.
2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



Figure 2-122 • AC Loading

Table 2-127 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 1.5 | 0.75 | - | 35 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-128 • 1.5 V LVCMOS Low Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 1.4\text{ V}$
 Applicable to Pro I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 14.11 | 0.04 | 1.70 | 2.14 | 0.43 | 14.37 | 13.14 | 3.40 | 2.68 | 16.61 | 15.37 | ns |
| | -1 | 0.56 | 12.00 | 0.04 | 1.44 | 1.82 | 0.36 | 12.22 | 11.17 | 2.90 | 2.28 | 14.13 | 13.08 | ns |
| | -2 | 0.49 | 10.54 | 0.03 | 1.27 | 1.60 | 0.32 | 10.73 | 9.81 | 2.54 | 2.00 | 12.40 | 11.48 | ns |
| 4 mA | Std. | 0.66 | 11.23 | 0.04 | 1.70 | 2.14 | 0.43 | 11.44 | 9.87 | 3.77 | 3.36 | 13.68 | 12.10 | ns |
| | -1 | 0.56 | 9.55 | 0.04 | 1.44 | 1.82 | 0.36 | 9.73 | 8.39 | 3.21 | 2.86 | 11.63 | 10.29 | ns |
| | -2 | 0.49 | 8.39 | 0.03 | 1.27 | 1.60 | 0.32 | 8.54 | 7.37 | 2.81 | 2.51 | 10.21 | 9.04 | ns |
| 8 mA | Std. | 0.66 | 10.45 | 0.04 | 1.70 | 2.14 | 0.43 | 10.65 | 9.24 | 3.84 | 3.55 | 12.88 | 11.48 | ns |
| | -1 | 0.56 | 8.89 | 0.04 | 1.44 | 1.82 | 0.36 | 9.06 | 7.86 | 3.27 | 3.02 | 10.96 | 9.76 | ns |
| | -2 | 0.49 | 7.81 | 0.03 | 1.27 | 1.60 | 0.32 | 7.95 | 6.90 | 2.87 | 2.65 | 9.62 | 8.57 | ns |
| 12 mA | Std. | 0.66 | 10.02 | 0.04 | 1.70 | 2.14 | 0.43 | 10.20 | 9.23 | 3.97 | 4.22 | 12.44 | 11.47 | ns |
| | -1 | 0.56 | 8.52 | 0.04 | 1.44 | 1.82 | 0.36 | 8.68 | 7.85 | 3.38 | 3.59 | 10.58 | 9.75 | ns |
| | -2 | 0.49 | 7.48 | 0.03 | 1.27 | 1.60 | 0.32 | 7.62 | 6.89 | 2.97 | 3.15 | 9.29 | 8.56 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-129 • 1.5 V LVCMOS High Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 1.4\text{ V}$
 Applicable to Pro I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 8.53 | 0.04 | 1.70 | 2.14 | 0.43 | 7.26 | 8.53 | 3.39 | 2.79 | 9.50 | 10.77 | ns |
| | -1 | 0.56 | 7.26 | 0.04 | 1.44 | 1.82 | 0.36 | 6.18 | 7.26 | 2.89 | 2.37 | 8.08 | 9.16 | ns |
| | -2 | 0.49 | 6.37 | 0.03 | 1.27 | 1.60 | 0.32 | 5.42 | 6.37 | 2.53 | 2.08 | 7.09 | 8.04 | ns |
| 4 mA | Std. | 0.66 | 5.41 | 0.04 | 1.70 | 2.14 | 0.43 | 5.22 | 5.41 | 3.75 | 3.48 | 7.45 | 7.65 | ns |
| | -1 | 0.56 | 4.60 | 0.04 | 1.44 | 1.82 | 0.36 | 4.44 | 4.60 | 3.19 | 2.96 | 6.34 | 6.50 | ns |
| | -2 | 0.49 | 4.04 | 0.03 | 1.27 | 1.60 | 0.32 | 3.89 | 4.04 | 2.80 | 2.60 | 5.56 | 5.71 | ns |
| 8 mA | Std. | 0.66 | 4.80 | 0.04 | 1.70 | 2.14 | 0.43 | 4.89 | 4.75 | 3.83 | 3.67 | 7.13 | 6.98 | ns |
| | -1 | 0.56 | 4.09 | 0.04 | 1.44 | 1.82 | 0.36 | 4.16 | 4.04 | 3.26 | 3.12 | 6.06 | 5.94 | ns |
| | -2 | 0.49 | 3.59 | 0.03 | 1.27 | 1.60 | 0.32 | 3.65 | 3.54 | 2.86 | 2.74 | 5.32 | 5.21 | ns |
| 12 mA | Std. | 0.66 | 4.42 | 0.04 | 1.70 | 2.14 | 0.43 | 4.50 | 3.62 | 3.96 | 4.37 | 6.74 | 5.86 | ns |
| | -1 | 0.56 | 3.76 | 0.04 | 1.44 | 1.82 | 0.36 | 3.83 | 3.08 | 3.37 | 3.72 | 5.73 | 4.98 | ns |
| | -2 | 0.49 | 3.30 | 0.03 | 1.27 | 1.60 | 0.32 | 3.36 | 2.70 | 2.96 | 3.27 | 5.03 | 4.37 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-130 • 1.5 V LVC MOS Low Slew

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 1.4\text{ V}$
 Applicable to Advanced I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 12.78 | 0.04 | 1.31 | 0.43 | 12.81 | 12.78 | 3.40 | 2.64 | 15.05 | 15.02 | ns |
| | -1 | 0.56 | 10.87 | 0.04 | 1.11 | 0.36 | 10.90 | 10.87 | 2.89 | 2.25 | 12.80 | 12.78 | ns |
| | -2 | 0.49 | 9.55 | 0.03 | 0.98 | 0.32 | 9.57 | 9.55 | 2.54 | 1.97 | 11.24 | 11.22 | ns |
| 4 mA | Std. | 0.66 | 10.01 | 0.04 | 1.31 | 0.43 | 10.19 | 9.55 | 3.75 | 3.27 | 12.43 | 11.78 | ns |
| | -1 | 0.56 | 8.51 | 0.04 | 1.11 | 0.36 | 8.67 | 8.12 | 3.19 | 2.78 | 10.57 | 10.02 | ns |
| | -2 | 0.49 | 7.47 | 0.03 | 0.98 | 0.32 | 7.61 | 7.13 | 2.80 | 2.44 | 9.28 | 8.80 | ns |
| 8 mA | Std. | 0.66 | 9.33 | 0.04 | 1.31 | 0.43 | 9.51 | 8.89 | 3.83 | 3.43 | 11.74 | 11.13 | ns |
| | -1 | 0.56 | 7.94 | 0.04 | 1.11 | 0.36 | 8.09 | 7.56 | 3.26 | 2.92 | 9.99 | 9.47 | ns |
| | -2 | 0.49 | 6.97 | 0.03 | 0.98 | 0.32 | 7.10 | 6.64 | 2.86 | 2.56 | 8.77 | 8.31 | ns |
| 12 mA | Std. | 0.66 | 8.91 | 0.04 | 1.31 | 0.43 | 9.07 | 8.89 | 3.95 | 4.05 | 11.31 | 11.13 | ns |
| | -1 | 0.56 | 7.58 | 0.04 | 1.11 | 0.36 | 7.72 | 7.57 | 3.36 | 3.44 | 9.62 | 9.47 | ns |
| | -2 | 0.49 | 6.65 | 0.03 | 0.98 | 0.32 | 6.78 | 6.64 | 2.95 | 3.02 | 8.45 | 8.31 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

Table 2-131 • 1.5 V LVC MOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 1.4\text{ V}$
 Applicable to Advanced I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 8.36 | 0.04 | 1.44 | 0.43 | 6.82 | 8.36 | 3.39 | 2.77 | 9.06 | 10.60 | ns |
| | -1 | 0.56 | 7.11 | 0.04 | 1.22 | 0.36 | 5.80 | 7.11 | 2.88 | 2.35 | 7.71 | 9.02 | ns |
| | -2 | 0.49 | 6.24 | 0.03 | 1.07 | 0.32 | 5.10 | 6.24 | 2.53 | 2.06 | 6.76 | 7.91 | ns |
| 4 mA | Std. | 0.66 | 5.31 | 0.04 | 1.44 | 0.43 | 4.85 | 5.31 | 3.74 | 3.40 | 7.09 | 7.55 | ns |
| | -1 | 0.56 | 4.52 | 0.04 | 1.22 | 0.36 | 4.13 | 4.52 | 3.18 | 2.89 | 6.03 | 6.42 | ns |
| | -2 | 0.49 | 3.97 | 0.03 | 1.07 | 0.32 | 3.62 | 3.97 | 2.79 | 2.54 | 5.29 | 5.64 | ns |
| 8 mA | Std. | 0.66 | 4.67 | 0.04 | 1.44 | 0.43 | 4.55 | 4.67 | 3.82 | 3.56 | 6.78 | 6.90 | ns |
| | -1 | 0.56 | 3.97 | 0.04 | 1.22 | 0.36 | 3.87 | 3.97 | 3.25 | 3.03 | 5.77 | 5.87 | ns |
| | -2 | 0.49 | 3.49 | 0.03 | 1.07 | 0.32 | 3.40 | 3.49 | 2.85 | 2.66 | 5.07 | 5.16 | ns |
| 12 mA | Std. | 0.66 | 4.08 | 0.04 | 1.44 | 0.43 | 4.15 | 3.58 | 3.94 | 4.20 | 6.39 | 5.81 | ns |
| | -1 | 0.56 | 3.47 | 0.04 | 1.22 | 0.36 | 3.53 | 3.04 | 3.36 | 3.58 | 5.44 | 4.95 | ns |
| | -2 | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

Table 2-132 • 1.5 V LVCMOS Low Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 1.4\text{ V}$
 Applicable to Standard I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 12.33 | 0.04 | 1.42 | 0.43 | 11.79 | 12.33 | 2.45 | 2.32 | ns |
| | -1 | 0.56 | 10.49 | 0.04 | 1.21 | 0.36 | 10.03 | 10.49 | 2.08 | 1.98 | ns |
| | -2 | 0.49 | 9.21 | 0.03 | 1.06 | 0.32 | 8.81 | 9.21 | 1.83 | 1.73 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

Table 2-133 • 1.5 V LVCMOS High Slew
 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 1.4\text{ V}$
 Applicable to Standard I/Os

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA | Std. | 0.66 | 7.65 | 0.04 | 1.42 | 0.43 | 6.31 | 7.65 | 2.45 | 2.45 | ns |
| | -1 | 0.56 | 6.50 | 0.04 | 1.21 | 0.36 | 5.37 | 6.50 | 2.08 | 2.08 | ns |
| | -2 | 0.49 | 5.71 | 0.03 | 1.06 | 0.32 | 4.71 | 5.71 | 1.83 | 1.83 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

3.3 V PCI, 3.3 V PCI-X

The Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-134 • Minimum and Maximum DC Input and Output Levels

| 3.3 V PCI/PCI-X | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|-----------------------|----------------|--------|--------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| Per PCI specification | Per PCI curves | | | | | | | | | | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in [Figure 2-123](#).

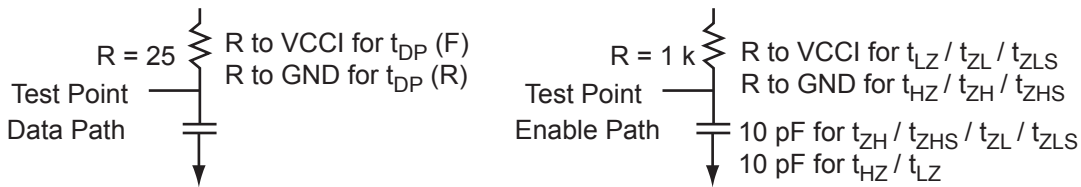


Figure 2-123 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the data path; Microsemi loading for tristate is described in [Table 2-135](#).

Table 2-135 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|--|-----------------|------------------------|
| 0 | 3.3 | 0.285 * VCCI for t _{DP(R)} 0.615 * VCCI for t _{DP(F)} | – | 10 |

Note: *Measuring point = Vtrip. See [Table 2-90](#) on [page 2-166](#) for a complete table of trip points.

Timing Characteristics
Table 2-136 • 3.3 V PCI/PCI-X

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = 3.0 V
 Applicable to Pro I/Os

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| Std. | 0.66 | 2.81 | 0.04 | 1.05 | 1.67 | 0.43 | 2.86 | 2.00 | 3.28 | 3.61 | 5.09 | 4.23 | ns |
| -1 | 0.56 | 2.39 | 0.04 | 0.89 | 1.42 | 0.36 | 2.43 | 1.70 | 2.79 | 3.07 | 4.33 | 3.60 | ns |
| -2 | 0.49 | 2.09 | 0.03 | 0.78 | 1.25 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Table 2-137 • 3.3 V PCI/PCI-X

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = 3.0 V
 Applicable to Advanced I/Os

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| Std. | 0.66 | 2.68 | 0.04 | 0.86 | 0.43 | 2.73 | 1.95 | 3.21 | 3.58 | 4.97 | 4.19 | 0.66 | ns |
| -1 | 0.56 | 2.28 | 0.04 | 0.73 | 0.36 | 2.32 | 1.66 | 2.73 | 3.05 | 4.22 | 3.56 | 0.56 | ns |
| -2 | 0.49 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | 0.49 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

Voltage Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-138 • Minimum and Maximum DC Input and Output Levels

| 3.3 V GTL Drive Strength | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|--------------------------------|-----------|-------------|-------------|-----------|-----------|-----------|-----|-----|-----------------|-----------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | mA ³ | mA ³ | μA ⁴ | μA ⁴ |
| 20 mA ³ | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 | 181 | 268 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

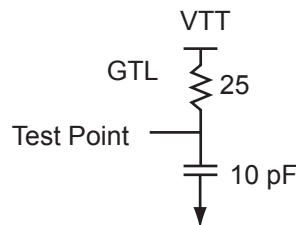


Figure 2-124 • AC Loading

Table 2-139 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.05 | VREF + 0.05 | 0.8 | 0.8 | 1.2 | 10 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-140 • 3.3 V GTL

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = 3.0 V, VREF = 0.8 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.08 | 0.04 | 2.93 | 0.43 | 2.04 | 2.08 | | | 4.27 | 4.31 | ns |
| -1 | 0.56 | 1.77 | 0.04 | 2.50 | 0.36 | 1.73 | 1.77 | | | 3.63 | 3.67 | ns |
| -2 | 0.49 | 1.55 | 0.03 | 2.19 | 0.32 | 1.52 | 1.55 | | | 3.19 | 3.22 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-141 • Minimum and Maximum DC Input and Output Levels

| 2.5 GTL | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|--------------------|--------|-------------|-------------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 20 mA ³ | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 | 124 | 169 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.



Figure 2-125 • AC Loading

Table 2-142 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.05 | VREF + 0.05 | 0.8 | 0.8 | 1.2 | 10 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-143 • 2.5 V GTL

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 0.8 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.13 | 0.04 | 2.46 | 0.43 | 2.16 | 2.13 | | | 4.40 | 4.36 | ns |
| -1 | 0.56 | 1.81 | 0.04 | 2.09 | 0.36 | 1.84 | 1.81 | | | 3.74 | 3.71 | ns |
| -2 | 0.49 | 1.59 | 0.03 | 1.83 | 0.32 | 1.61 | 1.59 | | | 3.28 | 3.26 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-144 • Minimum and Maximum DC Input and Output Levels

| 3.3 V GTL+ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|------------|--------|------------|------------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 35 mA | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 35 | 35 | 181 | 268 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

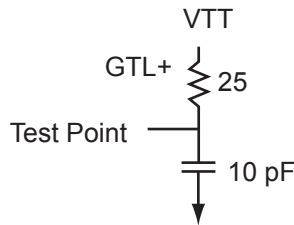


Figure 2-126 • AC Loading

Table 2-145 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 1.0 | 1.0 | 1.5 | 10 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-146 • 3.3 V GTL+

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.0 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.06 | 0.04 | 1.59 | 0.43 | 2.09 | 2.06 | | | 4.33 | 4.29 | ns |
| -1 | 0.56 | 1.75 | 0.04 | 1.35 | 0.36 | 1.78 | 1.75 | | | 3.68 | 3.65 | ns |
| -2 | 0.49 | 1.53 | 0.03 | 1.19 | 0.32 | 1.56 | 1.53 | | | 3.23 | 3.20 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-147 • Minimum and Maximum DC Input and Output Levels

| 2.5 V GTL+ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|------------|--------|------------|------------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 33 mA | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 33 | 33 | 124 | 169 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.



Figure 2-127 • AC Loading

Table 2-148 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 1.0 | 1.0 | 1.5 | 10 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-149 • 2.5 V GTL+

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.0 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.21 | 0.04 | 1.51 | 0.43 | 2.25 | 2.10 | | | 4.48 | 4.34 | ns |
| -1 | 0.56 | 1.88 | 0.04 | 1.29 | 0.36 | 1.91 | 1.79 | | | 3.81 | 3.69 | ns |
| -2 | 0.49 | 1.65 | 0.03 | 1.13 | 0.32 | 1.68 | 1.57 | | | 3.35 | 4.34 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-150 • Minimum and Maximum DC Input and Output Levels

| HSTL Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|--------------|--------|------------|------------|--------|--------|------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 8 mA | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 8 | 8 | 39 | 32 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.



Figure 2-128 • AC Loading

Table 2-151 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-152 • HSTL Class I

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 3.18 | 0.04 | 2.12 | 0.43 | 3.24 | 3.14 | | | 5.47 | 5.38 | ns |
| -1 | 0.56 | 2.70 | 0.04 | 1.81 | 0.36 | 2.75 | 2.67 | | | 4.66 | 4.58 | ns |
| -2 | 0.49 | 2.37 | 0.03 | 1.59 | 0.32 | 2.42 | 2.35 | | | 4.09 | 4.02 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-153 • Minimum and Maximum DC Input and Output Levels

| HSTL Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|--------------------|--------|------------|------------|--------|--------|------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 15 mA ³ | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 15 | 15 | 55 | 66 | 10 | 10 |

Note:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Output drive strength is below JEDEC specification.



Figure 2-129 • AC Loading

Table 2-154 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-155 • HSTL Class II

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 3.02 | 0.04 | 2.12 | 0.43 | 3.08 | 2.71 | | | 5.32 | 4.95 | ns |
| -1 | 0.56 | 2.57 | 0.04 | 1.81 | 0.36 | 2.62 | 2.31 | | | 4.52 | 4.21 | ns |
| -2 | 0.49 | 2.26 | 0.03 | 1.59 | 0.32 | 2.30 | 2.03 | | | 3.97 | 3.70 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

| SSTL2 Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|---------------|--------|------------|------------|--------|--------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 15 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.54 | VCCI - 0.62 | 15 | 15 | 87 | 83 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.



Figure 2-130 • AC Loading

Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-158 • SSTL 2 Class I

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.13 | 0.04 | 1.33 | 0.43 | 2.17 | 1.85 | | | 4.40 | 4.08 | ns |
| -1 | 0.56 | 1.81 | 0.04 | 1.14 | 0.36 | 1.84 | 1.57 | | | 3.74 | 3.47 | ns |
| -2 | 0.49 | 1.59 | 0.03 | 1.00 | 0.32 | 1.62 | 1.38 | | | 3.29 | 3.05 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-159 • Minimum and Maximum DC Input and Output Levels

| SSTL2 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|----------------|--------|------------|------------|--------|--------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 18 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI - 0.43 | 18 | 18 | 124 | 169 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.



Figure 2-131 • AC Loading

Table 2-160 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-161 • SSTL 2 Class II

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = 2.3 V, VREF = 1.25 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.17 | 0.04 | 1.33 | 0.43 | 2.21 | 1.77 | | | 4.44 | 4.01 | ns |
| -1 | 0.56 | 1.84 | 0.04 | 1.14 | 0.36 | 1.88 | 1.51 | | | 3.78 | 3.41 | ns |
| -2 | 0.49 | 1.62 | 0.03 | 1.00 | 0.32 | 1.65 | 1.32 | | | 3.32 | 2.99 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-162 • Minimum and Maximum DC Input and Output Levels

| SSTL3 Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|----------------|--------|------------|------------|--------|--------|------------|-----|-----|----------------------|----------------------|------------------|------------------|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 14 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.7 | VCCI - 1.1 | 14 | 14 | 54 | 51 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.



Figure 2-132 • AC Loading

Table 2-163 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.5 | 1.5 | 1.485 | 30 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-164 • SSTL3 Class I

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.31 | 0.04 | 1.25 | 0.43 | 2.35 | 1.84 | | | 4.59 | 4.07 | ns |
| -1 | 0.56 | 1.96 | 0.04 | 1.06 | 0.36 | 2.00 | 1.56 | | | 3.90 | 3.46 | ns |
| -2 | 0.49 | 1.72 | 0.03 | 0.93 | 0.32 | 1.75 | 1.37 | | | 3.42 | 3.04 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-165 • Minimum and Maximum DC Input and Output Levels

| SSTL3 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|----------------|--------|------------|------------|--------|--------|------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 21 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.5 | VCCI - 0.9 | 21 | 21 | 109 | 103 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

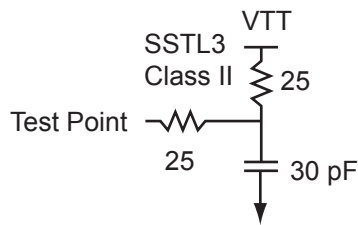


Figure 2-133 • AC Loading

Table 2-166 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.5 | 1.5 | 1.485 | 30 |

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-167 • SSTL3- Class II

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.07 | 0.04 | 1.25 | 0.43 | 2.10 | 1.67 | | | 4.34 | 3.91 | ns |
| -1 | 0.56 | 1.76 | 0.04 | 1.06 | 0.36 | 1.79 | 1.42 | | | 3.69 | 3.32 | ns |
| -2 | 0.49 | 1.54 | 0.03 | 0.93 | 0.32 | 1.57 | 1.25 | | | 3.24 | 2.92 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Differential I/O Characteristics

Configuration of the I/O modules as a differential pair is handled by the Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-134](#). The building blocks of the LVDS transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

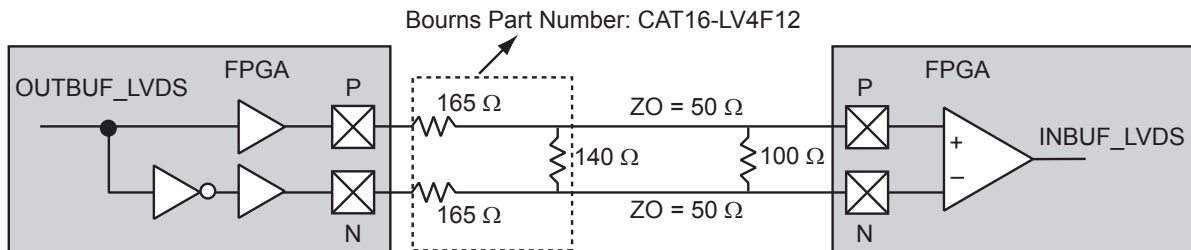


Figure 2-134 • LVDS Circuit Diagram and Board-Level Implementation

Table 2-168 • Minimum and Maximum DC Input and Output Levels

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|--------------------|-----------------------------|-------|-------|-------|-------|
| VCCI | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Input High Voltage | 1.25 | 1.425 | 1.6 | V |
| IOL ¹ | Output Low Voltage | 0.65 | 0.91 | 1.16 | mA |
| IOH ¹ | Output High Voltage | 0.65 | 0.91 | 1.16 | mA |
| VI | Input Voltage | 0 | | 2.925 | V |
| IIL ^{2,3} | Input Low Voltage | | | 10 | μA |
| IIH ^{2,4} | Input High Voltage | | | 10 | μA |
| VODIFF | Differential Output Voltage | 250 | 350 | 450 | mV |
| VOCM | Output Common Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| VICM | Input Common Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| VIDIFF | Input Differential Voltage | 100 | 350 | | mV |

Notes:

1. IOL/IOH defined by VODIFF/(Resistor Network)
2. Currents are measured at 85°C junction temperature.
3. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
4. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.

Table 2-169 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---------------|----------------|----------------------|-----------------|
| 1.075 | 1.325 | Cross point | – |

Note: *Measuring point = V_{trip} . See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-170 • LVDS

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Pro I/Os

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| Std. | 0.66 | 2.10 | 0.04 | 1.82 | ns |
| –1 | 0.56 | 1.79 | 0.04 | 1.55 | ns |
| –2 | 0.49 | 1.57 | 0.03 | 1.36 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

BLVDS/M-LVDS

Bus LVDS (BLVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations can contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The driver requires series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus, since the driver can be located anywhere on the bus. These configurations can be implemented using TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-135. The input and output buffer delays are available in the LVDS section in Table 2-171.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case industrial operating conditions at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").


Figure 2-135 • BLVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-136](#). The building blocks of the LVPECL transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.



Figure 2-136 • LVPECL Circuit Diagram and Board-Level Implementation

Table 2-171 • Minimum and Maximum DC Input and Output Levels

| DC Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
|--------------|--------------------------------|-------|------|-------|------|-------|------|-------|
| VCCI | Supply Voltage | 3.0 | | 3.3 | | 3.6 | | V |
| VOL | Output Low Voltage | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| VOH | Output High Voltage | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| VIL, VIH | Input Low, Input High Voltages | 0 | 3.6 | 0 | 3.6 | 0 | 3.6 | V |
| VODIFF | Differential Output Voltage | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V |
| VOCM | Output Common Mode Voltage | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V |
| VICM | Input Common Mode Voltage | 1.01 | 2.57 | 1.01 | 2.57 | 1.01 | 2.57 | V |
| VIDIFF | Input Differential Voltage | 300 | | 300 | | 300 | | mV |

Table 2-172 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---------------|----------------|----------------------|-----------------|
| 1.64 | 1.94 | Cross point | – |

Note: *Measuring point = V_{trip} . See [Table 2-90](#) on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-173 • LVPECL

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = 3.0 V
 Applicable to Pro I/Os

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| Std. | 0.66 | 2.14 | 0.04 | 1.63 | ns |
| –1 | 0.56 | 1.82 | 0.04 | 1.39 | ns |
| –2 | 0.49 | 1.60 | 0.03 | 1.22 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset



Figure 2-137 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Table 2-174 • Parameter Definitions and Measuring Nodes

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|-----------------------|--|-----------------------------|
| t _{OCLKQ} | Clock-to-Q of the Output Data Register | H, DOUT |
| t _{OSUD} | Data Setup Time for the Output Data Register | F, H |
| t _{OHD} | Data Hold Time for the Output Data Register | F, H |
| t _{OSUE} | Enable Setup Time for the Output Data Register | G, H |
| t _{OHE} | Enable Hold Time for the Output Data Register | G, H |
| t _{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | L, DOUT |
| t _{OREMPRE} | Asynchronous Preset Removal Time for the Output Data Register | L, H |
| t _{ORECPRE} | Asynchronous Preset Recovery Time for the Output Data Register | L, H |
| t _{OECLKQ} | Clock-to-Q of the Output Enable Register | H, EOUT |
| t _{OESUD} | Data Setup Time for the Output Enable Register | J, H |
| t _{OEHD} | Data Hold Time for the Output Enable Register | J, H |
| t _{OESUE} | Enable Setup Time for the Output Enable Register | K, H |
| t _{OEHE} | Enable Hold Time for the Output Enable Register | K, H |
| t _{OEPRE2Q} | Asynchronous Preset-to-Q of the Output Enable Register | I, EOUT |
| t _{OEREMPRE} | Asynchronous Preset Removal Time for the Output Enable Register | I, H |
| t _{OERECPRE} | Asynchronous Preset Recovery Time for the Output Enable Register | I, H |
| t _{ICLKQ} | Clock-to-Q of the Input Data Register | A, E |
| t _{ISUD} | Data Setup Time for the Input Data Register | C, A |
| t _{IHD} | Data Hold Time for the Input Data Register | C, A |
| t _{ISUE} | Enable Setup Time for the Input Data Register | B, A |
| t _{IHE} | Enable Hold Time for the Input Data Register | B, A |
| t _{IPRE2Q} | Asynchronous Preset-to-Q of the Input Data Register | D, E |
| t _{IEMPRE} | Asynchronous Preset Removal Time for the Input Data Register | D, A |
| t _{IRECPRE} | Asynchronous Preset Recovery Time for the Input Data Register | D, A |

Note: *See Figure 2-137 on page 2-212 for more information.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

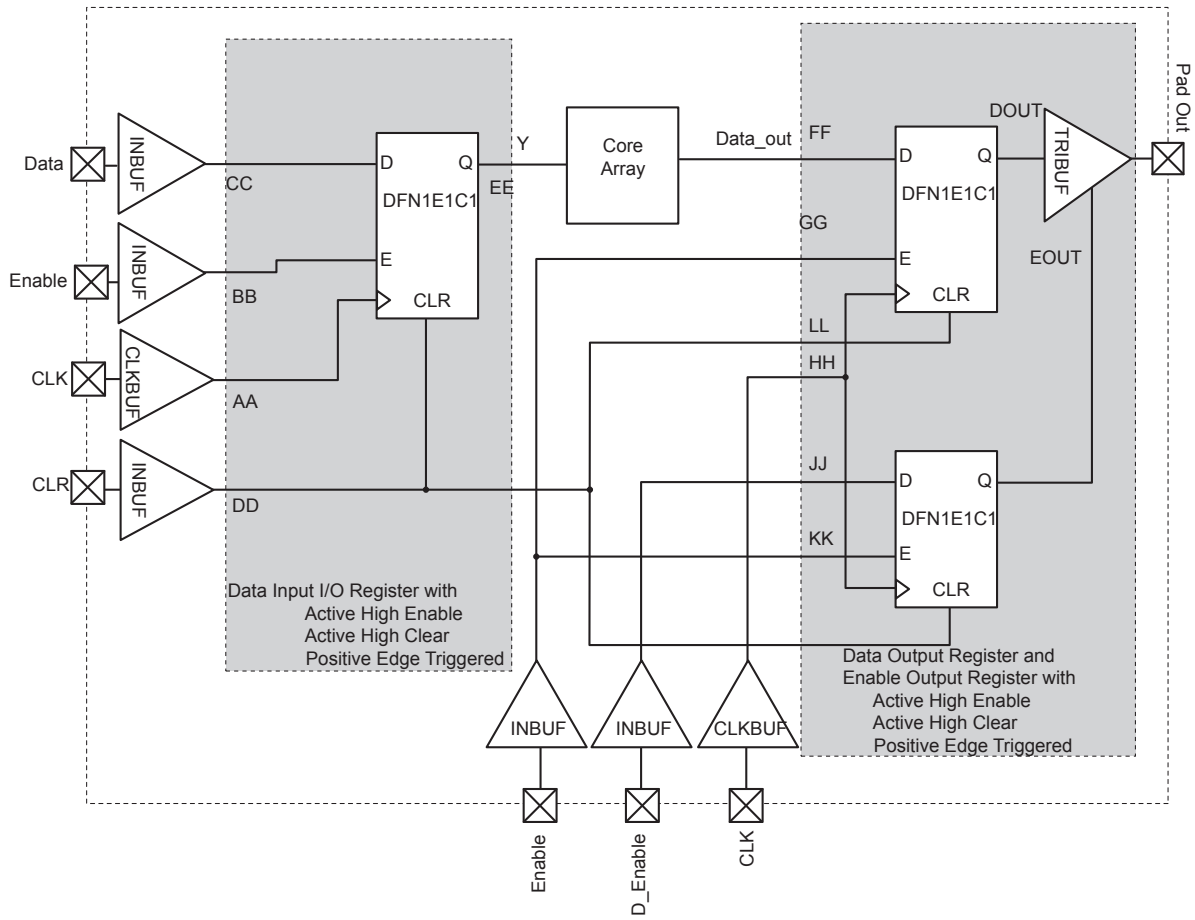


Figure 2-138 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Table 2-175 • Parameter Definitions and Measuring Nodes

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|-----------------------|---|-----------------------------|
| t _{OCLKQ} | Clock-to-Q of the Output Data Register | HH, DOUT |
| t _{OSUD} | Data Setup Time for the Output Data Register | FF, HH |
| t _{OHD} | Data Hold Time for the Output Data Register | FF, HH |
| t _{OSUE} | Enable Setup Time for the Output Data Register | GG, HH |
| t _{OHE} | Enable Hold Time for the Output Data Register | GG, HH |
| t _{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| t _{OREMCLR} | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| t _{ORECCLR} | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| t _{OECLKQ} | Clock-to-Q of the Output Enable Register | HH, EOUT |
| t _{OESUD} | Data Setup Time for the Output Enable Register | JJ, HH |
| t _{OEH} | Data Hold Time for the Output Enable Register | JJ, HH |
| t _{OESUE} | Enable Setup Time for the Output Enable Register | KK, HH |
| t _{OEH} | Enable Hold Time for the Output Enable Register | KK, HH |
| t _{OECLR2Q} | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| t _{OEREMCLR} | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| t _{OERECCLR} | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| t _I CLKQ | Clock-to-Q of the Input Data Register | AA, EE |
| t _I SUD | Data Setup Time for the Input Data Register | CC, AA |
| t _I HD | Data Hold Time for the Input Data Register | CC, AA |
| t _I SUE | Enable Setup Time for the Input Data Register | BB, AA |
| t _I HE | Enable Hold Time for the Input Data Register | BB, AA |
| t _I CLR2Q | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| t _I REMCLR | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| t _I RECCLR | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

Note: *See Figure 2-138 on page 2-214 for more information.

Input Register

Figure 2-139 • Input Register Timing Diagram
Timing Characteristics
Table 2-176 • Input Data Register Propagation Delays

 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------|---|------|------|------|-------|
| t_{ICLKQ} | Clock-to-Q of the Input Data Register | 0.24 | 0.27 | 0.32 | ns |
| t_{ISUD} | Data Setup Time for the Input Data Register | 0.26 | 0.30 | 0.35 | ns |
| t_{IHD} | Data Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{ISUE} | Enable Setup Time for the Input Data Register | 0.37 | 0.42 | 0.50 | ns |
| t_{IHE} | Enable Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{ICLR2Q} | Asynchronous Clear-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| t_{IPRE2Q} | Asynchronous Preset-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{IWCLR} | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{IWPRE} | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.32 | 0.37 | 0.43 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

Output Register



Figure 2-140 • Output Register Timing Diagram

Timing Characteristics

Table 2-177 • Output Data Register Propagation Delays
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------|--|------|------|------|-------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | 0.59 | 0.67 | 0.79 | ns |
| t_{OSUD} | Data Setup Time for the Output Data Register | 0.31 | 0.36 | 0.42 | ns |
| t_{OHD} | Data Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{OSUE} | Enable Setup Time for the Output Data Register | 0.44 | 0.50 | 0.59 | ns |
| t_{OHE} | Enable Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | 0.80 | 0.91 | 1.07 | ns |
| t_{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | 0.80 | 0.91 | 1.07 | ns |
| t_{OEMCLR} | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{OEMPRE} | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{OWCLR} | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{OWPRE} | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OCLMPWH}$ | Clock Minimum Pulse Width High for the Output Data Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{OCLMPWL}$ | Clock Minimum Pulse Width Low for the Output Data Register | 0.32 | 0.37 | 0.43 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Output Enable Register



Figure 2-141 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-178 • Output Enable Register Propagation Delays

Commercial Temperature Range Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------|--|------|------|------|-------|
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | 0.44 | 0.51 | 0.59 | ns |
| t_{OESUD} | Data Setup Time for the Output Enable Register | 0.31 | 0.36 | 0.42 | ns |
| t_{OEHD} | Data Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | 0.44 | 0.50 | 0.58 | ns |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| t_{OEWCLR} | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEWPRES}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.32 | 0.37 | 0.43 | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on page 3-9.

DDR Module Specifications

Input DDR Module



Figure 2-142 • Input DDR Timing Model

Table 2-179 • Parameter Definitions

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|------------------|------------------------------|----------------------------|
| $t_{DDRICKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR Input | A, B |
| t_{DDRIHD} | Data Hold Time of DDR Input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIEMCLR}$ | Clear Removal | C, B |
| $t_{DDRIECCLR}$ | Clear Recovery | C, B |


Figure 2-143 • Input DDR Timing Diagram
Timing Characteristics
Table 2-180 • Input DDR Propagation Delays

 Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|-------------------------|--|------|------|------|-------|
| t_{DDRICKQ1} | Clock-to-Out Out_QR for Input DDR | 0.39 | 0.44 | 0.52 | ns |
| t_{DDRICKQ2} | Clock-to-Out Out_QF for Input DDR | 0.27 | 0.31 | 0.37 | ns |
| t_{DDRISUD} | Data Setup for Input DDR | 0.28 | 0.32 | 0.38 | ns |
| t_{DDRIHD} | Data Hold for Input DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDRICLR2Q1}}$ | Asynchronous Clear-to-Out Out_QR for Input DDR | 0.57 | 0.65 | 0.76 | ns |
| $t_{\text{DDRICLR2Q2}}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 0.46 | 0.53 | 0.62 | ns |
| $t_{\text{DDRIREMCLR}}$ | Asynchronous Clear Removal Time for Input DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDRIRECCLR}}$ | Asynchronous Clear Recovery Time for Input DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{\text{DDR IWCLR}}$ | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{\text{DDRICKMPWH}}$ | Clock Minimum Pulse Width High for Input DDR | 0.36 | 0.41 | 0.48 | ns |
| $t_{\text{DDRICKMPWL}}$ | Clock Minimum Pulse Width Low for Input DDR | 0.32 | 0.37 | 0.43 | ns |
| F_{DDRIMAX} | Maximum Frequency for Input DDR | 1404 | 1232 | 1048 | MHz |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7](#) on [page 3-9](#).

Output DDR

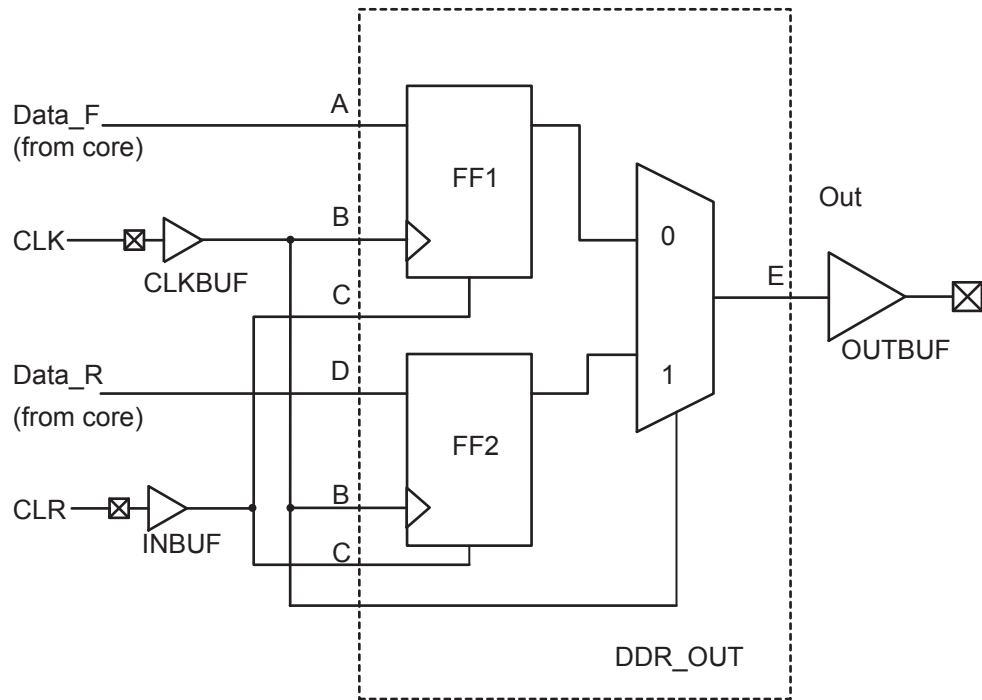


Figure 2-144 • Output DDR Timing Model

Table 2-181 • Parameter Definitions

| Parameter Name | Parameter Definition | Measuring Nodes (From, To) |
|------------------|---------------------------|----------------------------|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |



Figure 2-145 • Output DDR Timing Diagram

Timing Characteristics

Table 2-182 • Output DDR Propagation Delays

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|------------------|---|------|------|------|-------|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 0.70 | 0.80 | 0.94 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 0.38 | 0.43 | 0.51 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 0.38 | 0.43 | 0.51 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 0.80 | 0.91 | 1.07 | ns |
| $t_{DDROEMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDROECLLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width High for the Output DDR | 0.36 | 0.41 | 0.48 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width Low for the Output DDR | 0.32 | 0.37 | 0.43 | ns |
| F_{DDOMAX} | Maximum Frequency for the Output DDR | 1404 | 1232 | 1048 | MHz |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. Note: In FG256, FG484, and FG676 packages, GNDQ and GND pins are connected within the package and are labeled as GND pins in the respective package pin assignment tables.

ADCGNDREF **Analog Reference Ground**

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA **Ground (analog)**

Quiet ground supply voltage to the Analog Block of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation.

GNDQA **Ground (analog quiet)**

Quiet ground supply voltage to the analog I/O of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation. Note: In FG256, FG484, and FG676 packages, GNDQA and GNDA pins are connected within the package and are labeled as GNDA pins in the respective package pin assignment tables.

GNDNVM **Flash Memory Ground**

Ground supply used by the Fusion device's flash memory block module(s).

GNDOSC **Oscillator Ground**

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

VCC15A **Analog Power Supply (1.5 V)**

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

VCC33A **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

VCC33N **Negative 3.3 V Output**

This is the -3.3 V output from the voltage converter. A 2.2 μ F capacitor must be connected from this pin to ground.

VCC33PMP **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the analog charge pump. To avoid high current draw, VCC33PMP should be powered up simultaneously with or after VCC33A.

VCCNVM **Flash Memory Block Power Supply (1.5 V)**

1.5 V power supply input used by the Fusion device's flash memory block module(s). To avoid high current draw, VCC should be powered up before or simultaneously with VCCNVM.

VCCOSC **Oscillator Power Supply (3.3 V)**

Power supply for both integrated RC oscillator and crystal oscillator circuit. The internal 100 MHz oscillator, powered by the VCCOSC pin, is needed for device programming, operation of the VDDN33 pump, and eNVM operation. VCCOSC is off only when VCCA is off. VCCOSC must be powered whenever the Fusion device needs to function.

VCC Core Supply Voltage

Supply voltage to the FPGA core, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a Fusion device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the Fusion device.

VCCIBx I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are either four (AFS090 and AFS250) or five (AFS600 and AFS1500) I/O banks on the Fusion devices plus a dedicated VJTAG bank.

Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VCCPLA/B PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5 V, where A and B refer to the PLL. AFS090 and AFS250 each have a single PLL. The AFS600 and AFS1500 devices each have two PLLs. Microsemi recommends tying VCCPLX to VCC and using proper filtering circuits to decouple VCC noise from PLL. If unused, VCCPLA/B should be tied to GND.

VCOMPLA/B Ground for West and East PLL

VCOMPLA is the ground of the west PLL (CCC location F) and VCOMPLB is the ground of the east PLL (CCC location C).

VJTAG JTAG Supply Voltage

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a Fusion device is in a JTAG chain of interconnected boards and it is desired to power down the board containing the Fusion device, this may be done provided both VJTAG and VCC to the Fusion part remain powered; otherwise, JTAG signals will not be able to transition the Fusion device, even in bypass mode.

VPUMP Programming Supply Voltage

Fusion devices support single-voltage ISP programming of the configuration flash and FlashROM. For programming, VPUMP should be in the 3.3 V +/-5% range. During normal device operation, VPUMP can be left floating or can be tied to any voltage between 0 V and 3.6 V.

When the VPUMP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

User-Defined Supply Pins

VREF I/O Voltage Reference

Reference voltage for I/O minibanks. Both AFS600 and AFS1500 (north bank only) support Microsemi Pro I/O. These I/O banks support voltage reference standard I/O. The VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated as the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

VAREF Analog Reference Voltage

The Fusion device can be configured to generate a 2.56 V internal reference voltage that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREF pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF is internally generated by the Fusion device, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 μ F and 22 μ F, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. Depending on the capacitor value selected in the Analog System Builder, a tool in Libero SoC, an automatic delay circuit will be generated using logic tiles available within the FPGA to ensure that VAREF has achieved the 2.56 V value. Microsemi recommends customers use 10 μ F as the value of the bypass capacitor. Designers choosing to use an external VAREF need to ensure that a stable and clean VAREF source is supplied to the VAREF pin before initiating conversions by the ADC. Designers should also make sure that the ADCRESET signal is deasserted before initiating valid conversions.²

If the user connects VAREF to external 3.3 V on their board, the internal VAREF driving OpAmp tries to bring the pin down to the nominal 2.56 V until the device is programmed and up/functional. Under this scenario, it is recommended to connect an external 3.3 V supply through a ~1 K Ω resistor to limit current, along with placing a 10-100nF capacitor between VAREF and GNDA.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are configured as inputs with pull-up resistors.

During programming, I/Os become tristated and weakly pulled up to VCCI. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os get instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

Axy Analog Input/Output

Analog I/O pin, where x is the analog pad type (C = current pad, G = Gate driver pad, T = Temperature pad, V = Voltage pad) and y is the Analog Quad number (0 to 9). There is a minimum 1 M Ω to ground on AV, AC, and AT. This pin can be left floating when it is unused.

2. The ADC is functional with an external reference down to 1V, however to meet the performance parameters highlighted in the datasheet refer to the VAREF specification in [Table 3-2 on page 3-3](#).

ATRTNx Temperature Monitor Return

AT returns are the returns for the temperature sensors. The cathode terminal of the external diodes should be connected to these pins. There is one analog return pin for every two Analog Quads. The x in the ATRTNx designator indicates the quad pairing (x = 0 for AQ1 and AQ2, x = 1 for AQ2 and AQ3, ..., x = 4 for AQ8 and AQ9). The signals that drive these pins are called out as ATRETURNxy in the software (where x and y refer to the quads that share the return signal). ATRTN is internally connected to ground. It can be left floating when it is unused. The maximum capacitance allowed across the AT pins is 500 pF.

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "[Clock Conditioning Circuits](#)" section on page 2-22.

Refer to the "[User I/O Naming Convention](#)" section on page 2-158 for a description of naming of global pins.

JTAG Pins

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device.

Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND or VJTAG through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to [Table 2-183](#) for more information.

Table 2-183 • Recommended Tie-Off Values for the TCK and TRST Pins

| VJTAG | Tie-Off Resistance ^{2, 3} |
|----------------|------------------------------------|
| VJTAG at 3.3 V | 200 Ω to 1 kΩ |
| VJTAG at 2.5 V | 200 Ω to 1 kΩ |
| VJTAG at 1.8 V | 500 Ω to 1 kΩ |
| VJTAG at 1.5 V | 500 Ω to 1 kΩ |

Notes:

1. Equivalent parallel resistance if more than one device is on JTAG chain.
2. The TCK pin can be pulled up/down.
3. The TRST pin can only be pulled down.

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from [Table 2-183](#) and must satisfy the parallel resistance value requirement. The values in [Table 2-183](#) correspond to the resistor recommended when a single device is used and to the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

Special Function Pins

NC No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC Don't Connect

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

NCAP Negative Capacitor

Negative Capacitor is where the negative terminal of the charge pump capacitor is connected. A capacitor, with a 2.2 μF recommended value, is required to connect between PCAP and NCAP.

PCAP Positive Capacitor

Positive Capacitor is where the positive terminal of the charge pump capacitor is connected. A capacitor, with a 2.2 μF recommended value, is required to connect between PCAP and NCAP.

PUB Push Button

Push button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

PTBASE Pass Transistor Base

Pass Transistor Base is the control signal of the voltage regulator. This pin should be connected to the base of the external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.

PTEM Pass Transistor Emitter

Pass Transistor Emitter is the feedback input of the voltage regulator.

This pin should be connected to the emitter of the external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.

XTAL1 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

XTAL2 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates highly secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a security-protected programming environment (such as the Microsemi in-house programming center), and then “blank” parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and with high level security by simply sending a STAPL file with AES-encrypted data. Highly secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the [Fusion Security](#) application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (protected with security) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain as secure as possible.

AES decryption can also be used on the 1,024-bit FlashROM to allow for remote updates of the FlashROM contents. This allows for easy support of subscription model products and protects them with measures designed to provide the highest level of security available. See the application note [Fusion Security](#) for more details.

AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This provides the best available security during update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Microsemi).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.

ISP

Fusion devices support IEEE 1532 ISP via JTAG and require a single VPUMP voltage of 3.3 V during programming. In addition, programming via a microcontroller in a target system can be achieved. Refer to the standard or the “In-System Programming (ISP) of Microsemi’s Low Power Flash Devices Using FlashPro4/3/3X” chapter of the *Fusion FPGA Fabric User’s Guide* for more details.

JTAG IEEE 1532

Programming with IEEE 1532

Fusion devices support the JTAG-based IEEE1532 standard for ISP. As part of this support, when a Fusion device is in an unprogrammed state, all user I/O pins are disabled. This is achieved by keeping the global IO_EN signal deactivated, which also has the effect of disabling the input buffers. Consequently, the SAMPLE instruction will have no effect while the Fusion device is in this unprogrammed state—different behavior from that of the ProASIC^{PLUS}® device family. This is done because SAMPLE is defined in the IEEE1532 specification as a noninvasive instruction. If the input buffers were to be enabled by SAMPLE temporarily turning on the I/Os, then it would not truly be a noninvasive instruction. Refer to the standard or the “In-System Programming (ISP) of Microsemi’s Low Power Flash Devices Using FlashPro4/3/3X” chapter of the *Fusion FPGA Fabric User’s Guide* for more details.

Boundary Scan

Fusion devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary scan testing. The basic Fusion boundary scan logic circuit is composed of the test access port (TAP) controller, test data registers, and instruction register ([Figure 2-146 on page 2-230](#)). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction ([Table 2-185 on page 2-230](#)).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary scan test usage. Refer to the “JTAG Pins” section on [page 2-226](#) for pull-up/-down recommendations for TDO and TCK pins. The TAP controller is a 4-bit state machine (16 states) that operates as shown in [Figure 2-146 on page 2-230](#). The 1s and 0s represent the values that must be present on TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

Table 2-184 • TRST and TCK Pull-Down Recommendations

| VJTAG | Tie-Off Resistance* |
|----------------|---------------------|
| VJTAG at 3.3 V | 200 Ω to 1 kΩ |
| VJTAG at 2.5 V | 200 Ω to 1 kΩ |
| VJTAG at 1.8 V | 500 Ω to 1 kΩ |
| VJTAG at 1.5 V | 500 Ω to 1 kΩ |

Note: *Equivalent parallel resistance if more than one device is on JTAG chain.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain High for five TCK cycles. The TRST pin can also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

Fusion devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number, and version). The boundary scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin.

The serial pins are used to serially connect all the boundary scan register cells in a device into a boundary scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are

connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

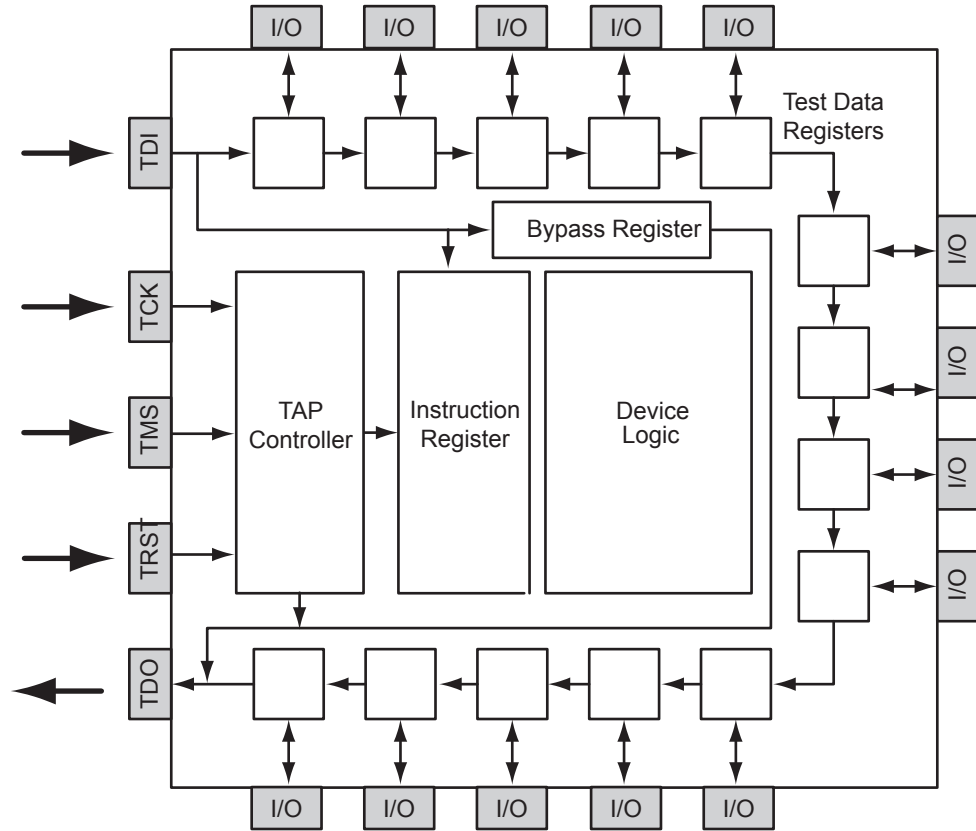


Figure 2-146 • Boundary Scan Chain in Fusion

Table 2-185 • Boundary Scan Opcodes

| | Hex Opcode |
|----------------|------------|
| EXTEST | 00 |
| HIGHZ | 07 |
| USERCODE | 0E |
| SAMPLE/PRELOAD | 01 |
| IDCODE | 0F |
| CLAMP | 05 |
| BYPASS | FF |

IEEE 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/Os" section on page 2-132 for more details.

Timing Characteristics

Table 2-186 • JTAG 1532

Commercial Temperature Range Conditions: $T_j = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------|-----------------------------|-------|-------|-------|-------|
| t_{DISU} | Test Data Input Setup Time | 0.50 | 0.57 | 0.67 | ns |
| t_{DIHD} | Test Data Input Hold Time | 1.00 | 1.13 | 1.33 | ns |
| t_{TMSSU} | Test Mode Select Setup Time | 0.50 | 0.57 | 0.67 | ns |
| t_{TMDHD} | Test Mode Select Hold Time | 1.00 | 1.13 | 1.33 | ns |
| t_{TCK2Q} | Clock to Q (data out) | 6.00 | 6.80 | 8.00 | ns |
| t_{RSTB2Q} | Reset to Q (data out) | 20.00 | 22.67 | 26.67 | ns |
| F_{TCKMAX} | TCK Maximum Frequency | 25.00 | 22.00 | 19.00 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.20 | 0.23 | 0.27 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | TBD | TBD | ns |

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

3 – DC and Power Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in [Table 3-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in [Table 3-2](#) on [page 3-3](#).

Table 3-1 • Absolute Maximum Ratings

| Symbol | Parameter | Commercial | Industrial | Units |
|----------|--|---|---------------------------|-------|
| VCC | DC core supply voltage | –0.3 to 1.65 | –0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | –0.3 to 3.75 | –0.3 to 3.75 | V |
| VPUMP | Programming voltage | –0.3 to 3.75 | –0.3 to 3.75 | V |
| VCCPLL | Analog power supply (PLL) | –0.3 to 1.65 | –0.3 to 1.65 | V |
| VCCI | DC I/O output buffer supply voltage | –0.3 to 3.75 | –0.3 to 3.75 | V |
| VI | I/O input voltage ¹ | –0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled) | | V |
| VCC33A | +3.3 V power supply | –0.3 to 3.75 ² | –0.3 to 3.75 ² | V |
| VCC33PMP | +3.3 V power supply | –0.3 to 3.75 ² | –0.3 to 3.75 ² | V |
| VAREF | Voltage reference for ADC | –0.3 to 3.75 | –0.3 to 3.75 | V |
| VCC15A | Digital power supply for the analog system | –0.3 to 1.65 | –0.3 to 1.65 | V |
| VCCNVM | Embedded flash power supply | –0.3 to 1.65 | –0.3 to 1.65 | V |
| VCCOSC | Oscillator power supply | –0.3 to 3.75 | –0.3 to 3.75 | V |

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 3-4](#) on [page 3-4](#).
2. Analog data not valid beyond 3.65 V.
3. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
4. For flash programming and retention maximum limits, refer to [Table 3-5](#) on [page 3-5](#). For recommended operating limits refer to [Table 3-2](#) on [page 3-3](#).

Table 3-1 • Absolute Maximum Ratings (continued)

| Symbol | Parameter | Commercial | Industrial | Units |
|-------------------------------|---|---------------|---------------|-------|
| AV, AC | Unpowered, ADC reset asserted or unconfigured | -11.0 to 12.6 | -11.0 to 12.0 | V |
| | Analog input (+16 V to +2 V prescaler range) | -0.4 to 12.6 | -0.4 to 12.0 | V |
| | Analog input (+1 V to +0.125 V prescaler range) | -0.4 to 3.75 | -0.4 to 3.75 | V |
| | Analog input (-16 V to -2 V prescaler range) | -11.0 to 0.4 | -11.0 to 0.4 | V |
| | Analog input (-1 V to -0.125 V prescaler range) | -3.75 to 0.4 | -3.75 to 0.4 | V |
| | Analog input (direct input to ADC) | -0.4 to 3.75 | -0.4 to 3.75 | V |
| | Digital input | -0.4 to 12.6 | -0.4 to 12.0 | V |
| AG | Unpowered, ADC reset asserted or unconfigured | -11.0 to 12.6 | -11.0 to 12.0 | V |
| | Low Current Mode (1 μ A, 3 μ A, 10 μ A, 30 μ A) | -0.4 to 12.6 | -0.4 to 12.0 | V |
| | Low Current Mode (-1 μ A, -3 μ A, -10 μ A, -30 μ A) | -11.0 to 0.4 | -11.0 to 0.4 | V |
| | High Current Mode ³ | -11.0 to 12.6 | -11.0 to 12.0 | V |
| AT | Unpowered, ADC reset asserted or unconfigured | -0.4 to 16.0 | -0.4 to 15.0 | V |
| | Analog input (+16 V, 4 V prescaler range) | -0.4 to 16.0 | -0.4 to 15.0 | V |
| | Analog input (direct input to ADC) | -0.4 to 3.75 | -0.4 to 3.75 | V |
| | Digital input | -0.4 to 16.0 | -0.4 to 15.0 | V |
| T _{STG} ⁴ | Storage temperature | -65 to +150 | | °C |
| T _J ⁴ | Junction temperature | +125 | | °C |

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 3-4 on page 3-4](#).
2. Analog data not valid beyond 3.65 V.
3. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
4. For flash programming and retention maximum limits, refer to [Table 3-5 on page 3-5](#). For recommended operating limits refer to [Table 3-2 on page 3-3](#).

Table 3-2 • Recommended Operating Conditions¹

| Symbol | Parameter ² | Commercial | Industrial | Units | |
|---------------------|---|-------------------------------|----------------|--------------|---|
| T _J | Junction temperature | 0 to +85 | -40 to +100 | °C | |
| VCC | 1.5 V DC core supply voltage | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| VJTAG | JTAG DC voltage | 1.4 to 3.6 | 1.4 to 3.6 | V | |
| VPUMP | Programming voltage | Programming mode ³ | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation ⁴ | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL | Analog power supply (PLL) | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| VCCI | 1.5 V DC supply voltage | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| | 1.8 V DC supply voltage | 1.7 to 1.9 | 1.7 to 1.9 | V | |
| | 2.5 V DC supply voltage | 2.3 to 2.7 | 2.3 to 2.7 | V | |
| | 3.3 V DC supply voltage | 3.0 to 3.6 | 3.0 to 3.6 | V | |
| | LVDS differential I/O | 2.375 to 2.625 | 2.375 to 2.625 | V | |
| | LVPECL differential I/O | 3.0 to 3.6 | 3.0 to 3.6 | V | |
| VCC33A | +3.3 V power supply | 2.97 to 3.63 | 2.97 to 3.63 | V | |
| VCC33PMP | +3.3 V power supply | 2.97 to 3.63 | 2.97 to 3.63 | V | |
| VAREF | Voltage reference for ADC | 2.527 to 2.593 | 2.527 to 2.593 | V | |
| VCC15A ⁵ | Digital power supply for the analog system | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| VCCNVM | Embedded flash power supply | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| VCCOSC | Oscillator power supply | 2.97 to 3.63 | 2.97 to 3.63 | V | |
| AV, AC ⁶ | Unpowered, ADC reset asserted or unconfigured | -10.5 to 12.0 | -10.5 to 11.6 | V | |
| | Analog input (+16 V to +2 V prescaler range) | -0.3 to 12.0 | -0.3 to 11.6 | V | |
| | Analog input (+1 V to +0.125 V prescaler range) | -0.3 to 3.6 | -0.3 to 3.6 | V | |
| | Analog input (-16 V to -2 V prescaler range) | -10.5 to 0.3 | -10.5 to 0.3 | V | |
| | Analog input (-1 V to -0.125 V prescaler range) | -3.6 to 0.3 | -3.6 to 0.3 | V | |
| | Analog input (direct input to ADC) | -0.3 to 3.6 | -0.3 to 3.6 | V | |
| | Digital input | -0.3 to 12.0 | -0.3 to 11.6 | V | |
| AG ⁶ | Unpowered, ADC reset asserted or unconfigured | -10.5 to 12.0 | -10.5 to 11.6 | V | |
| | Low Current Mode (1 μA, 3 μA, 10 μA, 30 μA) | -0.3 to 12.0 | -0.3 to 11.6 | V | |
| | Low Current Mode (-1 μA, -3 μA, -10 μA, -30 μA) | -10.5 to 0.3 | -10.5 to 0.3 | V | |
| | High Current Mode ⁷ | -10.5 to 12.0 | -10.5 to 11.6 | V | |
| AT ⁶ | Unpowered, ADC reset asserted or unconfigured | -0.3 to 15.5 | -0.3 to 14.5 | V | |
| | Analog input (+16 V, +4 V prescaler range) | -0.3 to 15.5 | -0.3 to 14.5 | V | |
| | Analog input (direct input to ADC) | -0.3 to 3.6 | -0.3 to 3.6 | V | |
| | Digital input | -0.3 to 15.5 | -0.3 to 14.5 | V | |

Notes:

1. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-85 on page 2-157.
2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
3. The programming temperature range supported is $T_{\text{ambient}} = 0^{\circ}\text{C}$ to 85°C .
4. VPUMP can be left floating during normal operation (not programming mode).
5. Violating the V_{CC15A} recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.
6. The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.
7. The AG pad should also conform to the limits as specified in Table 2-48 on page 2-114.

Table 3-3 • Input Resistance of Analog Pads

| Pads | Pad Configuration | Prescaler Range | Input Resistance to Ground |
|---------------|------------------------------------|------------------------|----------------------------|
| AV, AC | Analog Input (direct input to ADC) | – | 2 k Ω (typical) |
| | | – | > 10 M Ω |
| | Analog Input (positive prescaler) | +16 V to +2 V | 1 M Ω (typical) |
| | | +1 V to +0.125 V | > 10 M Ω |
| | Analog Input (negative prescaler) | –16 V to –2 V | 1 M Ω (typical) |
| | | –1 V to –0.125 V | > 10 M Ω |
| | Digital input | +16 V to +2 V | 1 M Ω (typical) |
| | Current monitor | +16 V to +2 V | 1 M Ω (typical) |
| –16 V to –2 V | | 1 M Ω (typical) | |
| AT | Analog Input (direct input to ADC) | – | 1 M Ω (typical) |
| | Analog Input (positive prescaler) | +16 V, +4 V | 1 M Ω (typical) |
| | Digital input | +16 V, +4 V | 1 M Ω (typical) |
| | Temperature monitor | +16 V, +4 V | > 10 M Ω |

Table 3-4 • Overshoot and Undershoot Limits ¹

| VCCI | Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ² | Maximum Overshoot/Undershoot ² |
|---------------|---|---|
| 2.7 V or less | 10% | 1.4 V |
| | 5% | 1.49 V |
| 3.0 V | 10% | 1.1 V |
| | 5% | 1.19 V |
| 3.3 V | 10% | 0.79 V |
| | 5% | 0.88 V |
| 3.6 V | 10% | 0.45 V |
| | 5% | 0.54 V |

Notes:

1. Based on reliability requirements at a junction temperature of 85°C.
2. The duration is allowed at one cycle out of six clock cycle. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

Table 3-5 • FPGA Programming, Storage, and Operating Limits

| Product Grade | Storage Temperature | Element | Grade Programming Cycles | Retention |
|---------------|--|----------------|--------------------------|-----------|
| Commercial | Min. $T_J = 0^\circ\text{C}$ Max. $T_J = 85^\circ\text{C}$ | FPGA/FlashROM | 500 | 20 years |
| | | Embedded Flash | < 1,000 | 20 years |
| | | | < 10,000 | 10 years |
| | | | < 15,000 | 5 years |
| Industrial | Min. $T_J = -40^\circ\text{C}$ Max. $T_J = 100^\circ\text{C}$ | FPGA/FlashROM | 500 | 20 years |
| | | Embedded Flash | < 1,000 | 20 years |
| | | | < 10,000 | 10 years |
| | | | < 15,000 | 5 years |

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every Fusion device. These circuits ensure easy transition from the powered off state to the powered up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 3-1 on page 3-6](#).

There are five regions to consider during power-up.

Fusion I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 3-1](#)).
2. $V_{CCI} > V_{CC} - 0.75\text{ V}$ (typical).
3. Chip is in the operating mode.

V_{CCI} Trip Point:

Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.2\text{ V}$

Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1.1\text{ V}$

V_{CC} Trip Point:

Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.1\text{ V}$

Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1\text{ V}$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels. The V_{CC} activation level is specified as 1.1 V worst-case (see [Figure 3-1 on page 3-6](#) for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$), the PLL output lock signal goes low and/or the output clock is lost.



Figure 3-1 • I/O State as a Function of VCCI and VCC Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JB} = Junction-to-board thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_B = Board temperature (measured 1.0 mm away from the package edge)
- T_C = Case temperature
- P = Total power dissipated by the device

Table 3-6 • Package Thermal Resistance

| Product | θ_{JA} | | | θ_{JC} | θ_{JB} | Units |
|---------------------------|---------------|---------|---------|---------------|---------------|-------|
| | Still Air | 1.0 m/s | 2.5 m/s | | | |
| AFS090-QN108 | 34.5 | 30.0 | 27.7 | 8.1 | 16.7 | °C/W |
| AFS090-QN180 | 33.3 | 27.6 | 25.7 | 9.2 | 21.2 | °C/W |
| AFS250-QN180 | 32.2 | 26.5 | 24.7 | 5.7 | 15.0 | °C/W |
| AFS250-PQ208 ¹ | 42.1 | 38.4 | 37 | 20.5 | 36.3 | °C/W |
| AFS600-PQ208 ¹ | 23.9 | 21.3 | 20.48 | 6.1 | 16.5 | °C/W |
| AFS090-FG256 | 37.7 | 33.9 | 32.2 | 11.5 | 29.7 | °C/W |
| AFS250-FG256 | 33.7 | 30.0 | 28.3 | 9.3 | 24.8 | °C/W |
| AFS600-FG256 | 28.9 | 25.2 | 23.5 | 6.8 | 19.9 | °C/W |
| AFS1500-FG256 | 23.3 | 19.6 | 18.0 | 4.3 | 14.2 | °C/W |
| AFS600-FG484 | 21.8 | 18.2 | 16.7 | 7.7 | 16.8 | °C/W |
| AFS1500-FG484 | 21.6 | 16.8 | 15.2 | 5.6 | 14.9 | °C/W |
| AFS1500-FG676 | TBD | TBD | TBD | TBD | TBD | °C/W |

1. The package PQ208 is discontinued. For more information, see PDN 1407: Specific Part / Package Combinations.

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

where

$$\theta_{JA} = 19.00^{\circ}\text{C/W (taken from Table 3-6 on page 3-7).}$$

$$T_A = 75.00^{\circ}\text{C}$$

$$\text{Maximum Power Allowed} = \frac{100.00^{\circ}\text{C} - 75.00^{\circ}\text{C}}{19.00^{\circ}\text{C/W}} = 1.3 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

$$T_J = 100.00^{\circ}\text{C}$$

$$T_A = 70.00^{\circ}\text{C}$$

From the datasheet:

$$\theta_{JA} = 17.00^{\circ}\text{C/W}$$

$$\theta_{JC} = 8.28^{\circ}\text{C/W}$$

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100^{\circ}\text{C} - 70^{\circ}\text{C}}{17.00 \text{ W}} = 1.76 \text{ W}$$

EQ 6

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{ja(\text{total})} = \frac{T_J - T_A}{P} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{3.00\text{ W}} = 10.00^\circ\text{C/W}$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(\text{TOTAL})} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

- θ_{JA} = 0.37°C/W
- = Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer
- θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(\text{TOTAL})} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33^\circ\text{C/W} - 8.28^\circ\text{C/W} - 0.37^\circ\text{C/W} = 5.01^\circ\text{C/W}$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Microsemi FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 3-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, Worst-Case VCC = 1.425 V)

| Array Voltage VCC (V) | Junction Temperature (°C) | | | | | |
|-----------------------|---------------------------|------|------|------|------|-------|
| | -40°C | 0°C | 25°C | 70°C | 85°C | 100°C |
| 1.425 | 0.88 | 0.93 | 0.95 | 1.00 | 1.02 | 1.05 |
| 1.500 | 0.83 | 0.88 | 0.90 | 0.95 | 0.96 | 0.99 |
| 1.575 | 0.80 | 0.85 | 0.87 | 0.91 | 0.93 | 0.96 |

Calculating Power Dissipation

Quiescent Supply Current

Table 3-8 • AFS1500 Quiescent Supply Current Characteristics

| Parameter | Description | Conditions | Temp. | Min. | Typ. | Max. | Unit |
|--------------------|----------------------------------|---|------------------------|------|------|------|------|
| ICC ¹ | 1.5 V quiescent current | Operational standby ⁴ , VCC = 1.575 V | T _J = 25°C | | 20 | 40 | mA |
| | | | T _J = 85°C | | 32 | 65 | mA |
| | | | T _J = 100°C | | 59 | 120 | mA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VCC = 0 V | | | 0 | 0 | μA |
| ICC33 ² | 3.3 V analog supplies current | Operational standby ⁴ , VCC33 = 3.63 V | T _J = 25°C | | 9.8 | 13 | mA |
| | | | T _J = 85°C | | 10.7 | 14 | mA |
| | | | T _J = 100°C | | 10.8 | 15 | mA |
| | | Operational standby, only Analog Quad and -3.3 V output ON, VCC33 = 3.63 V | T _J = 25°C | | 0.31 | 2 | mA |
| | | | T _J = 85°C | | 0.35 | 2 | mA |
| | | | T _J = 100°C | | 0.45 | 2 | mA |
| | | Standby mode ⁵ , VCC33 = 3.63 V | T _J = 25°C | | 2.9 | 3.6 | mA |
| | | | T _J = 85°C | | 2.9 | 4 | mA |
| | | | T _J = 100°C | | 3.3 | 6 | mA |
| | | Sleep mode ⁶ , VCC33 = 3.63 V | T _J = 25°C | | 17 | 19 | μA |
| | | | T _J = 85°C | | 18 | 20 | μA |
| | | | T _J = 100°C | | 24 | 25 | μA |
| ICCI ³ | I/O quiescent current | Operational standby ⁴ , Standby mode, and Sleep Mode ⁶ , VCC1x = 3.63 V | T _J = 25°C | | 417 | 649 | μA |
| | | | T _J = 85°C | | 417 | 649 | μA |
| | | | T _J = 100°C | | 417 | 649 | μA |

Notes:

1. ICC is the 1.5 V power supplies, ICC and ICC15A.
2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.
4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

Table 3-8 • AFS1500 Quiescent Supply Current Characteristics (continued)

| Parameter | Description | Conditions | Temp. | Min. | Typ. | Max. | Unit |
|-----------|-----------------------------|---|------------------------|------|------|------|------|
| IJTAG | JTAG I/O quiescent current | Operational standby ⁴ , VJTAG = 3.63 V | T _J = 25°C | | 80 | 100 | μA |
| | | | T _J = 85°C | | 80 | 100 | μA |
| | | | T _J = 100°C | | 80 | 100 | μA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VJTAG = 0 V | | | 0 | 0 | μA |
| IPP | Programming supply current | Non-programming mode, VPUMP = 3.63 V | T _J = 25°C | | 39 | 80 | μA |
| | | | T _J = 85°C | | 40 | 80 | μA |
| | | | T _J = 100°C | | 40 | 80 | μA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VPUMP = 0 V | | | 0 | 0 | μA |
| ICCNVM | Embedded NVM current | Reset asserted, V _{CCNVM} = 1.575 V | T _J = 25°C | | 50 | 150 | μA |
| | | | T _J = 85°C | | 50 | 150 | μA |
| | | | T _J = 100°C | | 50 | 150 | μA |
| ICCPLL | 1.5 V PLL quiescent current | Operational standby , VCCPLL = 1.575 V | T _J = 25°C | | 130 | 200 | μA |
| | | | T _J = 85°C | | 130 | 200 | μA |
| | | | T _J = 100°C | | 130 | 200 | μA |

Notes:

1. ICC is the 1.5 V power supplies, ICC and ICC15A.
2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.
4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

Table 3-9 • AFS600 Quiescent Supply Current Characteristics

| Parameter | Description | Conditions | Temp. | Min | Typ | Max | Unit |
|--------------------|-------------------------------|--|------------------------|-----|------|-----|------|
| ICC ¹ | 1.5 V quiescent current | Operational standby ⁴ , VCC = 1.575 V | T _J = 25°C | | 13 | 25 | mA |
| | | | T _J = 85°C | | 20 | 45 | mA |
| | | | T _J = 100°C | | 25 | 75 | mA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VCC = 0 V | | | 0 | 0 | μA |
| ICC33 ² | 3.3 V analog supplies current | Operational standby ⁴ , VCC33 = 3.63 V | T _J = 25°C | | 9.8 | 13 | mA |
| | | | T _J = 85°C | | 10.7 | 14 | mA |
| | | | T _J = 100°C | | 10.8 | 15 | mA |
| | | Operational standby, only Analog Quad and -3.3 V output ON, VCC33 = 3.63 V | T _J = 25°C | | 0.31 | 2 | mA |
| | | | T _J = 85°C | | 0.35 | 2 | mA |
| | | | T _J = 100°C | | 0.45 | 2 | mA |
| | | Standby mode ⁵ , VCC33 = 3.63 V | T _J = 25°C | | 2.8 | 3.6 | mA |
| | | | T _J = 85°C | | 2.9 | 4 | mA |
| | | | T _J = 100°C | | 3.5 | 6 | mA |
| | | Sleep mode ⁶ , VCC33 = 3.63 V | T _J = 25°C | | 17 | 19 | μA |
| | | | T _J = 85°C | | 18 | 20 | μA |
| | | | T _J = 100°C | | 24 | 25 | μA |
| ICCI ³ | I/O quiescent current | Operational standby ⁴ , VCC1x = 3.63 V | T _J = 25°C | | 417 | 648 | μA |
| | | | T _J = 85°C | | 417 | 648 | μA |
| | | | T _J = 100°C | | 417 | 649 | μA |
| IJTAG | JTAG I/O quiescent current | Operational standby ⁴ , VJTAG = 3.63 V | T _J = 25°C | | 80 | 100 | μA |
| | | | T _J = 85°C | | 80 | 100 | μA |
| | | | T _J = 100°C | | 80 | 100 | μA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VJTAG = 0 V | | | 0 | 0 | μA |

Notes:

1. ICC is the 1.5 V power supplies, ICC and ICC15A.
2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.
4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

Table 3-9 • AFS600 Quiescent Supply Current Characteristics (continued)

| Parameter | Description | Conditions | Temp. | Min | Typ | Max | Unit |
|-----------|-----------------------------|--|------------------------|-----|-----|-----|------|
| IPP | Programming supply current | Non-programming mode, VPUMP = 3.63 V | T _J = 25°C | | 36 | 80 | μA |
| | | | T _J = 85°C | | 36 | 80 | μA |
| | | | T _J = 100°C | | 36 | 80 | μA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VPUMP = 0 V | | | 0 | 0 | μA |
| ICCNVM | Embedded NVM current | Reset asserted, VCCNVM = 1.575 V | T _J = 25°C | | 22 | 80 | μA |
| | | | T _J = 85°C | | 24 | 80 | μA |
| | | | T _J = 100°C | | 25 | 80 | μA |
| ICCPLL | 1.5 V PLL quiescent current | Operational standby, VCCPLL = 1.575 V | T _J = 25°C | | 130 | 200 | μA |
| | | | T _J = 85°C | | 130 | 200 | μA |
| | | | T _J = 100°C | | 130 | 200 | μA |

Notes:

1. ICC is the 1.5 V power supplies, ICC and ICC15A.
2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.
4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

Table 3-10 • AFS250 Quiescent Supply Current Characteristics

| Parameter | Description | Conditions | Temp. | Min | Typ | Max | Unit |
|--------------------|-------------------------------|--|------------------------|-----|------|-----|------|
| ICC ¹ | 1.5 V quiescent current | Operational standby ⁴ , VCC = 1.575 V | T _J = 25°C | | 4.8 | 10 | mA |
| | | | T _J = 85°C | | 8.2 | 30 | mA |
| | | | T _J = 100°C | | 15 | 50 | mA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VCC = 0 V | | | 0 | 0 | μA |
| ICC33 ² | 3.3 V analog supplies current | Operational standby ⁴ , VCC33 = 3.63 V | T _J = 25°C | | 9.8 | 13 | mA |
| | | | T _J = 85°C | | 9.8 | 14 | mA |
| | | | T _J = 100°C | | 10.8 | 15 | mA |
| | | Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V | T _J = 25°C | | 0.29 | 2 | mA |
| | | | T _J = 85°C | | 0.31 | 2 | mA |
| | | | T _J = 100°C | | 0.45 | 2 | mA |
| | | Standby mode ⁵ , VCC33 = 3.63V | T _J = 25°C | | 2.9 | 3.0 | mA |
| | | | T _J = 85°C | | 2.9 | 3.1 | mA |
| | | | T _J = 100°C | | 3.5 | 6 | mA |
| | | Sleep mode ⁶ , VCC33 = 3.63 V | T _J = 25°C | | 19 | 18 | μA |
| | | | T _J = 85°C | | 19 | 20 | μA |
| | | | T _J = 100°C | | 24 | 25 | μA |
| ICCI ³ | I/O quiescent current | Operational standby ⁶ , VCCIx = 3.63 V | T _J = 25°C | | 266 | 437 | μA |
| | | | T _J = 85°C | | 266 | 437 | μA |
| | | | T _J = 100°C | | 266 | 437 | μA |
| IJTAG | JTAG I/O quiescent current | Operational standby ⁴ , VJTAG = 3.63 V | T _J = 25°C | | 80 | 100 | μA |
| | | | T _J = 85°C | | 80 | 100 | μA |
| | | | T _J = 100°C | | 80 | 100 | μA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VJTAG = 0 V | | | 0 | 0 | μA |

Notes:

1. ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.
2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
3. ICCI includes all ICCI0, ICCI1, and ICCI2.
4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

Table 3-10 • AFS250 Quiescent Supply Current Characteristics (continued)

| Parameter | Description | Conditions | Temp. | Min | Typ | Max | Unit |
|-----------|-----------------------------|--|------------------------|-----|-----|-----|------|
| IPP | Programming supply current | Non-programming mode, VPUMP = 3.63 V | T _J = 25°C | | 37 | 80 | μA |
| | | | T _J = 85°C | | 37 | 80 | μA |
| | | | T _J = 100°C | | 80 | 100 | μA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VPUMP = 0 V | | | 0 | 0 | μA |
| ICCNVM | Embedded NVM current | Reset asserted, VCCNVM = 1.575 V | T _J = 25°C | | 10 | 40 | μA |
| | | | T _J = 85°C | | 14 | 40 | μA |
| | | | T _J = 100°C | | 14 | 40 | μA |
| ICCPLL | 1.5 V PLL quiescent current | Operational standby, VCCPLL = 1.575 V | T _J = 25°C | | 65 | 100 | μA |
| | | | T _J = 85°C | | 65 | 100 | μA |
| | | | T _J = 100°C | | 65 | 100 | μA |

Notes:

1. ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.
2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
3. ICCI includes all ICCI0, ICCI1, and ICCI2.
4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

Table 3-11 • AFS090 Quiescent Supply Current Characteristics

| Parameter | Description | Conditions | Temp. | Min | Typ | Max | Unit |
|--------------------|-------------------------------|--|------------------------|-----|------|-----|------|
| ICC ¹ | 1.5 V quiescent current | Operational standby ⁴ , VCC = 1.575 V | T _J = 25°C | | 5 | 7.5 | mA |
| | | | T _J = 85°C | | 6.5 | 20 | mA |
| | | | T _J = 100°C | | 14 | 48 | mA |
| | | Standby mode ⁵ or Sleep mode ⁶ , V _{CC} = 0 V | | | 0 | 0 | μA |
| ICC33 ² | 3.3 V analog supplies current | Operational standby ⁴ , VCC33 = 3.63 V | T _J = 25°C | | 9.8 | 12 | mA |
| | | | T _J = 85°C | | 9.8 | 12 | mA |
| | | | T _J = 100°C | | 10.7 | 15 | mA |
| | | Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V | T _J = 25°C | | 0.30 | 2 | mA |
| | | | T _J = 85°C | | 0.30 | 2 | mA |
| | | | T _J = 100°C | | 0.45 | 2 | mA |
| | | Standby mode ⁵ , VCC33 = 3.63 V | T _J = 25°C | | 2.9 | 2.9 | mA |
| | | | T _J = 85°C | | 2.9 | 3.0 | mA |
| | | | T _J = 100°C | | 3.5 | 6 | mA |
| | | Sleep mode ⁶ , VCC33 = 3.63 V | T _J = 25°C | | 17 | 18 | μA |
| | | | T _J = 85°C | | 18 | 20 | μA |
| | | | T _J = 100°C | | 24 | 25 | μA |
| ICCI ³ | I/O quiescent current | Operational standby ⁶ , VCCIx = 3.63 V | T _J = 25°C | | 260 | 437 | μA |
| | | | T _J = 85°C | | 260 | 437 | μA |
| | | | T _J = 100°C | | 260 | 437 | μA |
| IJTAG | JTAG I/O quiescent current | Operational standby ⁴ , VJTAG = 3.63 V | T _J = 25°C | | 80 | 100 | μA |
| | | | T _J = 85°C | | 80 | 100 | μA |
| | | | T _J = 100°C | | 80 | 100 | μA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VJTAG = 0 V | | | 0 | 0 | μA |
| IPP | Programming supply current | Non-programming mode, VPUMP = 3.63 V | T _J = 25°C | | 37 | 80 | μA |
| | | | T _J = 85°C | | 37 | 80 | μA |
| | | | T _J = 100°C | | 80 | 100 | μA |
| | | Standby mode ⁵ or Sleep mode ⁶ , VPUMP = 0 V | | | 0 | 0 | μA |

Notes:

1. ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.
2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
3. ICCI includes all ICCI0, ICCI1, and ICCI2.
4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

Table 3-11 • AFS090 Quiescent Supply Current Characteristics (continued)

| Parameter | Description | Conditions | Temp. | Min | Typ | Max | Unit |
|-----------|-----------------------------|--|------------------------|-----|-----|-----|------|
| ICCNVM | Embedded NVM current | Reset asserted, VCCNVM = 1.575 V | T _J = 25°C | | 10 | 40 | μA |
| | | | T _J = 85°C | | 14 | 40 | μA |
| | | | T _J = 100°C | | 14 | 40 | μA |
| ICCPLL | 1.5 V PLL quiescent current | Operational standby, VCCPLL = 1.575 V | T _J = 25°C | | 65 | 100 | μA |
| | | | T _J = 85°C | | 65 | 100 | μA |
| | | | T _J = 100°C | | 65 | 100 | μA |

Notes:

1. ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.
2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
3. ICCI includes all ICCI0, ICCI1, and ICCI2.
4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.

Power per I/O Pin

Table 3-12 • Summary of I/O Input Buffer Power (per pin)—Default I/O Software Settings

| | VCCI (V) | Static Power PDC7 (mW) ¹ | Dynamic Power PAC9 (μW/MHz) ² |
|---|----------|--|---|
| Applicable to Pro I/O Banks | | | |
| Single-Ended | | | |
| 3.3 V LVTTTL/LVCMOS | 3.3 | – | 17.39 |
| 3.3 V LVTTTL/LVCMOS – Schmitt trigger | 3.3 | – | 25.51 |
| 2.5 V LVCMOS | 2.5 | – | 5.76 |
| 2.5 V LVCMOS – Schmitt trigger | 2.5 | – | 7.16 |
| 1.8 V LVCMOS | 1.8 | – | 2.72 |
| 1.8 V LVCMOS – Schmitt trigger | 1.8 | – | 2.80 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 2.08 |
| 1.5 V LVCMOS (JESD8-11) – Schmitt trigger | 1.5 | – | 2.00 |
| 3.3 V PCI | 3.3 | – | 18.82 |
| 3.3 V PCI – Schmitt trigger | 3.3 | – | 20.12 |
| 3.3 V PCI-X | 3.3 | – | 18.82 |
| 3.3 V PCI-X – Schmitt trigger | 3.3 | – | 20.12 |
| Voltage-Referenced | | | |
| 3.3 V GTL | 3.3 | 2.90 | 8.23 |
| 2.5 V GTL | 2.5 | 2.13 | 4.78 |
| 3.3 V GTL+ | 3.3 | 2.81 | 4.14 |
| 2.5 V GTL+ | 2.5 | 2.57 | 3.71 |
| HSTL (I) | 1.5 | 0.17 | 2.03 |
| HSTL (II) | 1.5 | 0.17 | 2.03 |
| SSTL2 (I) | 2.5 | 1.38 | 4.48 |
| SSTL2 (II) | 2.5 | 1.38 | 4.48 |
| SSTL3 (I) | 3.3 | 3.21 | 9.26 |
| SSTL3 (II) | 3.3 | 3.21 | 9.26 |
| Differential | | | |
| LVDS | 2.5 | 2.26 | 1.50 |
| LVPECL | 3.3 | 5.71 | 2.17 |

Notes:

1. PDC7 is the static power (where applicable) measured on VCCI.
2. PAC9 is the total dynamic power measured on VCC and VCCI.

Table 3-12 • Summary of I/O Input Buffer Power (per pin)—Default I/O Software Settings (continued)

| | VCCI (V) | Static Power PDC7 (mW) ¹ | Dynamic Power PAC9 (μW/MHz) ² |
|---|----------|--|---|
| Applicable to Advanced I/O Banks | | | |
| Single-Ended | | | |
| 3.3 V LVTTTL/LVCMOS | 3.3 | – | 16.69 |
| 2.5 V LVCMOS | 2.5 | – | 5.12 |
| 1.8 V LVCMOS | 1.8 | – | 2.13 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 1.45 |
| 3.3 V PCI | 3.3 | – | 18.11 |
| 3.3 V PCI-X | 3.3 | – | 18.11 |
| Differential | | | |
| LVDS | 2.5 | 2.26 | 1.20 |
| LVPECL | 3.3 | 5.72 | 1.87 |
| Applicable to Standard I/O Banks | | | |
| 3.3 V LVTTTL/LVCMOS | 3.3 | – | 16.79 |
| 2.5 V LVCMOS | 2.5 | – | 5.19 |
| 1.8 V LVCMOS | 1.8 | – | 2.18 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 1.52 |

Notes:

1. PDC7 is the static power (where applicable) measured on VCCI.
2. PAC9 is the total dynamic power measured on VCC and VCCI.

Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings¹

| | C _{LOAD} (pF) | V _{CCI} (V) | Static Power PDC8 (mW) ² | Dynamic Power PAC10 (μW/MHz) ³ |
|---|------------------------|----------------------|-------------------------------------|---|
| Applicable to Pro I/O Banks | | | | |
| Single-Ended | | | | |
| 3.3 V LVTTTL/LVCMOS | 35 | 3.3 | – | 474.70 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 270.73 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 151.78 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 104.55 |
| 3.3 V PCI | 10 | 3.3 | – | 204.61 |
| 3.3 V PCI-X | 10 | 3.3 | – | 204.61 |
| Voltage-Referenced | | | | |
| 3.3 V GTL | 10 | 3.3 | – | 24.08 |
| 2.5 V GTL | 10 | 2.5 | – | 13.52 |
| 3.3 V GTL+ | 10 | 3.3 | – | 24.10 |
| 2.5 V GTL+ | 10 | 2.5 | – | 13.54 |
| HSTL (I) | 20 | 1.5 | 7.08 | 26.22 |
| HSTL (II) | 20 | 1.5 | 13.88 | 27.22 |
| SSTL2 (I) | 30 | 2.5 | 16.69 | 105.56 |
| SSTL2 (II) | 30 | 2.5 | 25.91 | 116.60 |
| SSTL3 (I) | 30 | 3.3 | 26.02 | 114.87 |
| SSTL3 (II) | 30 | 3.3 | 42.21 | 131.76 |
| Differential | | | | |
| LVDS | – | 2.5 | 7.70 | 89.62 |
| LVPECL | – | 3.3 | 19.42 | 168.02 |
| Applicable to Advanced I/O Banks | | | | |
| Single-Ended | | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 35 | 3.3 | – | 468.67 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 267.48 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 149.46 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 103.12 |
| 3.3 V PCI | 10 | 3.3 | – | 201.02 |
| 3.3 V PCI-X | 10 | 3.3 | – | 201.02 |

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.
2. PDC8 is the static power (where applicable) measured on V_{CCI}.
3. PAC10 is the total dynamic power measured on V_{CC} and V_{CCI}.

Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings¹ (continued)

| | C_{LOAD} (pF) | VCCI (V) | Static Power PDC8 (mW) ² | Dynamic Power PAC10 (μ W/MHz) ³ |
|---|-----------------|----------|-------------------------------------|---|
| Differential | | | | |
| LVDS | – | 2.5 | 7.74 | 88.92 |
| LVPECL | – | 3.3 | 19.54 | 166.52 |
| Applicable to Standard I/O Banks | | | | |
| Single-Ended | | | | |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 35 | 3.3 | – | 431.08 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 247.36 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 128.46 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 89.46 |

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.
2. PDC8 is the static power (where applicable) measured on VCCI.
3. PAC10 is the total dynamic power measured on VCC and VCCI.

Dynamic Power Consumption of Various Internal Resources

Table 3-14 • Different Components Contributing to the Dynamic Power Consumption in Fusion Devices

| Parameter | Definition | Power Supply | | Device-Specific Dynamic Contributions | | | | Units |
|-----------|--|--------------|-----------------------------|---------------------------------------|--------|--------|--------|--------|
| | | Name | Setting | AFS1500 | AFS600 | AFS250 | AFS090 | |
| PAC1 | Clock contribution of a Global Rib | VCC | 1.5 V | 14.5 | 12.8 | 11 | 11 | μW/MHz |
| PAC2 | Clock contribution of a Global Spine | VCC | 1.5 V | 2.5 | 1.9 | 1.6 | 0.8 | μW/MHz |
| PAC3 | Clock contribution of a VersaTile row | VCC | 1.5 V | 0.81 | | | | μW/MHz |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | VCC | 1.5 V | 0.11 | | | | μW/MHz |
| PAC5 | First contribution of a VersaTile used as a sequential module | VCC | 1.5 V | 0.07 | | | | μW/MHz |
| PAC6 | Second contribution of a VersaTile used as a sequential module | VCC | 1.5 V | 0.29 | | | | μW/MHz |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | VCC | 1.5 V | 0.29 | | | | μW/MHz |
| PAC8 | Average contribution of a routing net | VCC | 1.5 V | 0.70 | | | | μW/MHz |
| PAC9 | Contribution of an I/O input pin (standard dependent) | VCCI | See Table 3-12 on page 3-18 | | | | | |
| PAC10 | Contribution of an I/O output pin (standard dependent) | VCCI | See Table 3-13 on page 3-20 | | | | | |
| PAC11 | Average contribution of a RAM block during a read operation | VCC | 1.5 V | 25 | | | | μW/MHz |
| PAC12 | Average contribution of a RAM block during a write operation | VCC | 1.5 V | 30 | | | | μW/MHz |
| PAC13 | Dynamic Contribution for PLL | VCC | 1.5 V | 2.6 | | | | μW/MHz |
| PAC15 | Contribution of NVM block during a read operation (F < 33MHz) | VCC | 1.5 V | 358 | | | | μW/MHz |
| PAC16 | 1st contribution of NVM block during a read operation (F > 33 MHz) | VCC | 1.5 V | 12.88 | | | | mW |
| PAC17 | 2nd contribution of NVM block during a read operation (F > 33 MHz) | VCC | 1.5 V | 4.8 | | | | μW/MHz |
| PAC18 | Crystal Oscillator contribution | VCC33A | 3.3 V | 0.63 | | | | mW |
| PAC19 | RC Oscillator contribution | VCC33A | 3.3 V | 3.3 | | | | mW |
| PAC20 | Analog Block dynamic power contribution of ADC | VCC | 1.5 V | 3 | | | | mW |

Static Power Consumption of Various Internal Resources

Table 3-15 • Different Components Contributing to the Static Power Consumption in Fusion Devices

| Parameter | Definition | Power Supply | | Device-Specific Static Contributions | | | | Units |
|-----------|---|--------------|---|--------------------------------------|--------|--------|--------|-------|
| | | | | AFS1500 | AFS600 | AFS250 | AFS090 | |
| PDC1 | Core static power contribution in operating mode | VCC | 1.5 V | 18 | 7.5 | 4.50 | 3.00 | mW |
| PDC2 | Device static power contribution in standby mode | VCC33A | 3.3 V | 0.66 | | | | mW |
| PDC3 | Device static power contribution in sleep mode | VCC33A | 3.3 V | 0.03 | | | | mW |
| PDC4 | NVM static power contribution | VCC | 1.5 V | 1.19 | | | | mW |
| PDC5 | Analog Block static power contribution of ADC | VCC33A | 3.3 V | 8.25 | | | | mW |
| PDC6 | Analog Block static power contribution per Quad | VCC33A | 3.3 V | 3.3 | | | | mW |
| PDC7 | Static contribution per input pin – standard dependent contribution | VCCI | See Table 3-12 on page 3-18 | | | | | |
| PDC8 | Static contribution per input pin – standard dependent contribution | VCCI | See Table 3-13 on page 3-20 | | | | | |
| PDC9 | Static contribution for PLL | VCC | 1.5 V | 2.55 | | | | mW |

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of NVM blocks used in the design
- The number of Analog Quads used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 3-16 on page 3-27](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 3-17 on page 3-27](#).
- Read rate and write rate to the RAM—guidelines are provided for typical applications in [Table 3-17 on page 3-27](#).
- Read rate to the NVM blocks

The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

Operating Mode, Standby Mode, and Sleep Mode

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

Operating Mode

$$P_{STAT} = PDC1 + (N_{NVM-BLOCKS} * PDC4) + PDC5 + (N_{QUADS} * PDC6) + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8) + (N_{PLLs} * PDC9)$$

$N_{NVM-BLOCKS}$ is the number of NVM blocks available in the device.

N_{QUADS} is the number of Analog Quads used in the design.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLs} is the number of PLLs available in the device.

Standby Mode

$$P_{STAT} = PDC2$$

Sleep Mode

$$P_{STAT} = PDC3$$

Total Dynamic Power Consumption— P_{DYN}

Operating Mode

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL-OSC} + P_{RC-OSC} + P_{AB}$$

Standby Mode

$$P_{DYN} = P_{XTL-OSC}$$

Sleep Mode

$$P_{DYN} = 0 \text{ W}$$

Global Clock Dynamic Contribution— P_{CLOCK}

Operating Mode

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the “Spine Architecture” section of the Global Resources chapter in the [Fusion and Extended Temperature Fusion FPGA Fabric User's Guide](#).

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the “Spine Architecture” section of the Global Resources chapter in the [Fusion and Extended Temperature Fusion FPGA Fabric User's Guide](#).

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Sleep Mode

$$P_{CLOCK} = 0 \text{ W}$$

Sequential Cells Dynamic Contribution— P_{S-CELL}

Operating Mode

$$P_{S-CELL} = N_{S-CELL} * (PAC5 + (\alpha_1 / 2) * PAC6) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 3-16 on page 3-27](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$$P_{S-CELL} = 0 \text{ W}$$

Combinatorial Cells Dynamic Contribution— P_{C-CELL}

Operating Mode

$$P_{C-CELL} = N_{C-CELL} * (\alpha_1 / 2) * PAC7 * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 3-16 on page 3-27](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$$P_{C-CELL} = 0 \text{ W}$$

Routing Net Dynamic Contribution— P_{NET}

Operating Mode

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * (\alpha_1 / 2) * PAC8 * F_{CLK}$$

N_{S-CELL} is the number VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 3-16 on page 3-27](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$$P_{NET} = 0 \text{ W}$$

I/O Input Buffer Dynamic Contribution— P_{INPUTS}

Operating Mode

$$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 3-16 on page 3-27](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$$P_{INPUTS} = 0 \text{ W}$$

I/O Output Buffer Dynamic Contribution— $P_{OUTPUTS}$

Operating Mode

$$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 3-16 on page 3-27](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 3-17 on page 3-27](#).

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$$P_{OUTPUTS} = 0 \text{ W}$$

RAM Dynamic Contribution— P_{MEMORY}

Operating Mode

$$P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ-CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE-CLOCK})$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in [Table 3-17 on page 3-27](#).

β_3 the RAM enable rate for write operations—guidelines are provided in [Table 3-17 on page 3-27](#).

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

Standby Mode and Sleep Mode

$$P_{MEMORY} = 0 \text{ W}$$

PLL/CCC Dynamic Contribution— P_{PLL}

Operating Mode

$$P_{PLL} = PAC13 * F_{CLKOUT}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.¹

Standby Mode and Sleep Mode

$$P_{PLL} = 0 \text{ W}$$

Nonvolatile Memory Dynamic Contribution— P_{NVM}

Operating Mode

The NVM dynamic power consumption is a piecewise linear function of frequency.

$$P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * PAC15 * F_{READ-NVM} \text{ when } F_{READ-NVM} \leq 33 \text{ MHz,}$$

$$P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * (PAC16 + PAC17 * F_{READ-NVM} \text{ when } F_{READ-NVM} > 33 \text{ MHz}$$

$N_{NVM-BLOCKS}$ is the number of NVM blocks used in the design (2 in AFS600).

β_4 is the NVM enable rate for read operations. Default is 0 (NVM mainly in idle state).

$F_{READ-NVM}$ is the NVM read clock frequency.

Standby Mode and Sleep Mode

$$P_{NVM} = 0 \text{ W}$$

Crystal Oscillator Dynamic Contribution— $P_{XTL-OSC}$

Operating Mode

$$P_{XTL-OSC} = PAC18$$

Standby Mode

$$P_{XTL-OSC} = PAC18$$

Sleep Mode

$$P_{XTL-OSC} = 0 \text{ W}$$

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.

RC Oscillator Dynamic Contribution— P_{RC-OSC}

Operating Mode

$$P_{RC-OSC} = PAC19$$

Standby Mode and Sleep Mode

$$P_{RC-OSC} = 0 \text{ W}$$

Analog System Dynamic Contribution— P_{AB}

Operating Mode

$$P_{AB} = PAC20$$

Standby Mode and Sleep Mode

$$P_{AB} = 0 \text{ W}$$

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

Table 3-16 • Toggle Rate Guidelines Recommended for Power Calculation

| Component | Definition | Guideline |
|------------|----------------------------------|-----------|
| α_1 | Toggle rate of VersaTile outputs | 10% |
| α_2 | I/O buffer toggle rate | 10% |

Table 3-17 • Enable Rate Guidelines Recommended for Power Calculation

| Component | Definition | Guideline |
|-----------|--------------------------------------|-----------|
| β_1 | I/O output buffer enable rate | 100% |
| β_2 | RAM enable rate for read operations | 12.5% |
| β_3 | RAM enable rate for write operations | 12.5% |
| β_4 | NVM enable rate for read operations | 0% |

Example of Power Calculation

This example considers a shift register with 5,000 storage tiles, including a counter and memory that stores analog information. The shift register is clocked at 50 MHz and stores and reads information from a RAM.

The device used is a commercial AFS600 device operating in typical conditions.

The calculation below uses the power calculation methodology previously presented and shows how to determine the dynamic and static power consumption of resources used in the application.

Also included in the example is the calculation of power consumption in operating, standby, and sleep modes to illustrate the benefit of power-saving modes.

Global Clock Contribution— P_{CLOCK}

$$F_{\text{CLK}} = 50 \text{ MHz}$$

$$\text{Number of sequential VersaTiles: } N_{\text{S-CELL}} = 5,000$$

$$\text{Estimated number of Spines: } N_{\text{SPINES}} = 5$$

$$\text{Estimated number of Rows: } N_{\text{ROW}} = 313$$

Operating Mode

$$P_{\text{CLOCK}} = (\text{PAC1} + N_{\text{SPINE}} * \text{PAC2} + N_{\text{ROW}} * \text{PAC3} + N_{\text{S-CELL}} * \text{PAC4}) * F_{\text{CLK}}$$

$$P_{\text{CLOCK}} = (0.0128 + 5 * 0.0019 + 313 * 0.00081 + 5,000 * 0.00011) * 50$$

$$P_{\text{CLOCK}} = 41.28 \text{ mW}$$

Standby Mode and Sleep Mode

$$P_{\text{CLOCK}} = 0 \text{ W}$$

Logic—Sequential Cells, Combinational Cells, and Routing Net Contributions— $P_{\text{S-CELL}}$, $P_{\text{C-CELL}}$, and P_{NET}

$$F_{\text{CLK}} = 50 \text{ MHz}$$

$$\text{Number of sequential VersaTiles: } N_{\text{S-CELL}} = 5,000$$

$$\text{Number of combinatorial VersaTiles: } N_{\text{C-CELL}} = 6,000$$

$$\text{Estimated toggle rate of VersaTile outputs: } \alpha_1 = 0.1 \text{ (10\%)}$$

Operating Mode

$$P_{\text{S-CELL}} = N_{\text{S-CELL}} * (\text{PAC5} + (\alpha_1 / 2) * \text{PAC6}) * F_{\text{CLK}}$$

$$P_{\text{S-CELL}} = 5,000 * (0.00007 + (0.1 / 2) * 0.00029) * 50$$

$$P_{\text{S-CELL}} = 21.13 \text{ mW}$$

$$P_{\text{C-CELL}} = N_{\text{C-CELL}} * (\alpha_1 / 2) * \text{PAC7} * F_{\text{CLK}}$$

$$P_{\text{C-CELL}} = 6,000 * (0.1 / 2) * 0.00029 * 50$$

$$P_{\text{C-CELL}} = 4.35 \text{ mW}$$

$$P_{\text{NET}} = (N_{\text{S-CELL}} + N_{\text{C-CELL}}) * (\alpha_1 / 2) * \text{PAC8} * F_{\text{CLK}}$$

$$P_{\text{NET}} = (5,000 + 6,000) * (0.1 / 2) * 0.0007 * 50$$

$$P_{\text{NET}} = 19.25 \text{ mW}$$

$$P_{\text{LOGIC}} = P_{\text{S-CELL}} + P_{\text{C-CELL}} + P_{\text{NET}}$$

$$P_{\text{LOGIC}} = 21.13 \text{ mW} + 4.35 \text{ mW} + 19.25 \text{ mW}$$

$$P_{\text{LOGIC}} = 44.73 \text{ mW}$$

Standby Mode and Sleep Mode

$$P_{S-CELL} = 0 \text{ W}$$

$$P_{C-CELL} = 0 \text{ W}$$

$$P_{NET} = 0 \text{ W}$$

$$P_{LOGIC} = 0 \text{ W}$$

I/O Input and Output Buffer Contribution— $P_{I/O}$

This example uses LVTTTL 3.3 V I/O cells. The output buffers are 12 mA-capable, configured with high output slew and driving a 35 pF output load.

$$F_{CLK} = 50 \text{ MHz}$$

$$\text{Number of input pins used: } N_{INPUTS} = 30$$

$$\text{Number of output pins used: } N_{OUTPUTS} = 40$$

$$\text{Estimated I/O buffer toggle rate: } \alpha_2 = 0.1 \text{ (10\%)}$$

$$\text{Estimated IO buffer enable rate: } \beta_1 = 1 \text{ (100\%)}$$

Operating Mode

$$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$$

$$P_{INPUTS} = 30 * (0.1 / 2) * 0.01739 * 50$$

$$P_{INPUTS} = 1.30 \text{ mW}$$

$$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * PAC10 * F_{CLK}$$

$$P_{OUTPUTS} = 40 * (0.1 / 2) * 1 * 0.4747 * 50$$

$$P_{OUTPUTS} = 47.47 \text{ mW}$$

$$P_{I/O} = P_{INPUTS} + P_{OUTPUTS}$$

$$P_{I/O} = 1.30 \text{ mW} + 47.47 \text{ mW}$$

$$P_{I/O} = 48.77 \text{ mW}$$

Standby Mode and Sleep Mode

$$P_{INPUTS} = 0 \text{ W}$$

$$P_{OUTPUTS} = 0 \text{ W}$$

$$P_{I/O} = 0 \text{ W}$$

RAM Contribution— P_{MEMORY}

$$\text{Frequency of Read Clock: } F_{READ-CLOCK} = 10 \text{ MHz}$$

$$\text{Frequency of Write Clock: } F_{WRITE-CLOCK} = 10 \text{ MHz}$$

$$\text{Number of RAM blocks: } N_{BLOCKS} = 20$$

$$\text{Estimated RAM Read Enable Rate: } \beta_2 = 0.125 \text{ (12.5\%)}$$

$$\text{Estimated RAM Write Enable Rate: } \beta_3 = 0.125 \text{ (12.5\%)}$$

Operating Mode

$$P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ-CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE-CLOCK})$$

$$P_{MEMORY} = (20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10)$$

$$P_{MEMORY} = 1.38 \text{ mW}$$

Standby Mode and Sleep Mode

$$P_{MEMORY} = 0 \text{ W}$$

PLL/CCC Contribution— P_{PLL}

PLL is not used in this application.

$$P_{PLL} = 0 \text{ W}$$

Nonvolatile Memory— P_{NVM}

Nonvolatile memory is not used in this application.

$$P_{NVM} = 0 \text{ W}$$

Crystal Oscillator— $P_{XTL-OSC}$

The application utilizes standby mode. The crystal oscillator is assumed to be active.

Operating Mode

$$P_{XTL-OSC} = PAC18$$

$$P_{XTL-OSC} = 0.63 \text{ mW}$$

Standby Mode

$$P_{XTL-OSC} = PAC18$$

$$P_{XTL-OSC} = 0.63 \text{ mW}$$

Sleep Mode

$$P_{XTL-OSC} = 0 \text{ W}$$

RC Oscillator— P_{RC-OSC}
Operating Mode

$$P_{RC-OSC} = PAC19$$

$$P_{RC-OSC} = 3.30 \text{ mW}$$

Standby Mode and Sleep Mode

$$P_{RC-OSC} = 0 \text{ W}$$

Analog System— P_{AB}

Number of Quads used: $N_{QUADS} = 4$

Operating Mode

$$P_{AB} = PAC20$$

$$P_{AB} = 3.00 \text{ mW}$$

Standby Mode and Sleep Mode

$$P_{AB} = 0 \text{ W}$$

Total Dynamic Power Consumption— P_{DYN}
Operating Mode

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL-OSC} + P_{RC-OSC} + P_{AB}$$

$$P_{DYN} = 41.28 \text{ mW} + 21.1 \text{ mW} + 4.35 \text{ mW} + 19.25 \text{ mW} + 1.30 \text{ mW} + 47.47 \text{ mW} + 1.38 \text{ mW} + 0 + 0 + 0.63 \text{ mW} + 3.30 \text{ mW} + 3.00 \text{ mW}$$

$$P_{DYN} = 143.06 \text{ mW}$$

Standby Mode

$$P_{DYN} = P_{XTL-OSC}$$

$$P_{DYN} = 0.63 \text{ mW}$$

Sleep Mode

$$P_{DYN} = 0 \text{ W}$$

Total Static Power Consumption— P_{STAT}

 Number of Quads used: $N_{QUADS} = 4$

 Number of NVM blocks available (AFS600): $N_{NVM-BLOCKS} = 2$

 Number of input pins used: $N_{INPUTS} = 30$

 Number of output pins used: $N_{OUTPUTS} = 40$
Operating Mode

$$P_{STAT} = PDC1 + (N_{NVM-BLOCKS} * PDC4) + PDC5 + (N_{QUADS} * PDC6) + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8)$$

$$P_{STAT} = 7.50 \text{ mW} + (2 * 1.19 \text{ mW}) + 8.25 \text{ mW} + (4 * 3.30 \text{ mW}) + (30 * 0.00) + (40 * 0.00)$$

$$P_{STAT} = 31.33 \text{ mW}$$

Standby Mode

$$P_{STAT} = PDC2$$

$$P_{STAT} = 0.03 \text{ mW}$$

Sleep Mode

$$P_{STAT} = PDC3$$

$$P_{STAT} = 0.03 \text{ mW}$$

Total Power Consumption— P_{TOTAL}

In operating mode, the total power consumption of the device is 174.39 mW:

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

$$P_{TOTAL} = 143.06 \text{ mW} + 31.33 \text{ mW}$$

$$P_{TOTAL} = 174.39 \text{ mW}$$

In standby mode, the total power consumption of the device is limited to 0.66 mW:

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

$$P_{TOTAL} = 0.03 \text{ mW} + 0.63 \text{ mW}$$

$$P_{TOTAL} = 0.66 \text{ mW}$$

In sleep mode, the total power consumption of the device drops as low as 0.03 mW:

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

$$P_{TOTAL} = 0.03 \text{ mW}$$

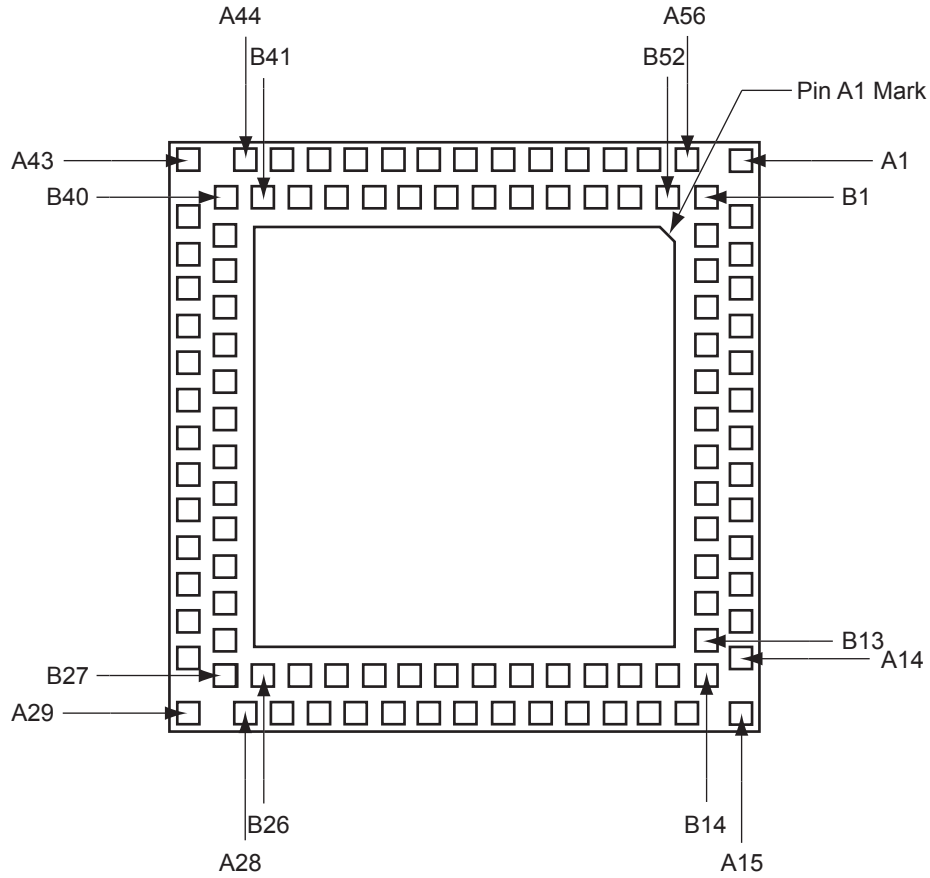
Power Consumption

Table 3-18 • Power Consumption

| Parameter | Description | Condition | Min. | Typical | Max. | Units |
|---------------------------|---------------------------------------|----------------|------|--|------|--|
| Crystal Oscillator | | | | | | |
| ISTBXTAL | Standby Current of Crystal Oscillator | | | 10 | | μA |
| IDYNXTAL | Operating Current | RC | | 0.6 | | mA |
| | | 0.032–0.2 | | 0.19 | | mA |
| | | 0.2–2.0 | | 0.6 | | mA |
| | | 2.0–20.0 | | 0.6 | | mA |
| RC Oscillator | | | | | | |
| IDYNRC | Operating Current | | | 1 | | mA |
| ACM | | | | | | |
| | Operating Current (fixed clock) | | | 200 | | μA/MHz |
| | Operating Current (user clock) | | | 30 | | μA |
| NVM System | | | | | | |
| | NVM Array Operating Power | Idle | | 795 | | μA |
| | | Read operation | | See Table 3-15 on page 3-23. | | See Table 3-15 on page 3-23. |
| | | Erase | | 900 | | μA |
| | | Write | | 900 | | μA |
| PNVMCTRL | NVM Controller Operating Power | | | 20 | | μW/MHz |

4 – Package Pin Assignments

QN108



Note: The die attach paddle center of the package is tied to ground (GND).

Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| QN108 | |
|------------|-----------------|
| Pin Number | AFS090 Function |
| A1 | NC |
| A2 | GNDQ |
| A3 | GAA2/IO52PDB3V0 |
| A4 | GND |
| A5 | GFA1/IO47PDB3V0 |
| A6 | GEB1/IO45PDB3V0 |
| A7 | VCCOSC |
| A8 | XTAL2 |
| A9 | GEA1/IO44PPB3V0 |
| A10 | GEA0/IO44NPB3V0 |
| A11 | GEB2/IO42PDB3V0 |
| A12 | VCCNVM |
| A13 | VCC15A |
| A14 | PCAP |
| A15 | NC |
| A16 | GNDA |
| A17 | AV0 |
| A18 | AG0 |
| A19 | ATRNT0 |
| A20 | AT1 |
| A21 | AC1 |
| A22 | AV2 |
| A23 | AG2 |
| A24 | AT2 |
| A25 | AT3 |
| A26 | AC3 |
| A27 | GNDQA |
| A28 | ADCGNDREF |
| A29 | NC |
| A30 | GNDA |
| A31 | PTEM |
| A32 | GNDNVM |
| A33 | VPUMP |
| A34 | TCK |
| A35 | TMS |
| A36 | TRST |
| A37 | GDB1/IO39PSB1V0 |
| A38 | GDC1/IO38PDB1V0 |

| QN108 | |
|------------|-----------------|
| Pin Number | AFS090 Function |
| A39 | GND |
| A40 | GCB1/IO35PDB1V0 |
| A41 | GCB2/IO33PDB1V0 |
| A42 | GBA2/IO31PDB1V0 |
| A43 | NC |
| A44 | GBA1/IO30RSB0V0 |
| A45 | GBB1/IO28RSB0V0 |
| A46 | GND |
| A47 | VCC |
| A48 | GBC1/IO26RSB0V0 |
| A49 | IO21RSB0V0 |
| A50 | IO19RSB0V0 |
| A51 | IO09RSB0V0 |
| A52 | GAC0/IO04RSB0V0 |
| A53 | VCCIB0 |
| A54 | GND |
| A55 | GAB0/IO02RSB0V0 |
| A56 | GAA0/IO00RSB0V0 |
| B1 | VCOMPLA |
| B2 | VCCIB3 |
| B3 | GAB2/IO52NDB3V0 |
| B4 | VCCIB3 |
| B5 | GFA0/IO47NDB3V0 |
| B6 | GEB0/IO45NDB3V0 |
| B7 | XTAL1 |
| B8 | GNDOSC |
| B9 | GEC2/IO43PSB3V0 |
| B10 | GEA2/IO42NDB3V0 |
| B11 | VCC |
| B12 | GNDNVM |
| B13 | NCAP |
| B14 | VCC33PMP |
| B15 | VCC33N |
| B16 | GNDQA |
| B17 | AC0 |
| B18 | AT0 |
| B19 | AG1 |
| B20 | AV1 |

| QN108 | |
|------------|-----------------|
| Pin Number | AFS090 Function |
| B21 | AC2 |
| B22 | ATRNT1 |
| B23 | AG3 |
| B24 | AV3 |
| B25 | VCC33A |
| B26 | VAREF |
| B27 | PUB |
| B28 | VCC33A |
| B29 | PTBASE |
| B30 | VCCNVM |
| B31 | VCC |
| B32 | TDI |
| B33 | TDO |
| B34 | VJTAG |
| B35 | GDC0/IO38NDB1V0 |
| B36 | VCCIB1 |
| B37 | GCB0/IO35NDB1V0 |
| B38 | GCC2/IO33NDB1V0 |
| B39 | GBB2/IO31NDB1V0 |
| B40 | VCCIB1 |
| B41 | GNDQ |
| B42 | GBA0/IO29RSB0V0 |
| B43 | VCCIB0 |
| B44 | GBB0/IO27RSB0V0 |
| B45 | GBC0/IO25RSB0V0 |
| B46 | IO20RSB0V0 |
| B47 | IO10RSB0V0 |
| B48 | GAC1/IO05RSB0V0 |
| B49 | GAB1/IO03RSB0V0 |
| B50 | VCC |
| B51 | GAA1/IO01RSB0V0 |
| B52 | VCCPLA |

QN180



Note: The die attach paddle center of the package is tied to ground (GND).

Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| QN180 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS090 Function | AFS250 Function |
| A1 | GNDQ | GNDQ |
| A2 | VCCIB3 | VCCIB3 |
| A3 | GAB2/IO52NDB3V0 | IO74NDB3V0 |
| A4 | GFA2/IO51NDB3V0 | IO71NDB3V0 |
| A5 | GFC2/IO50NDB3V0 | IO69NPB3V0 |
| A6 | VCCIB3 | VCCIB3 |
| A7 | GFA1/IO47PPB3V0 | GFB1/IO67PPB3V0 |
| A8 | GEB0/IO45NDB3V0 | NC |
| A9 | XTAL1 | XTAL1 |
| A10 | GNDOSC | GNDOSC |
| A11 | GEC2/IO43PPB3V0 | GEA1/IO61PPB3V0 |
| A12 | IO43NPB3V0 | GEA0/IO61NPB3V0 |
| A13 | NC | VCCIB3 |
| A14 | GNDNVM | GNDNVM |
| A15 | PCAP | PCAP |
| A16 | VCC33PMP | VCC33PMP |
| A17 | NC | NC |
| A18 | AV0 | AV0 |
| A19 | AG0 | AG0 |
| A20 | ATRTN0 | ATRTN0 |
| A21 | AG1 | AG1 |
| A22 | AC1 | AC1 |
| A23 | AV2 | AV2 |
| A24 | AT2 | AT2 |
| A25 | AT3 | AT3 |
| A26 | AC3 | AC3 |
| A27 | AV4 | AV4 |
| A28 | AC4 | AC4 |
| A29 | AT4 | AT4 |
| A30 | NC | AG5 |
| A31 | NC | AV5 |
| A32 | ADCGNDREF | ADCGNDREF |
| A33 | VCC33A | VCC33A |
| A34 | GNDA | GNDA |
| A35 | PTBASE | PTBASE |
| A36 | VCCNVM | VCCNVM |

| QN180 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS090 Function | AFS250 Function |
| A37 | VPUMP | VPUMP |
| A38 | TDI | TDI |
| A39 | TDO | TDO |
| A40 | VJTAG | VJTAG |
| A41 | GDB1/IO39PPB1V0 | GDA1/IO54PPB1V0 |
| A42 | GDC1/IO38PDB1V0 | GDB1/IO53PDB1V0 |
| A43 | VCC | VCC |
| A44 | GCB0/IO35NPB1V0 | GCB0/IO48NPB1V0 |
| A45 | GCC1/IO34PDB1V0 | GCC1/IO47PDB1V0 |
| A46 | VCCIB1 | VCCIB1 |
| A47 | GBC2/IO32PPB1V0 | GGB2/IO41PPB1V0 |
| A48 | VCCIB1 | VCCIB1 |
| A49 | NC | NC |
| A50 | GBA0/IO29RSB0V0 | GGB1/IO37RSB0V0 |
| A51 | VCCIB0 | VCCIB0 |
| A52 | GBB0/IO27RSB0V0 | GBC0/IO34RSB0V0 |
| A53 | GBC1/IO26RSB0V0 | IO33RSB0V0 |
| A54 | IO24RSB0V0 | IO29RSB0V0 |
| A55 | IO21RSB0V0 | IO26RSB0V0 |
| A56 | VCCIB0 | VCCIB0 |
| A57 | IO15RSB0V0 | IO21RSB0V0 |
| A58 | IO10RSB0V0 | IO13RSB0V0 |
| A59 | IO07RSB0V0 | IO10RSB0V0 |
| A60 | GAC0/IO04RSB0V0 | IO06RSB0V0 |
| A61 | GAB1/IO03RSB0V0 | GAC1/IO05RSB0V0 |
| A62 | VCC | VCC |
| A63 | GAA1/IO01RSB0V0 | GAB0/IO02RSB0V0 |
| A64 | NC | NC |
| B1 | VCOMPLA | VCOMPLA |
| B2 | GAA2/IO52PDB3V0 | GAC2/IO74PDB3V0 |
| B3 | GAC2/IO51PDB3V0 | GFA2/IO71PDB3V0 |
| B4 | GFB2/IO50PDB3V0 | GFB2/IO70PSB3V0 |
| B5 | VCC | VCC |
| B6 | GFC0/IO49NDB3V0 | GFC0/IO68NDB3V0 |
| B7 | GEB1/IO45PDB3V0 | NC |
| B8 | VCCOSC | VCCOSC |

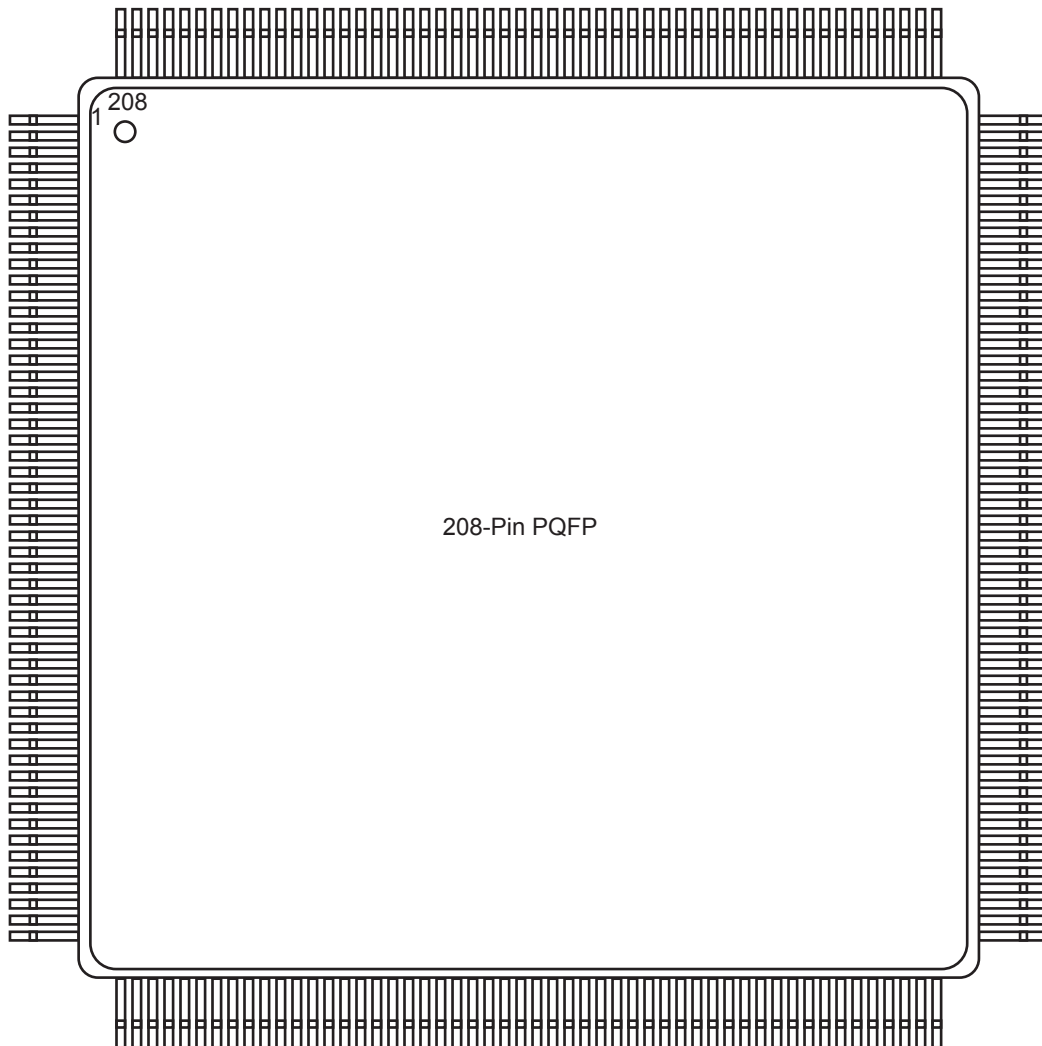
| QN180 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS090 Function | AFS250 Function |
| B9 | XTAL2 | XTAL2 |
| B10 | GEA0/IO44NDB3V0 | GFA0/IO66NDB3V0 |
| B11 | GEB2/IO42PDB3V0 | IO60NDB3V0 |
| B12 | VCC | VCC |
| B13 | VCCNVM | VCCNVM |
| B14 | VCC15A | VCC15A |
| B15 | NCAP | NCAP |
| B16 | VCC33N | VCC33N |
| B17 | GNDQAQ | GNDQAQ |
| B18 | AC0 | AC0 |
| B19 | AT0 | AT0 |
| B20 | AT1 | AT1 |
| B21 | AV1 | AV1 |
| B22 | AC2 | AC2 |
| B23 | ATRTN1 | ATRTN1 |
| B24 | AG3 | AG3 |
| B25 | AV3 | AV3 |
| B26 | AG4 | AG4 |
| B27 | ATRTN2 | ATRTN2 |
| B28 | NC | AC5 |
| B29 | VCC33A | VCC33A |
| B30 | VAREF | VAREF |
| B31 | PUB | PUB |
| B32 | PTEM | PTEM |
| B33 | GNDNVM | GNDNVM |
| B34 | VCC | VCC |
| B35 | TCK | TCK |
| B36 | TMS | TMS |
| B37 | TRST | TRST |
| B38 | GDB2/IO41PSB1V0 | GDA2/IO55PSB1V0 |
| B39 | GDC0/IO38NDB1V0 | GDB0/IO53NDB1V0 |
| B40 | VCCIB1 | VCCIB1 |
| B41 | GCA1/IO36PDB1V0 | GCA1/IO49PDB1V0 |
| B42 | GCC0/IO34NDB1V0 | GCC0/IO47NDB1V0 |
| B43 | GCB2/IO33PSB1V0 | GBC2/IO42PSB1V0 |
| B44 | VCC | VCC |

| QN180 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS090 Function | AFS250 Function |
| B45 | GBA2/IO31PDB1V0 | GBA2/IO40PDB1V0 |
| B46 | GNDQ | GNDQ |
| B47 | GBA1/IO30RSB0V0 | GBA0/IO38RSB0V0 |
| B48 | GBB1/IO28RSB0V0 | GBC1/IO35RSB0V0 |
| B49 | VCC | VCC |
| B50 | GBC0/IO25RSB0V0 | IO31RSB0V0 |
| B51 | IO23RSB0V0 | IO28RSB0V0 |
| B52 | IO20RSB0V0 | IO25RSB0V0 |
| B53 | VCC | VCC |
| B54 | IO11RSB0V0 | IO14RSB0V0 |
| B55 | IO08RSB0V0 | IO11RSB0V0 |
| B56 | GAC1/IO05RSB0V0 | IO08RSB0V0 |
| B57 | VCCIB0 | VCCIB0 |
| B58 | GAB0/IO02RSB0V0 | GAC0/IO04RSB0V0 |
| B59 | GAA0/IO00RSB0V0 | GAA1/IO01RSB0V0 |
| B60 | VCCPLA | VCCPLA |
| C1 | NC | NC |
| C2 | NC | VCCIB3 |
| C3 | GND | GND |
| C4 | NC | GFC2/IO69PPB3V0 |
| C5 | GFC1/IO49PDB3V0 | GFC1/IO68PDB3V0 |
| C6 | GFA0/IO47NPB3V0 | GFB0/IO67NPB3V0 |
| C7 | VCCIB3 | NC |
| C8 | GND | GND |
| C9 | GEA1/IO44PDB3V0 | GFA1/IO66PDB3V0 |
| C10 | GEA2/IO42NDB3V0 | GEC2/IO60PDB3V0 |
| C11 | NC | GEA2/IO58PSB3V0 |
| C12 | NC | NC |
| C13 | GND | GND |
| C14 | NC | NC |
| C15 | NC | NC |
| C16 | GNDA | GNDA |
| C17 | NC | NC |
| C18 | NC | NC |
| C19 | NC | NC |
| C20 | NC | NC |

| QN180 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS090 Function | AFS250 Function |
| C21 | AG2 | AG2 |
| C22 | NC | NC |
| C23 | NC | NC |
| C24 | NC | NC |
| C25 | NC | AT5 |
| C26 | GND | GND |
| C27 | NC | NC |
| C28 | NC | NC |
| C29 | NC | NC |
| C30 | NC | NC |
| C31 | GND | GND |
| C32 | NC | NC |
| C33 | NC | NC |
| C34 | NC | NC |
| C35 | GND | GND |
| C36 | GDB0/IO39NPB1V0 | GDA0/IO54NPB1V0 |
| C37 | GDA1/IO37NSB1V0 | GDC0/IO52NSB1V0 |
| C38 | GCA0/IO36NDB1V0 | GCA0/IO49NDB1V0 |
| C39 | GCB1/IO35PPB1V0 | GCB1/IO48PPB1V0 |
| C40 | GND | GND |
| C41 | GCA2/IO32NPB1V0 | IO41NPB1V0 |
| C42 | GBB2/IO31NDB1V0 | IO40NDB1V0 |
| C43 | NC | NC |
| C44 | NC | GBA1/IO39RSB0V0 |
| C45 | NC | GBB0/IO36RSB0V0 |
| C46 | GND | GND |
| C47 | NC | IO30RSB0V0 |
| C48 | IO22RSB0V0 | IO27RSB0V0 |
| C49 | GND | GND |
| C50 | IO13RSB0V0 | IO16RSB0V0 |
| C51 | IO09RSB0V0 | IO12RSB0V0 |
| C52 | IO06RSB0V0 | IO09RSB0V0 |
| C53 | GND | GND |
| C54 | NC | GAB1/IO03RSB0V0 |
| C55 | NC | GAA0/IO00RSB0V0 |
| C56 | NC | NC |

| QN180 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS090 Function | AFS250 Function |
| D1 | NC | NC |
| D2 | NC | NC |
| D3 | NC | NC |
| D4 | NC | NC |

PQ208



Note

1. Package PQ208 is discontinued.
2. For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| PQ208 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS250 Function | AFS600 Function |
| 1 | VCCPLA | VCCPLA |
| 2 | VCOMPLA | VCOMPLA |
| 3 | GNDQ | GAA2/IO85PDB4V0 |
| 4 | VCCIB3 | IO85NDB4V0 |
| 5 | GAA2/IO76PDB3V0 | GAB2/IO84PDB4V0 |
| 6 | IO76NDB3V0 | IO84NDB4V0 |
| 7 | GAB2/IO75PDB3V0 | GAC2/IO83PDB4V0 |
| 8 | IO75NDB3V0 | IO83NDB4V0 |
| 9 | NC | IO77PDB4V0 |
| 10 | NC | IO77NDB4V0 |
| 11 | VCC | IO76PDB4V0 |
| 12 | GND | IO76NDB4V0 |
| 13 | VCCIB3 | VCC |
| 14 | IO72PDB3V0 | GND |
| 15 | IO72NDB3V0 | VCCIB4 |
| 16 | GFA2/IO71PDB3V0 | GFA2/IO75PDB4V0 |
| 17 | IO71NDB3V0 | IO75NDB4V0 |
| 18 | GFB2/IO70PDB3V0 | GFC2/IO73PDB4V0 |
| 19 | IO70NDB3V0 | IO73NDB4V0 |
| 20 | GFC2/IO69PDB3V0 | VCCOSC |
| 21 | IO69NDB3V0 | XTAL1 |
| 22 | VCC | XTAL2 |
| 23 | GND | GNDOSC |
| 24 | VCCIB3 | GFC1/IO72PDB4V0 |
| 25 | GFC1/IO68PDB3V0 | GFC0/IO72NDB4V0 |
| 26 | GFC0/IO68NDB3V0 | GFB1/IO71PDB4V0 |
| 27 | GFB1/IO67PDB3V0 | GFB0/IO71NDB4V0 |
| 28 | GFB0/IO67NDB3V0 | GFA1/IO70PDB4V0 |
| 29 | VCCOSC | GFA0/IO70NDB4V0 |
| 30 | XTAL1 | IO69PDB4V0 |
| 31 | XTAL2 | IO69NDB4V0 |
| 32 | GNDOSC | VCC |
| 33 | GEB1/IO62PDB3V0 | GND |
| 34 | GEB0/IO62NDB3V0 | VCCIB4 |
| 35 | GEA1/IO61PDB3V0 | GEC1/IO63PDB4V0 |
| 36 | GEA0/IO61NDB3V0 | GEC0/IO63NDB4V0 |
| 37 | GEC2/IO60PDB3V0 | GEB1/IO62PDB4V0 |

| PQ208 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS250 Function | AFS600 Function |
| 38 | IO60NDB3V0 | GEB0/IO62NDB4V0 |
| 39 | GND | GEB1/IO61PDB4V0 |
| 40 | VCCIB3 | GEB0/IO61NDB4V0 |
| 41 | GEB2/IO59PDB3V0 | GEC2/IO60PDB4V0 |
| 42 | IO59NDB3V0 | IO60NDB4V0 |
| 43 | GEB2/IO58PDB3V0 | VCCIB4 |
| 44 | IO58NDB3V0 | GNDQ |
| 45 | VCC | VCC |
| 46 | VCCNVM | VCCNVM |
| 47 | GNDNVM | GNDNVM |
| 48 | GND | GND |
| 49 | VCC15A | VCC15A |
| 50 | PCAP | PCAP |
| 51 | NCAP | NCAP |
| 52 | VCC33PMP | VCC33PMP |
| 53 | VCC33N | VCC33N |
| 54 | GND A | GND A |
| 55 | GND A Q | GND A Q |
| 56 | NC | AV0 |
| 57 | NC | AC0 |
| 58 | NC | AG0 |
| 59 | NC | AT0 |
| 60 | NC | ATR TN0 |
| 61 | NC | AT1 |
| 62 | NC | AG1 |
| 63 | NC | AC1 |
| 64 | NC | AV1 |
| 65 | AV0 | AV2 |
| 66 | AC0 | AC2 |
| 67 | AG0 | AG2 |
| 68 | AT0 | AT2 |
| 69 | ATR TN0 | ATR TN1 |
| 70 | AT1 | AT3 |
| 71 | AG1 | AG3 |
| 72 | AC1 | AC3 |
| 73 | AV1 | AV3 |

| PQ208 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS250 Function | AFS600 Function |
| 74 | AV2 | AV4 |
| 75 | AC2 | AC4 |
| 76 | AG2 | AG4 |
| 77 | AT2 | AT4 |
| 78 | ATR TN1 | ATR TN2 |
| 79 | AT3 | AT5 |
| 80 | AG3 | AG5 |
| 81 | AC3 | AC5 |
| 82 | AV3 | AV5 |
| 83 | AV4 | AV6 |
| 84 | AC4 | AC6 |
| 85 | AG4 | AG6 |
| 86 | AT4 | AT6 |
| 87 | ATR TN2 | ATR TN3 |
| 88 | AT5 | AT7 |
| 89 | AG5 | AG7 |
| 90 | AC5 | AC7 |
| 91 | AV5 | AV7 |
| 92 | NC | AV8 |
| 93 | NC | AC8 |
| 94 | NC | AG8 |
| 95 | NC | AT8 |
| 96 | NC | ATR TN4 |
| 97 | NC | AT9 |
| 98 | NC | AG9 |
| 99 | NC | AC9 |
| 100 | NC | AV9 |
| 101 | GND AQ | GND AQ |
| 102 | VCC33A | VCC33A |
| 103 | ADCGNDREF | ADCGNDREF |
| 104 | VAREF | VAREF |
| 105 | PUB | PUB |
| 106 | VCC33A | VCC33A |
| 107 | GND A | GND A |
| 108 | PTEM | PTEM |
| 109 | PTBASE | PTBASE |
| 110 | GND NVM | GND NVM |

| PQ208 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS250 Function | AFS600 Function |
| 111 | VCCNVM | VCCNVM |
| 112 | VCC | VCC |
| 112 | VCC | VCC |
| 113 | VPUMP | VPUMP |
| 114 | GND Q | NC |
| 115 | VCCIB1 | TCK |
| 116 | TCK | TDI |
| 117 | TDI | TMS |
| 118 | TMS | TDO |
| 119 | TDO | TRST |
| 120 | TRST | VJTAG |
| 121 | VJTAG | IO57NDB2V0 |
| 122 | IO57NDB1V0 | GDC2/IO57PDB2V0 |
| 123 | GDC2/IO57PDB1V0 | IO56NDB2V0 |
| 124 | IO56NDB1V0 | GDB2/IO56PDB2V0 |
| 125 | GDB2/IO56PDB1V0 | IO55NDB2V0 |
| 126 | VCCIB1 | GDA2/IO55PDB2V0 |
| 127 | GND | GDA0/IO54NDB2V0 |
| 128 | IO55NDB1V0 | GDA1/IO54PDB2V0 |
| 129 | GDA2/IO55PDB1V0 | VCCIB2 |
| 130 | GDA0/IO54NDB1V0 | GND |
| 131 | GDA1/IO54PDB1V0 | VCC |
| 132 | GDB0/IO53NDB1V0 | GCA0/IO45NDB2V0 |
| 133 | GDB1/IO53PDB1V0 | GCA1/IO45PDB2V0 |
| 134 | GDC0/IO52NDB1V0 | GCB0/IO44NDB2V0 |
| 135 | GDC1/IO52PDB1V0 | GCB1/IO44PDB2V0 |
| 136 | IO51NSB1V0 | GCC0/IO43NDB2V0 |
| 137 | VCCIB1 | GCC1/IO43PDB2V0 |
| 138 | GND | IO42NDB2V0 |
| 139 | VCC | IO42PDB2V0 |
| 140 | IO50NDB1V0 | IO41NDB2V0 |
| 141 | IO50PDB1V0 | GCC2/IO41PDB2V0 |
| 142 | GCA0/IO49NDB1V0 | VCCIB2 |
| 143 | GCA1/IO49PDB1V0 | GND |
| 144 | GCB0/IO48NDB1V0 | VCC |
| 145 | GCB1/IO48PDB1V0 | IO40NDB2V0 |
| 146 | GCC0/IO47NDB1V0 | GCB2/IO40PDB2V0 |

| PQ208 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS250 Function | AFS600 Function |
| 147 | GCC1/IO47PDB1V0 | IO39NDB2V0 |
| 148 | IO42NDB1V0 | GCA2/IO39PDB2V0 |
| 149 | GBC2/IO42PDB1V0 | IO31NDB2V0 |
| 150 | VCCIB1 | GBB2/IO31PDB2V0 |
| 151 | GND | IO30NDB2V0 |
| 152 | VCC | GBA2/IO30PDB2V0 |
| 153 | IO41NDB1V0 | VCCIB2 |
| 154 | GBB2/IO41PDB1V0 | GNDQ |
| 155 | IO40NDB1V0 | VCOMPLB |
| 156 | GBA2/IO40PDB1V0 | VCCPLB |
| 157 | GBA1/IO39RSB0V0 | VCCIB1 |
| 158 | GBA0/IO38RSB0V0 | GNDQ |
| 159 | GBB1/IO37RSB0V0 | GBB1/IO27PPB1V1 |
| 160 | GBB0/IO36RSB0V0 | GBA1/IO28PPB1V1 |
| 161 | GBC1/IO35RSB0V0 | GBB0/IO27NPB1V1 |
| 162 | VCCIB0 | GBA0/IO28NPB1V1 |
| 163 | GND | VCCIB1 |
| 164 | VCC | GND |
| 165 | GBC0/IO34RSB0V0 | VCC |
| 166 | IO33RSB0V0 | GBC1/IO26PDB1V1 |
| 167 | IO32RSB0V0 | GBC0/IO26NDB1V1 |
| 168 | IO31RSB0V0 | IO24PPB1V1 |
| 169 | IO30RSB0V0 | IO23PPB1V1 |
| 170 | IO29RSB0V0 | IO24NPB1V1 |
| 171 | IO28RSB0V0 | IO23NPB1V1 |
| 172 | IO27RSB0V0 | IO22PPB1V0 |
| 173 | IO26RSB0V0 | IO21PPB1V0 |
| 174 | IO25RSB0V0 | IO22NPB1V0 |
| 175 | VCCIB0 | IO21NPB1V0 |
| 176 | GND | IO20PSB1V0 |
| 177 | VCC | IO19PSB1V0 |
| 178 | IO24RSB0V0 | IO14NSB0V1 |
| 179 | IO23RSB0V0 | IO12PDB0V1 |
| 180 | IO22RSB0V0 | IO12NDB0V1 |
| 181 | IO21RSB0V0 | VCCIB0 |
| 182 | IO20RSB0V0 | GND |
| 183 | IO19RSB0V0 | VCC |

| PQ208 | | |
|------------|-----------------|-----------------|
| Pin Number | AFS250 Function | AFS600 Function |
| 184 | IO18RSB0V0 | IO10PPB0V1 |
| 185 | IO17RSB0V0 | IO09PPB0V1 |
| 186 | IO16RSB0V0 | IO10NPB0V1 |
| 187 | IO15RSB0V0 | IO09NPB0V1 |
| 188 | VCCIB0 | IO08PPB0V1 |
| 189 | GND | IO07PPB0V1 |
| 190 | VCC | IO08NPB0V1 |
| 191 | IO14RSB0V0 | IO07NPB0V1 |
| 192 | IO13RSB0V0 | IO06PPB0V0 |
| 193 | IO12RSB0V0 | IO05PPB0V0 |
| 194 | IO11RSB0V0 | IO06NPB0V0 |
| 195 | IO10RSB0V0 | IO04PPB0V0 |
| 196 | IO09RSB0V0 | IO05NPB0V0 |
| 197 | IO08RSB0V0 | IO04NPB0V0 |
| 198 | IO07RSB0V0 | GAC1/IO03PDB0V0 |
| 199 | IO06RSB0V0 | GAC0/IO03NDB0V0 |
| 200 | GAC1/IO05RSB0V0 | VCCIB0 |
| 201 | VCCIB0 | GND |
| 202 | GND | VCC |
| 203 | VCC | GAB1/IO02PDB0V0 |
| 204 | GAC0/IO04RSB0V0 | GAB0/IO02NDB0V0 |
| 205 | GAB1/IO03RSB0V0 | GAA1/IO01PDB0V0 |
| 206 | GAB0/IO02RSB0V0 | GAA0/IO01NDB0V0 |
| 207 | GAA1/IO01RSB0V0 | GNDQ |
| 208 | GAA0/IO00RSB0V0 | VCCIB0 |

FG256



Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| FG256 | | | | |
|------------|-----------------|-----------------|-----------------|------------------|
| Pin Number | AFS090 Function | AFS250 Function | AFS600 Function | AFS1500 Function |
| A1 | GND | GND | GND | GND |
| A2 | VCCIB0 | VCCIB0 | VCCIB0 | VCCIB0 |
| A3 | GAB0/IO02RSB0V0 | GAA0/IO00RSB0V0 | GAA0/IO01NDB0V0 | GAA0/IO01NDB0V0 |
| A4 | GAB1/IO03RSB0V0 | GAA1/IO01RSB0V0 | GAA1/IO01PDB0V0 | GAA1/IO01PDB0V0 |
| A5 | GND | GND | GND | GND |
| A6 | IO07RSB0V0 | IO11RSB0V0 | IO10PDB0V1 | IO07PDB0V1 |
| A7 | IO10RSB0V0 | IO14RSB0V0 | IO12PDB0V1 | IO13PDB0V2 |
| A8 | IO11RSB0V0 | IO15RSB0V0 | IO12NDB0V1 | IO13NDB0V2 |
| A9 | IO16RSB0V0 | IO24RSB0V0 | IO22NDB1V0 | IO24NDB1V0 |
| A10 | IO17RSB0V0 | IO25RSB0V0 | IO22PDB1V0 | IO24PDB1V0 |
| A11 | IO18RSB0V0 | IO26RSB0V0 | IO24NDB1V1 | IO29NDB1V1 |
| A12 | GND | GND | GND | GND |
| A13 | GBC0/IO25RSB0V0 | GBA0/IO38RSB0V0 | GBA0/IO28NDB1V1 | GBA0/IO42NDB1V2 |
| A14 | GBA0/IO29RSB0V0 | IO32RSB0V0 | IO29NDB1V1 | IO43NDB1V2 |
| A15 | VCCIB0 | VCCIB0 | VCCIB1 | VCCIB1 |
| A16 | GND | GND | GND | GND |
| B1 | VCOMPLA | VCOMPLA | VCOMPLA | VCOMPLA |
| B2 | VCCPLA | VCCPLA | VCCPLA | VCCPLA |
| B3 | GAA0/IO00RSB0V0 | IO07RSB0V0 | IO00NDB0V0 | IO00NDB0V0 |
| B4 | GAA1/IO01RSB0V0 | IO06RSB0V0 | IO00PDB0V0 | IO00PDB0V0 |
| B5 | NC | GAB1/IO03RSB0V0 | GAB1/IO02PPB0V0 | GAB1/IO02PPB0V0 |
| B6 | IO06RSB0V0 | IO10RSB0V0 | IO10NDB0V1 | IO07NDB0V1 |
| B7 | VCCIB0 | VCCIB0 | VCCIB0 | VCCIB0 |
| B8 | IO12RSB0V0 | IO16RSB0V0 | IO18NDB1V0 | IO22NDB1V0 |
| B9 | IO13RSB0V0 | IO17RSB0V0 | IO18PDB1V0 | IO22PDB1V0 |
| B10 | VCCIB0 | VCCIB0 | VCCIB1 | VCCIB1 |
| B11 | IO19RSB0V0 | IO27RSB0V0 | IO24PDB1V1 | IO29PDB1V1 |
| B12 | GBB0/IO27RSB0V0 | GBC0/IO34RSB0V0 | GBC0/IO26NPB1V1 | GBC0/IO40NPB1V2 |
| B13 | GBC1/IO26RSB0V0 | GBA1/IO39RSB0V0 | GBA1/IO28PDB1V1 | GBA1/IO42PDB1V2 |
| B14 | GBA1/IO30RSB0V0 | IO33RSB0V0 | IO29PDB1V1 | IO43PDB1V2 |
| B15 | NC | NC | VCCPLB | VCCPLB |
| B16 | NC | NC | VCOMPLB | VCOMPLB |
| C1 | VCCIB3 | VCCIB3 | VCCIB4 | VCCIB4 |
| C2 | GND | GND | GND | GND |
| C3 | VCCIB3 | VCCIB3 | VCCIB4 | VCCIB4 |
| C4 | NC | NC | VCCIB0 | VCCIB0 |
| C5 | VCCIB0 | VCCIB0 | VCCIB0 | VCCIB0 |
| C6 | GAC1/IO05RSB0V0 | GAC1/IO05RSB0V0 | GAC1/IO03PDB0V0 | GAC1/IO03PDB0V0 |

| FG256 | | | | |
|------------|-----------------|-----------------|-----------------|------------------|
| Pin Number | AFS090 Function | AFS250 Function | AFS600 Function | AFS1500 Function |
| C7 | IO09RSB0V0 | IO12RSB0V0 | IO06NDB0V0 | IO09NDB0V1 |
| C8 | IO14RSB0V0 | IO22RSB0V0 | IO16PDB1V0 | IO23PDB1V0 |
| C9 | IO15RSB0V0 | IO23RSB0V0 | IO16NDB1V0 | IO23NDB1V0 |
| C10 | IO22RSB0V0 | IO30RSB0V0 | IO25NDB1V1 | IO31NDB1V1 |
| C11 | IO20RSB0V0 | IO31RSB0V0 | IO25PDB1V1 | IO31PDB1V1 |
| C12 | VCCIB0 | VCCIB0 | VCCIB1 | VCCIB1 |
| C13 | GBB1/IO28RSB0V0 | GBC1/IO35RSB0V0 | GBC1/IO26PPB1V1 | GBC1/IO40PPB1V2 |
| C14 | VCCIB1 | VCCIB1 | VCCIB2 | VCCIB2 |
| C15 | GND | GND | GND | GND |
| C16 | VCCIB1 | VCCIB1 | VCCIB2 | VCCIB2 |
| D1 | GFC2/IO50NPB3V0 | IO75NDB3V0 | IO84NDB4V0 | IO124NDB4V0 |
| D2 | GFA2/IO51NDB3V0 | GAB2/IO75PDB3V0 | GAB2/IO84PDB4V0 | GAB2/IO124PDB4V0 |
| D3 | GAC2/IO51PDB3V0 | IO76NDB3V0 | IO85NDB4V0 | IO125NDB4V0 |
| D4 | GAA2/IO52PDB3V0 | GAA2/IO76PDB3V0 | GAA2/IO85PDB4V0 | GAA2/IO125PDB4V0 |
| D5 | GAB2/IO52NDB3V0 | GAB0/IO02RSB0V0 | GAB0/IO02NPB0V0 | GAB0/IO02NPB0V0 |
| D6 | GAC0/IO04RSB0V0 | GAC0/IO04RSB0V0 | GAC0/IO03NDB0V0 | GAC0/IO03NDB0V0 |
| D7 | IO08RSB0V0 | IO13RSB0V0 | IO06PDB0V0 | IO09PDB0V1 |
| D8 | NC | IO20RSB0V0 | IO14NDB0V1 | IO15NDB0V2 |
| D9 | NC | IO21RSB0V0 | IO14PDB0V1 | IO15PDB0V2 |
| D10 | IO21RSB0V0 | IO28RSB0V0 | IO23PDB1V1 | IO37PDB1V2 |
| D11 | IO23RSB0V0 | GBB0/IO36RSB0V0 | GBB0/IO27NDB1V1 | GBB0/IO41NDB1V2 |
| D12 | NC | NC | VCCIB1 | VCCIB1 |
| D13 | GBA2/IO31PDB1V0 | GBA2/IO40PDB1V0 | GBA2/IO30PDB2V0 | GBA2/IO44PDB2V0 |
| D14 | GBB2/IO31NDB1V0 | IO40NDB1V0 | IO30NDB2V0 | IO44NDB2V0 |
| D15 | GBC2/IO32PDB1V0 | GBB2/IO41PDB1V0 | GBB2/IO31PDB2V0 | GBB2/IO45PDB2V0 |
| D16 | GCA2/IO32NDB1V0 | IO41NDB1V0 | IO31NDB2V0 | IO45NDB2V0 |
| E1 | GND | GND | GND | GND |
| E2 | GFB0/IO48NPB3V0 | IO73NDB3V0 | IO81NDB4V0 | IO118NDB4V0 |
| E3 | GFB2/IO50PPB3V0 | IO73PDB3V0 | IO81PDB4V0 | IO118PDB4V0 |
| E4 | VCCIB3 | VCCIB3 | VCCIB4 | VCCIB4 |
| E5 | NC | IO74NPB3V0 | IO83NPB4V0 | IO123NPB4V0 |
| E6 | NC | IO08RSB0V0 | IO04NPB0V0 | IO05NPB0V1 |
| E7 | GND | GND | GND | GND |
| E8 | NC | IO18RSB0V0 | IO08PDB0V1 | IO11PDB0V1 |
| E9 | NC | NC | IO20NDB1V0 | IO27NDB1V1 |
| E10 | GND | GND | GND | GND |
| E11 | IO24RSB0V0 | GBB1/IO37RSB0V0 | GBB1/IO27PDB1V1 | GBB1/IO41PDB1V2 |
| E12 | NC | IO50PPB1V0 | IO33PSB2V0 | IO48PSB2V0 |

| FG256 | | | | |
|------------|-----------------|-----------------|-----------------|------------------|
| Pin Number | AFS090 Function | AFS250 Function | AFS600 Function | AFS1500 Function |
| E13 | VCCIB1 | VCCIB1 | VCCIB2 | VCCIB2 |
| E14 | GCC2/IO33NDB1V0 | IO42NDB1V0 | IO32NDB2V0 | IO46NDB2V0 |
| E15 | GCB2/IO33PDB1V0 | GBC2/IO42PDB1V0 | GBC2/IO32PDB2V0 | GBC2/IO46PDB2V0 |
| E16 | GND | GND | GND | GND |
| F1 | NC | NC | IO79NDB4V0 | IO111NDB4V0 |
| F2 | NC | NC | IO79PDB4V0 | IO111PDB4V0 |
| F3 | GFB1/IO48PPB3V0 | IO72NDB3V0 | IO76NDB4V0 | IO112NDB4V0 |
| F4 | GFC0/IO49NDB3V0 | IO72PDB3V0 | IO76PDB4V0 | IO112PDB4V0 |
| F5 | NC | NC | IO82PSB4V0 | IO120PSB4V0 |
| F6 | GFC1/IO49PDB3V0 | GAC2/IO74PPB3V0 | GAC2/IO83PPB4V0 | GAC2/IO123PPB4V0 |
| F7 | NC | IO09RSB0V0 | IO04PPB0V0 | IO05PPB0V1 |
| F8 | NC | IO19RSB0V0 | IO08NDB0V1 | IO11NDB0V1 |
| F9 | NC | NC | IO20PDB1V0 | IO27PDB1V1 |
| F10 | NC | IO29RSB0V0 | IO23NDB1V1 | IO37NDB1V2 |
| F11 | NC | IO43NDB1V0 | IO36NDB2V0 | IO50NDB2V0 |
| F12 | NC | IO43PDB1V0 | IO36PDB2V0 | IO50PDB2V0 |
| F13 | NC | IO44NDB1V0 | IO39NDB2V0 | IO59NDB2V0 |
| F14 | NC | GCA2/IO44PDB1V0 | GCA2/IO39PDB2V0 | GCA2/IO59PDB2V0 |
| F15 | GCC1/IO34PDB1V0 | GCB2/IO45PDB1V0 | GCB2/IO40PDB2V0 | GCB2/IO60PDB2V0 |
| F16 | GCC0/IO34NDB1V0 | IO45NDB1V0 | IO40NDB2V0 | IO60NDB2V0 |
| G1 | GEC0/IO46NPB3V0 | IO70NPB3V0 | IO74NPB4V0 | IO109NPB4V0 |
| G2 | VCCIB3 | VCCIB3 | VCCIB4 | VCCIB4 |
| G3 | GEC1/IO46PPB3V0 | GFB2/IO70PPB3V0 | GFB2/IO74PPB4V0 | GFB2/IO109PPB4V0 |
| G4 | GFA1/IO47PDB3V0 | GFA2/IO71PDB3V0 | GFA2/IO75PDB4V0 | GFA2/IO110PDB4V0 |
| G5 | GND | GND | GND | GND |
| G6 | GFA0/IO47NDB3V0 | IO71NDB3V0 | IO75NDB4V0 | IO110NDB4V0 |
| G7 | GND | GND | GND | GND |
| G8 | VCC | VCC | VCC | VCC |
| G9 | GND | GND | GND | GND |
| G10 | VCC | VCC | VCC | VCC |
| G11 | GDA1/IO37NDB1V0 | GCC0/IO47NDB1V0 | GCC0/IO43NDB2V0 | GCC0/IO62NDB2V0 |
| G12 | GND | GND | GND | GND |
| G13 | IO37PDB1V0 | GCC1/IO47PDB1V0 | GCC1/IO43PDB2V0 | GCC1/IO62PDB2V0 |
| G14 | GCB0/IO35NPB1V0 | IO46NPB1V0 | IO41NPB2V0 | IO61NPB2V0 |
| G15 | VCCIB1 | VCCIB1 | VCCIB2 | VCCIB2 |
| G16 | GCB1/IO35PPB1V0 | GCC2/IO46PPB1V0 | GCC2/IO41PPB2V0 | GCC2/IO61PPB2V0 |
| H1 | GEB1/IO45PDB3V0 | GFC2/IO69PDB3V0 | GFC2/IO73PDB4V0 | GFC2/IO108PDB4V0 |
| H2 | GEB0/IO45NDB3V0 | IO69NDB3V0 | IO73NDB4V0 | IO108NDB4V0 |

| FG256 | | | | |
|------------|-----------------|-----------------|-----------------|------------------|
| Pin Number | AFS090 Function | AFS250 Function | AFS600 Function | AFS1500 Function |
| H3 | XTAL2 | XTAL2 | XTAL2 | XTAL2 |
| H4 | XTAL1 | XTAL1 | XTAL1 | XTAL1 |
| H5 | GNDOSC | GNDOSC | GNDOSC | GNDOSC |
| H6 | VCCOSC | VCCOSC | VCCOSC | VCCOSC |
| H7 | VCC | VCC | VCC | VCC |
| H8 | GND | GND | GND | GND |
| H9 | VCC | VCC | VCC | VCC |
| H10 | GND | GND | GND | GND |
| H11 | GDC0/IO38NDB1V0 | IO51NDB1V0 | IO47NDB2V0 | IO69NDB2V0 |
| H12 | GDC1/IO38PDB1V0 | IO51PDB1V0 | IO47PDB2V0 | IO69PDB2V0 |
| H13 | GDB1/IO39PDB1V0 | GCA1/IO49PDB1V0 | GCA1/IO45PDB2V0 | GCA1/IO64PDB2V0 |
| H14 | GDB0/IO39NDB1V0 | GCA0/IO49NDB1V0 | GCA0/IO45NDB2V0 | GCA0/IO64NDB2V0 |
| H15 | GCA0/IO36NDB1V0 | GCB0/IO48NDB1V0 | GCB0/IO44NDB2V0 | GCB0/IO63NDB2V0 |
| H16 | GCA1/IO36PDB1V0 | GCB1/IO48PDB1V0 | GCB1/IO44PDB2V0 | GCB1/IO63PDB2V0 |
| J1 | GEA0/IO44NDB3V0 | GFA0/IO66NDB3V0 | GFA0/IO70NDB4V0 | GFA0/IO105NDB4V0 |
| J2 | GEA1/IO44PDB3V0 | GFA1/IO66PDB3V0 | GFA1/IO70PDB4V0 | GFA1/IO105PDB4V0 |
| J3 | IO43NDB3V0 | GFB0/IO67NDB3V0 | GFB0/IO71NDB4V0 | GFB0/IO106NDB4V0 |
| J4 | GEC2/IO43PDB3V0 | GFB1/IO67PDB3V0 | GFB1/IO71PDB4V0 | GFB1/IO106PDB4V0 |
| J5 | NC | GFC0/IO68NDB3V0 | GFC0/IO72NDB4V0 | GFC0/IO107NDB4V0 |
| J6 | NC | GFC1/IO68PDB3V0 | GFC1/IO72PDB4V0 | GFC1/IO107PDB4V0 |
| J7 | GND | GND | GND | GND |
| J8 | VCC | VCC | VCC | VCC |
| J9 | GND | GND | GND | GND |
| J10 | VCC | VCC | VCC | VCC |
| J11 | GDC2/IO41NPB1V0 | IO56NPB1V0 | IO56NPB2V0 | IO83NPB2V0 |
| J12 | NC | GDB0/IO53NPB1V0 | GDB0/IO53NPB2V0 | GDB0/IO80NPB2V0 |
| J13 | NC | GDA1/IO54PDB1V0 | GDA1/IO54PDB2V0 | GDA1/IO81PDB2V0 |
| J14 | GDA0/IO40PDB1V0 | GDC1/IO52PPB1V0 | GDC1/IO52PPB2V0 | GDC1/IO79PPB2V0 |
| J15 | NC | IO50NPB1V0 | IO51NSB2V0 | IO77NSB2V0 |
| J16 | GDA2/IO40NDB1V0 | GDC0/IO52NPB1V0 | GDC0/IO52NPB2V0 | GDC0/IO79NPB2V0 |
| K1 | NC | IO65NPB3V0 | IO67NPB4V0 | IO92NPB4V0 |
| K2 | VCCIB3 | VCCIB3 | VCCIB4 | VCCIB4 |
| K3 | NC | IO65PPB3V0 | IO67PPB4V0 | IO92PPB4V0 |
| K4 | NC | IO64PDB3V0 | IO65PDB4V0 | IO96PDB4V0 |
| K5 | GND | GND | GND | GND |
| K6 | NC | IO64NDB3V0 | IO65NDB4V0 | IO96NDB4V0 |
| K7 | VCC | VCC | VCC | VCC |
| K8 | GND | GND | GND | GND |

| FG256 | | | | |
|------------|-----------------|-----------------|-----------------|------------------|
| Pin Number | AFS090 Function | AFS250 Function | AFS600 Function | AFS1500 Function |
| K9 | VCC | VCC | VCC | VCC |
| K10 | GND | GND | GND | GND |
| K11 | NC | GDC2/IO57PPB1V0 | GDC2/IO57PPB2V0 | GDC2/IO84PPB2V0 |
| K12 | GND | GND | GND | GND |
| K13 | NC | GDA0/IO54NDB1V0 | GDA0/IO54NDB2V0 | GDA0/IO81NDB2V0 |
| K14 | NC | GDA2/IO55PPB1V0 | GDA2/IO55PPB2V0 | GDA2/IO82PPB2V0 |
| K15 | VCCIB1 | VCCIB1 | VCCIB2 | VCCIB2 |
| K16 | NC | GDB1/IO53PPB1V0 | GDB1/IO53PPB2V0 | GDB1/IO80PPB2V0 |
| L1 | NC | GEC1/IO63PDB3V0 | GEC1/IO63PDB4V0 | GEC1/IO90PDB4V0 |
| L2 | NC | GEC0/IO63NDB3V0 | GEC0/IO63NDB4V0 | GEC0/IO90NDB4V0 |
| L3 | NC | GEB1/IO62PDB3V0 | GEB1/IO62PDB4V0 | GEB1/IO89PDB4V0 |
| L4 | NC | GEB0/IO62NDB3V0 | GEB0/IO62NDB4V0 | GEB0/IO89NDB4V0 |
| L5 | NC | IO60NDB3V0 | IO60NDB4V0 | IO87NDB4V0 |
| L6 | NC | GEC2/IO60PDB3V0 | GEC2/IO60PDB4V0 | GEC2/IO87PDB4V0 |
| L7 | GNDA | GNDA | GNDA | GNDA |
| L8 | AC0 | AC0 | AC2 | AC2 |
| L9 | AV2 | AV2 | AV4 | AV4 |
| L10 | AC3 | AC3 | AC5 | AC5 |
| L11 | PTEM | PTEM | PTEM | PTEM |
| L12 | TDO | TDO | TDO | TDO |
| L13 | VJTAG | VJTAG | VJTAG | VJTAG |
| L14 | NC | IO57NPB1V0 | IO57NPB2V0 | IO84NPB2V0 |
| L15 | GDB2/IO41PPB1V0 | GDB2/IO56PPB1V0 | GDB2/IO56PPB2V0 | GDB2/IO83PPB2V0 |
| L16 | NC | IO55NPB1V0 | IO55NPB2V0 | IO82NPB2V0 |
| M1 | GND | GND | GND | GND |
| M2 | NC | GEA1/IO61PDB3V0 | GEA1/IO61PDB4V0 | GEA1/IO88PDB4V0 |
| M3 | NC | GEA0/IO61NDB3V0 | GEA0/IO61NDB4V0 | GEA0/IO88NDB4V0 |
| M4 | VCCIB3 | VCCIB3 | VCCIB4 | VCCIB4 |
| M5 | NC | IO58NPB3V0 | IO58NPB4V0 | IO85NPB4V0 |
| M6 | NC | NC | AV0 | AV0 |
| M7 | NC | NC | AC1 | AC1 |
| M8 | AG1 | AG1 | AG3 | AG3 |
| M9 | AC2 | AC2 | AC4 | AC4 |
| M10 | AC4 | AC4 | AC6 | AC6 |
| M11 | NC | AG5 | AG7 | AG7 |
| M12 | VPUMP | VPUMP | VPUMP | VPUMP |
| M13 | VCCIB1 | VCCIB1 | VCCIB2 | VCCIB2 |
| M14 | TMS | TMS | TMS | TMS |

| FG256 | | | | |
|------------|-----------------|-----------------|-----------------|------------------|
| Pin Number | AFS090 Function | AFS250 Function | AFS600 Function | AFS1500 Function |
| M15 | TRST | TRST | TRST | TRST |
| M16 | GND | GND | GND | GND |
| N1 | GEB2/IO42PDB3V0 | GEB2/IO59PDB3V0 | GEB2/IO59PDB4V0 | GEB2/IO86PDB4V0 |
| N2 | GEA2/IO42NDB3V0 | IO59NDB3V0 | IO59NDB4V0 | IO86NDB4V0 |
| N3 | NC | GEA2/IO58PPB3V0 | GEA2/IO58PPB4V0 | GEA2/IO85PPB4V0 |
| N4 | VCC33PMP | VCC33PMP | VCC33PMP | VCC33PMP |
| N5 | VCC15A | VCC15A | VCC15A | VCC15A |
| N6 | NC | NC | AG0 | AG0 |
| N7 | AC1 | AC1 | AC3 | AC3 |
| N8 | AG3 | AG3 | AG5 | AG5 |
| N9 | AV3 | AV3 | AV5 | AV5 |
| N10 | AG4 | AG4 | AG6 | AG6 |
| N11 | NC | NC | AC8 | AC8 |
| N12 | GND A | GND A | GND A | GND A |
| N13 | VCC33A | VCC33A | VCC33A | VCC33A |
| N14 | VCCNVM | VCCNVM | VCCNVM | VCCNVM |
| N15 | TCK | TCK | TCK | TCK |
| N16 | TDI | TDI | TDI | TDI |
| P1 | VCCNVM | VCCNVM | VCCNVM | VCCNVM |
| P2 | GNDNVM | GNDNVM | GNDNVM | GNDNVM |
| P3 | GND A | GND A | GND A | GND A |
| P4 | NC | NC | AC0 | AC0 |
| P5 | NC | NC | AG1 | AG1 |
| P6 | NC | NC | AV1 | AV1 |
| P7 | AG0 | AG0 | AG2 | AG2 |
| P8 | AG2 | AG2 | AG4 | AG4 |
| P9 | GND A | GND A | GND A | GND A |
| P10 | NC | AC5 | AC7 | AC7 |
| P11 | NC | NC | AV8 | AV8 |
| P12 | NC | NC | AG8 | AG8 |
| P13 | NC | NC | AV9 | AV9 |
| P14 | ADCGNDREF | ADCGNDREF | ADCGNDREF | ADCGNDREF |
| P15 | PTBASE | PTBASE | PTBASE | PTBASE |
| P16 | GNDNVM | GNDNVM | GNDNVM | GNDNVM |
| R1 | VCCIB3 | VCCIB3 | VCCIB4 | VCCIB4 |
| R2 | PCAP | PCAP | PCAP | PCAP |
| R3 | NC | NC | AT1 | AT1 |
| R4 | NC | NC | AT0 | AT0 |

| FG256 | | | | |
|------------|-----------------|-----------------|-----------------|------------------|
| Pin Number | AFS090 Function | AFS250 Function | AFS600 Function | AFS1500 Function |
| R5 | AV0 | AV0 | AV2 | AV2 |
| R6 | AT0 | AT0 | AT2 | AT2 |
| R7 | AV1 | AV1 | AV3 | AV3 |
| R8 | AT3 | AT3 | AT5 | AT5 |
| R9 | AV4 | AV4 | AV6 | AV6 |
| R10 | NC | AT5 | AT7 | AT7 |
| R11 | NC | AV5 | AV7 | AV7 |
| R12 | NC | NC | AT9 | AT9 |
| R13 | NC | NC | AG9 | AG9 |
| R14 | NC | NC | AC9 | AC9 |
| R15 | PUB | PUB | PUB | PUB |
| R16 | VCCIB1 | VCCIB1 | VCCIB2 | VCCIB2 |
| T1 | GND | GND | GND | GND |
| T2 | NCAP | NCAP | NCAP | NCAP |
| T3 | VCC33N | VCC33N | VCC33N | VCC33N |
| T4 | NC | NC | ATR TN0 | ATR TN0 |
| T5 | AT1 | AT1 | AT3 | AT3 |
| T6 | ATR TN0 | ATR TN0 | ATR TN1 | ATR TN1 |
| T7 | AT2 | AT2 | AT4 | AT4 |
| T8 | ATR TN1 | ATR TN1 | ATR TN2 | ATR TN2 |
| T9 | AT4 | AT4 | AT6 | AT6 |
| T10 | ATR TN2 | ATR TN2 | ATR TN3 | ATR TN3 |
| T11 | NC | NC | AT8 | AT8 |
| T12 | NC | NC | ATR TN4 | ATR TN4 |
| T13 | GND A | GND A | GND A | GND A |
| T14 | VCC33A | VCC33A | VCC33A | VCC33A |
| T15 | VAREF | VAREF | VAREF | VAREF |
| T16 | GND | GND | GND | GND |

FG484



Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| A1 | GND | GND |
| A2 | VCC | NC |
| A3 | GAA1/IO01PDB0V0 | GAA1/IO01PDB0V0 |
| A4 | GAB0/IO02NDB0V0 | GAB0/IO02NDB0V0 |
| A5 | GAB1/IO02PDB0V0 | GAB1/IO02PDB0V0 |
| A6 | IO07NDB0V1 | IO07NDB0V1 |
| A7 | IO07PDB0V1 | IO07PDB0V1 |
| A8 | IO10PDB0V1 | IO09PDB0V1 |
| A9 | IO14NDB0V1 | IO13NDB0V2 |
| A10 | IO14PDB0V1 | IO13PDB0V2 |
| A11 | IO17PDB1V0 | IO24PDB1V0 |
| A12 | IO18PDB1V0 | IO26PDB1V0 |
| A13 | IO19NDB1V0 | IO27NDB1V1 |
| A14 | IO19PDB1V0 | IO27PDB1V1 |
| A15 | IO24NDB1V1 | IO35NDB1V2 |
| A16 | IO24PDB1V1 | IO35PDB1V2 |
| A17 | GBC0/IO26NDB1V1 | GBC0/IO40NDB1V2 |
| A18 | GBA0/IO28NDB1V1 | GBA0/IO42NDB1V2 |
| A19 | IO29NDB1V1 | IO43NDB1V2 |
| A20 | IO29PDB1V1 | IO43PDB1V2 |
| A21 | VCC | NC |
| A22 | GND | GND |
| AA1 | VCC | NC |
| AA2 | GND | GND |
| AA3 | VCCIB4 | VCCIB4 |
| AA4 | VCCIB4 | VCCIB4 |
| AA5 | PCAP | PCAP |
| AA6 | AG0 | AG0 |
| AA7 | GNDA | GNDA |
| AA8 | AG1 | AG1 |
| AA9 | AG2 | AG2 |
| AA10 | GNDA | GNDA |
| AA11 | AG3 | AG3 |
| AA12 | AG6 | AG6 |
| AA13 | GNDA | GNDA |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| AA14 | AG7 | AG7 |
| AA15 | AG8 | AG8 |
| AA16 | GNDA | GNDA |
| AA17 | AG9 | AG9 |
| AA18 | VAREF | VAREF |
| AA19 | VCCIB2 | VCCIB2 |
| AA20 | PTEM | PTEM |
| AA21 | GND | GND |
| AA22 | VCC | NC |
| AB1 | GND | GND |
| AB2 | VCC | NC |
| AB3 | NC | IO94NSB4V0 |
| AB4 | GND | GND |
| AB5 | VCC33N | VCC33N |
| AB6 | AT0 | AT0 |
| AB7 | ATR TN0 | ATR TN0 |
| AB8 | AT1 | AT1 |
| AB9 | AT2 | AT2 |
| AB10 | ATR TN1 | ATR TN1 |
| AB11 | AT3 | AT3 |
| AB12 | AT6 | AT6 |
| AB13 | ATR TN3 | ATR TN3 |
| AB14 | AT7 | AT7 |
| AB15 | AT8 | AT8 |
| AB16 | ATR TN4 | ATR TN4 |
| AB17 | AT9 | AT9 |
| AB18 | VCC33A | VCC33A |
| AB19 | GND | GND |
| AB20 | NC | IO76NPB2V0 |
| AB21 | VCC | NC |
| AB22 | GND | GND |
| B1 | VCC | NC |
| B2 | GND | GND |
| B3 | GAA0/IO01NDB0V0 | GAA0/IO01NDB0V0 |
| B4 | GND | GND |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| B5 | IO05NDB0V0 | IO04NDB0V0 |
| B6 | IO05PDB0V0 | IO04PDB0V0 |
| B7 | GND | GND |
| B8 | IO10NDB0V1 | IO09NDB0V1 |
| B9 | IO13PDB0V1 | IO11PDB0V1 |
| B10 | GND | GND |
| B11 | IO17NDB1V0 | IO24NDB1V0 |
| B12 | IO18NDB1V0 | IO26NDB1V0 |
| B13 | GND | GND |
| B14 | IO21NDB1V0 | IO31NDB1V1 |
| B15 | IO21PDB1V0 | IO31PDB1V1 |
| B16 | GND | GND |
| B17 | GBC1/IO26PDB1V1 | GBC1/IO40PDB1V2 |
| B18 | GBA1/IO28PDB1V1 | GBA1/IO42PDB1V2 |
| B19 | GND | GND |
| B20 | VCCPLB | VCCPLB |
| B21 | GND | GND |
| B22 | VCC | NC |
| C1 | IO82PDB4V0 | IO121PDB4V0 |
| C2 | NC | IO122PSB4V0 |
| C3 | IO00NDB0V0 | IO00NDB0V0 |
| C4 | IO00PDB0V0 | IO00PDB0V0 |
| C5 | VCCIB0 | VCCIB0 |
| C6 | IO06NDB0V0 | IO05NDB0V1 |
| C7 | IO06PDB0V0 | IO05PDB0V1 |
| C8 | VCCIB0 | VCCIB0 |
| C9 | IO13NDB0V1 | IO11NDB0V1 |
| C10 | IO11PDB0V1 | IO14PDB0V2 |
| C11 | VCCIB0 | VCCIB0 |
| C12 | VCCIB1 | VCCIB1 |
| C13 | IO20NDB1V0 | IO29NDB1V1 |
| C14 | IO20PDB1V0 | IO29PDB1V1 |
| C15 | VCCIB1 | VCCIB1 |
| C16 | IO25NDB1V1 | IO37NDB1V2 |
| C17 | GBB0/IO27NDB1V1 | GBB0/IO41NDB1V2 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| C18 | VCCIB1 | VCCIB1 |
| C19 | VCOMPLB | VCOMPLB |
| C20 | GBA2/IO30PDB2V0 | GBA2/IO44PDB2V0 |
| C21 | NC | IO48PSB2V0 |
| C22 | GBB2/IO31PDB2V0 | GBB2/IO45PDB2V0 |
| D1 | IO82NDB4V0 | IO121NDB4V0 |
| D2 | GND | GND |
| D3 | IO83NDB4V0 | IO123NDB4V0 |
| D4 | GAC2/IO83PDB4V0 | GAC2/IO123PDB4V0 |
| D5 | GAA2/IO85PDB4V0 | GAA2/IO125PDB4V0 |
| D6 | GAC0/IO03NDB0V0 | GAC0/IO03NDB0V0 |
| D7 | GAC1/IO03PDB0V0 | GAC1/IO03PDB0V0 |
| D8 | IO09NDB0V1 | IO10NDB0V1 |
| D9 | IO09PDB0V1 | IO10PDB0V1 |
| D10 | IO11NDB0V1 | IO14NDB0V2 |
| D11 | IO16NDB1V0 | IO23NDB1V0 |
| D12 | IO16PDB1V0 | IO23PDB1V0 |
| D13 | NC | IO32NPB1V1 |
| D14 | IO23NDB1V1 | IO34NDB1V1 |
| D15 | IO23PDB1V1 | IO34PDB1V1 |
| D16 | IO25PDB1V1 | IO37PDB1V2 |
| D17 | GBB1/IO27PDB1V1 | GBB1/IO41PDB1V2 |
| D18 | VCCIB2 | VCCIB2 |
| D19 | NC | IO47PPB2V0 |
| D20 | IO30NDB2V0 | IO44NDB2V0 |
| D21 | GND | GND |
| D22 | IO31NDB2V0 | IO45NDB2V0 |
| E1 | IO81NDB4V0 | IO120NDB4V0 |
| E2 | IO81PDB4V0 | IO120PDB4V0 |
| E3 | VCCIB4 | VCCIB4 |
| E4 | GAB2/IO84PDB4V0 | GAB2/IO124PDB4V0 |
| E5 | IO85NDB4V0 | IO125NDB4V0 |
| E6 | GND | GND |
| E7 | VCCIB0 | VCCIB0 |
| E8 | NC | IO08NDB0V1 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| E9 | NC | IO08PDB0V1 |
| E10 | GND | GND |
| E11 | IO15NDB1V0 | IO22NDB1V0 |
| E12 | IO15PDB1V0 | IO22PDB1V0 |
| E13 | GND | GND |
| E14 | NC | IO32PPB1V1 |
| E15 | NC | IO36NPB1V2 |
| E16 | VCCIB1 | VCCIB1 |
| E17 | GND | GND |
| E18 | NC | IO47NPB2V0 |
| E19 | IO33PDB2V0 | IO49PDB2V0 |
| E20 | VCCIB2 | VCCIB2 |
| E21 | IO32NDB2V0 | IO46NDB2V0 |
| E22 | GBC2/IO32PDB2V0 | GBC2/IO46PDB2V0 |
| F1 | IO80NDB4V0 | IO118NDB4V0 |
| F2 | IO80PDB4V0 | IO118PDB4V0 |
| F3 | NC | IO119NSB4V0 |
| F4 | IO84NDB4V0 | IO124NDB4V0 |
| F5 | GND | GND |
| F6 | VCOMPLA | VCOMPLA |
| F7 | VCCPLA | VCCPLA |
| F8 | VCCIB0 | VCCIB0 |
| F9 | IO08NDB0V1 | IO12NDB0V1 |
| F10 | IO08PDB0V1 | IO12PDB0V1 |
| F11 | VCCIB0 | VCCIB0 |
| F12 | VCCIB1 | VCCIB1 |
| F13 | IO22NDB1V0 | IO30NDB1V1 |
| F14 | IO22PDB1V0 | IO30PDB1V1 |
| F15 | VCCIB1 | VCCIB1 |
| F16 | NC | IO36PPB1V2 |
| F17 | NC | IO38NPB1V2 |
| F18 | GND | GND |
| F19 | IO33NDB2V0 | IO49NDB2V0 |
| F20 | IO34PDB2V0 | IO50PDB2V0 |
| F21 | IO34NDB2V0 | IO50NDB2V0 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| F22 | IO35PDB2V0 | IO51PDB2V0 |
| G1 | IO77PDB4V0 | IO115PDB4V0 |
| G2 | GND | GND |
| G3 | IO78NDB4V0 | IO116NDB4V0 |
| G4 | IO78PDB4V0 | IO116PDB4V0 |
| G5 | VCCIB4 | VCCIB4 |
| G6 | NC | IO117PDB4V0 |
| G7 | VCCIB4 | VCCIB4 |
| G8 | GND | GND |
| G9 | IO04NDB0V0 | IO06NDB0V1 |
| G10 | IO04PDB0V0 | IO06PDB0V1 |
| G11 | IO12NDB0V1 | IO16NDB0V2 |
| G12 | IO12PDB0V1 | IO16PDB0V2 |
| G13 | NC | IO28NDB1V1 |
| G14 | NC | IO28PDB1V1 |
| G15 | GND | GND |
| G16 | NC | IO38PPB1V2 |
| G17 | NC | IO53PDB2V0 |
| G18 | VCCIB2 | VCCIB2 |
| G19 | IO36PDB2V0 | IO52PDB2V0 |
| G20 | IO36NDB2V0 | IO52NDB2V0 |
| G21 | GND | GND |
| G22 | IO35NDB2V0 | IO51NDB2V0 |
| H1 | IO77NDB4V0 | IO115NDB4V0 |
| H2 | IO76PDB4V0 | IO113PDB4V0 |
| H3 | VCCIB4 | VCCIB4 |
| H4 | IO79NDB4V0 | IO114NDB4V0 |
| H5 | IO79PDB4V0 | IO114PDB4V0 |
| H6 | NC | IO117NDB4V0 |
| H7 | GND | GND |
| H8 | VCC | VCC |
| H9 | VCCIB0 | VCCIB0 |
| H10 | GND | GND |
| H11 | VCCIB0 | VCCIB0 |
| H12 | VCCIB1 | VCCIB1 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| H13 | GND | GND |
| H14 | VCCIB1 | VCCIB1 |
| H15 | GND | GND |
| H16 | GND | GND |
| H17 | NC | IO53NDB2V0 |
| H18 | IO38PDB2V0 | IO57PDB2V0 |
| H19 | GCA2/IO39PDB2V0 | GCA2/IO59PDB2V0 |
| H20 | VCCIB2 | VCCIB2 |
| H21 | IO37NDB2V0 | IO54NDB2V0 |
| H22 | IO37PDB2V0 | IO54PDB2V0 |
| J1 | NC | IO112PPB4V0 |
| J2 | IO76NDB4V0 | IO113NDB4V0 |
| J3 | GFB2/IO74PDB4V0 | GFB2/IO109PDB4V0 |
| J4 | GFA2/IO75PDB4V0 | GFA2/IO110PDB4V0 |
| J5 | NC | IO112NPB4V0 |
| J6 | NC | IO104PDB4V0 |
| J7 | NC | IO111PDB4V0 |
| J8 | VCCIB4 | VCCIB4 |
| J9 | GND | GND |
| J10 | VCC | VCC |
| J11 | GND | GND |
| J12 | VCC | VCC |
| J13 | GND | GND |
| J14 | VCC | VCC |
| J15 | VCCIB2 | VCCIB2 |
| J16 | GCB2/IO40PDB2V0 | GCB2/IO60PDB2V0 |
| J17 | NC | IO58NDB2V0 |
| J18 | IO38NDB2V0 | IO57NDB2V0 |
| J19 | IO39NDB2V0 | IO59NDB2V0 |
| J20 | GCC2/IO41PDB2V0 | GCC2/IO61PDB2V0 |
| J21 | NC | IO55PSB2V0 |
| J22 | IO42PDB2V0 | IO56PDB2V0 |
| K1 | GFC2/IO73PDB4V0 | GFC2/IO108PDB4V0 |
| K2 | GND | GND |
| K3 | IO74NDB4V0 | IO109NDB4V0 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| K4 | IO75NDB4V0 | IO110NDB4V0 |
| K5 | GND | GND |
| K6 | NC | IO104NDB4V0 |
| K7 | NC | IO111NDB4V0 |
| K8 | GND | GND |
| K9 | VCC | VCC |
| K10 | GND | GND |
| K11 | VCC | VCC |
| K12 | GND | GND |
| K13 | VCC | VCC |
| K14 | GND | GND |
| K15 | GND | GND |
| K16 | IO40NDB2V0 | IO60NDB2V0 |
| K17 | NC | IO58PDB2V0 |
| K18 | GND | GND |
| K19 | NC | IO68NPB2V0 |
| K20 | IO41NDB2V0 | IO61NDB2V0 |
| K21 | GND | GND |
| K22 | IO42NDB2V0 | IO56NDB2V0 |
| L1 | IO73NDB4V0 | IO108NDB4V0 |
| L2 | VCCOSC | VCCOSC |
| L3 | VCCIB4 | VCCIB4 |
| L4 | XTAL2 | XTAL2 |
| L5 | GFC1/IO72PDB4V0 | GFC1/IO107PDB4V0 |
| L6 | VCCIB4 | VCCIB4 |
| L7 | GFB1/IO71PDB4V0 | GFB1/IO106PDB4V0 |
| L8 | VCCIB4 | VCCIB4 |
| L9 | GND | GND |
| L10 | VCC | VCC |
| L11 | GND | GND |
| L12 | VCC | VCC |
| L13 | GND | GND |
| L14 | VCC | VCC |
| L15 | VCCIB2 | VCCIB2 |
| L16 | IO48PDB2V0 | IO70PDB2V0 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| L17 | VCCIB2 | VCCIB2 |
| L18 | IO46PDB2V0 | IO69PDB2V0 |
| L19 | GCA1/IO45PDB2V0 | GCA1/IO64PDB2V0 |
| L20 | VCCIB2 | VCCIB2 |
| L21 | GCC0/IO43NDB2V0 | GCC0/IO62NDB2V0 |
| L22 | GCC1/IO43PDB2V0 | GCC1/IO62PDB2V0 |
| M1 | NC | IO103PDB4V0 |
| M2 | XTAL1 | XTAL1 |
| M3 | VCCIB4 | VCCIB4 |
| M4 | GNDOSC | GNDOSC |
| M5 | GFC0/IO72NDB4V0 | GFC0/IO107NDB4V0 |
| M6 | VCCIB4 | VCCIB4 |
| M7 | GFB0/IO71NDB4V0 | GFB0/IO106NDB4V0 |
| M8 | VCCIB4 | VCCIB4 |
| M9 | VCC | VCC |
| M10 | GND | GND |
| M11 | VCC | VCC |
| M12 | GND | GND |
| M13 | VCC | VCC |
| M14 | GND | GND |
| M15 | VCCIB2 | VCCIB2 |
| M16 | IO48NDB2V0 | IO70NDB2V0 |
| M17 | VCCIB2 | VCCIB2 |
| M18 | IO46NDB2V0 | IO69NDB2V0 |
| M19 | GCA0/IO45NDB2V0 | GCA0/IO64NDB2V0 |
| M20 | VCCIB2 | VCCIB2 |
| M21 | GCB0/IO44NDB2V0 | GCB0/IO63NDB2V0 |
| M22 | GCB1/IO44PDB2V0 | GCB1/IO63PDB2V0 |
| N1 | NC | IO103NDB4V0 |
| N2 | GND | GND |
| N3 | IO68PDB4V0 | IO101PDB4V0 |
| N4 | NC | IO100NPB4V0 |
| N5 | GND | GND |
| N6 | NC | IO99PDB4V0 |
| N7 | NC | IO97PDB4V0 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| N8 | GND | GND |
| N9 | GND | GND |
| N10 | VCC | VCC |
| N11 | GND | GND |
| N12 | VCC | VCC |
| N13 | GND | GND |
| N14 | VCC | VCC |
| N15 | GND | GND |
| N16 | GDB2/IO56PDB2V0 | GDB2/IO83PDB2V0 |
| N17 | NC | IO78PDB2V0 |
| N18 | GND | GND |
| N19 | IO47NDB2V0 | IO72NDB2V0 |
| N20 | IO47PDB2V0 | IO72PDB2V0 |
| N21 | GND | GND |
| N22 | IO49PDB2V0 | IO71PDB2V0 |
| P1 | GFA1/IO70PDB4V0 | GFA1/IO105PDB4V0 |
| P2 | GFA0/IO70NDB4V0 | GFA0/IO105NDB4V0 |
| P3 | IO68NDB4V0 | IO101NDB4V0 |
| P4 | IO65PDB4V0 | IO96PDB4V0 |
| P5 | IO65NDB4V0 | IO96NDB4V0 |
| P6 | NC | IO99NDB4V0 |
| P7 | NC | IO97NDB4V0 |
| P8 | VCCIB4 | VCCIB4 |
| P9 | VCC | VCC |
| P10 | GND | GND |
| P11 | VCC | VCC |
| P12 | GND | GND |
| P13 | VCC | VCC |
| P14 | GND | GND |
| P15 | VCCIB2 | VCCIB2 |
| P16 | IO56NDB2V0 | IO83NDB2V0 |
| P17 | NC | IO78NDB2V0 |
| P18 | GDA1/IO54PDB2V0 | GDA1/IO81PDB2V0 |
| P19 | GDB1/IO53PDB2V0 | GDB1/IO80PDB2V0 |
| P20 | IO51NDB2V0 | IO73NDB2V0 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| P21 | IO51PDB2V0 | IO73PDB2V0 |
| P22 | IO49NDB2V0 | IO71NDB2V0 |
| R1 | IO69PDB4V0 | IO102PDB4V0 |
| R2 | IO69NDB4V0 | IO102NDB4V0 |
| R3 | VCCIB4 | VCCIB4 |
| R4 | IO64PDB4V0 | IO91PDB4V0 |
| R5 | IO64NDB4V0 | IO91NDB4V0 |
| R6 | NC | IO92PDB4V0 |
| R7 | GND | GND |
| R8 | GND | GND |
| R9 | VCC33A | VCC33A |
| R10 | GND | GND |
| R11 | VCC33A | VCC33A |
| R12 | GND | GND |
| R13 | VCC33A | VCC33A |
| R14 | GND | GND |
| R15 | VCC | VCC |
| R16 | GND | GND |
| R17 | NC | IO74NDB2V0 |
| R18 | GDA0/IO54NDB2V0 | GDA0/IO81NDB2V0 |
| R19 | GDB0/IO53NDB2V0 | GDB0/IO80NDB2V0 |
| R20 | VCCIB2 | VCCIB2 |
| R21 | IO50NDB2V0 | IO75NDB2V0 |
| R22 | IO50PDB2V0 | IO75PDB2V0 |
| T1 | NC | IO100PPB4V0 |
| T2 | GND | GND |
| T3 | IO66PDB4V0 | IO95PDB4V0 |
| T4 | IO66NDB4V0 | IO95NDB4V0 |
| T5 | VCCIB4 | VCCIB4 |
| T6 | NC | IO92NDB4V0 |
| T7 | GNDNVM | GNDNVM |
| T8 | GND | GND |
| T9 | NC | NC |
| T10 | AV4 | AV4 |
| T11 | NC | NC |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| T12 | AV5 | AV5 |
| T13 | AC5 | AC5 |
| T14 | NC | NC |
| T15 | GND | GND |
| T16 | NC | IO77PPB2V0 |
| T17 | NC | IO74PDB2V0 |
| T18 | VCCIB2 | VCCIB2 |
| T19 | IO55NDB2V0 | IO82NDB2V0 |
| T20 | GDA2/IO55PDB2V0 | GDA2/IO82PDB2V0 |
| T21 | GND | GND |
| T22 | GDC1/IO52PDB2V0 | GDC1/IO79PDB2V0 |
| U1 | IO67PDB4V0 | IO98PDB4V0 |
| U2 | IO67NDB4V0 | IO98NDB4V0 |
| U3 | GEC1/IO63PDB4V0 | GEC1/IO90PDB4V0 |
| U4 | GEC0/IO63NDB4V0 | GEC0/IO90NDB4V0 |
| U5 | GND | GND |
| U6 | VCCNVM | VCCNVM |
| U7 | VCCIB4 | VCCIB4 |
| U8 | VCC15A | VCC15A |
| U9 | GND | GND |
| U10 | AC4 | AC4 |
| U11 | VCC33A | VCC33A |
| U12 | GND | GND |
| U13 | AG5 | AG5 |
| U14 | GND | GND |
| U15 | PUB | PUB |
| U16 | VCCIB2 | VCCIB2 |
| U17 | TDI | TDI |
| U18 | GND | GND |
| U19 | IO57NDB2V0 | IO84NDB2V0 |
| U20 | GDC2/IO57PDB2V0 | GDC2/IO84PDB2V0 |
| U21 | NC | IO77NPB2V0 |
| U22 | GDC0/IO52NDB2V0 | GDC0/IO79NDB2V0 |
| V1 | GEB1/IO62PDB4V0 | GEB1/IO89PDB4V0 |
| V2 | GEB0/IO62NDB4V0 | GEB0/IO89NDB4V0 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| V3 | VCCIB4 | VCCIB4 |
| V4 | GEA1/IO61PDB4V0 | GEA1/IO88PDB4V0 |
| V5 | GEA0/IO61NDB4V0 | GEA0/IO88NDB4V0 |
| V6 | GND | GND |
| V7 | VCC33PMP | VCC33PMP |
| V8 | NC | NC |
| V9 | VCC33A | VCC33A |
| V10 | AG4 | AG4 |
| V11 | AT4 | AT4 |
| V12 | ATRTN2 | ATRTN2 |
| V13 | AT5 | AT5 |
| V14 | VCC33A | VCC33A |
| V15 | NC | NC |
| V16 | VCC33A | VCC33A |
| V17 | GND | GND |
| V18 | TMS | TMS |
| V19 | VJTAG | VJTAG |
| V20 | VCCIB2 | VCCIB2 |
| V21 | TRST | TRST |
| V22 | TDO | TDO |
| W1 | NC | IO93PDB4V0 |
| W2 | GND | GND |
| W3 | NC | IO93NDB4V0 |
| W4 | GEB2/IO59PDB4V0 | GEB2/IO86PDB4V0 |
| W5 | IO59NDB4V0 | IO86NDB4V0 |
| W6 | AV0 | AV0 |
| W7 | GND | GND |
| W8 | AV1 | AV1 |
| W9 | AV2 | AV2 |
| W10 | GND | GND |
| W11 | AV3 | AV3 |
| W12 | AV6 | AV6 |
| W13 | GND | GND |
| W14 | AV7 | AV7 |
| W15 | AV8 | AV8 |

| FG484 | | |
|------------|-----------------|------------------|
| Pin Number | AFS600 Function | AFS1500 Function |
| W16 | GND | GND |
| W17 | AV9 | AV9 |
| W18 | VCCIB2 | VCCIB2 |
| W19 | NC | IO68PPB2V0 |
| W20 | TCK | TCK |
| W21 | GND | GND |
| W22 | NC | IO76PPB2V0 |
| Y1 | GEC2/IO60PDB4V0 | GEC2/IO87PDB4V0 |
| Y2 | IO60NDB4V0 | IO87NDB4V0 |
| Y3 | GEA2/IO58PDB4V0 | GEA2/IO85PDB4V0 |
| Y4 | IO58NDB4V0 | IO85NDB4V0 |
| Y5 | NCAP | NCAP |
| Y6 | AC0 | AC0 |
| Y7 | VCC33A | VCC33A |
| Y8 | AC1 | AC1 |
| Y9 | AC2 | AC2 |
| Y10 | VCC33A | VCC33A |
| Y11 | AC3 | AC3 |
| Y12 | AC6 | AC6 |
| Y13 | VCC33A | VCC33A |
| Y14 | AC7 | AC7 |
| Y15 | AC8 | AC8 |
| Y16 | VCC33A | VCC33A |
| Y17 | AC9 | AC9 |
| Y18 | ADCGNDREF | ADCGNDREF |
| Y19 | PTBASE | PTBASE |
| Y20 | GNDNVM | GNDNVM |
| Y21 | VCCNVM | VCCNVM |
| Y22 | VPUMP | VPUMP |

FG676



Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| A1 | NC |
| A2 | GND |
| A3 | NC |
| A4 | NC |
| A5 | GND |
| A6 | NC |
| A7 | NC |
| A8 | GND |
| A9 | IO17NDB0V2 |
| A10 | IO17PDB0V2 |
| A11 | GND |
| A12 | IO18NDB0V2 |
| A13 | IO18PDB0V2 |
| A14 | IO20NDB0V2 |
| A15 | IO20PDB0V2 |
| A16 | GND |
| A17 | IO21PDB0V2 |
| A18 | IO21NDB0V2 |
| A19 | GND |
| A20 | IO39NDB1V2 |
| A21 | IO39PDB1V2 |
| A22 | GND |
| A23 | NC |
| A24 | NC |
| A25 | GND |
| A26 | NC |
| AA1 | NC |
| AA2 | VCCIB4 |
| AA3 | IO93PDB4V0 |
| AA4 | GND |
| AA5 | IO93NDB4V0 |
| AA6 | GEB2/IO86PDB4V0 |
| AA7 | IO86NDB4V0 |
| AA8 | AV0 |
| AA9 | GNDA |
| AA10 | AV1 |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| AA11 | AV2 |
| AA12 | GNDA |
| AA13 | AV3 |
| AA14 | AV6 |
| AA15 | GNDA |
| AA16 | AV7 |
| AA17 | AV8 |
| AA18 | GNDA |
| AA19 | AV9 |
| AA20 | VCCIB2 |
| AA21 | IO68PPB2V0 |
| AA22 | TCK |
| AA23 | GND |
| AA24 | IO76PPB2V0 |
| AA25 | VCCIB2 |
| AA26 | NC |
| AB1 | GND |
| AB2 | NC |
| AB3 | GEC2/IO87PDB4V0 |
| AB4 | IO87NDB4V0 |
| AB5 | GEA2/IO85PDB4V0 |
| AB6 | IO85NDB4V0 |
| AB7 | NCAP |
| AB8 | AC0 |
| AB9 | VCC33A |
| AB10 | AC1 |
| AB11 | AC2 |
| AB12 | VCC33A |
| AB13 | AC3 |
| AB14 | AC6 |
| AB15 | VCC33A |
| AB16 | AC7 |
| AB17 | AC8 |
| AB18 | VCC33A |
| AB19 | AC9 |
| AB20 | ADCGNDREF |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| AB21 | PTBASE |
| AB22 | GNDNVM |
| AB23 | VCCNVM |
| AB24 | VPUMP |
| AB25 | NC |
| AB26 | GND |
| AC1 | NC |
| AC2 | NC |
| AC3 | NC |
| AC4 | GND |
| AC5 | VCCIB4 |
| AC6 | VCCIB4 |
| AC7 | PCAP |
| AC8 | AG0 |
| AC9 | GNDA |
| AC10 | AG1 |
| AC11 | AG2 |
| AC12 | GNDA |
| AC13 | AG3 |
| AC14 | AG6 |
| AC15 | GNDA |
| AC16 | AG7 |
| AC17 | AG8 |
| AC18 | GNDA |
| AC19 | AG9 |
| AC20 | VAREF |
| AC21 | VCCIB2 |
| AC22 | PTM |
| AC23 | GND |
| AC24 | NC |
| AC25 | NC |
| AC26 | NC |
| AD1 | NC |
| AD2 | NC |
| AD3 | GND |
| AD4 | NC |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| AD5 | IO94NPB4V0 |
| AD6 | GND |
| AD7 | VCC33N |
| AD8 | AT0 |
| AD9 | ATR TN0 |
| AD10 | AT1 |
| AD11 | AT2 |
| AD12 | ATR TN1 |
| AD13 | AT3 |
| AD14 | AT6 |
| AD15 | ATR TN3 |
| AD16 | AT7 |
| AD17 | AT8 |
| AD18 | ATR TN4 |
| AD19 | AT9 |
| AD20 | VCC33A |
| AD21 | GND |
| AD22 | IO76NPB2V0 |
| AD23 | NC |
| AD24 | GND |
| AD25 | NC |
| AD26 | NC |
| AE1 | GND |
| AE2 | GND |
| AE3 | NC |
| AE4 | NC |
| AE5 | NC |
| AE6 | NC |
| AE7 | NC |
| AE8 | NC |
| AE9 | GNDA |
| AE10 | NC |
| AE11 | NC |
| AE12 | GNDA |
| AE13 | NC |
| AE14 | NC |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| AE15 | GNDA |
| AE16 | NC |
| AE17 | NC |
| AE18 | GNDA |
| AE19 | NC |
| AE20 | NC |
| AE21 | NC |
| AE22 | NC |
| AE23 | NC |
| AE24 | NC |
| AE25 | GND |
| AE26 | GND |
| AF1 | NC |
| AF2 | GND |
| AF3 | NC |
| AF4 | NC |
| AF5 | NC |
| AF6 | NC |
| AF7 | NC |
| AF8 | NC |
| AF9 | VCC33A |
| AF10 | NC |
| AF11 | NC |
| AF12 | VCC33A |
| AF13 | NC |
| AF14 | NC |
| AF15 | VCC33A |
| AF16 | NC |
| AF17 | NC |
| AF18 | VCC33A |
| AF19 | NC |
| AF20 | NC |
| AF21 | NC |
| AF22 | NC |
| AF23 | NC |
| AF24 | NC |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| AF25 | GND |
| AF26 | NC |
| B1 | GND |
| B2 | GND |
| B3 | NC |
| B4 | NC |
| B5 | NC |
| B6 | VCCIB0 |
| B7 | NC |
| B8 | NC |
| B9 | VCCIB0 |
| B10 | IO15NDB0V2 |
| B11 | IO15PDB0V2 |
| B12 | VCCIB0 |
| B13 | IO19NDB0V2 |
| B14 | IO19PDB0V2 |
| B15 | VCCIB1 |
| B16 | IO25NDB1V0 |
| B17 | IO25PDB1V0 |
| B18 | VCCIB1 |
| B19 | IO33NDB1V1 |
| B20 | IO33PDB1V1 |
| B21 | VCCIB1 |
| B22 | NC |
| B23 | NC |
| B24 | NC |
| B25 | GND |
| B26 | GND |
| C1 | NC |
| C2 | NC |
| C3 | GND |
| C4 | NC |
| C5 | GAA1/IO01PDB0V0 |
| C6 | GAB0/IO02NDB0V0 |
| C7 | GAB1/IO02PDB0V0 |
| C8 | IO07NDB0V1 |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| C9 | IO07PDB0V1 |
| C10 | IO09PDB0V1 |
| C11 | IO13NDB0V2 |
| C12 | IO13PDB0V2 |
| C13 | IO24PDB1V0 |
| C14 | IO26PDB1V0 |
| C15 | IO27NDB1V1 |
| C16 | IO27PDB1V1 |
| C17 | IO35NDB1V2 |
| C18 | IO35PDB1V2 |
| C19 | GBC0/IO40NDB1V2 |
| C20 | GBA0/IO42NDB1V2 |
| C21 | IO43NDB1V2 |
| C22 | IO43PDB1V2 |
| C23 | NC |
| C24 | GND |
| C25 | NC |
| C26 | NC |
| D1 | NC |
| D2 | NC |
| D3 | NC |
| D4 | GND |
| D5 | GAA0/IO01NDB0V0 |
| D6 | GND |
| D7 | IO04NDB0V0 |
| D8 | IO04PDB0V0 |
| D9 | GND |
| D10 | IO09NDB0V1 |
| D11 | IO11PDB0V1 |
| D12 | GND |
| D13 | IO24NDB1V0 |
| D14 | IO26NDB1V0 |
| D15 | GND |
| D16 | IO31NDB1V1 |
| D17 | IO31PDB1V1 |
| D18 | GND |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| D19 | GBC1/IO40PDB1V2 |
| D20 | GBA1/IO42PDB1V2 |
| D21 | GND |
| D22 | VCCPLB |
| D23 | GND |
| D24 | NC |
| D25 | NC |
| D26 | NC |
| E1 | GND |
| E2 | IO122NPB4V0 |
| E3 | IO121PDB4V0 |
| E4 | IO122PPB4V0 |
| E5 | IO00NDB0V0 |
| E6 | IO00PDB0V0 |
| E7 | VCCIB0 |
| E8 | IO05NDB0V1 |
| E9 | IO05PDB0V1 |
| E10 | VCCIB0 |
| E11 | IO11NDB0V1 |
| E12 | IO14PDB0V2 |
| E13 | VCCIB0 |
| E14 | VCCIB1 |
| E15 | IO29NDB1V1 |
| E16 | IO29PDB1V1 |
| E17 | VCCIB1 |
| E18 | IO37NDB1V2 |
| E19 | GBB0/IO41NDB1V2 |
| E20 | VCCIB1 |
| E21 | VCOMPLB |
| E22 | GBA2/IO44PDB2V0 |
| E23 | IO48PPB2V0 |
| E24 | GBB2/IO45PDB2V0 |
| E25 | NC |
| E26 | GND |
| F1 | NC |
| F2 | VCCIB4 |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| F3 | IO121NDB4V0 |
| F4 | GND |
| F5 | IO123NDB4V0 |
| F6 | GAC2/IO123PDB4V0 |
| F7 | GAA2/IO125PDB4V0 |
| F8 | GAC0/IO03NDB0V0 |
| F9 | GAC1/IO03PDB0V0 |
| F10 | IO10NDB0V1 |
| F11 | IO10PDB0V1 |
| F12 | IO14NDB0V2 |
| F13 | IO23NDB1V0 |
| F14 | IO23PDB1V0 |
| F15 | IO32NPB1V1 |
| F16 | IO34NDB1V1 |
| F17 | IO34PDB1V1 |
| F18 | IO37PDB1V2 |
| F19 | GBB1/IO41PDB1V2 |
| F20 | VCCIB2 |
| F21 | IO47PPB2V0 |
| F22 | IO44NDB2V0 |
| F23 | GND |
| F24 | IO45NDB2V0 |
| F25 | VCCIB2 |
| F26 | NC |
| G1 | NC |
| G2 | IO119PPB4V0 |
| G3 | IO120NDB4V0 |
| G4 | IO120PDB4V0 |
| G5 | VCCIB4 |
| G6 | GAB2/IO124PDB4V0 |
| G7 | IO125NDB4V0 |
| G8 | GND |
| G9 | VCCIB0 |
| G10 | IO08NDB0V1 |
| G11 | IO08PDB0V1 |
| G12 | GND |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| G13 | IO22NDB1V0 |
| G14 | IO22PDB1V0 |
| G15 | GND |
| G16 | IO32PPB1V1 |
| G17 | IO36NPB1V2 |
| G18 | VCCIB1 |
| G19 | GND |
| G20 | IO47NPB2V0 |
| G21 | IO49PDB2V0 |
| G22 | VCCIB2 |
| G23 | IO46NDB2V0 |
| G24 | GBC2/IO46PDB2V0 |
| G25 | IO48NPB2V0 |
| G26 | NC |
| H1 | GND |
| H2 | NC |
| H3 | IO118NDB4V0 |
| H4 | IO118PDB4V0 |
| H5 | IO119NPB4V0 |
| H6 | IO124NDB4V0 |
| H7 | GND |
| H8 | VCOMPLA |
| H9 | VCCPLA |
| H10 | VCCIB0 |
| H11 | IO12NDB0V1 |
| H12 | IO12PDB0V1 |
| H13 | VCCIB0 |
| H14 | VCCIB1 |
| H15 | IO30NDB1V1 |
| H16 | IO30PDB1V1 |
| H17 | VCCIB1 |
| H18 | IO36PPB1V2 |
| H19 | IO38NPB1V2 |
| H20 | GND |
| H21 | IO49NDB2V0 |
| H22 | IO50PDB2V0 |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| H23 | IO50NDB2V0 |
| H24 | IO51PDB2V0 |
| H25 | NC |
| H26 | GND |
| J1 | NC |
| J2 | VCCIB4 |
| J3 | IO115PDB4V0 |
| J4 | GND |
| J5 | IO116NDB4V0 |
| J6 | IO116PDB4V0 |
| J7 | VCCIB4 |
| J8 | IO117PDB4V0 |
| J9 | VCCIB4 |
| J10 | GND |
| J11 | IO06NDB0V1 |
| J12 | IO06PDB0V1 |
| J13 | IO16NDB0V2 |
| J14 | IO16PDB0V2 |
| J15 | IO28NDB1V1 |
| J16 | IO28PDB1V1 |
| J17 | GND |
| J18 | IO38PPB1V2 |
| J19 | IO53PDB2V0 |
| J20 | VCCIB2 |
| J21 | IO52PDB2V0 |
| J22 | IO52NDB2V0 |
| J23 | GND |
| J24 | IO51NDB2V0 |
| J25 | VCCIB2 |
| J26 | NC |
| K1 | NC |
| K2 | NC |
| K3 | IO115NDB4V0 |
| K4 | IO113PDB4V0 |
| K5 | VCCIB4 |
| K6 | IO114NDB4V0 |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| K7 | IO114PDB4V0 |
| K8 | IO117NDB4V0 |
| K9 | GND |
| K10 | VCC |
| K11 | VCCIB0 |
| K12 | GND |
| K13 | VCCIB0 |
| K14 | VCCIB1 |
| K15 | GND |
| K16 | VCCIB1 |
| K17 | GND |
| K18 | GND |
| K19 | IO53NDB2V0 |
| K20 | IO57PDB2V0 |
| K21 | GCA2/IO59PDB2V0 |
| K22 | VCCIB2 |
| K23 | IO54NDB2V0 |
| K24 | IO54PDB2V0 |
| K25 | NC |
| K26 | NC |
| L1 | GND |
| L2 | NC |
| L3 | IO112PPB4V0 |
| L4 | IO113NDB4V0 |
| L5 | GFB2/IO109PDB4V0 |
| L6 | GFA2/IO110PDB4V0 |
| L7 | IO112NPB4V0 |
| L8 | IO104PDB4V0 |
| L9 | IO111PDB4V0 |
| L10 | VCCIB4 |
| L11 | GND |
| L12 | VCC |
| L13 | GND |
| L14 | VCC |
| L15 | GND |
| L16 | VCC |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| L17 | VCCIB2 |
| L18 | GCB2/IO60PDB2V0 |
| L19 | IO58NDB2V0 |
| L20 | IO57NDB2V0 |
| L21 | IO59NDB2V0 |
| L22 | GCC2/IO61PDB2V0 |
| L23 | IO55PPB2V0 |
| L24 | IO56PDB2V0 |
| L25 | IO55NPB2V0 |
| L26 | GND |
| M1 | NC |
| M2 | VCCIB4 |
| M3 | GFC2/IO108PDB4V0 |
| M4 | GND |
| M5 | IO109NDB4V0 |
| M6 | IO110NDB4V0 |
| M7 | GND |
| M8 | IO104NDB4V0 |
| M9 | IO111NDB4V0 |
| M10 | GND |
| M11 | VCC |
| M12 | GND |
| M13 | VCC |
| M14 | GND |
| M15 | VCC |
| M16 | GND |
| M17 | GND |
| M18 | IO60NDB2V0 |
| M19 | IO58PDB2V0 |
| M20 | GND |
| M21 | IO68NPB2V0 |
| M22 | IO61NDB2V0 |
| M23 | GND |
| M24 | IO56NDB2V0 |
| M25 | VCCIB2 |
| M26 | IO65PDB2V0 |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| N1 | NC |
| N2 | NC |
| N3 | IO108NDB4V0 |
| N4 | VCCOSC |
| N5 | VCCIB4 |
| N6 | XTAL2 |
| N7 | GFC1/IO107PDB4V0 |
| N8 | VCCIB4 |
| N9 | GFB1/IO106PDB4V0 |
| N10 | VCCIB4 |
| N11 | GND |
| N12 | VCC |
| N13 | GND |
| N14 | VCC |
| N15 | GND |
| N16 | VCC |
| N17 | VCCIB2 |
| N18 | IO70PDB2V0 |
| N19 | VCCIB2 |
| N20 | IO69PDB2V0 |
| N21 | GCA1/IO64PDB2V0 |
| N22 | VCCIB2 |
| N23 | GCC0/IO62NDB2V0 |
| N24 | GCC1/IO62PDB2V0 |
| N25 | IO66PDB2V0 |
| N26 | IO65NDB2V0 |
| P1 | NC |
| P2 | NC |
| P3 | IO103PDB4V0 |
| P4 | XTAL1 |
| P5 | VCCIB4 |
| P6 | GNDOSC |
| P7 | GFC0/IO107NDB4V0 |
| P8 | VCCIB4 |
| P9 | GFB0/IO106NDB4V0 |
| P10 | VCCIB4 |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| P11 | VCC |
| P12 | GND |
| P13 | VCC |
| P14 | GND |
| P15 | VCC |
| P16 | GND |
| P17 | VCCIB2 |
| P18 | IO70NDB2V0 |
| P19 | VCCIB2 |
| P20 | IO69NDB2V0 |
| P21 | GCA0/IO64NDB2V0 |
| P22 | VCCIB2 |
| P23 | GCB0/IO63NDB2V0 |
| P24 | GCB1/IO63PDB2V0 |
| P25 | IO66NDB2V0 |
| P26 | IO67PDB2V0 |
| R1 | NC |
| R2 | VCCIB4 |
| R3 | IO103NDB4V0 |
| R4 | GND |
| R5 | IO101PDB4V0 |
| R6 | IO100NPB4V0 |
| R7 | GND |
| R8 | IO99PDB4V0 |
| R9 | IO97PDB4V0 |
| R10 | GND |
| R11 | GND |
| R12 | VCC |
| R13 | GND |
| R14 | VCC |
| R15 | GND |
| R16 | VCC |
| R17 | GND |
| R18 | GDB2/IO83PDB2V0 |
| R19 | IO78PDB2V0 |
| R20 | GND |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| R21 | IO72NDB2V0 |
| R22 | IO72PDB2V0 |
| R23 | GND |
| R24 | IO71PDB2V0 |
| R25 | VCCIB2 |
| R26 | IO67NDB2V0 |
| T1 | GND |
| T2 | NC |
| T3 | GFA1/IO105PDB4V0 |
| T4 | GFA0/IO105NDB4V0 |
| T5 | IO101NDB4V0 |
| T6 | IO96PDB4V0 |
| T7 | IO96NDB4V0 |
| T8 | IO99NDB4V0 |
| T9 | IO97NDB4V0 |
| T10 | VCCIB4 |
| T11 | VCC |
| T12 | GND |
| T13 | VCC |
| T14 | GND |
| T15 | VCC |
| T16 | GND |
| T17 | VCCIB2 |
| T18 | IO83NDB2V0 |
| T19 | IO78NDB2V0 |
| T20 | GDA1/IO81PDB2V0 |
| T21 | GDB1/IO80PDB2V0 |
| T22 | IO73NDB2V0 |
| T23 | IO73PDB2V0 |
| T24 | IO71NDB2V0 |
| T25 | NC |
| T26 | GND |
| U1 | NC |
| U2 | NC |
| U3 | IO102PDB4V0 |
| U4 | IO102NDB4V0 |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| U5 | VCCIB4 |
| U6 | IO91PDB4V0 |
| U7 | IO91NDB4V0 |
| U8 | IO92PDB4V0 |
| U9 | GND |
| U10 | GND |
| U11 | VCC33A |
| U12 | GNDA |
| U13 | VCC33A |
| U14 | GNDA |
| U15 | VCC33A |
| U16 | GNDA |
| U17 | VCC |
| U18 | GND |
| U19 | IO74NDB2V0 |
| U20 | GDA0/IO81NDB2V0 |
| U21 | GDB0/IO80NDB2V0 |
| U22 | VCCIB2 |
| U23 | IO75NDB2V0 |
| U24 | IO75PDB2V0 |
| U25 | NC |
| U26 | NC |
| V1 | NC |
| V2 | VCCIB4 |
| V3 | IO100PPB4V0 |
| V4 | GND |
| V5 | IO95PDB4V0 |
| V6 | IO95NDB4V0 |
| V7 | VCCIB4 |
| V8 | IO92NDB4V0 |
| V9 | GNDNVM |
| V10 | GNDA |
| V11 | NC |
| V12 | AV4 |
| V13 | NC |
| V14 | AV5 |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| V15 | AC5 |
| V16 | NC |
| V17 | GNDA |
| V18 | IO77PPB2V0 |
| V19 | IO74PDB2V0 |
| V20 | VCCIB2 |
| V21 | IO82NDB2V0 |
| V22 | GDA2/IO82PDB2V0 |
| V23 | GND |
| V24 | GDC1/IO79PDB2V0 |
| V25 | VCCIB2 |
| V26 | NC |
| W1 | GND |
| W2 | IO94PPB4V0 |
| W3 | IO98PDB4V0 |
| W4 | IO98NDB4V0 |
| W5 | GEC1/IO90PDB4V0 |
| W6 | GEC0/IO90NDB4V0 |
| W7 | GND |
| W8 | VCCNVM |
| W9 | VCCIB4 |
| W10 | VCC15A |
| W11 | GNDA |
| W12 | AC4 |
| W13 | VCC33A |
| W14 | GNDA |
| W15 | AG5 |
| W16 | GNDA |
| W17 | PUB |
| W18 | VCCIB2 |
| W19 | TDI |
| W20 | GND |
| W21 | IO84NDB2V0 |
| W22 | GDC2/IO84PDB2V0 |
| W23 | IO77NPB2V0 |
| W24 | GDC0/IO79NDB2V0 |

| FG676 | |
|------------|------------------|
| Pin Number | AFS1500 Function |
| W25 | NC |
| W26 | GND |
| Y1 | NC |
| Y2 | NC |
| Y3 | GEB1/IO89PDB4V0 |
| Y4 | GEB0/IO89NDB4V0 |
| Y5 | VCCIB4 |
| Y6 | GEA1/IO88PDB4V0 |
| Y7 | GEA0/IO88NDB4V0 |
| Y8 | GND |
| Y9 | VCC33PMP |
| Y10 | NC |
| Y11 | VCC33A |
| Y12 | AG4 |
| Y13 | AT4 |
| Y14 | ATR TN2 |
| Y15 | AT5 |
| Y16 | VCC33A |
| Y17 | NC |
| Y18 | VCC33A |
| Y19 | GND |
| Y20 | TMS |
| Y21 | VJTAG |
| Y22 | VCCIB2 |
| Y23 | TRST |
| Y24 | TDO |
| Y25 | NC |
| Y26 | NC |

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the Fusion datasheet.

| Revision | Changes | Table |
|------------------------------|---|-----------------------|
| Revision 8 (May 2018) | In " Specifying I/O States During Programming ", the version of the software, v9.0 is removed to write Libero SoC, as Fusion family is supported in the Libero SoC (SAR 73296). | 1-9 |
| | In tables, Table 2-78 , Table 2-79 and Table 2-80 , "3" is edited to a tick mark, to show the I/O standards with available drive and slew settings (SAR 70900). | 2-152 |
| | The description for "LOCKREQUEST" is edited in " LOCKREQUEST " section (SAR 25423). | 2-44 |
| | A note is added to explain data corruption in SRAM block, when setup and hold requirements are violated on address inputs under " Clocking " (SAR 93618). | 2-61 |
| | A note is added where ever it is applicable in the datasheet that the package PQ208 is discontinued (SAR 76873). | |
| | A note is added in " Package Pin Assignments " to direct the user to PD3068: Package Mechanical Drawings (SAR 76874) | 4-1 |
| Revision 7 (May 2016) | Note added for discontinuance of PQ208 package to the " Package I/Os: Single-/Double-Ended (Analog) " table, " Product Ordering Codes ", and " Temperature Grade Offerings " table (SAR). | 1-II, 1-III, and 1-IV |
| | Updated Figure 2-42 (SAR 61872). | 2-51 |
| Revision 6 (March 2014) | Note added for the discontinuance of QN108 and QN180 packages to the " Package I/Os: Single-/Double-Ended (Analog) " table and the " Temperature Grade Offerings " table (SAR 55113, PDN 1306). | II and IV |
| | Updated details about page programming time in the " Program Operation " section (SAR 49291). | 2-46 |
| | ADC_START changed to ADCSTART in the " ADC Operation " section (SAR 44104). | 2-104 |
| Revision 5 (January 2014) | Calibrated offset values (AFS090, AFS250) of the external temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 51464). | 2-117 |
| | Specifications for the internal temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 50870). | 2-117 |

| Revision | Changes | Table |
|------------------------------|---|-----------------|
| Revision 4 (January 2013) | The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43177). | III |
| | The note in Table 2-12 • Fusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42563). | 2-28 |
| | Table 2-49 • Analog Channel Specifications was modified to update the uncalibrated offset values (AFS250) of the external and internal temperature monitors (SAR 43134). | 2-117 |
| | In Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3) , changed the column heading from 'Full-Scale Voltage' to 'Full Scale Voltage in 10-Bit Mode', and added and updated Notes as required (SAR 20812). | 2-130 |
| | The values for the Speed Grade (-1 and Std.) for FDDRIMAX (Table 2-180 • Input DDR Propagation Delays) and values for the Speed Grade (-2 and Std.) for FDDOMAX (Table 2-182 • Output DDR Propagation Delays) had been inadvertently interchanged. This has been rectified (SAR 38514). | 2-220, 2-222 |
| | Added description about what happens if a user connects VAREF to an external 3.3 V on their board to the " V_{AREF} Analog Reference Voltage " section (SAR 35188). | 2-225 |
| | Added a note to Table 3-2 • Recommended Operating Conditions¹ (SAR 43429): The programming temperature range supported is T _{ambient} = 0°C to 85°C. | 3-3 |
| | Added the Package Thermal details for AFS600-PQ208 and AFS250-PQ208 to Table 3-6 • Package Thermal Resistance (SAR 37816). Deleted the Die Size column from the table (SAR 43503). | 3-7 |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 42495). Live at Power-Up (LAPU) has been replaced with 'Instant On'. | NA |
| Revision 3 (August 2012) | Microblade U1AFS250 and U1AFS1500 devices were added to the product tables. | I – IV |
| | A sentence pertaining to the analog I/Os was added to the " Specifying I/O States During Programming " section (SAR 34831). | 1-9 |

| Revision | Changes | Table |
|----------------------------|---|---|
| Revision 3 (continued) | The "RC Oscillator" section was revised to correct a sentence that did not differentiate accuracy for commercial and industrial temperature ranges, which is given in Table 2-9 • Electrical Characteristics of RC Oscillator (SAR 33722). | 2-19 |
| | Figure 2-57 • FIFO Read and Figure 2-58 • FIFO Write are new (SAR 34840). | 2-72 |
| | The first paragraph of the "Offset" section was removed; it was intended to be replaced by the paragraph following it (SAR 22647). | 2-95 |
| | IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected in Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions (SAR 39813). | 2-164 |
| | The drive strength, IOL, and IOH for 3.3 V GTL and 2.5 V GTL were changed from 25 mA to 20 mA in the following tables (SAR 37373): Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings Table 2-96 • I/O Output Buffer Maximum Resistances ¹ Table 2-138 • Minimum and Maximum DC Input and Output Levels Table 2-141 • Minimum and Maximum DC Input and Output Levels | 2-164 2-167 2-169 2-199 2-200 |
| | The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34800): "It uses a 5 V–tolerant input buffer and push-pull output buffer." | 2-181 |
| | Corrected the inadvertent error in maximum values for LVPECL VIH and VIL and revised them to "3.6" in Table 2-171 • Minimum and Maximum DC Input and Output Levels, making these consistent with Table 3-1 • Absolute Maximum Ratings, and Table 3-4 • Overshoot and Undershoot Limits ¹ (SAR 37687). | 2-211 |
| | The maximum frequency for global clock parameter was removed from Table 2-5 • AFS1500 Global Resource Timing through Table 2-8 • AFS090 Global Resource Timing because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36955). | 2-16 to 2-17 |
| Revision 2 (March 2012) | The phrase "without debug" was removed from the "Soft ARM Cortex-M1 Fusion Devices (M1)" section (SAR 21390). | I |
| | The "In-System Programming (ISP) and Security" section, "Security" section, "Flash Advantages" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34679). | I, 1-2, 2-228 |
| | The Y security option and Licensed DPA Logo was added to the "Product Ordering Codes" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34721). | III |
| | The "Specifying I/O States During Programming" section is new (SAR 34693). | 1-9 |
| | The following information was added before Figure 2-17 • XTLOSC Macro: In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating (SAR 24119). | 2-20 |
| | Table 2-12 • Fusion CCC/PLL Specification was updated. A note was added indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34814). | 2-28 |

| Revision | Changes | Table |
|---------------------------|--|------------------------------|
| Revision 2 (continued) | A note was added to Figure 2-27 • Real-Time Counter System (not all the signals are shown for the AB macro) stating that the user is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off (SAR 21773). | 2-31 |
| | VPUMP was incorrectly represented as VPP in several places. This was corrected to VPUMP in the "Standby and Sleep Mode Circuit Implementation" section and Table 3-8 • AFS1500 Quiescent Supply Current Characteristics through Table 3-11 • AFS090 Quiescent Supply Current Characteristics (21963). | 2-32, 3-10 |
| | Additional information was added to the Flash Memory Block "Write Operation" section, including an explanation of the fact that a copy-page operation takes no less than 55 cycles (SAR 26338). | 2-45 |
| | The "FlashROM" section was revised to refer to Figure 2-46 • FlashROM Timing Diagram and Table 2-26 • FlashROM Access Time rather than stating 20 MHz as the maximum FlashROM access clock and 10 ns as the time interval for D0 to become valid or invalid (SAR 22105). | 2-53, 2-54 |
| | <p>The following figures were deleted (SAR 29991). Reference was made to a new application note, <i>Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs</i>, which covers these cases in detail (SAR 34862).</p> <p>Figure 2-55 • Write Access after Write onto Same Address Figure 2-56 • Read Access after Write onto Same Address Figure 2-57 • Write Access after Read onto Same Address</p> <p>The port names in the SRAM "Timing Waveforms", "Timing Characteristics", SRAM tables, Figure 2-55 • RAM Reset. Applicable to both RAM4K9 and RAM512x18., and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35753).</p> | 2-63, 2-66, 2-65, 2-75 |
| | <p>In several places throughout the datasheet, GNDREF was corrected to ADCGNDREF (SAR 20783):</p> <p>Figure 2-64 • Analog Block Macro Table 2-36 • Analog Block Pin Description "ADC Operation" section</p> | 2-77 2-78 2-104 |
| | <p>The following note was added below Figure 2-78 • Timing Diagram for the Temperature Monitor Strobe Signal:</p> <p>When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 μA sink into the Fusion device. (SAR 24796).</p> | 2-93 |
| | The "Analog-to-Digital Converter Block" section was extensively revised, reorganizing the information and adding the "ADC Theory of Operation" section and "Acquisition Time or Sample Time Control" section. The "ADC Example" section was reworked and corrected (SAR 20577). | 2-96 |
| | Table 2-49 • Analog Channel Specifications was modified to include calibrated and uncalibrated values for offset (AFS090 and AFS250) for the external and internal temperature monitors. The "Offset" section was revised accordingly and now references Table 2-49 • Analog Channel Specifications (SARs 22647, 27015). | 2-95, 2-117 |
| | The "Intra-Conversion" section and "Injected Conversion" section had definitions incorrectly interchanged and have been corrected. Figure 2-92 • Intra-Conversion Timing Diagram and Figure 2-93 • Injected Conversion Timing Diagram were also incorrectly interchanged and have been replaced correctly. Reference in the figure notes to EQ 10 has been corrected to EQ 23 (SAR 20547). | 2-110, 2-113, 2-113 |

| Revision | Changes | Table |
|--|---|-----------------|
| Revision 2 (continued) | The prescaler range for the 'Analog Input (direct input to ADC)' configurations was removed as inapplicable for direct inputs. The input resistance for direct inputs is covered in Table 2-50 • ADC Characteristics in Direct Input Mode (SAR 31201). | 2-120 |
| | The "Examples" for calibrating accuracy for ADC channels were revised and corrected to make them consistent with terminology in the associated tables (SARs 36791, 36773). | 2-124 |
| | A note was added to Table 2-56 • Analog Quad ACM Byte Assignment and the introductory text for Table 2-66 • Internal Temperature Monitor Control Truth Table , stating that for the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set (SAR 34418). | 2-129, 2-131 |
| | t_{DOUT} was corrected to t_{DIN} in Figure 2-116 • Input Buffer Timing Model and Delays (example) (SAR 37115). | 2-161 |
| | The formulas in the table notes for Table 2-97 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34751). | 2-171 |
| | The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34877). | 2-175 |
| | The following notes were removed from Table 2-168 • Minimum and Maximum DC Input and Output Levels (SAR 34808): ±5% Differential input voltage = ±350 mV | 2-209 |
| | An incomplete, duplicate sentence was removed from the end of the "GNDAQ Ground (analog quiet)" pin description (SAR 30185). | 2-223 |
| | Information about configuration of unused I/Os was added to the "User Pins" section (SAR 32642). | 2-225 |
| | The following information was added to the pin description for "XTAL1 Crystal Oscillator Circuit Input" and "XTAL2 Crystal Oscillator Circuit Input" (SAR 24119). | 2-227 |
| | The input resistance to ground value in Table 3-3 • Input Resistance of Analog Pads for Analog Input (direct input to ADC), was corrected from 1 MΩ (typical) to 2 kΩ (typical) (SAR 34371). | 3-4 |
| | The Storage Temperature column in Table 3-5 • FPGA Programming, Storage, and Operating Limits stated Min. T _J twice for commercial and industrial product grades and has been corrected to Min. T _J and Max. T _J (SAR 29416). | 3-5 |
| | The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Dynamic Contribution—P _{CLOCK} " section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the <i>Fusion FPGA Fabric User's Guide</i> (SAR 34741). | 3-24 |
| Package names used in the "Package Pin Assignments" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 36612). | 4-1 | |
| July 2010 | The versioning system for data-sheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Fusion Device Status" table indicates the status for each device in the device family. | N/A |

| Revision | Changes | Table |
|---------------------------------|---|-------|
| v2.0, Revision 1 (July 2009) | <p>The MicroBlade and Fusion datasheets have been combined. Pigeon Point information is new.</p> <p>CoreMP7 support was removed since it is no longer offered.</p> <p>–F was removed from the datasheet since it is no longer offered.</p> <p>The operating temperature was changed from ambient to junction to better reflect actual conditions of operations.</p> <p>Commercial: 0°C to 85°C</p> <p>Industrial: –40°C to 100°C</p> <p>The version number category was changed from Preliminary to Production, which means the datasheet contains information based on final characterization. The version number changed from Preliminary v1.7 to v2.0.</p> | N/A |
| | The "Integrated Analog Blocks and Analog I/Os" section was updated to include a reference to the "Analog System Characteristics" section in the <i>Device Architecture</i> chapter of the datasheet, which includes Table 2-46 • Analog Channel Specifications and specific voltage data. | 1-4 |
| | The phrase "Commercial-Case Conditions" in timing table titles was changed to "Commercial Temperature Range Conditions." | N/A |
| | The "Crystal Oscillator" section was updated significantly. Please review carefully. | 2-20 |
| | The "Real-Time Counter (part of AB macro)" section was updated significantly. Please review carefully. | 2-33 |
| | There was a typo in Table 2-19 • Flash Memory Block Pin Names for the ERASEPAGE description; it was the same as DISCARDPAGE. As a result, the ERASEPAGE description was updated. | 2-40 |
| | The $t_{FMAXCLKNVM}$ parameter was updated in Table 2-25 • Flash Memory Block Timing . | 2-52 |
| | Table 2-31 • RAM4K9 and Table 2-32 • RAM512X18 were updated. | 2-66 |
| | In Table 2-36 • Analog Block Pin Description , the Function description for PWRDWN was changed from "Comparator power-down if 1" to "ADC comparator power-down if 1. When asserted, the ADC will stop functioning, and the digital portion of the analog block will continue operating. This may result in invalid status flags from the analog block. Therefore, Microsemi does not recommend asserting the PWRDWN pin." | 2-78 |
| | Figure 2-75 • Gate Driver Example was updated. | 2-91 |
| | The "ADC Operation" section was updated. Please review carefully. | 2-104 |
| | Figure 2-92 • Intra-Conversion Timing Diagram and Figure 2-93 • Injected Conversion Timing Diagram are new. | 2-113 |
| | The "Typical Performance Characteristics" section is new. | 2-115 |
| | Table 2-49 • Analog Channel Specifications was significantly updated. | 2-117 |
| | Table 2-50 • ADC Characteristics in Direct Input Mode was significantly updated. | 2-120 |
| | In Table 2-52 • Calibrated Analog Channel Accuracy ^{1,2,3} , note 2 was updated. | 2-123 |
| | In Table 2-53 • Analog Channel Accuracy: Monitoring Standard Positive Voltages , note 1 was updated. | 2-124 |
| | In Table 2-54 • ACM Address Decode Table for Analog Quad , bit 89 was removed. | 2-126 |

| Revision | Changes | Table |
|---|--|-------------------|
| v2.0, Revision 1 (continued) | The data in the 2.5 V LCMOS and LVCMOS 2.5 V / 5.0 V rows were updated in Table 2-75 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities . | 2-143 |
| | In Table 2-78 • Fusion Standard I/O Standards—OUT_DRIVE Settings , LVCMOS 1.5 V, for OUT_DRIVE 2, was changed from a dash to a check mark. | 2-152 |
| | The " VCC15A Analog Power Supply (1.5 V) " definition was changed from "A 1.5 V analog power supply input should be used to provide this input" to "1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry." | 2-223 |
| | In the " VCC33PMP Analog Power Supply (3.3 V) " pin description, the following text was changed from "VCC33PMP should be powered up before or simultaneously with VCC33A" to "VCC33PMP should be powered up simultaneously with or after VCC33A." | 2-223 |
| | The " VCCOSC Oscillator Power Supply (3.3 V) " section was updated to include information about when to power the pin. | 2-223 |
| | In the " 128-Bit AES Decryption " section, FIPS-192 was incorrect and changed to FIPS-197. | 2-228 |
| | The note in Table 2-84 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications was updated. | 2-156 |
| | For 1.5 V LVCMOS, the VIL and VIH parameters, $0.30 * VCCI$ was changed to $0.35 * VCCI$ and $0.70 * VCCI$ was changed to $0.65 * VCCI$ in Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions , Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions , and Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions . In Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions , the VIH max column was updated. | 2-164 to 2-165 |
| | Table 2-89 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated to include notes 3 and 4. The temperature ranges were also updated in notes 1 and 2. | 2-165 |
| | The titles in Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings to Table 2-94 • Summary of I/O Timing Characteristics – Software Default Settings were updated to "VCCI = I/O Standard Dependent." | 2-167 to 2-168 |
| | Below Table 2-98 • I/O Short Currents IOSH/IOSL , the paragraph was updated to change 110°C to 100°C and three months was changed to six months. | 2-172 |
| | Table 2-99 • Short Current Event Duration before Failure was updated to remove 110°C data. | 2-174 |
| | In Table 2-101 • I/O Input Rise Time, Fall Time, and Related I/O Reliability , LVTTTL/LVCMOS rows were changed from 110°C to 100°C. | 2-174 |
| | VCC33PMP was added to Table 3-1 • Absolute Maximum Ratings . In addition, conditions for AV, AC, AG, and AT were also updated. | 3-1 |
| | VCC33PMP was added to Table 3-2 • Recommended Operating Conditions¹ . In addition, conditions for AV, AC, AG, and AT were also updated. | 3-3 |
| Table 3-5 • FPGA Programming, Storage, and Operating Limits was updated to include new data and the temperature ranges were changed. The notes were removed from the table. | 3-5 | |

| Revision | Changes | Table |
|------------------------------------|---|--------------|
| v2.0, Revision 1 (continued) | Table 3-6 • Package Thermal Resistance was updated to include new data. | 3-7 |
| | In EQ 4 to EQ 6, the junction temperature was changed from 110°C to 100°C. | 3-8 to 3-8 |
| | Table 3-8 • AFS1500 Quiescent Supply Current Characteristics through Table 3-11 • AFS090 Quiescent Supply Current Characteristics are new and have replaced the Quiescent Supply Current Characteristics (IDDQ) table. | 3-10 to 3-16 |
| | In Table 3-14 • Different Components Contributing to the Dynamic Power Consumption in Fusion Devices, the power supply for PAC9 and PAC10 were changed from VMV/VCC to VCCI. | 3-22 |
| | In Table 3-15 • Different Components Contributing to the Static Power Consumption in Fusion Devices, the power supply for PDC7 and PDC8 were changed from VMV/VCC to VCCI. PDC1 was updated from TBD to 18. | 3-23 |
| | The "QN108" table was updated to remove the duplicates of pins B12 and B34. | 4-2 |
| Preliminary v1.7 (October 2008) | The version number category was changed from Advance to Preliminary, which means the datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible. | |
| | For the VIL and VIH parameters, 0.30 * VCCI was changed to 0.35 * VCCI and 0.70 * VCCI was changed to 0.65 * VCCI in Table 2-126 • Minimum and Maximum DC Input and Output Levels. | 2-193 |
| | The version number category was changed from Advance to Preliminary, which means the datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible. | N/A |
| | The following updates were made to Table 2-141 • Minimum and Maximum DC Input and Output Levels: Temperature Digital Output 213 00 1111 1101 283 01 0001 1011 358 01 0110 0110 – only the digital output was updated. Temperature 358 remains in the temperature column. | 2-200 |
| | In Advance v1.2, the "V _{AREF} Analog Reference Voltage" pin description was significantly updated but the change was not noted in the change table. | 2-225 |
| Advance v1.6 (August 2008) | The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA. | N/A |
| | The references to the <i>Peripherals User's Guide</i> in the "No-Glitch MUX (NGMUX)" section and "Voltage Regulator Power Supply Monitor (VRPSM)" section were changed to <i>Fusion Handbook</i> . | 2-32, 2-42 |
| Advance v1.5 (July 2008) | The following bullet was updated from High-Voltage Input Tolerance: ±12 V to High-Voltage Input Tolerance: 10.5 V to 12 V. | I |
| | The following bullet was updated from Programmable 1, 3, 10, 30 µA and 25 mA Drive Strengths to Programmable 1, 3, 10, 30 µA and 20 mA Drive Strengths. | I |

| Revision | Changes | Table |
|-----------------------------|---|-------|
| Advance v1.5 (continued) | This bullet was added to the “ Integrated A/D Converter (ADC) and Analog I/O ” section: ADC Accuracy is Better than 1% | I |
| | In the “ Integrated Analog Blocks and Analog I/Os ” section, ± 4 LSB was changed to 0.72. The following sentence was deleted: The input range for voltage signals is from -12 V to $+12$ V with full-scale output values from 0.125 V to 16 V. In addition, 2°C was changed to 3°C : “One analog input in each quad can be connected to an external temperature monitor diode and achieves detection accuracy of $\pm 3^{\circ}\text{C}$.” The following sentence was deleted: The input range for voltage signals is from -12 V to $+12$ V with full-scale output values from 0.125 V to 16 V. | 1-4 |
| | The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA. | N/A |
| Advance v1.4 (July 2008) | In Table 3-8 • Quiescent Supply Current Characteristics (IDDQ)1 , footnote references were updated for $I_{\text{DC}2}$ and $I_{\text{DC}3}$. Footnote 3 and 4 were updated and footnote 5 is new. | 3-11 |
| Advance v1.3 (July 2008) | The “ ADC Description ” section was significantly updated. Please review carefully. | 2-102 |
| Advance v1.2 (May 2008) | Table 2-25 • Flash Memory Block Timing was significantly updated. | 2-55 |
| | The “ V_{AREF} Analog Reference Voltage ” pin description section was significantly update. Please review it carefully. | 2-226 |
| | Table 2-45 • ADC Interface Timing was significantly updated. | 2-110 |
| | Table 2-56 • Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3) was significantly updated. | 2-131 |
| | The following sentence was deleted from the “ Voltage Monitor ” section: The Analog Quad inputs are tolerant up to 12 V + 10%. | 2-86 |
| | The “ 180-Pin QFN ” figure was updated. D1 to D4 are new and the figure was changed to bottom view. The note below the figure is new. | 3-3 |
| Advance v1.1 (May 2008) | The following text was incorrect and therefore deleted: VCC33A Analog Power Filter Analog power pin for the analog power supply low-pass filter. An external 100 pF capacitor should be connected between this pin and ground. There is still a description of $V_{\text{CC}33\text{A}}$ on page 2-224 . | 2-204 |

| Revision | Changes | Table |
|---|---|-------|
| Advance v1.0 (January 2008) | All Timing Characteristics tables were updated. For the Differential I/O Standards, the Standard I/O support tables are new. | N/A |
| | Table 2-3 • Array Coordinates was updated to change the max x and y values | 2-9 |
| | Table 2-12 • Fusion CCC/PLL Specification was updated. | 2-31 |
| | A note was added to Table 2-16 • RTC ACM Memory Map. | 2-37 |
| | A reference to the Peripheral's User's Guide was added to the "Voltage Regulator Power Supply Monitor (VRPSM)" section. | 2-42 |
| | In Table 2-25 • Flash Memory Block Timing, the commercial conditions were updated. | 2-55 |
| | In Table 2-26 • FlashROM Access Time, the commercial conditions were missing and have been added below the title of the table. | 2-58 |
| | In Table 2-36 • Analog Block Pin Description, the function description was updated for the ADCRESET. | 2-82 |
| | In the "Voltage Monitor" section, the following sentence originally had $\pm 10\%$ and it was changed to $+10\%$. The Analog Quad inputs are tolerant up to 12 V + 10%. In addition, this statement was deleted from the datasheet: Each I/O will draw power when connected to power (3 mA at 3 V). | 2-86 |
| | The "Terminology" section is new. | 2-88 |
| | The "Current Monitor" section was significantly updated. Figure 2-72 • Timing Diagram for Current Monitor Strobe to Figure 2-74 • Negative Current Monitor and Table 2-37 • Recommended Resistor for Different Current Range Measurement are new. | 2-90 |
| | The "ADC Description" section was updated to add the "Terminology" section. | 2-93 |
| | In the "Gate Driver" section, 25 mA was changed to 20 mA and 1.5 MHz was changed to 1.3 MHz. In addition, the following sentence was deleted: The maximum AG pad switching frequency is 1.25 MHz. | 2-94 |
| | The "Temperature Monitor" section was updated to rewrite most of the text and add Figure 2-78, Figure 2-79, and Table 2-38 • Temperature Data Format. | 2-96 |
| | In Table 2-38 • Temperature Data Format, the temperature K column was changed for 85°C from 538 to 358. | 2-98 |
| | In Table 2-45 • ADC Interface Timing, "Typical-Case" was changed to "Worst-Case." | 2-110 |
| | The "ADC Interface Timing" section is new. | 2-110 |
| | Table 2-46 • Analog Channel Specifications was updated. | 2-118 |
| | The "V _{CC15A} Analog Power Supply (1.5 V)" section was updated. | 2-224 |
| | The "V _{CCPLA/B} PLL Supply Voltage" section is new. | 2-225 |
| In "V _{CCNVM} Flash Memory Block Power Supply (1.5 V)" section, supply was changed to supply input. | 2-224 | |
| The "V _{CCPLA/B} PLL Supply Voltage" pin description was updated to include the following statement: Actel recommends tying VCCPLX to VCC and using proper filtering circuits to decouple V _{CC} noise from PLL. | 2-225 | |
| The "V _{COMPLA/B} Ground for West and East PLL" section was updated. | 2-225 | |

| Revision | Changes | Table |
|--|--|-------|
| Advance 1.0 (continued) | In Table 2-47 • ADC Characteristics in Direct Input Mode , the commercial conditions were updated and note 2 is new. | 2-121 |
| | The $V_{CC33ACAP}$ signal name was changed to "XTAL1 Crystal Oscillator Circuit Input". | 2-228 |
| | Table 2-48 • Uncalibrated Analog Channel Accuracy* is new. | 2-123 |
| | Table 2-49 • Calibrated Analog Channel Accuracy^{1,2,3} is new. | 2-124 |
| | Table 2-50 • Analog Channel Accuracy: Monitoring Standard Positive Voltages is new. | 2-125 |
| | In Table 2-57 • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)* , the following I/O Bank names were changed: Hot-Swap changed to Standard LVDS changed to Advanced | 2-131 |
| | In Table 2-58 • Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3) , the following I/O Bank names were changed: Hot-Swap changed to Standard LVDS changed to Advanced | 2-132 |
| | In the title of Table 2-64 • I/O Standards Supported by Bank Type , LVDS I/O was changed to Advanced I/O. | 2-134 |
| | The title was changed from "Fusion Standard, LVDS, and Standard plus Hot-Swap I/O" to Table 2-68 • Fusion Standard and Advanced I/O Features . In addition, the table headings were all updated. The heading used to be Standard and LVDS I/O and was changed to Advanced I/O. Standard Hot-Swap was changed to just Standard. | 2-136 |
| | This sentence was deleted from the "Slew Rate Control and Drive Strength" section: The Standard hot-swap I/Os do not support slew rate control. In addition, these references were changed: • From: Fusion hot-swap I/O (Table 2-69 on page 2-122) To: Fusion Standard I/O • From: Fusion LVDS I/O (Table 2-70 on page 2-122) To: Fusion Advanced I/O | 2-152 |
| | The "Cold-Sparing Support" section was significantly updated. | 2-143 |
| | In the title of Table 2-75 • Fusion Standard I/O Standards—OUT_DRIVE Settings , Hot-Swap was changed to Standard. | 2-153 |
| | In the title of Table 2-76 • Fusion Advanced I/O Standards—SLEW and OUT_DRIVE Settings , LVDS was changed to Advanced. | 2-153 |
| | In the title of Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications , LVDS was changed to Advanced. | 2-157 |
| | In Figure 2-111 • Naming Conventions of Fusion Devices with Three Digital I/O Banks and Figure 2-112 • Naming Conventions of Fusion Devices with Four I/O Banks the following names were changed: Hot-Swap changed to Standard LVDS changed to Advanced | 2-160 |
| The Figure 2-113 • Timing Model was updated. | 2-161 | |
| In the notes for Table 2-86 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions , T_J was changed to T_A . | 2-166 | |

| Revision | Changes | Table |
|--------------------------------|---|------------|
| Advance v1.0 (continued) | This change table states that in the "208-Pin PQFP" table listed under the Advance v0.8 changes, the AFS090 device had a pin change. That is incorrect. Pin 102 was updated for AFS250 and AFS600. The function name changed from $V_{CC33ACAP}$ to V_{CC33A} . | 3-8 |
| Advance v0.9 (October 2007) | In the "Package I/Os: Single-/Double-Ended (Analog)" table, the AFS1500/M7AFS1500 I/O counts were updated for the following devices: FG484: 223/109 FG676: 252/126 | II |
| | In the "108-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pin: B25 | 3-2 |
| | In the "180-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: B29 AFS250: B29 | 3-4 |
| | In the "208-Pin PQFP" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: 102 AFS250: 102 | 3-8 |
| | In the "256-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: T14 AFS250: T14 AFS600: T14 AFS1500: T14 | 3-12 |
| Advance v0.9 (continued) | In the "484-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS600: AB18 AFS1500: AB18 | 3-20 |
| | In the "676-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS1500: AD20 | 3-28 |
| Advance v0.8 (June 2007) | Figure 2-16 • Fusion Clocking Options and the "RC Oscillator" section were updated to change GND_OSC and VCC_OSC to GNDOSC and VCCOSC. | 2-20, 2-21 |
| | Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro was updated to change the positions of OADIVRST and OADIVHALF, and a note was added. | 2-25 |
| | The "Crystal Oscillator" section was updated to include information about controlling and enabling/disabling the crystal oscillator. | 2-22 |
| | Table 2-11 • Electrical Characteristics of the Crystal Oscillator was updated to change the typical value of $I_{DYNXTAL}$ for 0.032–0.2 MHz to 0.19. | 2-24 |
| | The "1.5 V Voltage Regulator" section was updated to add "or floating" in the paragraph stating that an external pull-down is required on TRST to power down the VR. | 2-41 |
| | The "1.5 V Voltage Regulator" section was updated to include information on powering down with the VR. | 2-41 |

| Revision | Changes | Table |
|--|--|-----------------|
| Advance v0.8 (continued) | This sentence was updated in the "No-Glitch MUX (NGMUX)" section to delete GLA: The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC). | 2-32 |
| | In Table 2-13 • NGMUX Configuration and Selection Table, 10 and 11 were deleted. | 2-32 |
| | The method to enable sleep mode was updated for bit 0 in Table 2-16 • RTC Control/Status Register. | 2-38 |
| | S2 was changed to D2 in Figure 2-39 • Read Waveform (Pipe Mode, 32-bit access) for RD[31:0] was updated. | 2-51 |
| | The definitions for bits 2 and 3 were updated in Table 2-24 • Page Status Bit Definition. | 2-52 |
| | Figure 2-46 • FlashROM Timing Diagram was updated. | 2-58 |
| | Table 2-26 • FlashROM Access Time is new. | 2-58 |
| | Figure 2-55 • Write Access After Write onto Same Address, Figure 2-56 • Read Access After Write onto Same Address, and Figure 2-57 • Write Access After Read onto Same Address are new. | 2-68– 2-70 |
| | Table 2-31 • RAM4K9 and Table 2-32 • RAM512X18 were updated. | 2-71, 2-72 |
| | The VAREF and SAMPLE functions were updated in Table 2-36 • Analog Block Pin Description. | 2-82 |
| | The title of Figure 2-72 • Timing Diagram for Current Monitor Strobe was updated to add the word "positive." | 2-91 |
| | The "Gate Driver" section was updated to give information about the switching rate in High Current Drive mode. | 2-94 |
| | The "ADC Description" section was updated to include information about the SAMPLE and BUSY signals and the maximum frequencies for SYSCLK and ADCCLK. EQ 2 was updated to add parentheses around the entire expression in the denominator. | 2-102 |
| | Table 2-46 • Analog Channel Specifications and Table 2-47 • ADC Characteristics in Direct Input Mode were updated. | 2-118, 2-121 |
| | The note was removed from Table 2-55 • Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3). | 2-131 |
| | Table 2-63 • Internal Temperature Monitor Control Truth Table is new. | 2-132 |
| | The "Cold-Sparing Support" section was updated to add information about cases where current draw can occur. | 2-143 |
| | Figure 2-104 • Solution 4 was updated. | 2-147 |
| | Table 2-75 • Fusion Standard I/O Standards—OUT_DRIVE Settings was updated. | 2-153 |
| | The "GNDA Ground (analog)" section and "GNDAQ Ground (analog quiet)" section were updated to add information about maximum differential voltage. | 2-224 |
| The "V _{AREF} Analog Reference Voltage" section and "VPUMP Programming Supply Voltage" section were updated. | 2-226 | |
| The "V _{CCPLA/B} PLL Supply Voltage" section was updated to include information about the east and west PLLs. | 2-225 | |
| The V _{COMPLF} pin description was deleted. | N/A | |
| The "Axy Analog Input/Output" section was updated with information about grounding and floating the pin. | 2-226 | |

| Revision | Changes | Table |
|--------------------------------|---|-------|
| Advance v0.8 (continued) | The voltage range in the "VPUMP Programming Supply Voltage" section was updated. The parenthetical reference to "pulled up" was removed from the statement, "VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V." | 2-225 |
| | The "ATRTNx Temperature Monitor Return" section was updated with information about grounding and floating the pin. | 2-226 |
| | The following text was deleted from the "VREF I/O Voltage Reference" section: (all digital I/O). | 2-225 |
| | The "NCAP Negative Capacitor" section and "PCAP Positive Capacitor" section were updated to include information about the type of capacitor that is required to connect the two. | 2-228 |
| | 1 μ F was changed to 100 pF in the "XTAL1 Crystal Oscillator Circuit Input". | 2-228 |
| | The "Programming" section was updated to include information about V_{CCOSC} . | 2-229 |
| | The VMV pins have now been tied internally with the V_{CCI} pins. | N/A |
| | The AFS090 "108-Pin QFN" table was updated. | 3-2 |
| | The AFS090 and AFS250 devices were updated in the "108-Pin QFN" table. | 3-2 |
| | The AFS250 device was updated in the "208-Pin PQFP" table. | 3-8 |
| | The AFS600 device was updated in the "208-Pin PQFP" table. | 3-8 |
| | The AFS090, AFS250, AFS600, and AFS1500 devices were updated in the "256-Pin FBGA" table. | 3-12 |
| | The AFS600 and AFS1500 devices were updated in the "484-Pin FBGA" table. | 3-20 |
| Advance v0.7 (January 2007) | The AFS600 device was updated in the "676-Pin FBGA" table. | 3-28 |
| | The AFS1500 digital I/O count was updated in the "Fusion Family" table. | I |
| | The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double-Ended (Analog)" table. | II |
| Advance v0.6 (October 2006) | The second paragraph of the "PLL Macro" section was updated to include information about POWERDOWN. | 2-30 |
| | The description for bit 0 was updated in Table 2-17 · RTC Control/Status Register. | 2-38 |
| | 3.9 was changed to 7.8 in the "Crystal Oscillator (Xtal Osc)" section. | 2-40. |
| | All function descriptions in Table 2-18 · Signals for VRPSM Macro. | 2-42 |
| | In Table 2-19 · Flash Memory Block Pin Names, the RD[31:0] description was updated. | 2-43 |
| | The "RESET" section was updated. | 2-61 |
| | The "RESET" section was updated. | 2-64 |
| | Table 2-35 · FIFO was updated. | 2-79 |
| | The VAREF function description was updated in Table 2-36 · Analog Block Pin Description. | 2-82 |
| | The "Voltage Monitor" section was updated to include information about low power mode and sleep mode. | 2-86 |
| | The text in the "Current Monitor" section was changed from 2 mV to 1 mV. | 2-90 |
| | The "Gate Driver" section was updated to include information about forcing 1 V on the drain. | 2-94 |

| Revision | Changes | Table |
|--|--|-------|
| Advance v0.6 (continued) | The "Analog-to-Digital Converter Block" section was updated with the following statement: "All results are MSB justified in the ADC." | 2-99 |
| | The information about the ADCSTART signal was updated in the "ADC Description" section. | 2-102 |
| | Table 2-46 · Analog Channel Specifications was updated. | 2-118 |
| | Table 2-47 · ADC Characteristics in Direct Input Mode was updated. | 2-121 |
| | Table 2-51 · ACM Address Decode Table for Analog Quad was updated. | 2-127 |
| | In Table 2-53 · Analog Quad ACM Byte Assignment, the Function and Default Setting for Bit 6 in Byte 3 was updated. | 2-130 |
| | The "Introduction" section was updated to include information about digital inputs, outputs, and bbufs. | 2-133 |
| | In Table 2-69 · Fusion Pro I/O Features, the programmable delay descriptions were updated for the following features: Single-ended receiver Voltage-referenced differential receiver LVDS/LVPECL differential receiver features | 2-137 |
| | The "User I/O Naming Convention" section was updated to include "V" and "z" descriptions | 2-159 |
| | The "VCC33PMP Analog Power Supply (3.3 V)" section was updated to include information about avoiding high current draw. | 2-224 |
| | The "VCCNVM Flash Memory Block Power Supply (1.5 V)" section was updated to include information about avoiding high current draw. | 2-224 |
| | The "VMVx I/O Supply Voltage (quiet)" section was updated to include this statement: VMV and VCCI must be connected to the same power supply and VCCI pins within a given I/O bank. | 2-185 |
| | The "PUB Push Button" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| | The "PTBASE Pass Transistor Base" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| The "PTM Pass Transistor Emitter" section was updated to include information about leaving the pin floating if it is not used. | 2-228 | |
| The heading was incorrect in the "208-Pin PQFP" table. It should be AFS250 and not AFS090. | 3-8 | |

| Revision | Changes | Table |
|---|---|-------|
| Advance v0.5 (June 2006) | The low power modes of operation were updated and clarified. | N/A |
| | The AFS1500 digital I/O count was updated in Table 1 • Fusion Family . | i |
| | The AFS1500 digital I/O count was updated in the " Package I/Os: Single-/Double-Ended (Analog) " table. | ii |
| | The " Voltage Regulator Power Supply Monitor (VRPSM) " was updated. | 2-36 |
| | Figure 2-45 • FlashROM Timing Diagram was updated. | 2-53 |
| | The " 256-Pin FBGA " table for the AFS1500 is new. | 3-12 |
| Advance v0.4 (April 2006) | The G was moved in the " Product Ordering Codes " section. | III |
| Advance v0.3 (April 2006) | The " Features and Benefits " section was updated. | I |
| | The " Fusion Family " table was updated. | I |
| | The " Package I/Os: Single-/Double-Ended (Analog) " table was updated. | II |
| | The " Product Ordering Codes " table was updated. | III |
| | The " Temperature Grade Offerings " table was updated. | IV |
| | The " General Description " section was updated to include ARM information. | 1-1 |
| | Figure 2-46 • FlashROM Timing Diagram was updated. | 2-58 |
| | The " FlashROM " section was updated. | 2-57 |
| | The " RESET " section was updated. | 2-61 |
| | The " RESET " section was updated. | 2-64 |
| | Figure 2-27 • Real-Time Counter System was updated. | 2-35 |
| | Table 2-19 • Flash Memory Block Pin Names was updated. | 2-43 |
| | Figure 2-33 • Flash Memory Block Diagram was updated to include AUX block information. | 2-45 |
| | Figure 2-34 • Flash Memory Block Organization was updated to include AUX block information. | 2-46 |
| | The note in the " Program Operation " section was updated. | 2-48 |
| | Figure 2-76 • Gate Driver Example was updated. | 2-95 |
| | The " Analog Quad ACM Description " section was updated. | 2-130 |
| | Information about the maximum pad input frequency was added to the " Gate Driver " section. | 2-94 |
| | Figure 2-65 • Analog Block Macro was updated. | 2-81 |
| | Figure 2-65 • Analog Block Macro was updated. | 2-81 |
| | The " Analog Quad " section was updated. | 2-84 |
| | The " Voltage Monitor " section was updated. | 2-86 |
| The " Direct Digital Input " section was updated. | 2-89 | |
| The " Current Monitor " section was updated. | 2-90 | |
| Information about the maximum pad input frequency was added to the " Gate Driver " section. | 2-94 | |

| Revision | Changes | Table |
|--|--|-------|
| Advance v0.3 (continued) | The "Temperature Monitor" section was updated. | 2-96 |
| | EQ 2 is new. | 2-103 |
| | The "ADC Description" section was updated. | 2-102 |
| | Figure 2-16 • Fusion Clocking Options was updated. | 2-20 |
| | Table 2-46 • Analog Channel Specifications was updated. | 2-118 |
| | The notes in Table 2-72 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities were updated. | 2-144 |
| | The "Simultaneously Switching Outputs and PCB Layout" section is new. | 2-149 |
| | LVPECL and LVDS were updated in Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications. | 2-157 |
| | LVPECL and LVDS were updated in Table 2-82 • Fusion Pro I/O Attributes vs. I/O Standard Applications. | 2-158 |
| | The "Timing Model" was updated. | 2-161 |
| | All voltage-referenced Minimum and Maximum DC Input and Output Level tables were updated. | N/A |
| | All Timing Characteristic tables were updated | N/A |
| | Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated. | 2-165 |
| | Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated. | 2-134 |
| | Table 2-93 • I/O Output Buffer Maximum Resistances ¹ was updated. | 2-171 |
| | The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet. | 2-211 |
| | The "CoreMP7 and Cortex-M1 Software Tools" section is new. | 2-257 |
| | Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated. | 2-165 |
| | Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated. | 2-134 |
| | Table 2-93 • I/O Output Buffer Maximum Resistances ¹ was updated. | 2-171 |
| | The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet. | 2-211 |
| | The "108-Pin QFN" table for the AFS090 device is new. | 3-2 |
| | The "180-Pin QFN" table for the AFS090 device is new. | 3-4 |
| The "208-Pin PQFP" table for the AFS090 device is new. | 3-8 | |
| The "256-Pin FBGA" table for the AFS090 device is new. | 3-12 | |
| The "256-Pin FBGA" table for the AFS250 device is new. | 3-12 | |

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "Fusion Device Status" table, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.

