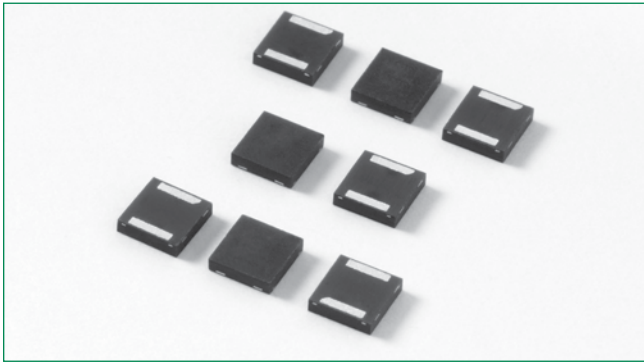


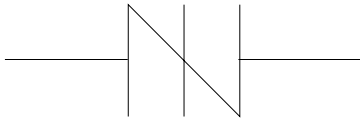
**Q2L Series - 3.3x3.3 QFN**



**Agency Approvals**

Agency	Agency File Number
	E133083

**Schematic Symbol**



**Additional Information**



**Datasheet**



**Resources**



**Samples**

**Description**

Q2L Series 3.3x3.3 QFN are low capacitance SIDACtor® devices designed to protect high density broadband equipment from damaging overvoltage transients.

The series provides a low profile, chip scale surface mount solution that enables broadband equipment to comply with global regulatory standards while limiting the impact to broadband signals and board space.

**Features and Benefits**

- Low profile
- Small footprint
- Low capacitance
- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A.01
- Recognized to UL 497B as an Isolated Loop Circuit Protector

**Applicable Global Standards**

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5
- YD/T 1082
- YD/T 993
- YD/T 950

**Electrical Characteristics**

Part Number	Marking	$V_{DRM}$ @ $I_{DRM} = 5\mu A$	$V_S$ @ $100V/\mu s$	$I_H$	$I_S$	$I_T$	$V_T @ I_T = 2.2$ Amps	Capacitance @ 1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0080Q22CLRP	P-8C	6	25	50	800	2.2	5	35	75
P0300Q22CLRP	P03C	25	40	50	800	2.2	5	25	45
P0640Q22CLRP	P06C	58	77	150	800	2.2	5	55	85
P0720Q22CLRP	P07C	65	88	150	800	2.2	5	50	75
P0900Q22CLRP	P09C	75	98	150	800	2.2	5	45	70
P1100Q22CLRP	P11C	90	130	150	800	2.2	5	45	70
P1200Q22CLRP	P12C	100	130	150	800	2.2	5	45	70
P1300Q22CLRP	P13C	120	160	150	800	2.2	5	40	60
P1500Q22CLRP	P15C	140	180	150	800	2.2	5	35	55
P1800Q22CLRP	P18C	170	220	150	800	2.2	5	35	50
P2000Q22CLRP	P20C	180	220	150	800	2.2	5	30	50
P2300Q22CLRP	P23C	190	260	150	800	2.2	5	30	50
P2500Q22CLRP	P25C	230	290	150	800	2.2	5	30	50
P2600Q22CLRP	P26C	220	300	150	800	2.2	5	30	45
P3100Q22CLRP	P31C	275	350	150	800	2.2	5	30	45
P3500Q22CLRP	P35C	320	400	150	800	2.2	5	25	40
P4500Q22CLRP	P45C	400	530	150	800	2.2	5	25	45

**Notes:**

- Absolute maximum ratings measured at  $T_A = 25^\circ C$  (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).


**Surge Ratings**

Series	2x10 <sup>1</sup> 2x10 <sup>2</sup>	8x20 <sup>1</sup> 1.2x50 <sup>2</sup>	10x160 <sup>1</sup> 10x160 <sup>2</sup>	10x560 <sup>1</sup> 10x560 <sup>2</sup>	10x1000 <sup>1</sup> 10x1000 <sup>2</sup>	5x310 <sup>1</sup> 10x700 <sup>2</sup>	I <sub>TSM</sub> 50/60 Hz	di/dt
	A min	A min	A min	A min	A min	A min	A min	A/μs max
C	500	400	200	150	100	200 <sup>3</sup>	30	500

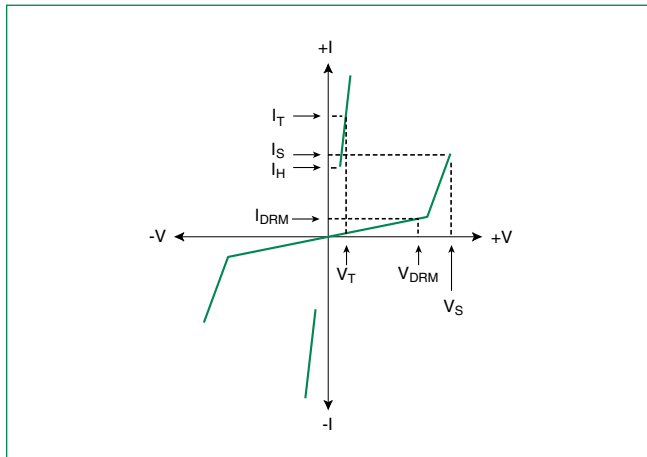
**Notes:**

1. Current waveform in μs
  2. Voltage waveform in μs
  3. For surge rating of P4500Q22CLRP 10x700μs min=150A & typical=180A
- Peak pulse current rating (I<sub>pp</sub>) is repetitive and guaranteed for the life of the product.
  - I<sub>pp</sub> ratings applicable over temperature range of -40°C to +85°C
  - The device must initially be in thermal equilibrium with -40°C ≤ T<sub>j</sub> ≤ +150°C

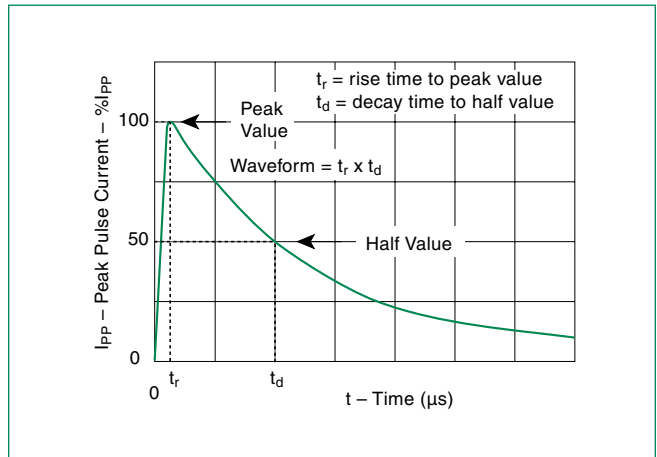
**Thermal Considerations**

Package	Symbol	Parameter	Value	Unit
3.3 x 3.3 QFN 	T <sub>J</sub>	Operating Junction Temperature Range	-40 to +150	°C
	T <sub>S</sub>	Storage Temperature Range	-65 to +150	°C
	R <sub>θJA</sub>	Thermal Resistance: Junction to Ambient	120	°C/W

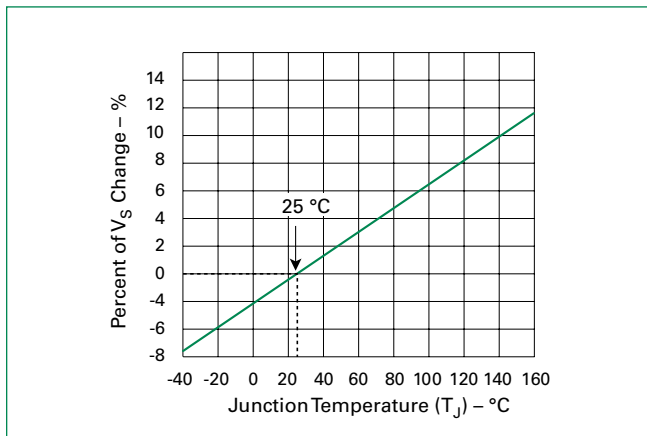
**V-I Characteristics**



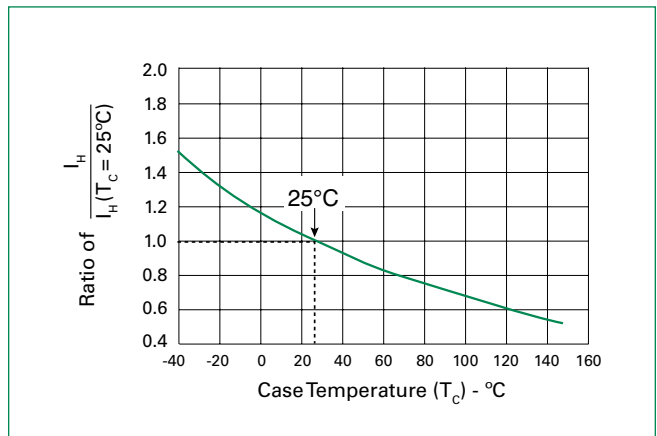
**t<sub>r</sub> x t<sub>d</sub> Pulse Waveform**



**Normalized V<sub>S</sub> Change vs. Junction Temperature**

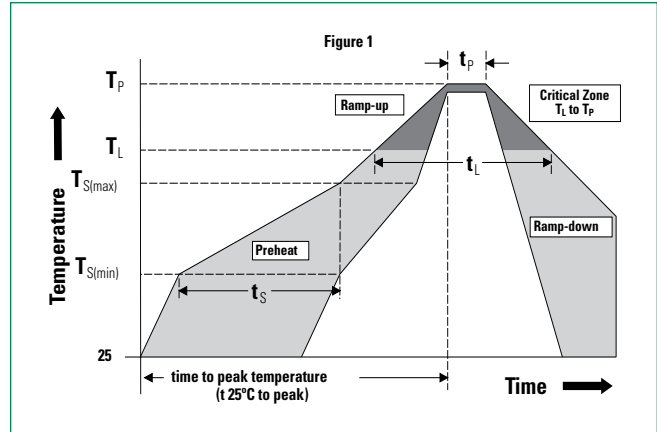


**Normalized DC Holding Current vs. Case Temperature**



**Soldering Parameters**

<b>Reflow Condition</b>		Pb-Free assembly
<b>Pre Heat</b>	- Temperature Min ( $T_{s(min)}$ )	+150°C
	- Temperature Max ( $T_{s(max)}$ )	+200°C
	- Time (Min to Max) ( $t_s$ )	60-180 secs.
<b>Average ramp up rate (Liquidus Temp (<math>T_L</math>) to peak)</b>		3°C/sec. Max.
<b><math>T_{s(max)}</math> to <math>T_L</math> - Ramp-up Rate</b>		3°C/sec. Max.
<b>Reflow</b>	- Temperature ( $T_L$ ) (Liquidus)	+217°C
	- Temperature ( $t_L$ )	60-150 secs.
<b>Peak Temp (<math>T_p</math>)</b>		+260(+0/-5)°C
<b>Time within 5°C of actual Peak Temp (<math>t_p</math>)</b>		30 secs. Max.
<b>Ramp-down Rate</b>		6°C/sec. Max.
<b>Time 25°C to Peak Temp (<math>T_p</math>)</b>		8 min. Max.
<b>Do not exceed</b>		+260°C



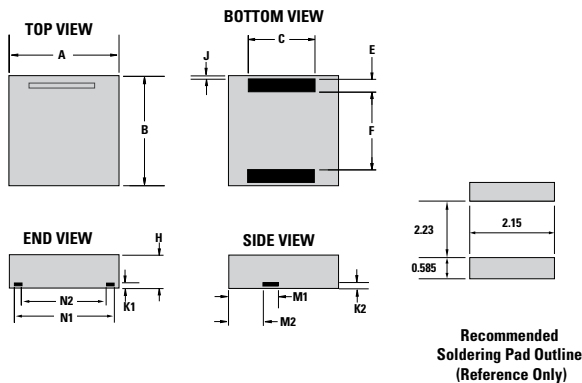
**Physical Specifications**

<b>Lead Material</b>	Copper Alloy
<b>Terminal Finish</b>	100% Matte-Tin Plated
<b>Body Material</b>	UL recognized epoxy meeting flammability classification 94V-0

**Environmental Specifications**

<b>High Temp Voltage Blocking</b>	80% Rated $V_{DRM}$ ( $V_{AC Peak}$ ) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
<b>Temp Cycling</b>	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A-104
<b>Biased Temp &amp; Humidity</b>	52 $V_{DC}$ (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
<b>High Temp Storage</b>	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
<b>Low Temp Storage</b>	-65°C, 1008 hrs.
<b>Thermal Shock</b>	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
<b>Resistance to Solder Heat</b>	+260°C, 30 secs. MIL-STD-750 (Method 2031)
<b>Moisture Sensitivity Level</b>	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

**Dimensions — 3.3x3.3 QFN**



Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
<b>A</b>	0.126	0.134	3.200	3.400
<b>B</b>	0.126	0.134	3.200	3.400
<b>C</b>	0.075	0.083	1.900	2.100
<b>E</b>	0.011	0.019	0.285	0.485
<b>F</b>	0.088	0.096	2.230	2.430
<b>H</b>	0.035	0.043	0.900	1.100
<b>J</b>	0.000	0.008	0.000	0.200
<b>K1</b>	0.004	0.012	0.100	0.300
<b>K2</b>	0.004	0.012	0.100	0.300
<b>M1</b>	0.063	0.071	1.610	1.810
<b>M2</b>	0.045	0.053	1.153	1.353
<b>N1</b>	0.095	0.103	2.420	2.620
<b>N2</b>	0.082	0.090	2.080	2.280