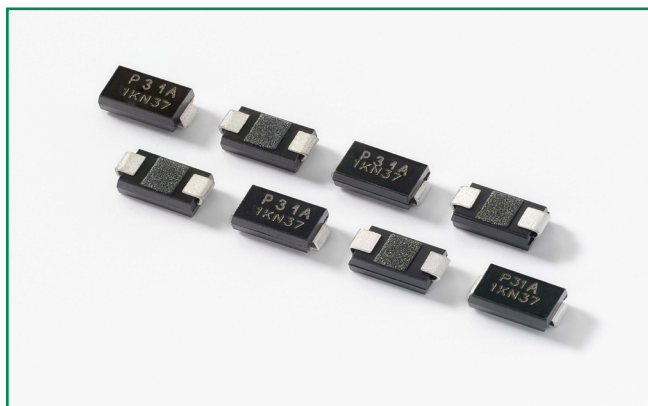



SIDACtor® Series - SMA



Agency Approvals

Agency	Agency File Number
	E133083

Applicable Global Standards

- TIA-968-A*
- TIA-968-B*
- ITU K.20/21/45 Enhanced Level*
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

* Line impedance required to pass operationally

Electrical Characteristics

Part Number	Marking	V_{DRM}	V_S	I_H	I_S	I_T	V_T	Capacitance	
		@ $I_{DRM}=5\mu A$ V min	@ 100V/ μs V max	mA min	mA max	A max	@ $I_T=2.2$ Amps V max	pF min	pF max
P0080S1ALRP	P-8A	6	25	50	800	2.2	4	25	35
P0220S1ALRP	P22A	15	32	50	800	2.2	4	10	30
P0300S1ALRP	P03A	25	40	50	800	2.2	4	10	30
P0640S1ALRP	P06A	58	77	150	800	2.2	4	10	30
P1800S1ALRP	P18A	170	220	150	800	2.2	4	10	30
P2300S1ALRP	P23A	190	260	150	800	2.2	4	10	30
P2600S1ALRP	P26A	220	300	150	800	2.2	4	10	30
P3100S1ALRP	P31A	275	350	150	800	2.2	4	10	30
P3500S1ALRP	P35A	320	400	150	800	2.2	4	10	30
P0080S1BLRP	P-8B	6	25	50	800	2.2	4	20	35
P0220S1BLRP	P22B	15	32	50	800	2.2	4	10	30
P0300S1BLRP	P03B	25	40	50	800	2.2	4	10	30
P0640S1BLRP	P06B	58	77	120	800	2.2	4	10	30
P1800S1BLRP	P18B	170	220	120	800	2.2	4	10	30
P2300S1BLRP	P23B	190	260	120	800	2.2	4	10	30
P2600S1BLRP	P26B	220	300	120	800	2.2	4	10	30
P3100S1BLRP	P31B	275	350	120	800	2.2	4	10	30
P3500S1BLRP	P35B	320	400	120	800	2.2	4	10	30

Notes:

- Absolute maximum ratings measured at $T_c = 25^\circ C$ (unless otherwise noted).

- Components are bi-directional (unless otherwise noted).

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Specifications are subject to change without notice.

Revised: 02/23/17

Description

SIDACtor® SMA Thyristors Series are designed to protect baseband equipment such as phones, faxes, modems, line cards, CPE and DSL from damaging overvoltage transients.

The series provides a surface mount solution that enables equipment to comply with global regulatory standards.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- RoHS Compliant and Halogen-Free
- Fails short circuit when surged in excess of ratings
- Low capacitance
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Schematic Symbol

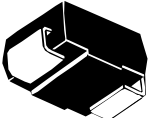


Surge Ratings

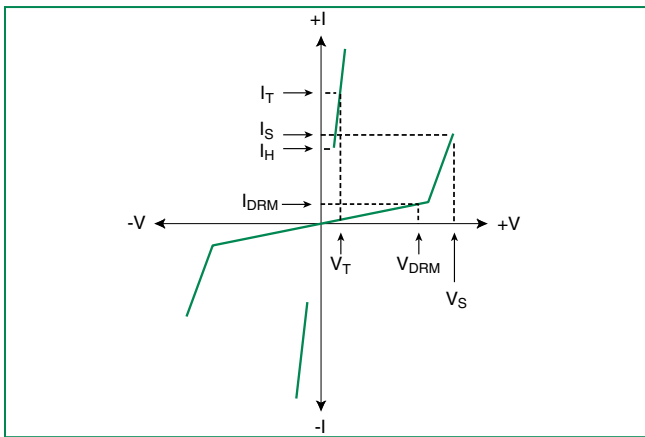
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 ¹	2/10 ¹	8/20 ¹	10/160 ¹	10/560 ¹	5/320 ¹	10/360 ¹	10/1000 ¹	5/310 ¹		
	0.5/700 ²	2/10 ²	1.2/50 ²	10/160 ²	10/560 ²	9/720 ²	10/360 ²	10/1000 ²	10/700 ²		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	Amps/μs max
A	20	150	150	90	50	75	75	50	75	20	500
B	-	250	250	90	60	75	75	55	75	25	500

Notes:
 1 Current waveform in μs - Peak pulse current rating (I_{pp}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
 2 Voltage waveform in μs - I_{pp} ratings applicable over temperature range of -40°C to +85°C
 - The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

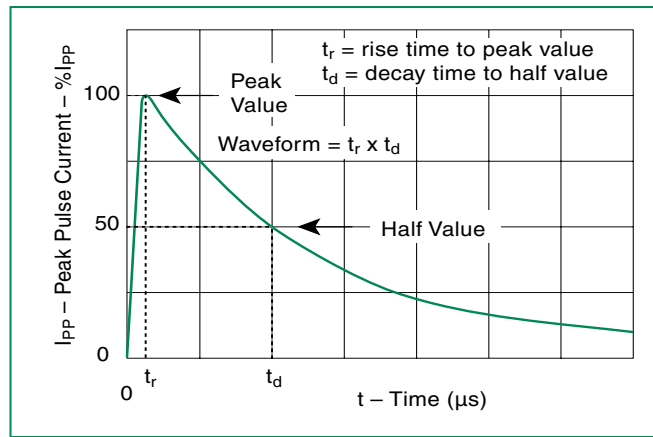
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
 DO-214AC	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	°C/W

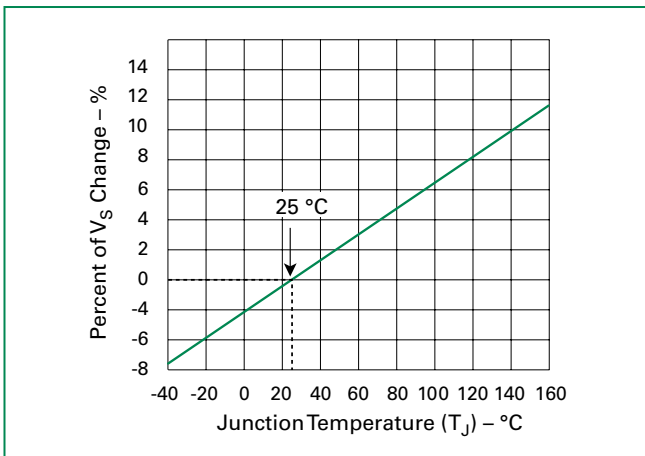
V-I Characteristics



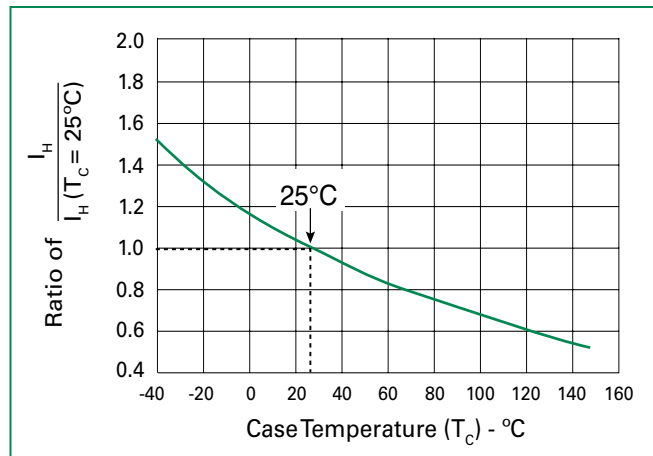
$t_r \times t_d$ Pulse Waveform



Normalized V_S Change vs. Junction Temperature

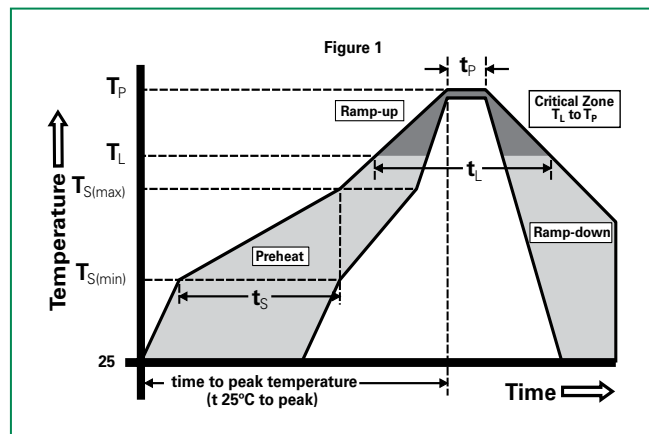


Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	- Temperature Min ($T_{s(min)}$)	+150°C
	- Temperature Max ($T_{s(max)}$)	+200°C
	- Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{s(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	- Temperature (T_L) (Liquidus)	+217°C
	- Temperature (t_L)	60-150 secs.
Peak Temp (T_p)		+260(+0/-5)°C
Time within 5°C of actual PeakTemp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_p)		8 min. Max.
Do not exceed		+260°C



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} ($V_{AC, Peak}$) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Additional Information



Datasheet



Resources



Samples