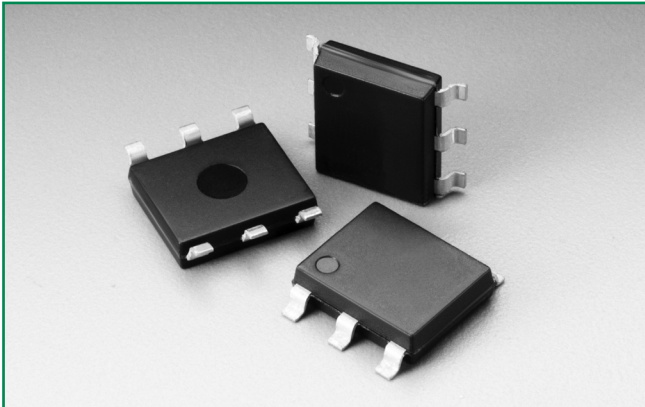


MC Multiport Series - MS-013



Description

The MC Multiport Series MS-013 are low capacitance SIDACtor® thyristors designed to protect broadband equipment from damaging overvoltage transients.

The series provides a dual port surface mount solution that enables equipment to comply with various global regulatory standards while limiting the impact to broadband signals.

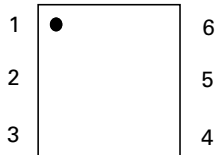
Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Two-pair protection
- 40% lower capacitance than our Baseband Protectors, for applications that demand greater signal integrity
- Replaces four discrete components
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

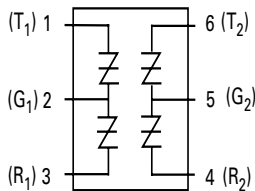
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level
- ITU K.20/21/45 Basic Level
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950
- GR 1089 Inter-building

Electrical Characteristics

Part Number	Marking	V_{DRM}	V_S	V_{DRM}	V_S	I_H	I_S	I_T	V_T	Capacitance
		@ $I_{DRM}=5\mu A$	@ 100V/ μs	@ $I_{DRM}=5\mu A$	@ 100V/ μs				@ $I_T=2.2$ Amps	
		V	V	V	V				V max	
		Pins 1-2, 3-2, 4-5, 6-5		Pins 1-3, 4-6		mA min	mA max	A max		
P0084UCMCLxx	P0084UCMC	6	25	12	50	50	800	2.2	8	See Capacitance Values Table
P0304UCMCLxx	P0304UCMC	25	40	50	80	50	800	2.2	8	
P0644UCMCLxx	P0644UCMC	58	77	116	154	150	800	2.2	8	
P0724UCMCLxx	P0724UCMC	65	88	130	176	150	800	2.2	8	
P0904UCMCLxx	P0904UCMC	75	98	150	196	150	800	2.2	8	
P1104UCMCLxx	P1104UCMC	90	130	180	260	150	800	2.2	8	
P1304UCMCLxx	P1304UCMC	120	160	240	320	150	800	2.2	8	

Notes:
 - Absolute maximum ratings measured at $T_A = 25^\circ C$ (unless otherwise noted).
 - Components are bi-directional.
 - **XX** Part Number Suffix: **TP** (Tube Pack) or **RP** (Reel Pack).

Table continues on next page.

Electrical Characteristics (continued)

Part Number	Marking	V_{DRM} @ $I_{DRM}=5\mu A$	V_S @ 100V/ μs	V_{DRM} @ $I_{DRM}=5\mu A$	V_S @ 100V/ μs	I_H	I_S	I_T	V_T @ $I_T=2.2$ Amps	Capacitance
		V	V	V	V	mA min	mA max	A max	V max	
		Pins 1-2, 3-2, 4-5, 6-5		Pins 1-3, 4-6						
P1504UCMCLxx	P1504UCMC	140	180	280	360	150	800	2.2	8	See Capacitance Values Table
P1804UCMCLxx	P1804UCMC	170	220	340	440	150	800	2.2	8	
P2304UCMCLxx	P2304UCMC	190	260	380	520	150	800	2.2	8	
P2604UCMCLxx	P2604UCMC	220	300	440	600	150	800	2.2	8	
P3104UCMCLxx	P3104UCMC	275	350	550	700	150	800	2.2	8	
P3504UCMCLxx	P3504UCMC	320	400	600	800	150	800	2.2	8	

Notes:
 - Absolute maximum ratings measured at $T_A=25^\circ C$ (unless otherwise noted).
 - Components are bi-directional.
 - **XX** Part Number Suffix: **TP** (Tube Pack) or **RP** (Reel Pack).

Capacitance Values

Part Number	pF Pin 1-2 / 3-2 (4-5 / 6-5) Tip-Ground, Ring-Ground		pF Pin 1-3 (4-6) Tip-Ring	
	MIN	MAX	MIN	MAX
P0084UCMCLxx	35	75	20	45
P0304UCMCLxx	25	45	10	25
P0644UCMCLxx	55	85	30	50
P0724UCMCLxx	50	75	25	45
P0904UCMCLxx	45	70	25	40
P1104UCMCLxx	45	70	25	40
P1304UCMCLxx	40	60	20	35
P1504UCMCLxx	35	55	20	35
P1804UCMCLxx	35	50	15	30
P2304UCMCLxx	30	50	15	30
P2604UCMCLxx	30	45	15	30
P3104UCMCLxx	30	45	15	25
P3504UCMCLxx	25	40	15	25

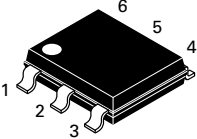
Note: Off-state capacitance (C_o) is measured at 1 MHz with a 2 V bias.

Surge Ratings

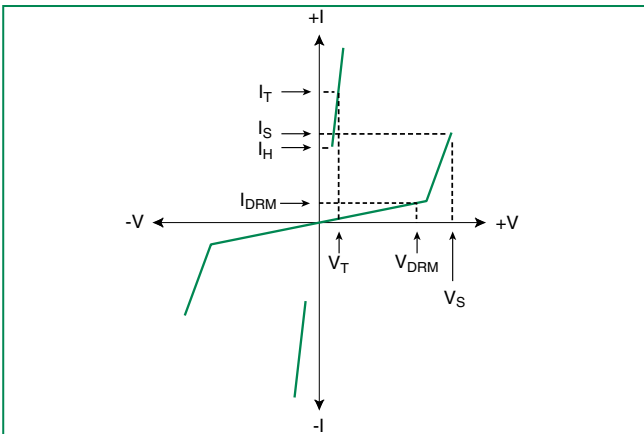
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 ¹ 0.5/700 ²	2/10 ¹ 2/10 ²	8/20 ¹ 1.2/50 ²	10/160 ¹ 10/160 ²	10/560 ¹ 10/560 ²	5/320 ¹ 9/720 ²	10/360 ¹ 10/360 ²	10/1000 ¹ 10/1000 ²	5/310 ¹ 10/700 ²		
	A min	A min	A min	A min	A min	A min	A min	A min	A min		
C	50	500	400	200	150	200	175	100	200	30	500

Notes:
 1 Current waveform in μs
 2 Voltage waveform in μs
 - Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
 - I_{PP} ratings applicable over temperature range of $-40^\circ C$ to $+85^\circ C$
 - The component must initially be in thermal equilibrium with $-40^\circ C \leq T_j \leq +150^\circ C$

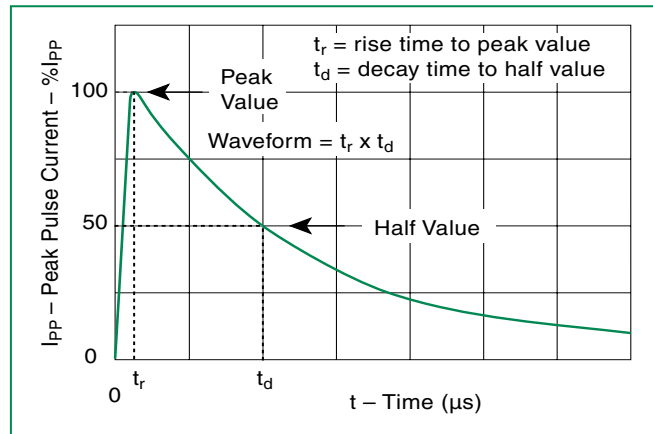
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

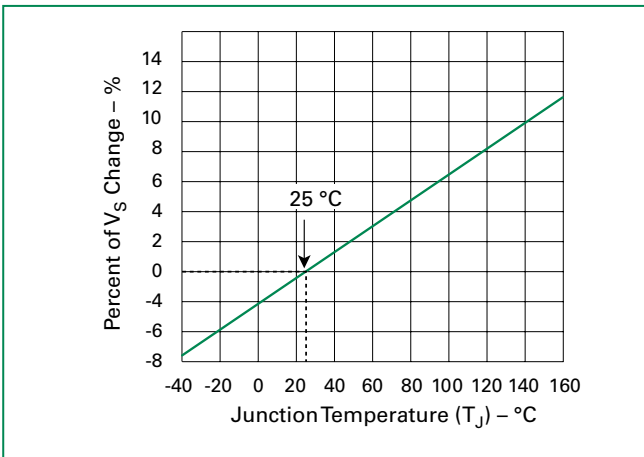
V-I Characteristics



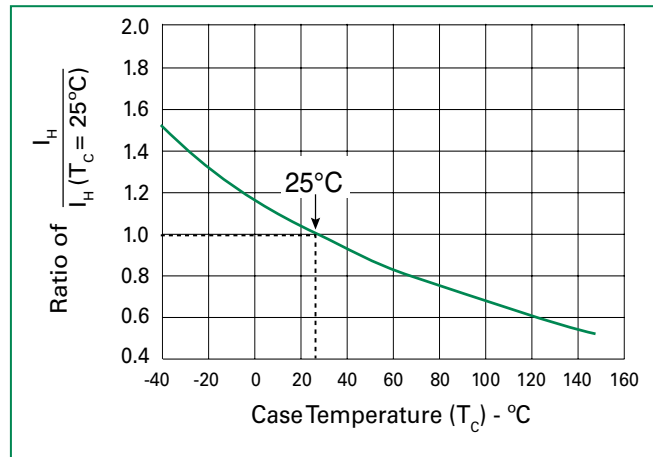
$t_r \times t_d$ Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



Additional Information



Datasheet



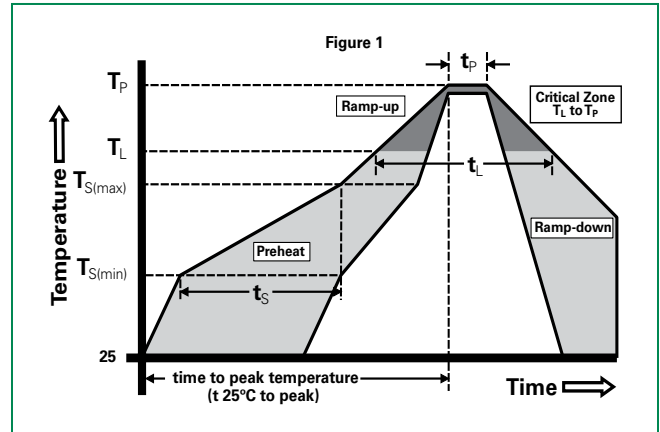
Resources



Samples

Soldering Parameters

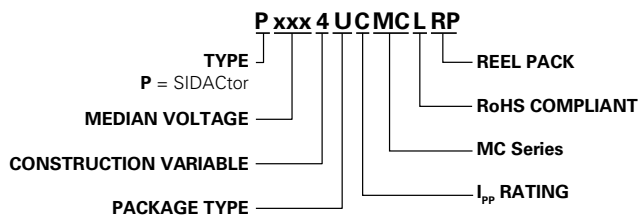
Reflow Condition	Pb-Free assembly (see Fig. 1)	
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)	3°C/sec. Max.	
$T_{s(max)}$ to T_L - Ramp-up Rate	3°C/sec. Max.	
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_p)	+260(+0/-5)°C	
Time within 5°C of actual PeakTemp (t_p)	30 secs. Max.	
Ramp-down Rate	6°C/sec. Max.	
Time 25°C to Peak Temp (T_p)	8 min. Max.	
Do not exceed	+260°C	



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Part Numbering



Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} ($V_{AC Peak}$) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Marking

