UM11385

P3A9606JK-EVB evaluation board

Rev. 1.0 — 21 June 2020 **User manual**

Document information

Information	Content
Keywords	P3A9606JK, Level Shifter, Level Translator, P3A9606JK-EVB evaluation board
Abstract	The P3A9606JK is a 2-bit, dual supply translating transceiver with auto direction sensing that enables bidirectional voltage level translation. This user manual describes the setup, configuration and operation of the P3A9606JK-EVB evaluation board.

Revision history

Rev	Date	Description
v.1.0	20210621	Initial version

Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

1 Introduction

The P3A9606JK is a 2-bit, dual supply translating transceiver with auto direction sensing that enables bidirectional voltage level translation. It features two 1-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins (VCC(A) and VCC(B)). VCC(A) can be supplied at any voltage between 0.7 V and 1.98 V and VCC(B) can be supplied at any voltage between 0.7 V and 1.98 V, making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V and 1.8 V). VCC(A) must be ≤ VCC(B) for minimum current consumption.

P3A9606JK can be used for both Open Drain as well as push-pull application which allows for level translation applications using SPMI, I2C and SPI protocols (see datasheet application section).

This document is intended to help the users to quickly setup, configure and operate the P3A9606JK-EVB evaluation board in the users' hardware platform.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for P3A9606JK-EVB evaluation board is at https://www.nxp.com/P3A9606JK-EVB.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting to know the hardware

3.1 Kit overview

P3A9606JK can be used as a stand-alone level shifter when a CERES is not available for evaluation and testing. The user can manually connect the signals to be shifted to port A1/A0 and B1/B0 of the P3A9606JK. External VCCA/VCCB can be manually selected and connected to the evaluation board.

As default, P3A9606JK-EVB evaluation board is configured (with jumper settings) to be mated to a CERES motherboard serial expansion bus as a level shifter on the SPMI bus. If needed, P3A9606JK-EVB evaluation board can be bypassed using jumper settings to remove it from the SPMI bus.

The evaluation boards are shipped with a P3A9606JK soldered on as U1; a socket (U2 on the schematic) can be used in place of U1 to allow the user the flexibility of repeatedly replacing P3A9606JK multiple times. U1 and U2 share the same PCB footprint, therefore, U1 must be removed first before U2 as a socket can be installed.

3.2 Connectors and jumpers

Please refer to Figure 1 to find the location of connectors and jumpers on the evaluation board.

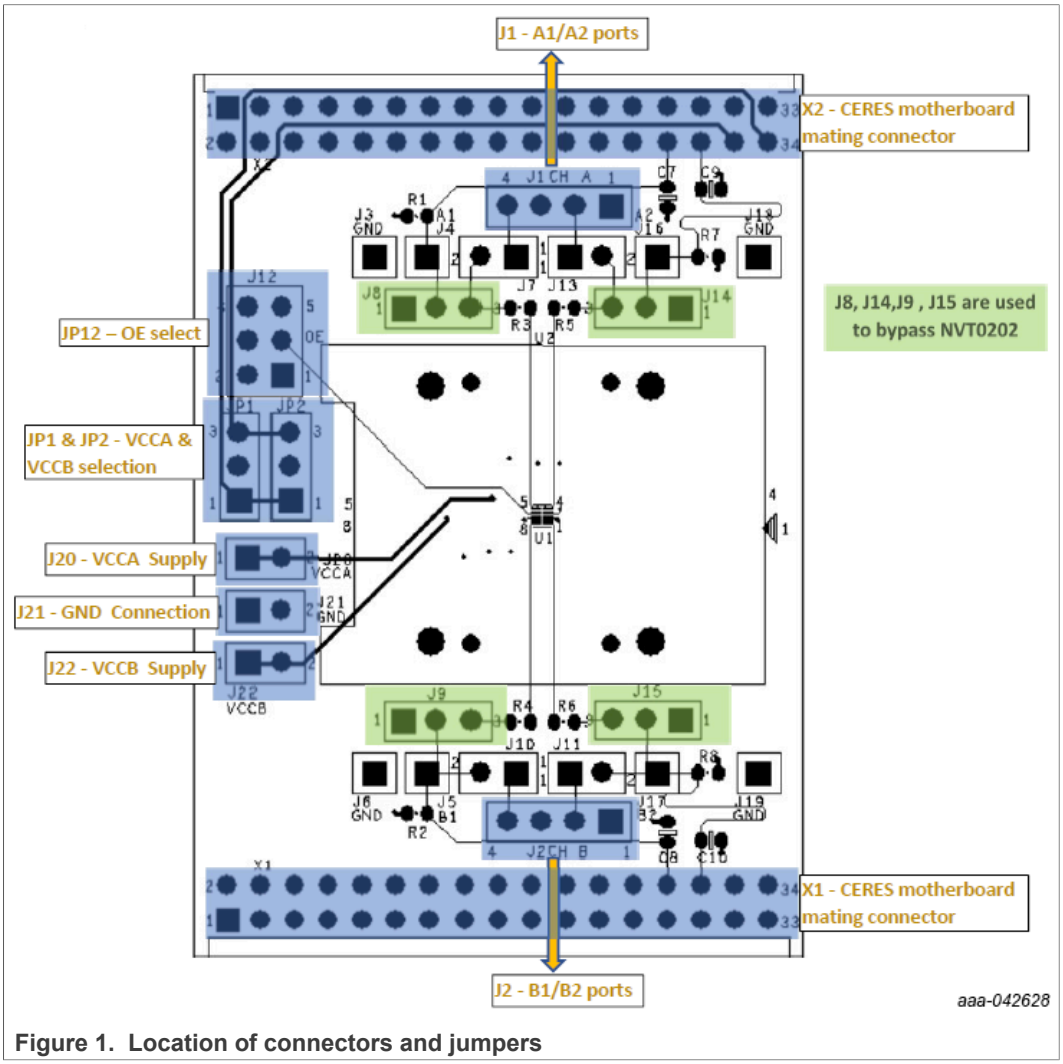

Figure 1. Location of connectors and jumpers

3.3 Default jumper settings (CERES motherboard SPMI bus option)

As default, P3A9606JK-EVB evaluation board is configured to be mated to a CERES motherboard serial expansion bus as a level shifter on the SPMI bus as shown in Table 1.

Table 1. Default jumper settings

Header	Jumper on	Comment
J8	2-3	Select P3A9606JK port A1
J9	2-3	Select P3A9606JK port B1
J14	2-3	Select P3A9606JK port A2
J15	2-3	Select P3A9606JK port B2
J12	1-3	OE is connected to VCCA

Table 1. Default jumper settings...*continued*

Header	Jumper on	Comment
JP2	Open	VCCA is supplied from external, J20
JP1	Open	VCCB is supplied from external, J22
J7	Open	Not used, CERES motherboard is on port A1
J10	Open	Not used, CERES motherboard is on port B1
J13	Open	Not used, CERES motherboard is on port B1
J11	Open	Not used, CERES motherboard is on port B2

3.4 Non-CERES motherboard jumper settings

P3A9606JK can be used as a stand-alone level shifter when a CERES is not available for evaluation and testing. The user can manually connect the signals to be shifted to port A1/A2 and B1/B2 of the P3A9606JK through jumpers J7, J13, J10, J11 as shown in Table 2.

Table 2. Non-CERES motherboard jumper settings

Header	Jumper on	Comment
J8	2-3	Select P3A9606JK port A1
J9	2-3	Select P3A9606JK port B1
J14	2-3	Select P3A9606JK port A2
J15	2-3	Select P3A9606JK port B2
J12	1-3	OE is connected to VCCA
JP2	Open	VCCA is supplied from external, J20
JP1	Open	VCCB is supplied from external, J22
J7	1-2	Port A1 of signal to be shifted
J10	1-2	Port B1 of signal to be shifted
J13	1-2	Port A2 of signal to be shifted
J11	1-2	Port B2 of signal to be shifted

3.5 P3A9606JK bypass

P3A9606JK can be electrically removed and bypassed from the bus at any time, such as during debugging a level shifting issue. Once bypassed using the jumper settings from Table 3, signal on A1 is directly connected to B1 and signal on A2 is directly connected to B2.

Table 3. Bypass jumper settings

Header	Jumper on	Comment
J8	1-2	Select P3A9606JK port A1
J9	1-2	Select P3A9606JK port B1
J14	1-2	Select P3A9606JK port A2
J15	1-2	Select P3A9606JK port B2

3.6 Test points

There are a number of test points to allow the user to monitor and observe signals coming in and out of P3A9606JK.

Table 4. Test points

Signal	Test point	Alternative test point
A1	J4	J1 pin 4
A2	J13	J1 pin 2
B1	J10	J2 pin 4
B2	J11	J2 pin 2

4 Errata list

Table 5. Errata list

Date	Errata Description	Impact to evaluation board	Solution
-	None	None	None

5 Legal information

5.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

5.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

5.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures