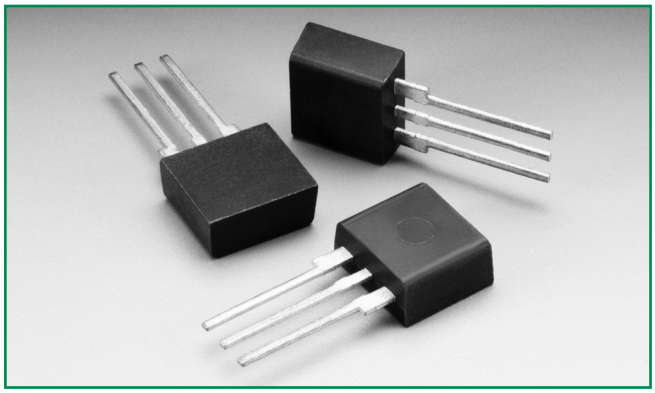
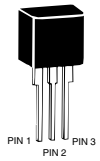
SIDACtor® Balanced Series - Modified TO-220



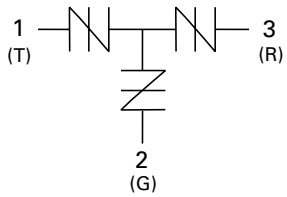
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

The SIDACtor® Balanced Series are designed to protect baseband equipment from damaging overvoltage transients. The patented "Y" configuration also ensures balanced overvoltage protection that prevents a longitudinal to differential conversion.

The series provides a single port through-hole solution that enables voice through DS-1 equipment to comply with various global requlatory standards.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Low capacitance
- Balanced overvoltage protection
- Single port protection
- Custom lead forms available
- RoHS Compliant and Lead-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level*
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A/B-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T@I_T= 2.2 Amps	Capacitance
		V min	V max	V min	V max	mA min	mA max	A max	V max	
		Pins 1-2, 3-2		Pins 1-3						
P1553AALxx	P1553AA	130	180	130	180	150	800	2.2	8	See Capacitance Values table
P1803AALxx	P1803AA	150	210	150	210	150	800	2.2	8	
P2103AALxx	P2103AA	170	250	170	250	150	800	2.2	8	
P2353AALxx	P2353AA	200	270	200	270	150	800	2.2	8	
P2703AALxx	P2703AA	230	300	230	300	150	800	2.2	8	
P3203AALxx	P3203AA	270	350	270	350	150	800	2.2	8	
P3403AALxx	P3403AA	300	400	300	400	150	800	2.2	8	
P5103AALxx	P5103AA	420	600	420	600	150	800	2.2	8	
P1553ABLxx	P1553AB	130	180	130	180	150	800	2.2	8	
P1803ABLxx	P1803AB	150	210	150	210	150	800	2.2	8	
P2103ABLxx	P2103AB	170	250	170	250	150	800	2.2	8	

Table continues on next page.

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Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T@I_T= 2.2 Amps	Capacitance
		V min	V max	V min	V max	mA min	mA max	A max	V max	
		Pins 1-2, 3-2		Pins 1-3						
P2353ABLxx	P2353AB	200	270	200	270	150	800	2.2	8	See Capacitance Values table
P2703ABLxx	P2703AB	230	300	230	300	150	800	2.2	8	
P3203ABLxx	P3203AB	270	350	270	350	150	800	2.2	8	
P3403ABLxx	P3403AB	300	400	300	400	150	800	2.2	8	
P5103ABLxx	P5103AB	420	600	420	600	150	800	2.2	8	
P1553ACLxx	P1553AC	130	180	130	180	150	800	2.2	8	
P1803ACLxx	P1803AC	150	210	150	210	150	800	2.2	8	
P2103ACLxx	P2103AC	170	250	170	250	150	800	2.2	8	
P2353ACLxx	P2353AC	200	270	200	270	150	800	2.2	8	
P2703ACLxx	P2703AC	230	300	230	300	150	800	2.2	8	
P3203ACLxx	P3203AC	270	350	270	350	150	800	2.2	8	
P3403ACLxx	P3403AC	300	400	300	400	150	800	2.2	8	
P5103ACLxx	P5103AC	420	600	420	600	150	800	2.2	8	

Notes:
- Absolute maximum ratings measured at T_A= 25°C.
- Components are bi-directional.
- **XX** Part Number Suffix: **'RP'** (Reel Pack), **Blank** (Bulk Pack), or **'60'** (Type 60 lead form, Bulk Pack)

Capacitance Values

Part Number	pF Pin 1-2 / 3-2 Tip-Ground, Ring-Ground		pF Pin 1-3 Tip-Ring	
	MIN	MAX	MIN	MAX
P1553AALxx	10	45	10	30
P1803AALxx	20	40	10	30
P2103AALxx	15	35	10	25
P2353AALxx	15	35	10	25
P2703AALxx	15	35	10	25
P3203AALxx	15	30	10	20
P3403AALxx	15	30	10	20
P5103AALxx	10	60	10	40
P1553ABLxx	25	95	15	60
P1803ABLxx	25	85	15	55
P2103ABLxx	20	85	10	55
P2353ABLxx	20	75	15	50

Part Number	pF Pin 1-2 / 3-2 Tip-Ground, Ring-Ground		pF Pin 1-3 Tip-Ring	
	MIN	MAX	MIN	MAX
P2703ABLxx	20	75	10	50
P3203ABLxx	20	70	10	45
P3403ABLxx	15	65	10	45
P5103ABLxx	15	60	10	40
P1553ACLxx	30	95	20	60
P1803ACLxx	30	85	15	55
P2103ACLxx	30	85	15	55
P2353ACLxx	25	75	15	50
P2703ACLxx	25	75	15	50
P3203ACLxx	25	70	15	45
P3403ACLxx	20	65	15	45
P5103ACLxx	20	60	10	40

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

Surge Ratings

Series	I_{PP} 0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]	I_{TSM} 50/60 Hz	di/dt A
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
B	25	250	250	150	100	100	125	80	100	25	500
C	50	500	400	200	150	200	175	100	200	50	500

Notes:
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

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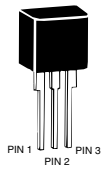
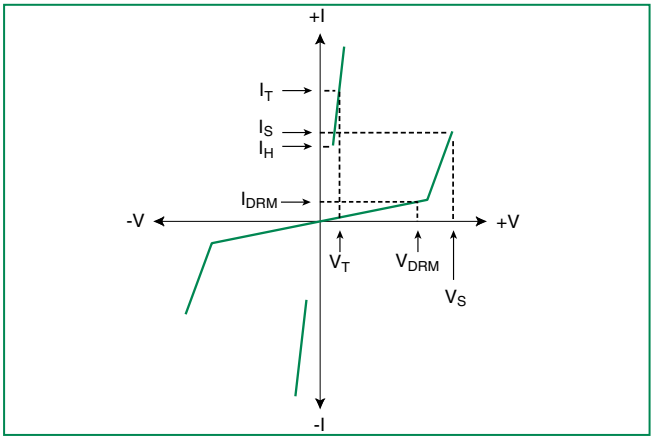
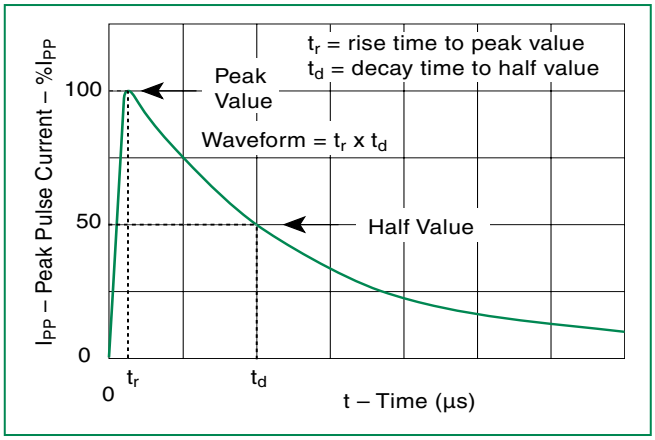
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified TO-220 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	50	°C/W

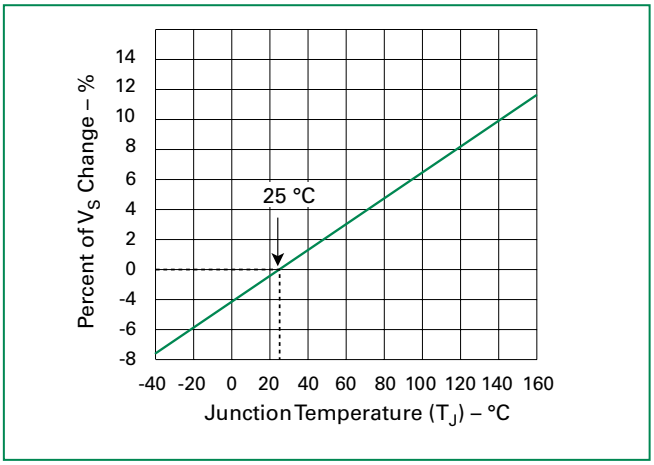
V-I Characteristics



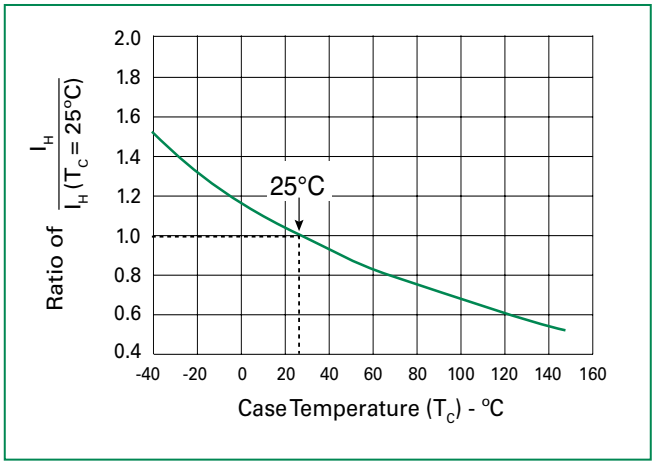
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



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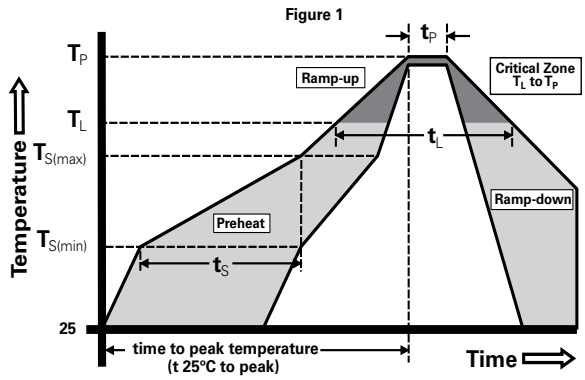
Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



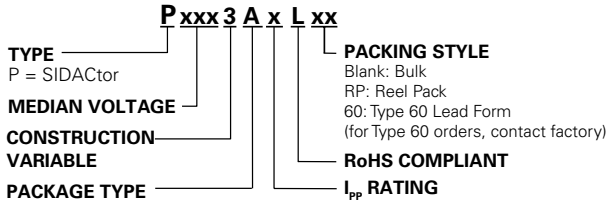
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

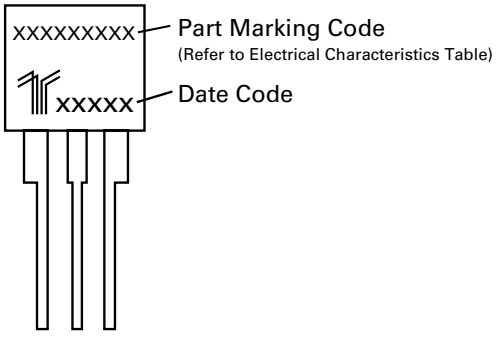
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering



Part Marking



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