

VC1902-PA-VIVA1596  
VC1802-PA-VIVA1596



## Xilinx Power Test Adaptor (PTA) - to test power delivery network to Versal ACAP VIVA1596 series FPGA's

ProGrAnalog Corp.  
08/18/2023  
Rev3.2

### Features

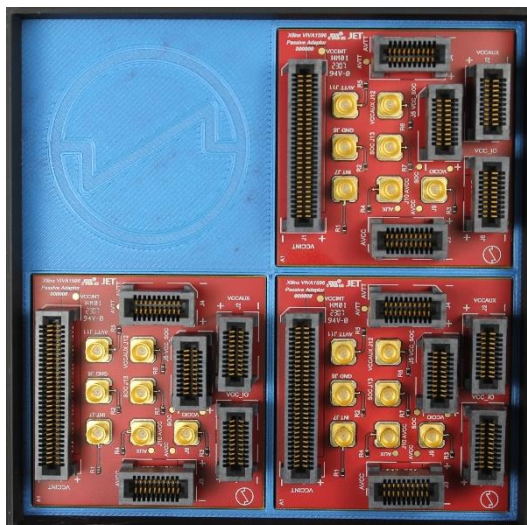
- Set of 3 Xilinx Power Test Adaptors (PTA) for PDN testing AMD Xilinx Versal ACAP AI VIVA1596 series FPGAs
- Options available for VC1902, VC1802.
- 6 Samtec connectors to slam: VCCINT, VCC\_IO, VCC\_SOC, VGTY\_AVTT, VCCAUX, AVCC
- 8 SMP connectors for testing: VCCINT\_SENSE, GND\_SENSE, GND, VCC\_IO, VCC\_SOC, VGTY\_AVTT, VCCAUX, AVCC
- PTA with BGA footprint reflows onto VIVA1596 PCB pads.
- Remote Vsense on Samtec connectors and SMP mini connectors.
- Most rails can be tested with an LSP200 controller.
- VCCINT >100A support with an LSP1000RS controller.
- GUI supports transient, pulse train, impedance and 3D plots.

### Typical Test Setup

- Xilinx PTA reflowed onto the test board.
- LSP1000RS connected into VCCINT connector.



Pack of 3 -VIVA1596 Series Xilinx PTA's



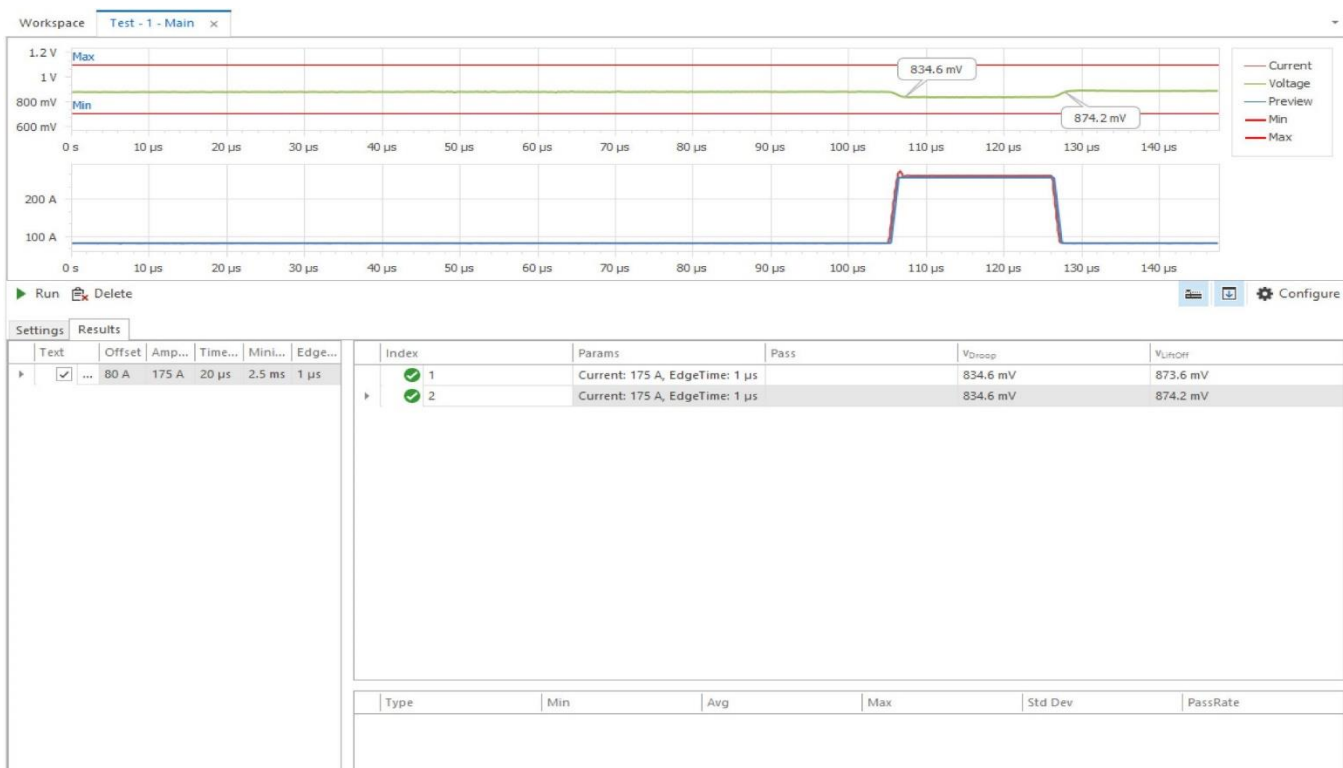
# LoadSlammer GUI

Workspace **Test - 1** x

Available Tests Name: Test - 1    Rail: None

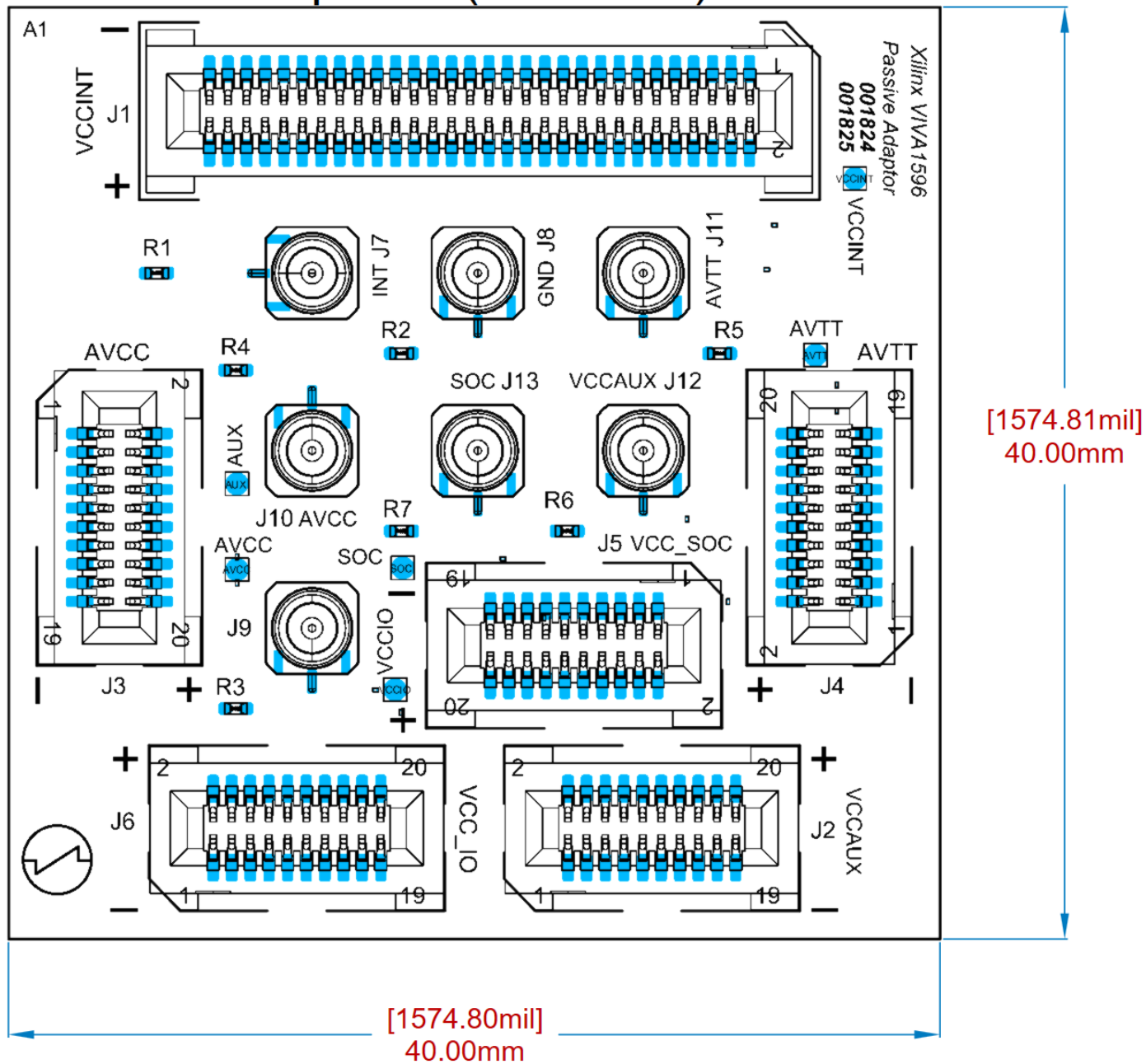
- Transient Test**  
Transient load step with adjustable rise times, current, and pulse width.
- Pulse Train**  
Repeating load steps with a configurable frequency and duty cycle.
- Impedance (Z)**  
Large signal output impedance with adjustable current amplitude and offset.
- DC Load**  
DC Load with timer.
- Delay**  
Timed delay.

## Transient test

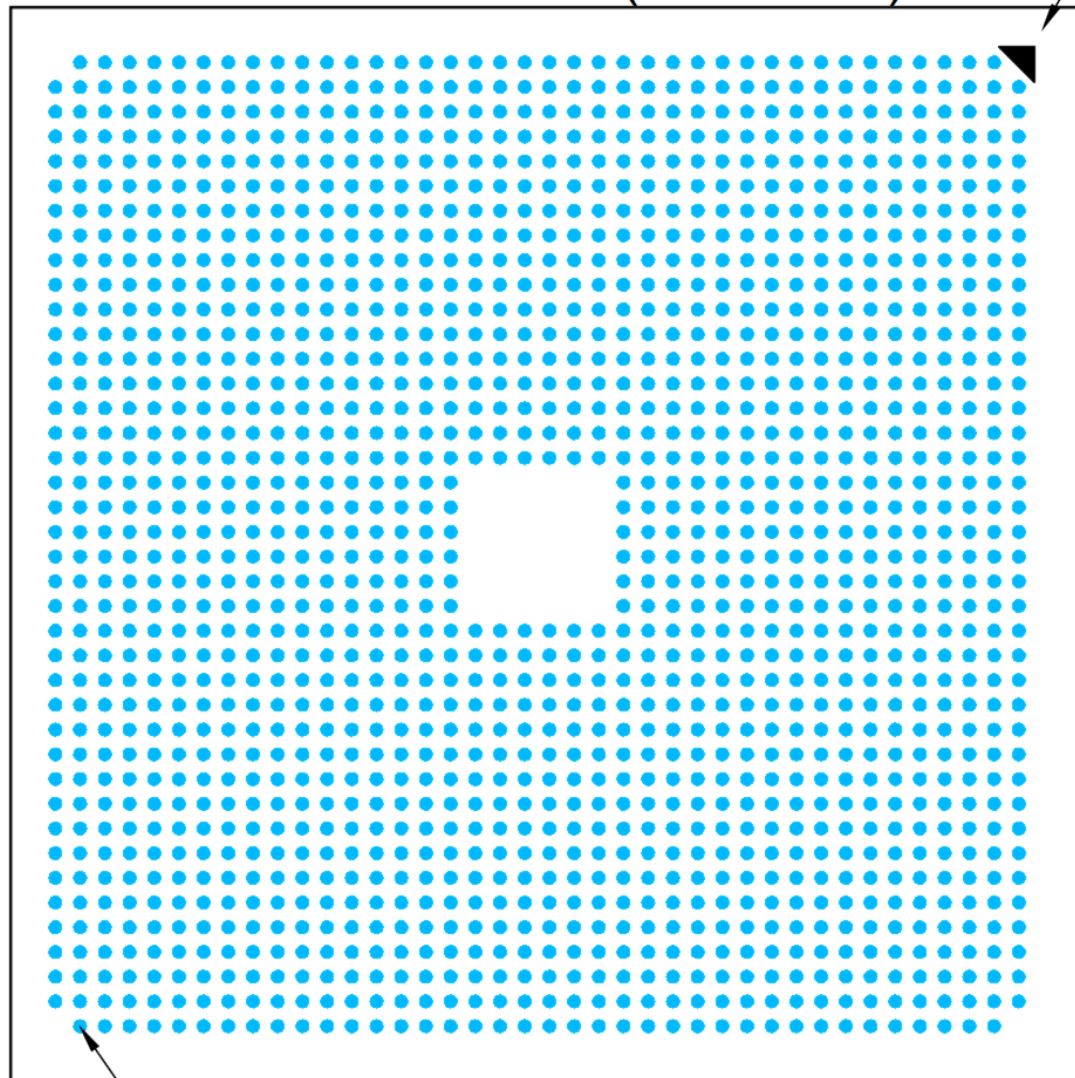


## Mechanical Specs

### View from Top side (Scale 3:1)



## View from Bottom side (Scale 3:1)



Pin 1 I.D.

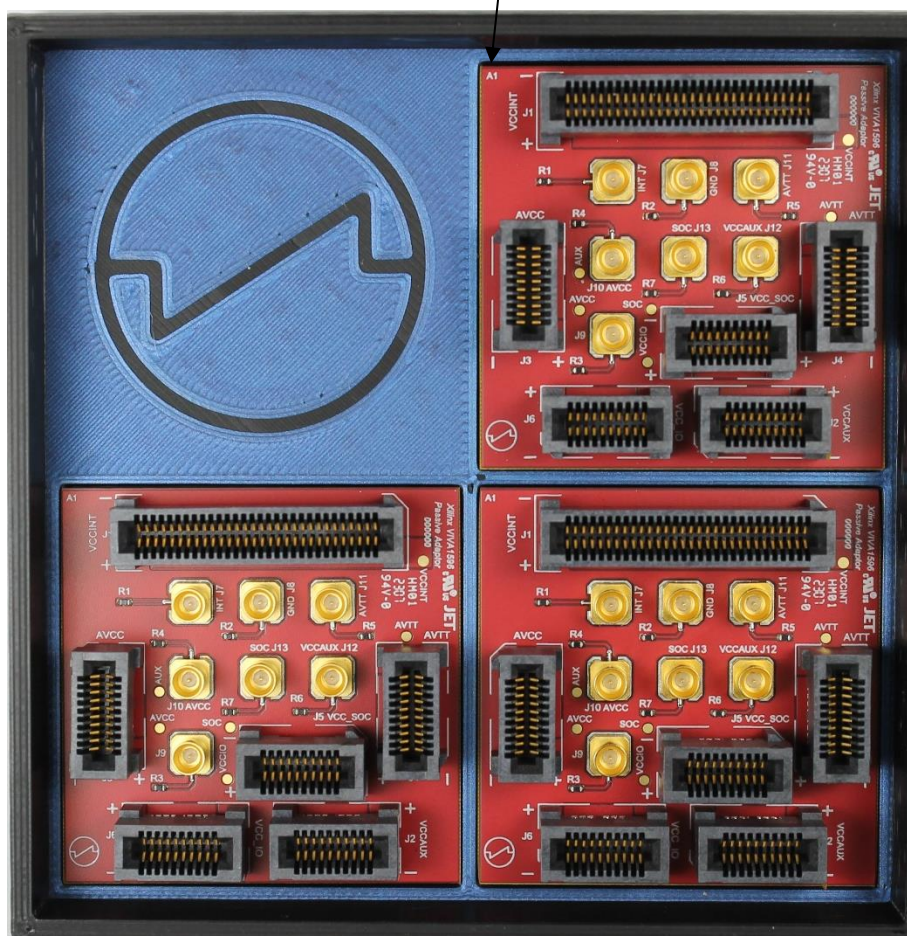
0.92mm BGA Pitch

**Sn96.5-Ag3.0-Cu0.5 0.5mm balls**

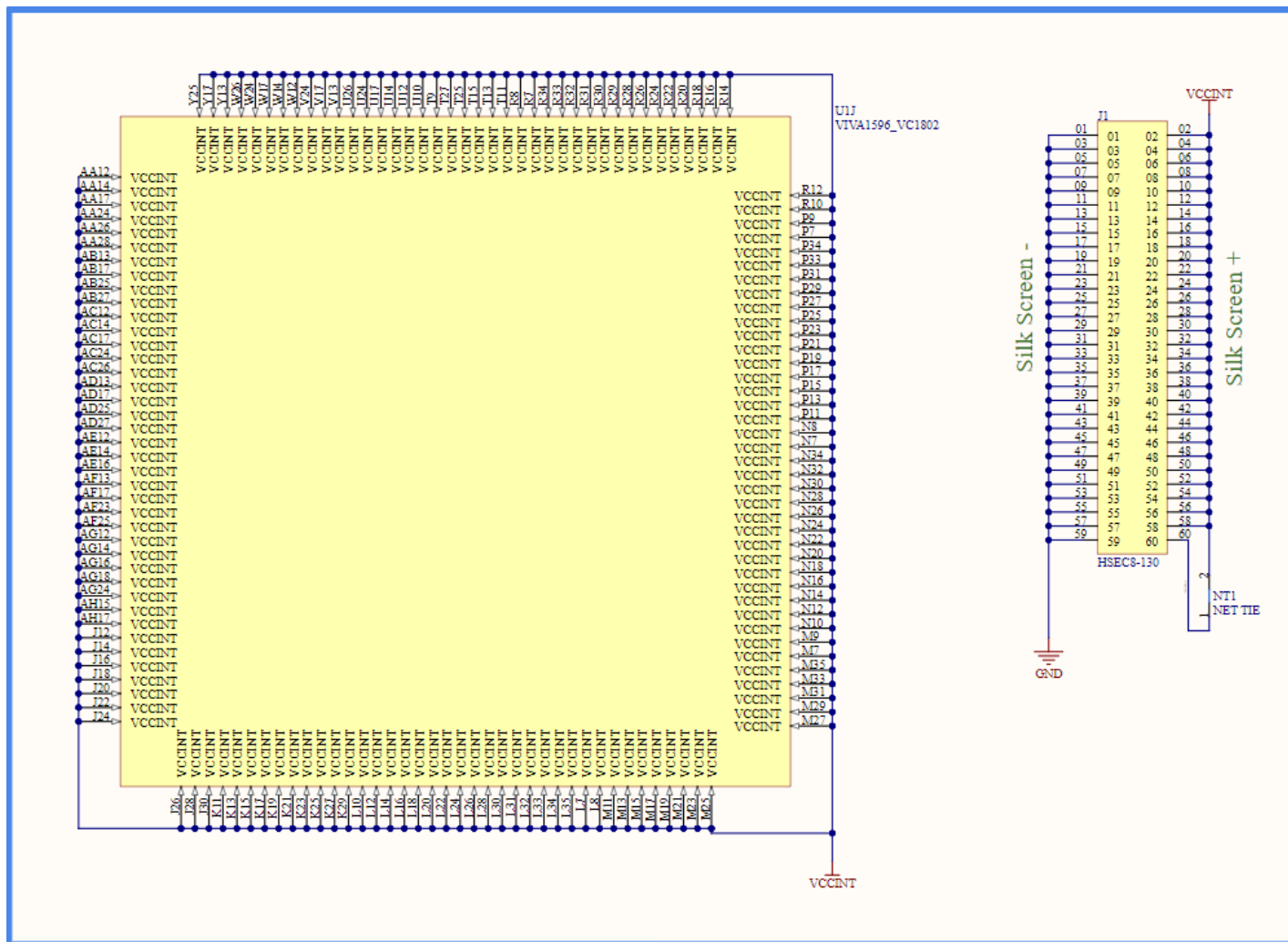
## Packing Tray Specs

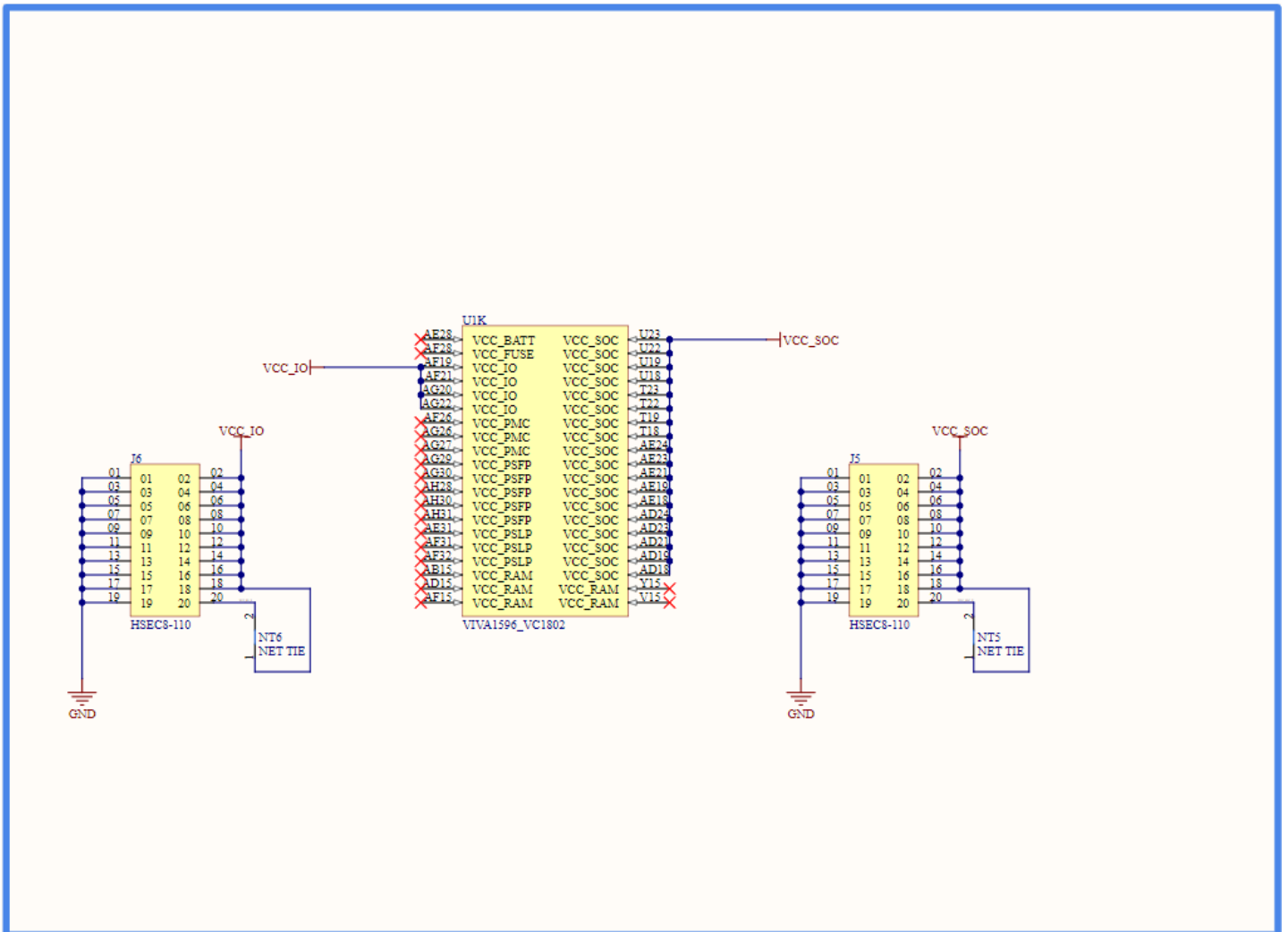
40x40mm package will have a 92x92x15mm tray

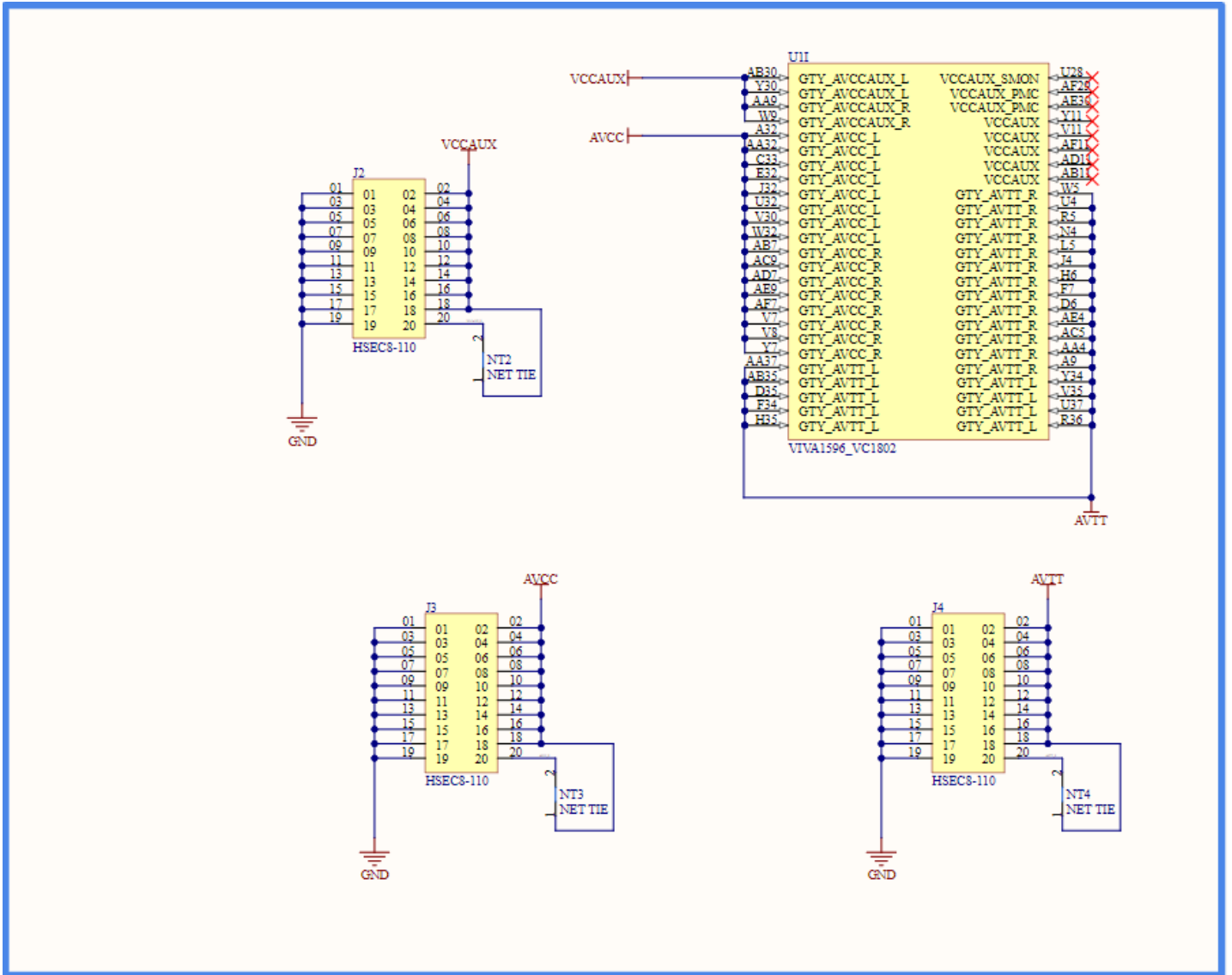
A1 top left corner



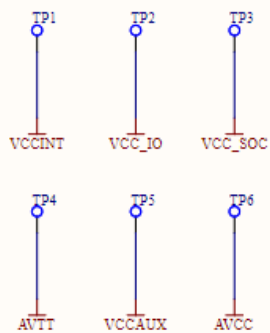
# Schematics



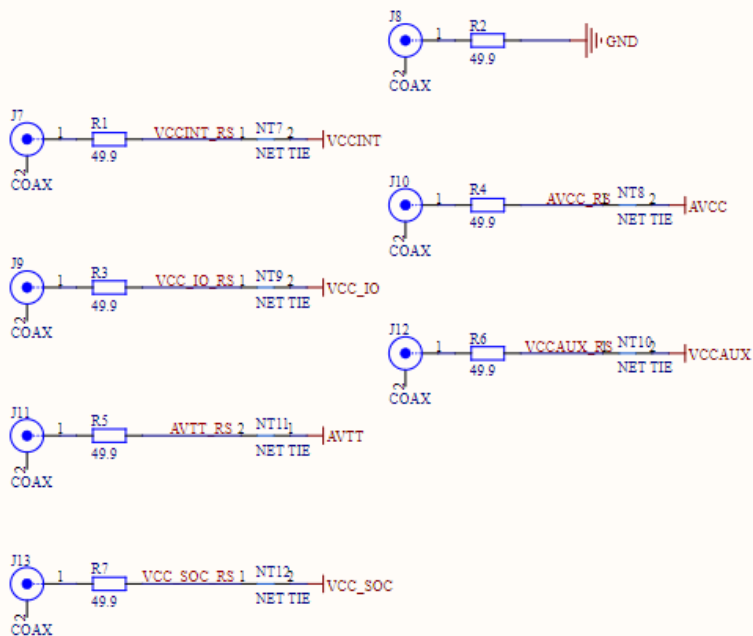








## TEST POINTS



## COAX SMP

