

VM1502-PA-VSVA2197
VM1802-PA-VSVA2197
VE1752-PA-VSVA2197
VC1502-PA-VSVA2197
VC1702-PA-VSVA2197
VC1802-PA-VSVA2197
VC1902-PA-VSVA2197



Xilinx Power Test Adaptor (PTA) - to test power delivery network (PDN) to Versal ACAP VSVA2197 series FPGAs

ProGrAnalog Corp.
08/18/2023
Rev 3.2

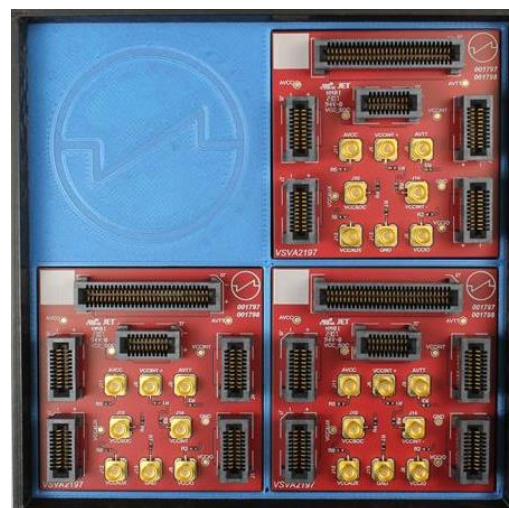
Features

- Set of 3 Xilinx Power Test Adaptors (PTA) for PDN testing AMD Xilinx Versal ACAP AI VSVA2197 series FPGAs
- Options available for VM1502, VM1802, VE1752, VC1502, VC1702, VC1802, VC1902
- 6 Samtec connectors to slam: VCCINT, VCC_IO, VCC_SOC, VGTY_AVTT, VCCAUX, AVCC
- 8 SMP connectors for measuring: VCCINT_SENSE, GND_SENSE, GND, VCC_IO, VCC_SOC, VGTY_AVTT, VCCAUX, AVCC
- PTA with BGA footprint reflows onto VSVA2197 PCB pads.
- Remote Vsense on Samtec connectors and SMP mini connectors.
- Most rails can be tested with an LSP200 controller.
- VCCINT >100A support with an LSP1000RS controller.
- GUI supports transient, pulse train, impedance and 3D plots.

Typical Test Setup

- Xilinx PTA reflowed onto the test board.
- LSP1000RS connected into VCCINT connector.

Pack of 3 -VSVA2197 Series Xilinx PTA's



LoadSlammer GUI

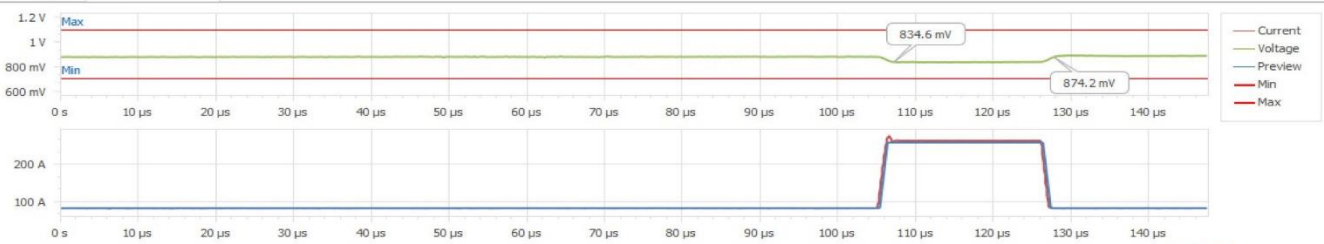
Workspace **Test - 1** x

Available Tests Name: Rail:

- Transient Test**
Transient load step with adjustable rise times, current, and pulse width.
- Pulse Train**
Repeating load steps with a configurable frequency and duty cycle.
- Impedance (Z)**
Large signal output impedance with adjustable current amplitude and offset.
- DC Load**
DC Load with timer.
- Delay**
Timed delay.

Transient test

Workspace **Test - 1 - Main** x



Run

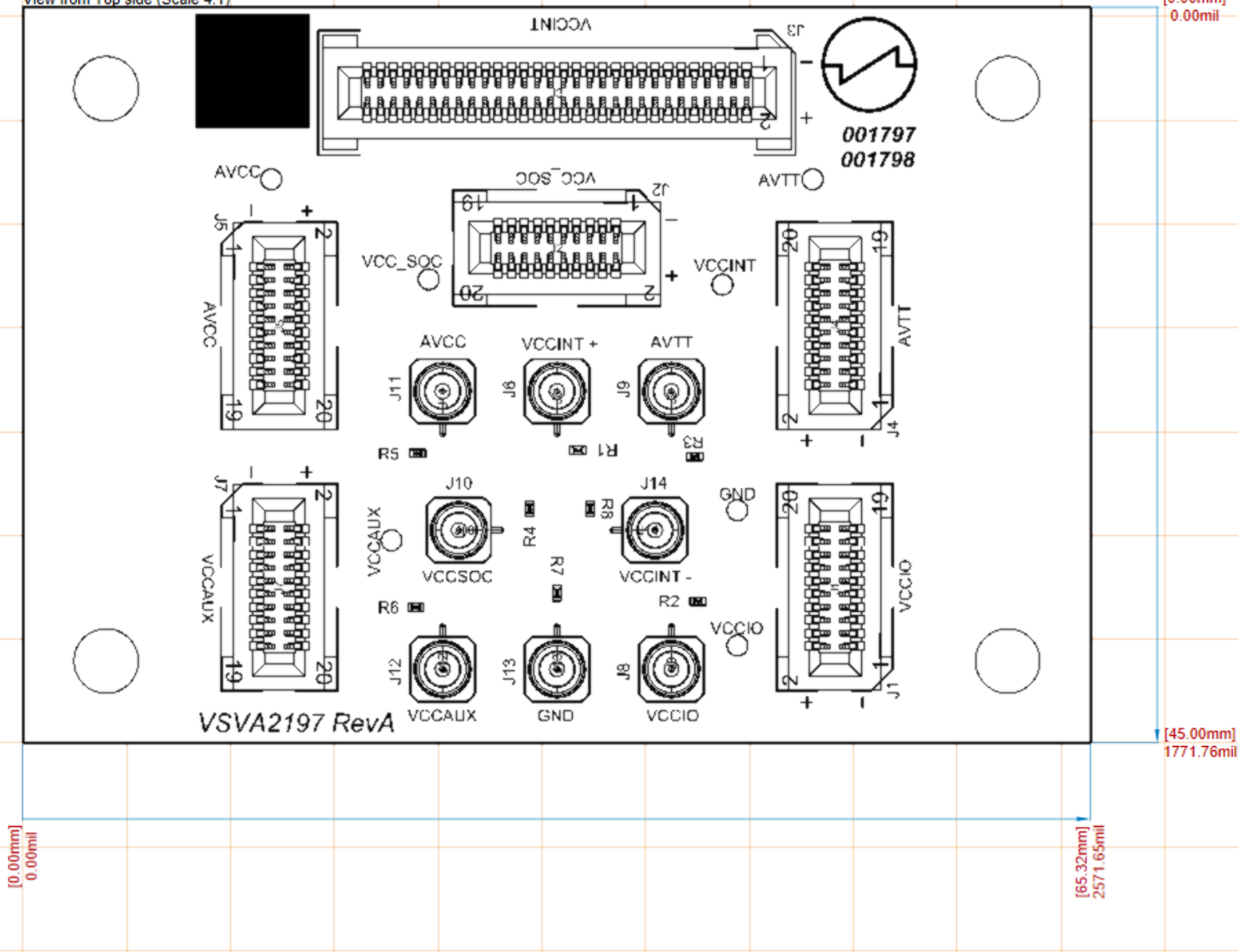
Text	Offset	Amp...	Time...	Mini...	Edge...	Index	Params	Pass	V _{droop}	V _{thdoff}
...	80 A	175 A	20 μ s	2.5 ms	1 μ s	1	Current: 175 A, EdgeTime: 1 μ s	✓	834.6 mV	873.6 mV
						2	Current: 175 A, EdgeTime: 1 μ s	✓	834.6 mV	874.2 mV

Type	Min	Avg	Max	Std Dev	PassRate



Mechanical Specs

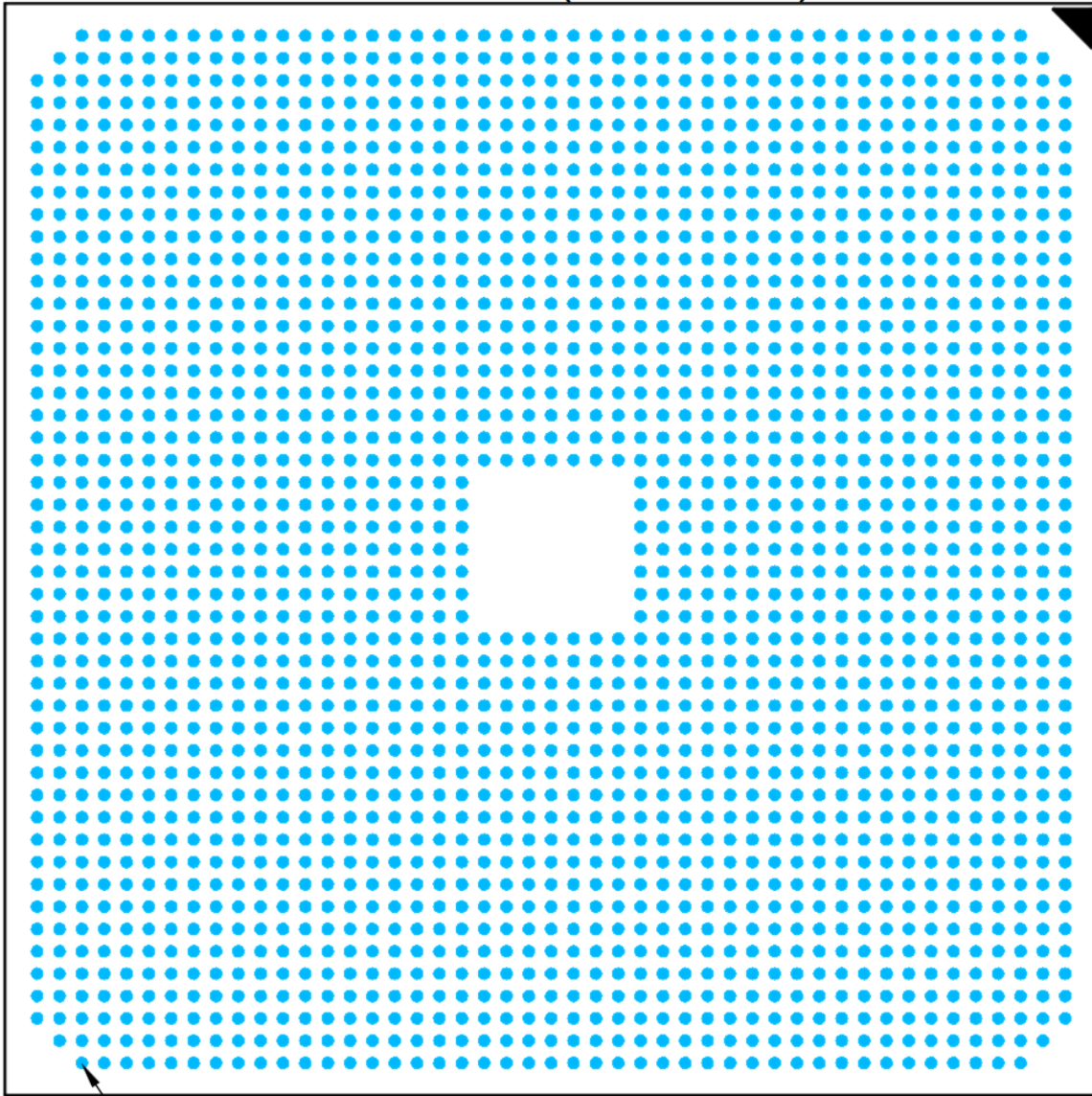
View from Top side (Scale 4:1)





Pin 1 I.D.

View from Bottom side (Scale 3:1)



0.92mm BGA Pitch

Sn96.5-Ag3.0-Cu0.5 0.6mm balls



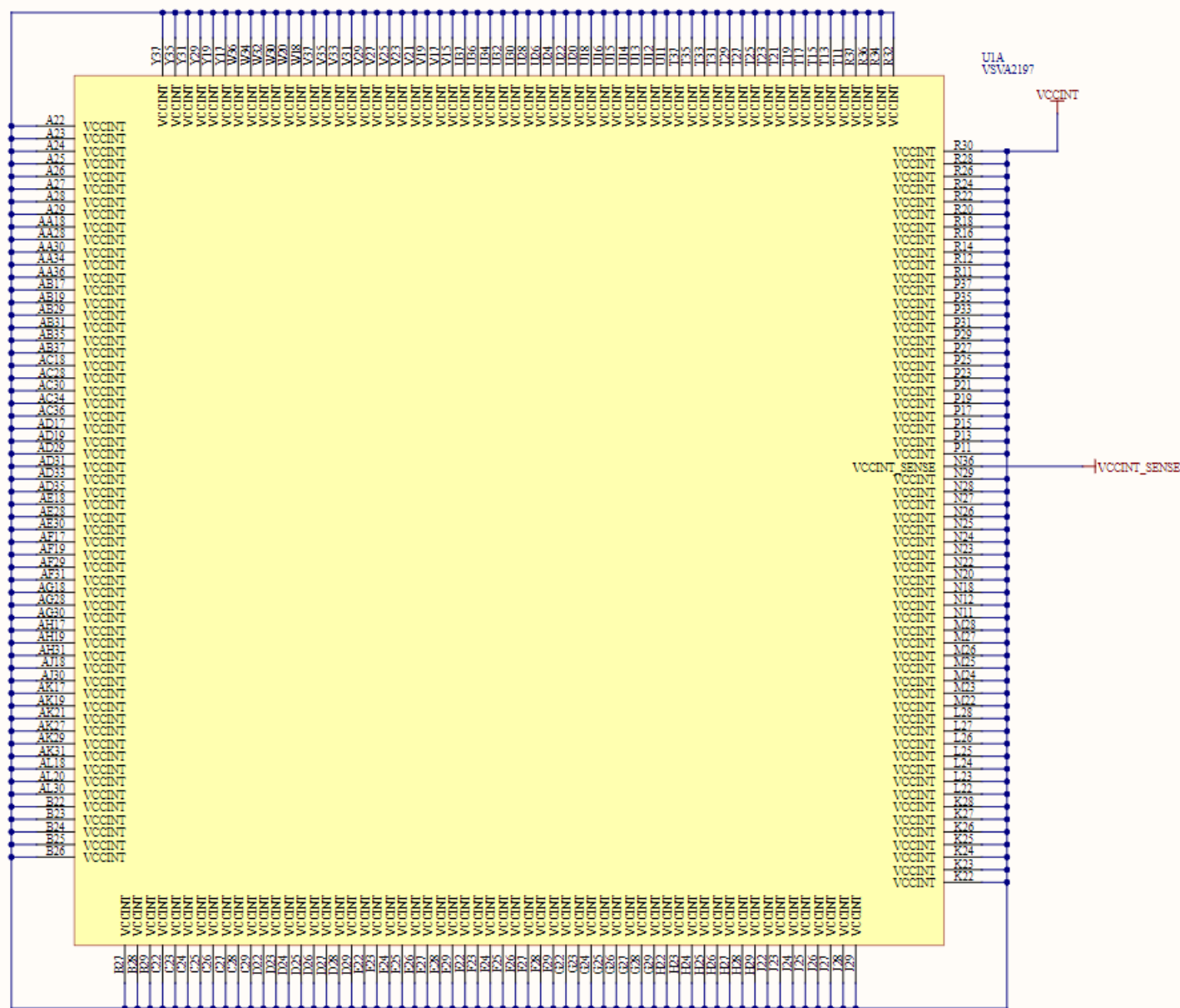
Packing Tray Specs

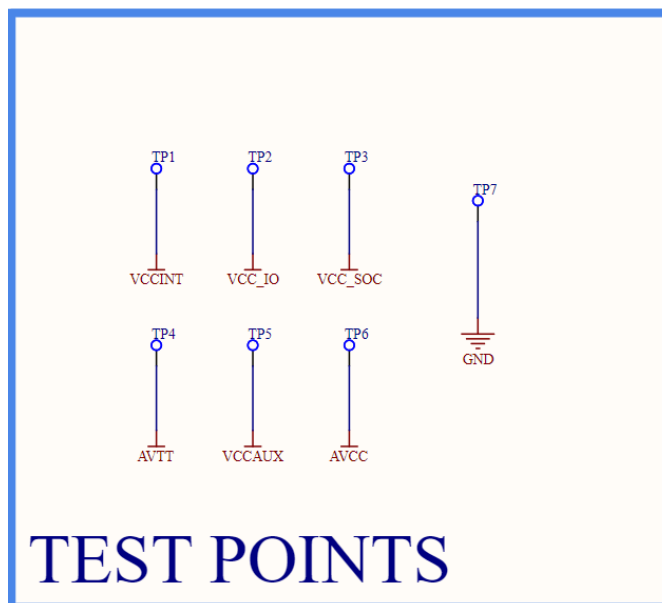
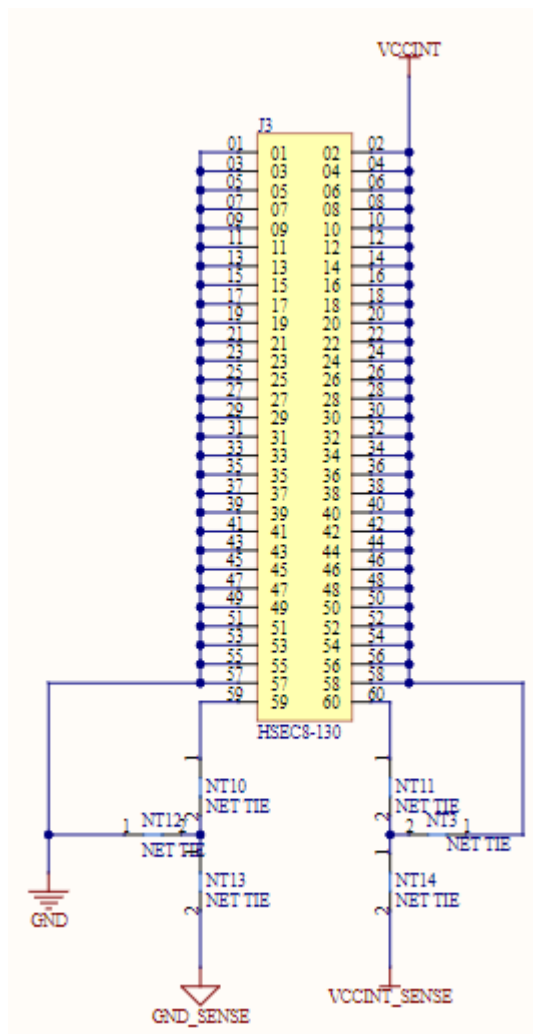
45 by 45mm package will have a 102x102x15mm tray

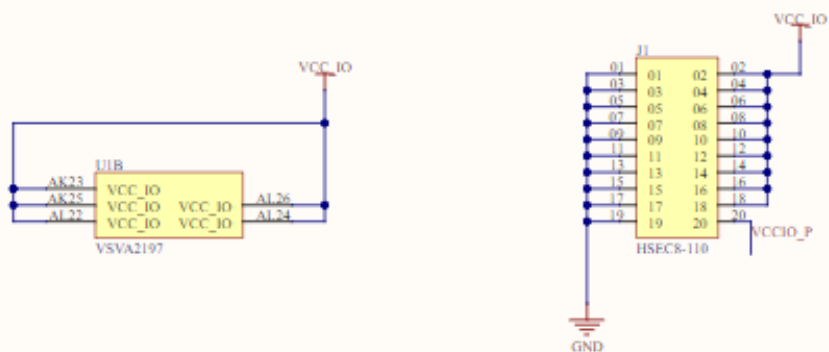
A1 top left corner



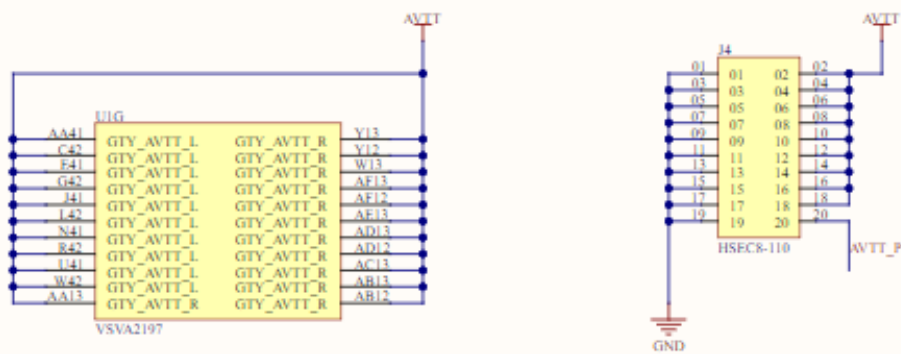
Schematics



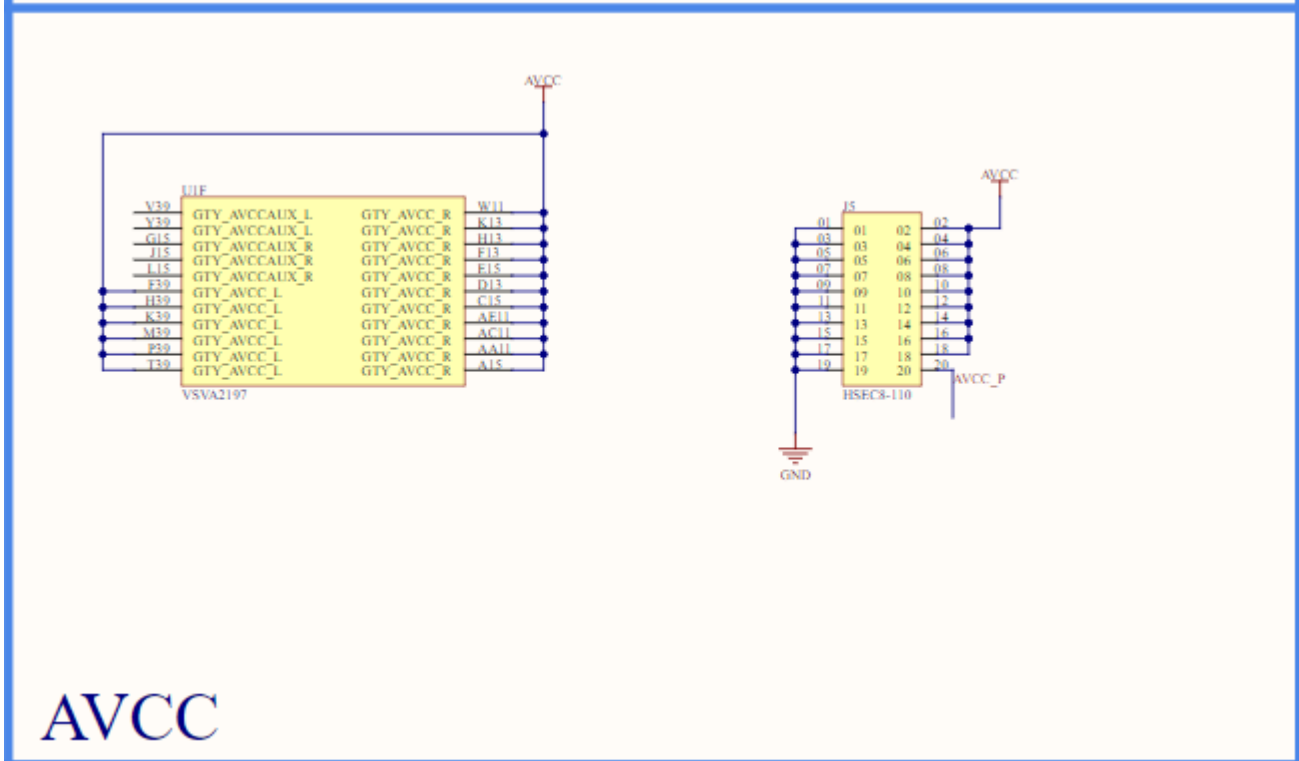
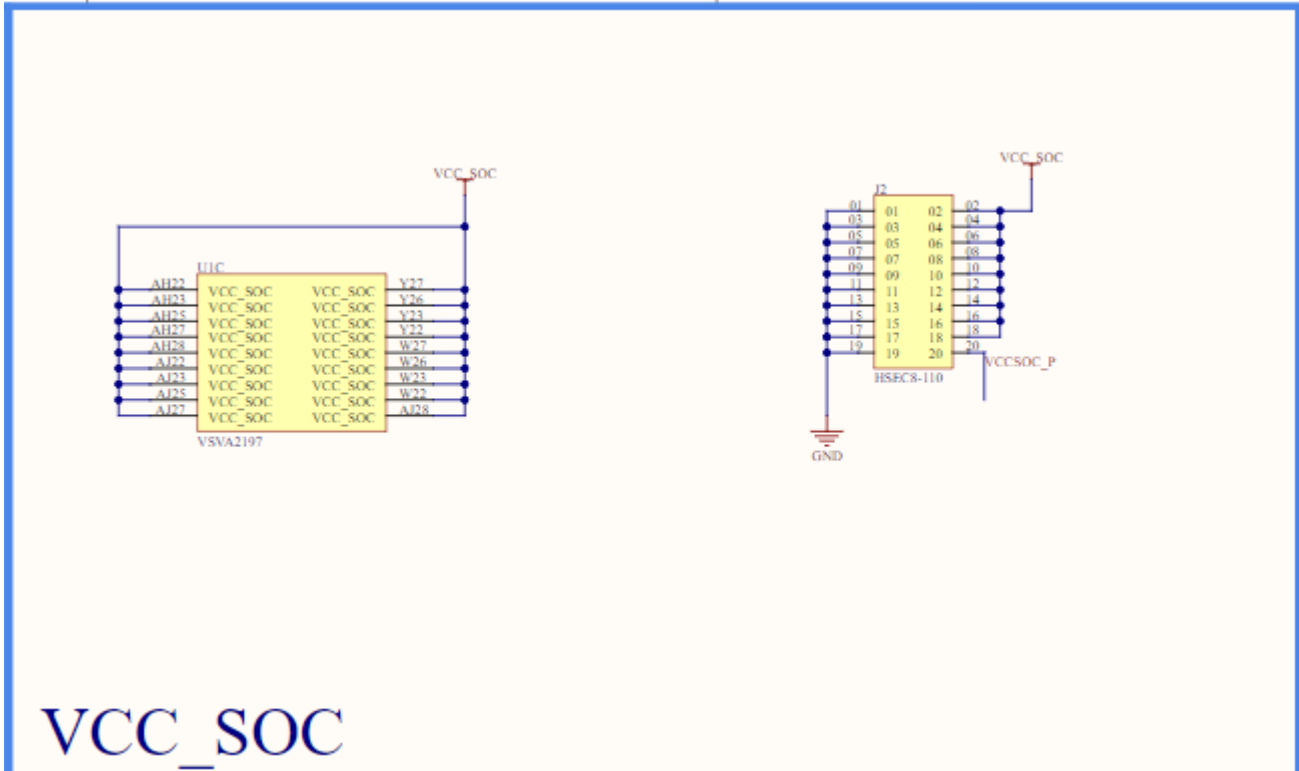


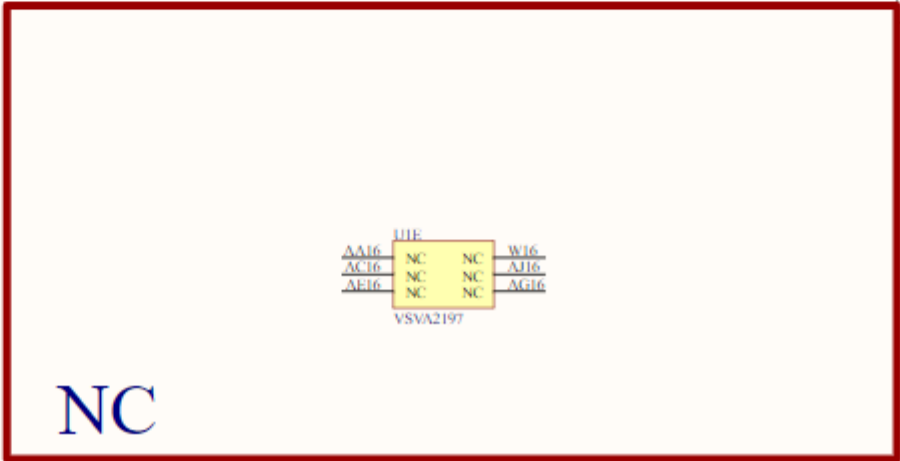
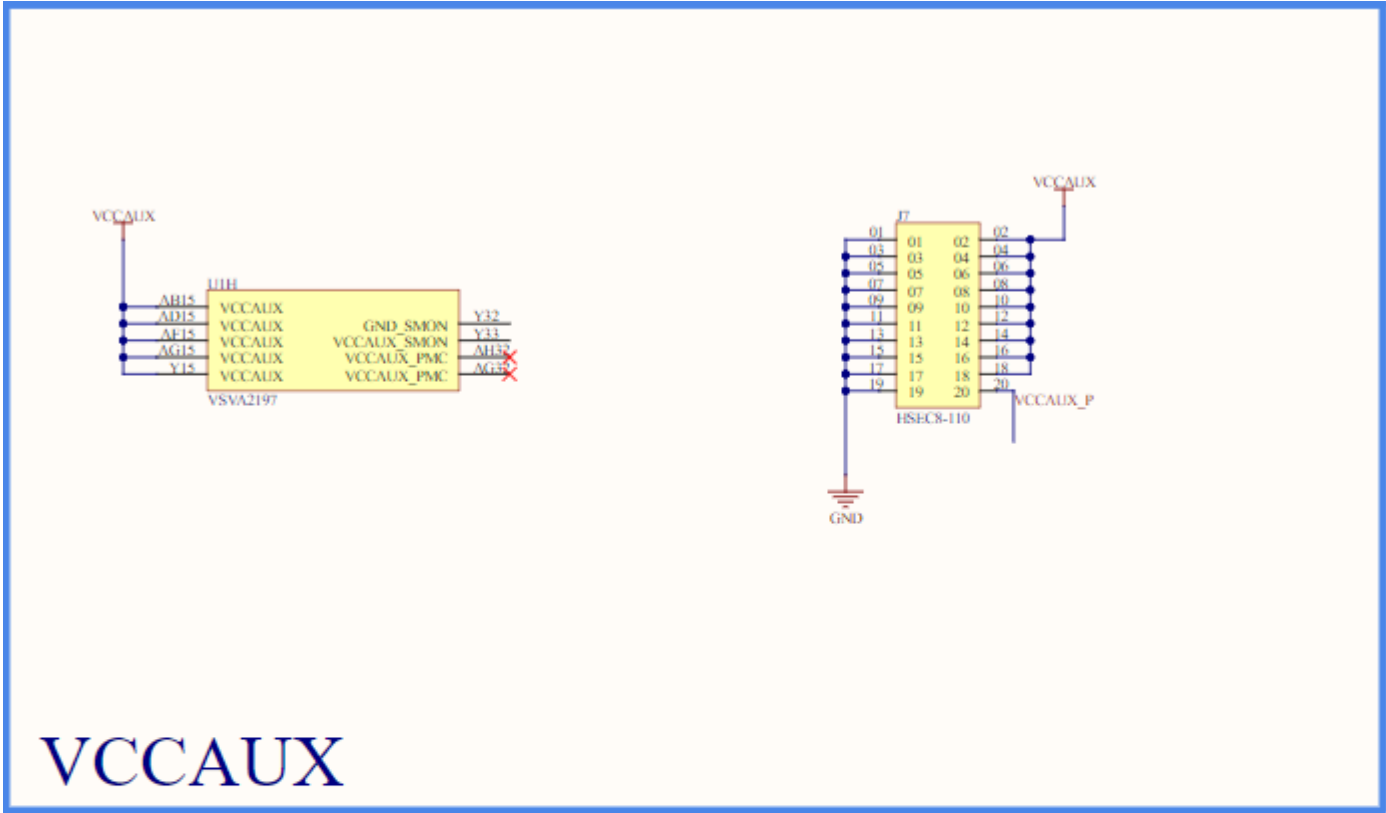


VCC_IO



AVTT



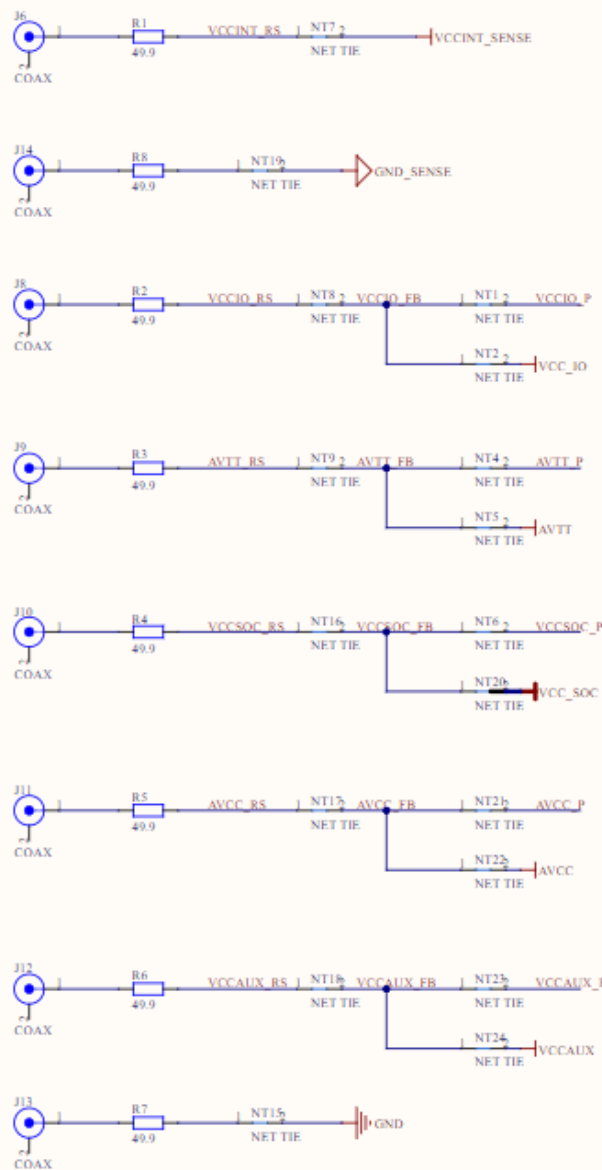


UID

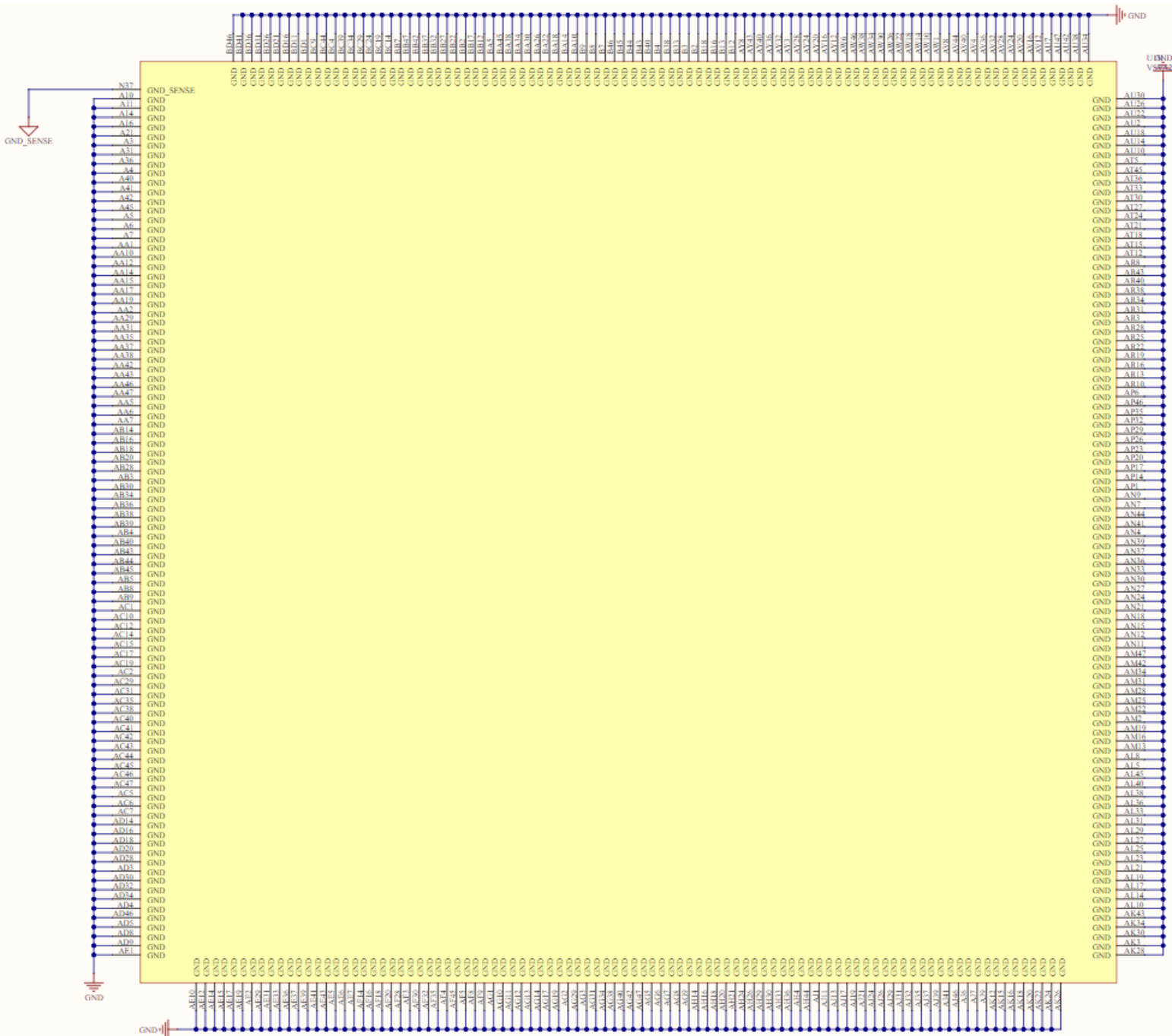
AG33	VCC_BATT		AJ20
AF33	VCC_FUSE	VCC_RAM	AG20
AJ33	VCC_PMC	VCC_RAM	AE20
AK32	VCC_PMC	VCC_RAM	AE20
AL32	VCC_PMC	VCC_RAM	AC20
AH34	VCC_PMC	VCC_RAM	AA20
AJ34	VCC_PSF	VCC_RAM	AH35
AJ34	VCC_PSF	VCC_PSLP	AH35
AK33	VCC_PSF	VCC_PSLP	AG35
AL34	VCC_PSF	VCC_PSLP	AF34

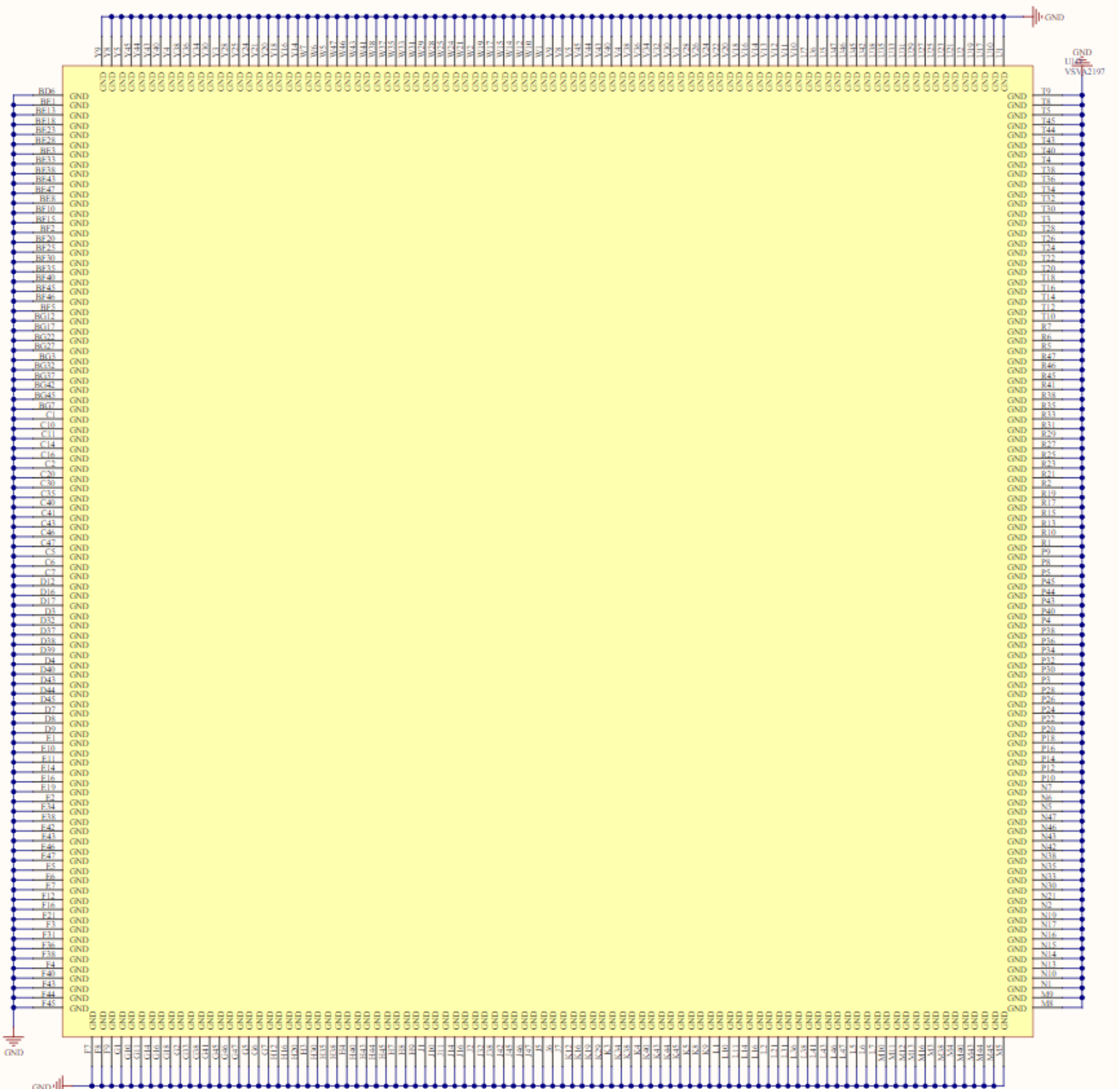
VSVA2197

VCC MISC



COAX SMP





UIM			
W40	GTY_REFCLKN0_103	GTY_TXP3_106	A43
U40	GTY_REFCLKN1_103	GTY_TXP2_106	B41
W39	GTY_REFCLKP0_103	GTY_TXP1_106	D41
U39	GTY_REFCLKP1_103	GTY_TXP0_106	F41
AB47	GTY_RXN0_103	GTY_TXN3_106	A44
AA45	GTY_RXN1_103	GTY_TXN2_106	B42
Y47	GTY_RXN2_103	GTY_TXN1_106	D42
W45	GTY_RXN3_103	GTY_TXN0_106	F42
AB46	GTY_RXP0_103	GTY_RXP3_106	C44
AA44	GTY_RXP1_103	GTY_RXP2_106	D46
Y46	GTY_RXP2_103	GTY_RXP1_106	E44
W44	GTY_RXP3_103	GTY_RXP0_106	F46
AB42	GTY_TXN0_103	GTY_RXN3_106	C45
Y42	GTY_TXN1_103	GTY_RXN2_106	D47
W42	GTY_TXN2_103	GTY_RXN1_106	E45
U44	GTY_TXN3_103	GTY_RXN0_106	F47
AB41	GTY_TXP0_103	GTY_REFCLKP1_106	E39
Y41	GTY_TXP1_103	GTY_REFCLKP0_106	G39
U41	GTY_TXP2_103	GTY_REFCLKN1_106	E40
W43	GTY_TXP3_103	GTY_REFCLKN0_106	G40
R40	GTY_REFCLKN0_104	GTY_TXP3_105	G43
N40	GTY_REFCLKN1_104	GTY_TXP2_105	H41
R39	GTY_REFCLKP0_104	GTY_TXP1_105	J43
N39	GTY_REFCLKP1_104	GTY_TXP0_105	K41
V47	GTY_RXN0_104	GTY_TXN3_105	G44
T47	GTY_RXN1_104	GTY_TXN2_105	H42
P47	GTY_RXN2_104	GTY_TXN1_105	J44
N45	GTY_RXN3_104	GTY_TXN0_105	K42
V46	GTY_RXP0_104	GTY_RXP3_105	H46
T46	GTY_RXP1_104	GTY_RXP2_105	K46
P46	GTY_RXP2_104	GTY_RXP1_105	L44
N44	GTY_RXP3_104	GTY_RXP0_105	M46
T42	GTY_TXN0_104	GTY_RXN3_105	H47
R44	GTY_TXN1_104	GTY_RXN2_105	K47
P42	GTY_TXN2_104	GTY_RXN1_105	L45
M42	GTY_TXN3_104	GTY_RXN0_105	M47
T41	GTY_TXP0_104	GTY_REFCLKP1_105	AA39
R43	GTY_TXP1_104	GTY_REFCLKP0_105	J39
P41	GTY_TXP2_104	GTY_REFCLKN1_105	L39
M41	GTY_TXP3_104	GTY_REFCLKN0_105	J40
AA40	GTY_AVTTTRCAL_L	GTY_REFCLKN0_105	L40

VSVA2197

UIL			
D15	GTY_REFCLKP1_205		A13
G3	GTY_RXN0_205	GTY_TXP3_206	A9
F1	GTY_RXN1_205	GTY_TXP2_206	B9
F5	GTY_RXN2_205	GTY_TXP1_206	B11
E3	GTY_RXN3_205	GTY_TXP0_206	C9
G4	GTY_RXP0_205	GTY_TXN3_206	A12
F2	GTY_RXP1_205	GTY_TXN2_206	A8
F6	GTY_RXP2_205	GTY_TXN1_206	B10
E4	GTY_RXP3_205	GTY_TXN0_206	C8
G8	GTY_TXN0_205	GTY_RXP3_206	B6
F10	GTY_TXN1_205	GTY_RXP2_206	C4
E8	GTY_TXN2_205	GTY_RXP1_206	D6
D10	GTY_TXN3_205	GTY_RXP0_206	D2
G9	GTY_TXP0_205	GTY_RXN3_206	B5
F11	GTY_TXP1_205	GTY_RXN2_206	C3
E9	GTY_TXP2_205	GTY_RXN1_206	D5
D11	GTY_TXP3_205	GTY_RXN0_206	D1
C12	GTY_REFCLKN0_206	GTY_REFCLKP1_206	B15
B14	GTY_REFCLKN1_206	GTY_REFCLKP0_206	C13

VSVA2197

UIK			
L37	IO_L0N_306	VCCO_306	M33
M37	IO_L0P_306	VCCO_306	J37
G37	IO_L10N_306	IO_L9P_306	J34
G36	IO_L10P_306	IO_L9N_306	J35
M34	IO_L1N_306	IO_L8P_306	H36
N34	IO_L1P_306	IO_L8N_306	H37
M36	IO_L2N_306	IO_L7P_306	J33
M35	IO_L2P_306	IO_L7N_306	H34
K33	IO_L3N_306	IO_L6P_HDGC_306	L35
L33	IO_L3P_306	IO_L6N_HDGC_306	K36
J36	IO_L4N_306	IO_L5P_HDGC_306	L34
K37	IO_L4P_306	IO_L5N_HDGC_306	K35

VSVA2197

UIJ			
M21	IO_L0N_406	VCCO_406	M18
M20	IO_L0P_406	VCCO_406	J17
G21	IO_L10N_406	IO_L9P_406	H19
H21	IO_L10P_406	IO_L9N_406	G20
L17	IO_L1N_406	IO_L8P_406	J20
M17	IO_L1P_406	IO_L8N_406	J21
L19	IO_L2N_406	IO_L7P_406	H17
M19	IO_L2P_406	IO_L7N_406	H18
K17	IO_L3N_406	IO_L6P_HDGC_406	K20
L18	IO_L3P_406	IO_L6N_HDGC_406	J19
K21	IO_L4N_406	IO_L5P_HDGC_406	K18
L20	IO_L4P_406	IO_L5N_HDGC_406	J18

VSVA2197

