

VC1902-PA-VSVD1760  
VC1802-PA-VSVD1760  
VM1302-PA-VSVD1760  
VM1402-PA-VSVD1760  
VM1802-PA-VSVD1760



## Passive Adaptors to test power delivery network to Versal ACAP AI-VSVD1760 series FPGAs

ProGrAnalog Corp.  
04/7/2023  
Rev 2.0

### Features

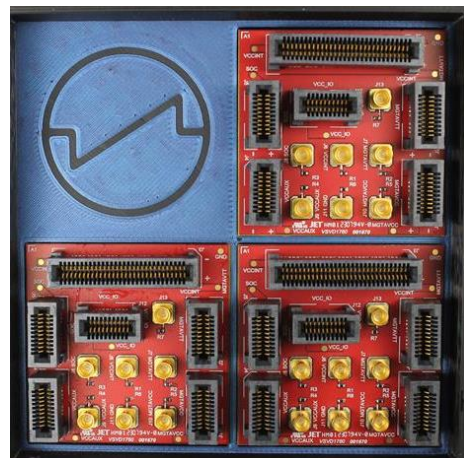
- Set of 3 Passive Adaptors (PA) for PDN testing AMD Xilinx Versal ACAP AI VSVD1760 series FPGAs
- Options available for VC1902, VC1802, VM1302, VM1402, VM1802
- 6 Samtec connectors to slam: VCCINT, VCC\_IO, VCC\_SOC, VGTY\_AVTT, VCCAUX, AVCC
- 7 SMP connectors for measuring: GND, VCCINT, VCC\_IO, VCC\_SOC, VGTY\_AVTT, VCCAUX, AVCC
- PA with BGA footprint reflows onto VSVD1760 PCB pads.
- Remote Vsense on Samtec connectors and SMP mini connectors.
- Most rails can be tested with an LSP200 controller.
- VCCINT >100A support with an LSP1000RS controller.
- GUI supports transient, pulse train, impedance and 3D plots.

### Typical Test Setup

Passive Adaptor reflowed onto the test board.  
LSP1000RS connected into VCCINT connector.



Pack of 3 -VSVD1760 Series PA's



# LoadSlammer GUI

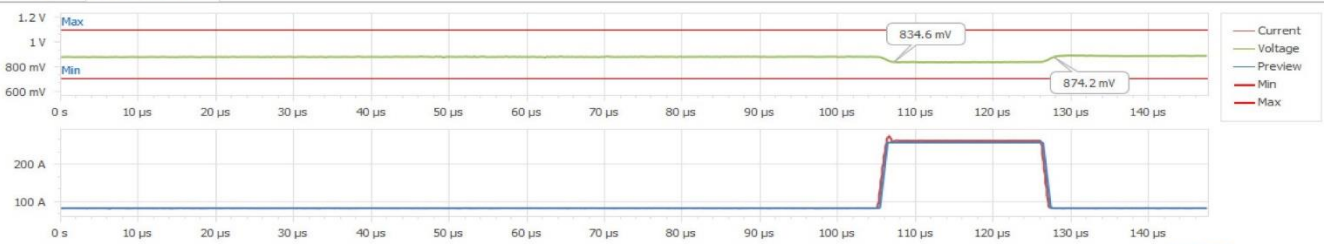
Workspace **Test - 1** x

Available Tests Name: Test - 1    Rail: None

- Transient Test**  
Transient load step with adjustable rise times, current, and pulse width.
- Pulse Train**  
Repeating load steps with a configurable frequency and duty cycle.
- Impedance (Z)**  
Large signal output impedance with adjustable current amplitude and offset.
- DC Load**  
DC Load with timer.
- Delay**  
Timed delay.

## Transient test

Workspace **Test - 1 - Main** x



Run Delete Configure

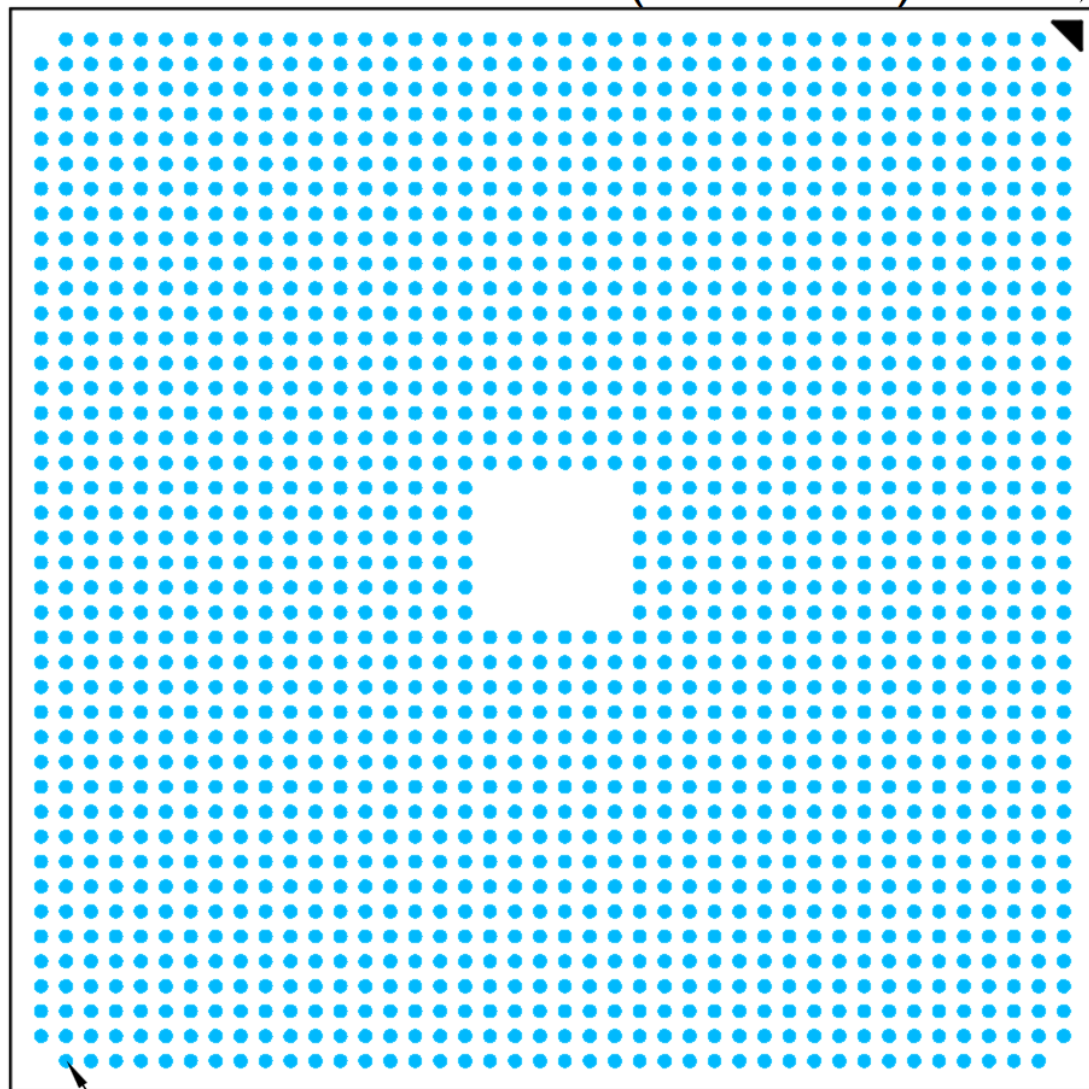
Text	Offset	Amp...	Time...	Mini...	Edge...	Index	Params	Pass	V <sub>droop</sub>	V <sub>thdOff</sub>
...	80 A	175 A	20 µs	2.5 ms	1 µs	1	Current: 175 A, EdgeTime: 1 µs	✓	834.6 mV	873.6 mV
						2	Current: 175 A, EdgeTime: 1 µs	✓	834.6 mV	874.2 mV

Type	Min	Avg	Max	Std Dev	PassRate





# View from Bottom side (Scale 3:1)



Pin 1 I.D.

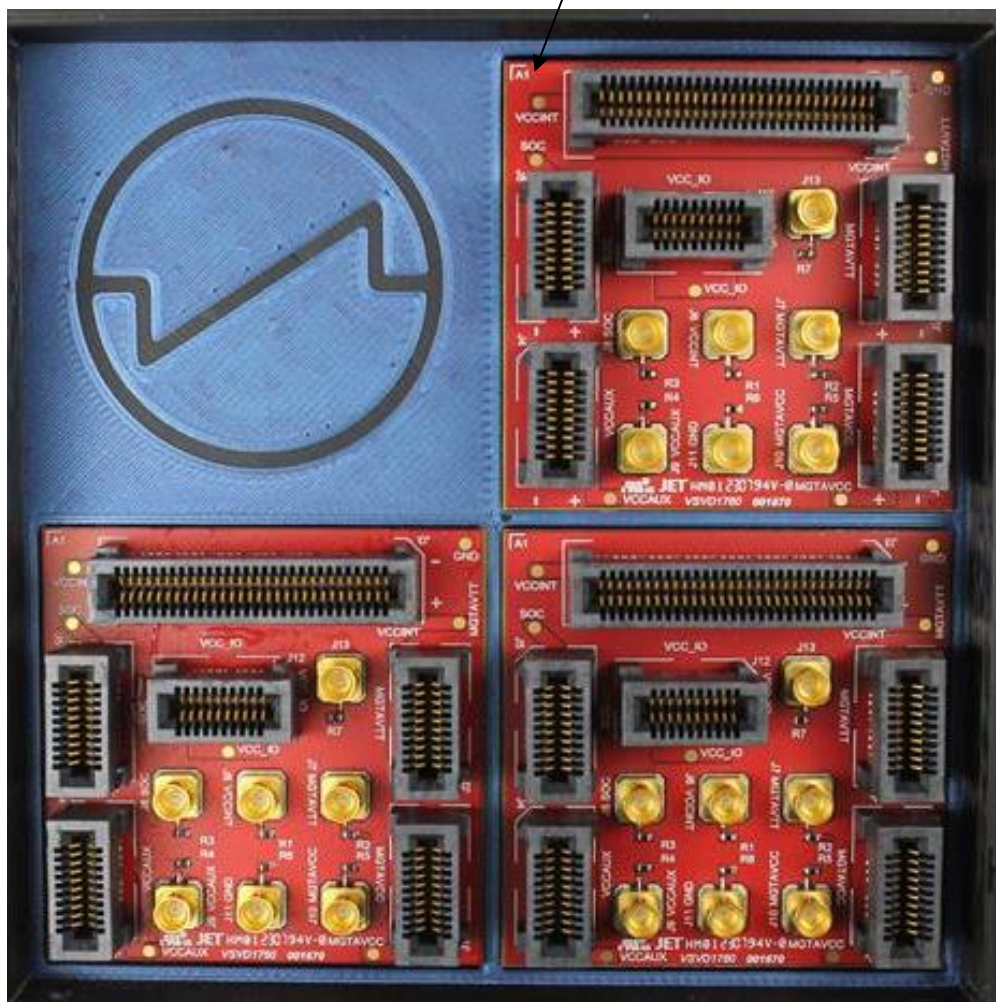
0.92mm BGA Pitch

**Sn96.5-Ag3.0-Cu0.5 0.6mm balls**

## Packing Tray Specs

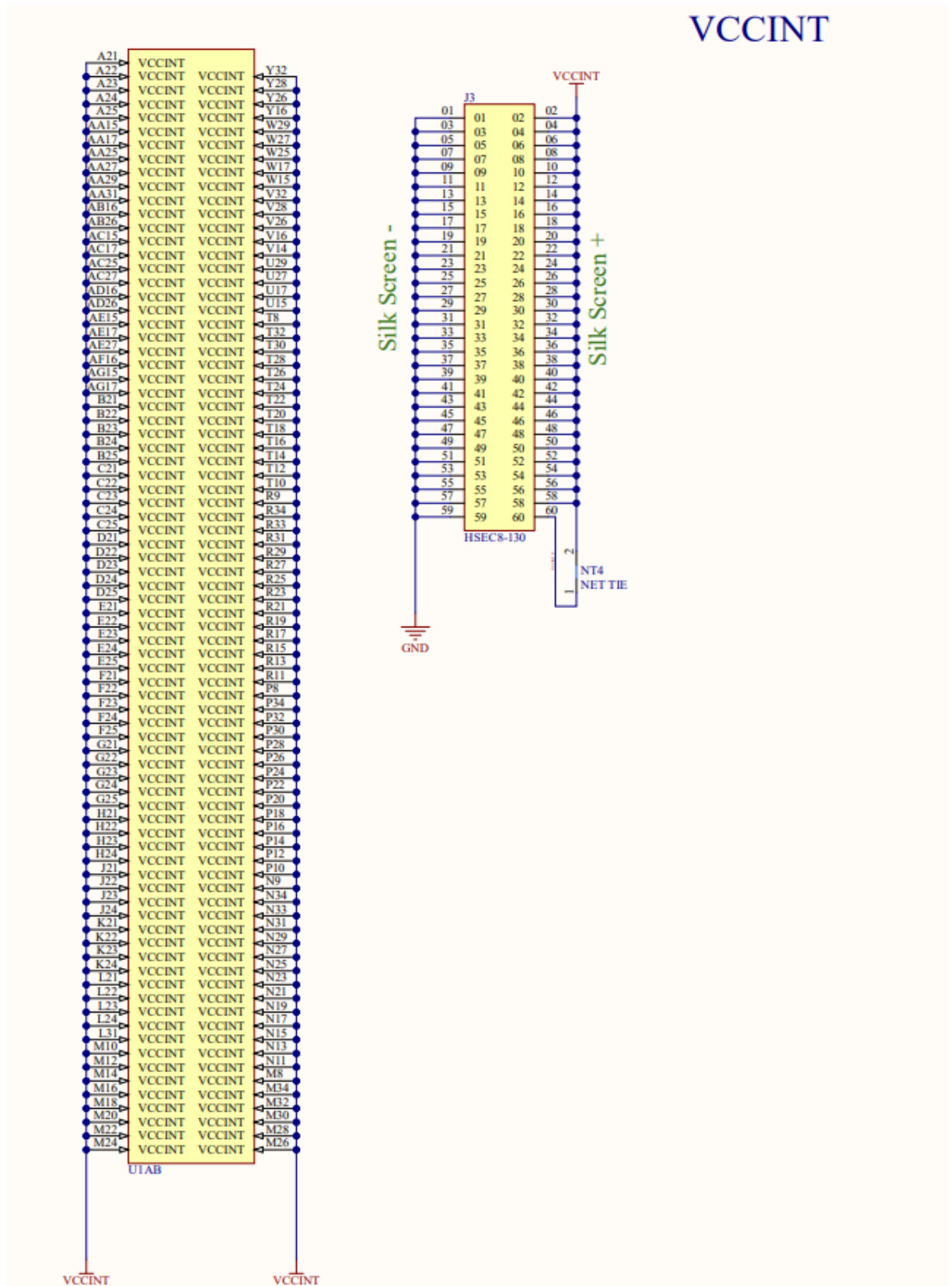
40x40mm package will have a 92x92x15mm tray.

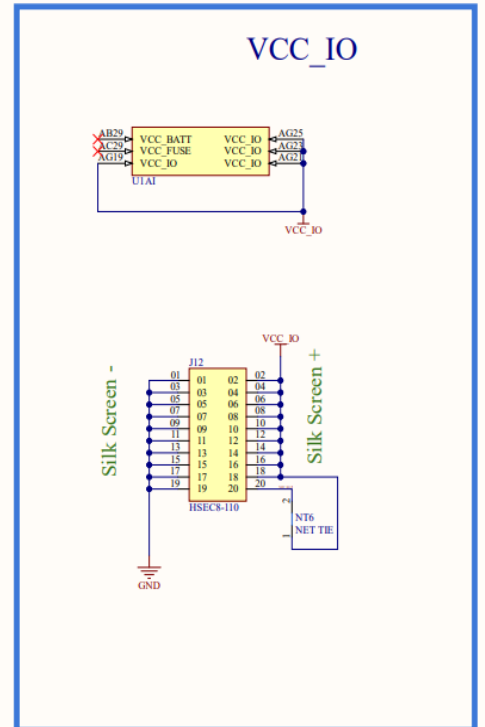
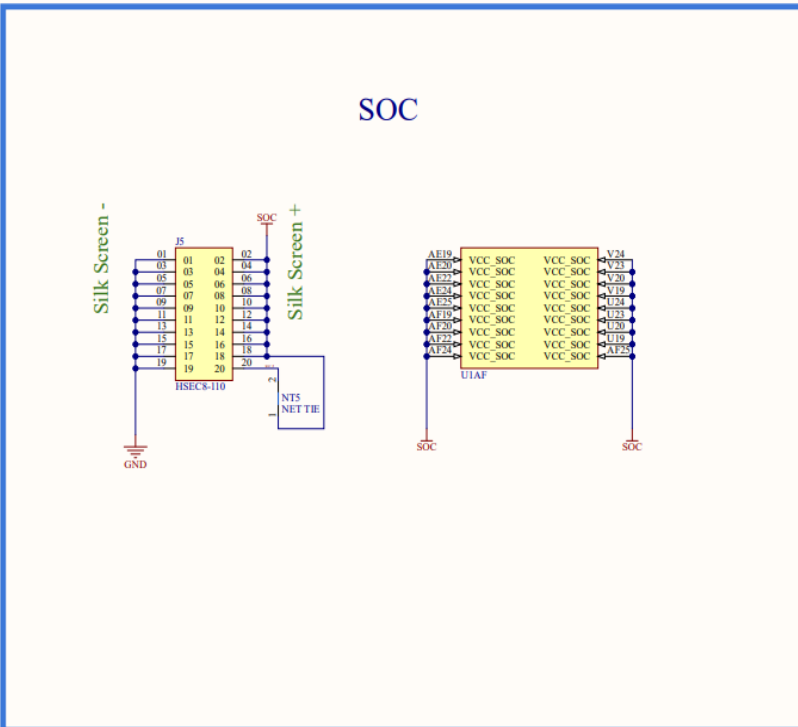
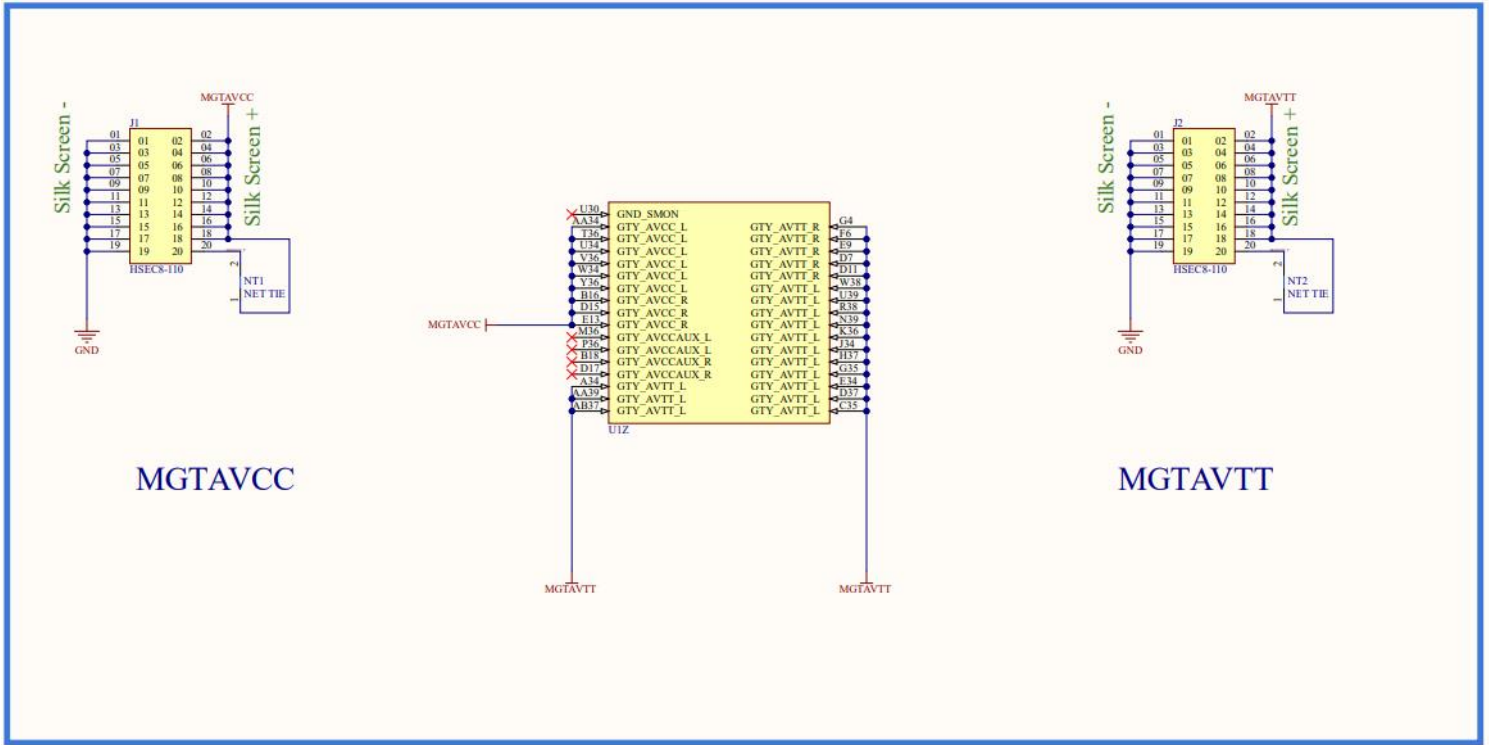
A1 top left corner

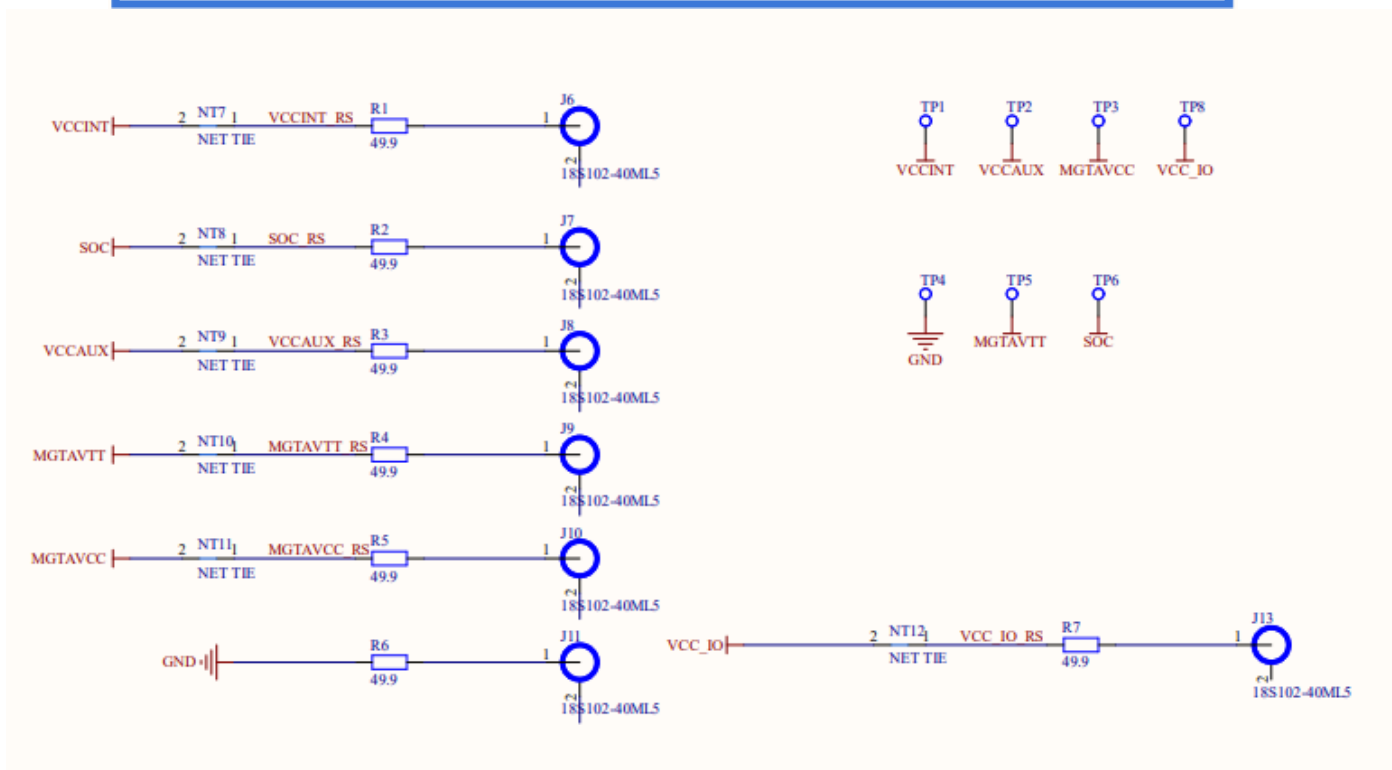
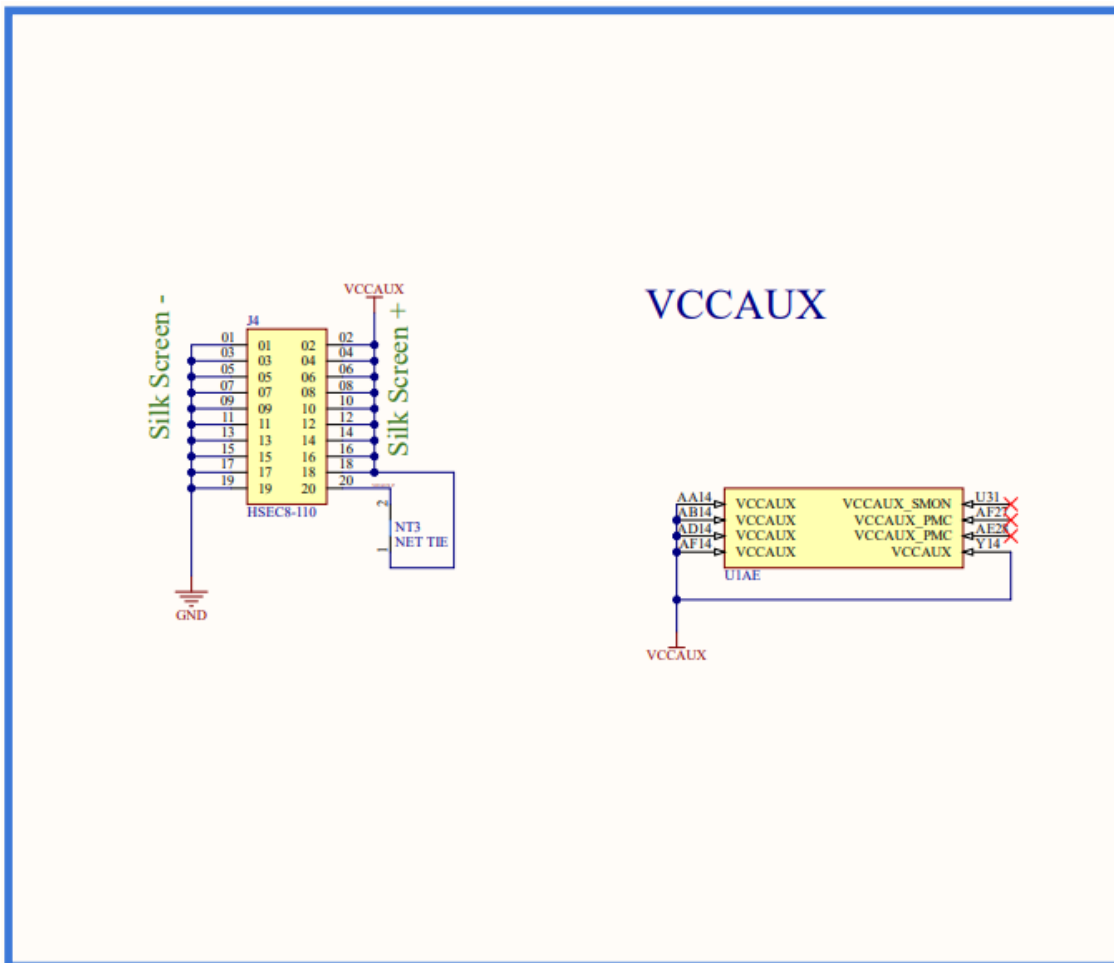


# Schematics

## VCCINT











# GND:

