

VC2602-PA-VSVH1760  
VC2802-PA-VSVH1760  
VE2602-PA-VSVH1760  
VE2802-PA-VSVH1760



## Xilinx Power Test Adaptor (PTA) - to test power delivery network (PDN) to Versal ACAP VSVH1760 series FPGA's

ProGrAnalog Corp.  
08/18/2023  
Rev 3.2

### Features

- Set of 3 Xilinx Power Test Adaptors (PTA) for PDN testing AMD Xilinx Versal VSVH1760 series FPGAs
- Options available for VC2602, VC2802, VE2602, VE2802
- 6 Samtec connectors to test: VCCINT, VCC\_IO, VCC\_SOC, VGTY\_AVTT, VCCAUX, AVCC
- 8 mini SMP connectors for measuring: VCCINT\_SENSE, GND\_SENSE, GND, VCC\_IO, VCC\_SOC, VGTY\_AVTT, VCCAUX, AVCC
- Xilinx PTA with BGA footprint reflows onto VSVH1760 PCB pads.
- Remote Vsense on Samtec connectors and SMP mini connectors.
- Most rails can be tested with an LSP200 controller.
- VCCINT >100A support with an LSP1000RS controller.
- GUI supports transient, pulse train, impedance and 3D plots.

### Typical Test Setup

- Xilinx PTA reflowed onto the test board.
- LSP1000RS connected into VCCINT connector.

Pack of 3 -VSVH1760 Series Xilinx PTA's



# LoadSlammer GUI

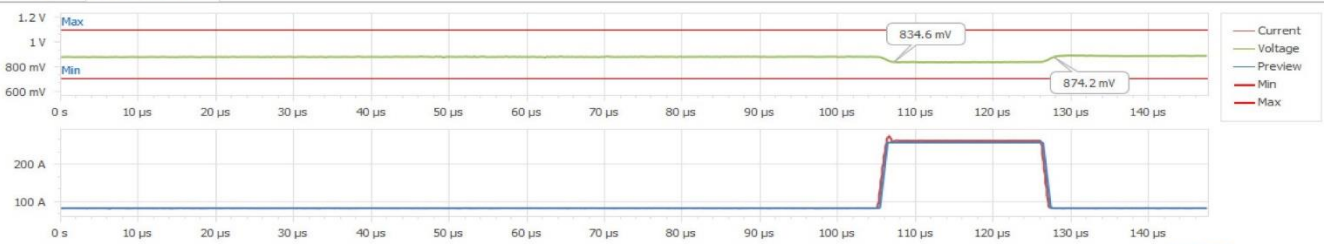
Workspace **Test - 1** x

**Available Tests** Name:  Rail:

- Transient Test**  
Transient load step with adjustable rise times, current, and pulse width.
- Pulse Train**  
Repeating load steps with a configurable frequency and duty cycle.
- Impedance (Z)**  
Large signal output impedance with adjustable current amplitude and offset.
- DC Load**  
DC Load with timer.
- Delay**  
Timed delay.

## Transient test

Workspace **Test - 1 - Main** x



Run

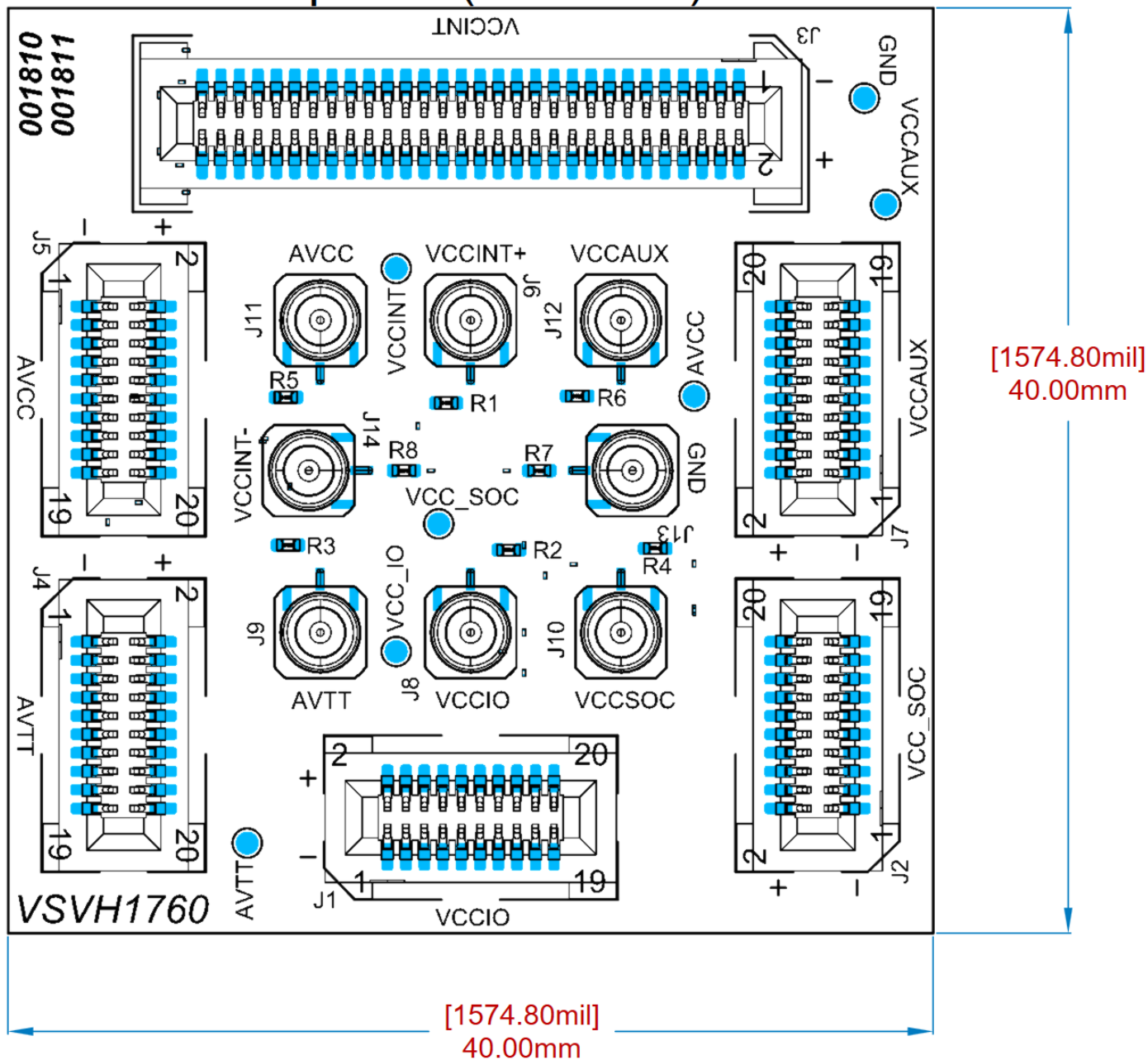
Text	Offset	Amp...	Time...	Mini...	Edge...	Index	Params	Pass	V <sub>droop</sub>	V <sub>thdOff</sub>
...	80 A	175 A	20 $\mu$ s	2.5 ms	1 $\mu$ s	1	Current: 175 A, EdgeTime: 1 $\mu$ s	✓	834.6 mV	873.6 mV
						2	Current: 175 A, EdgeTime: 1 $\mu$ s	✓	834.6 mV	874.2 mV

Type	Min	Avg	Max	Std Dev	PassRate

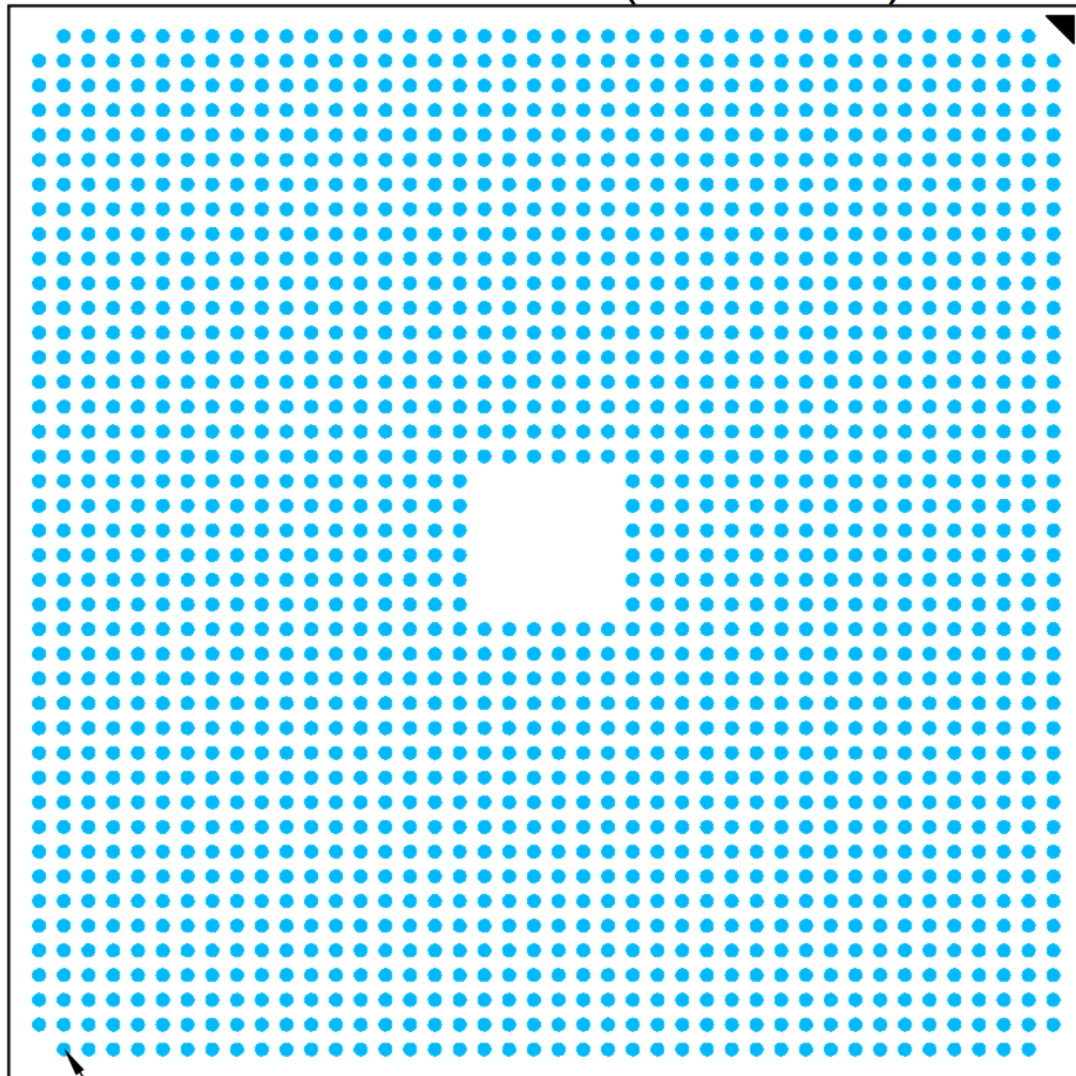


## Mechanical Specs

### View from Top side (Scale 3:1)



# View from Bottom side (Scale 3:1)



Pin 1 I.D.

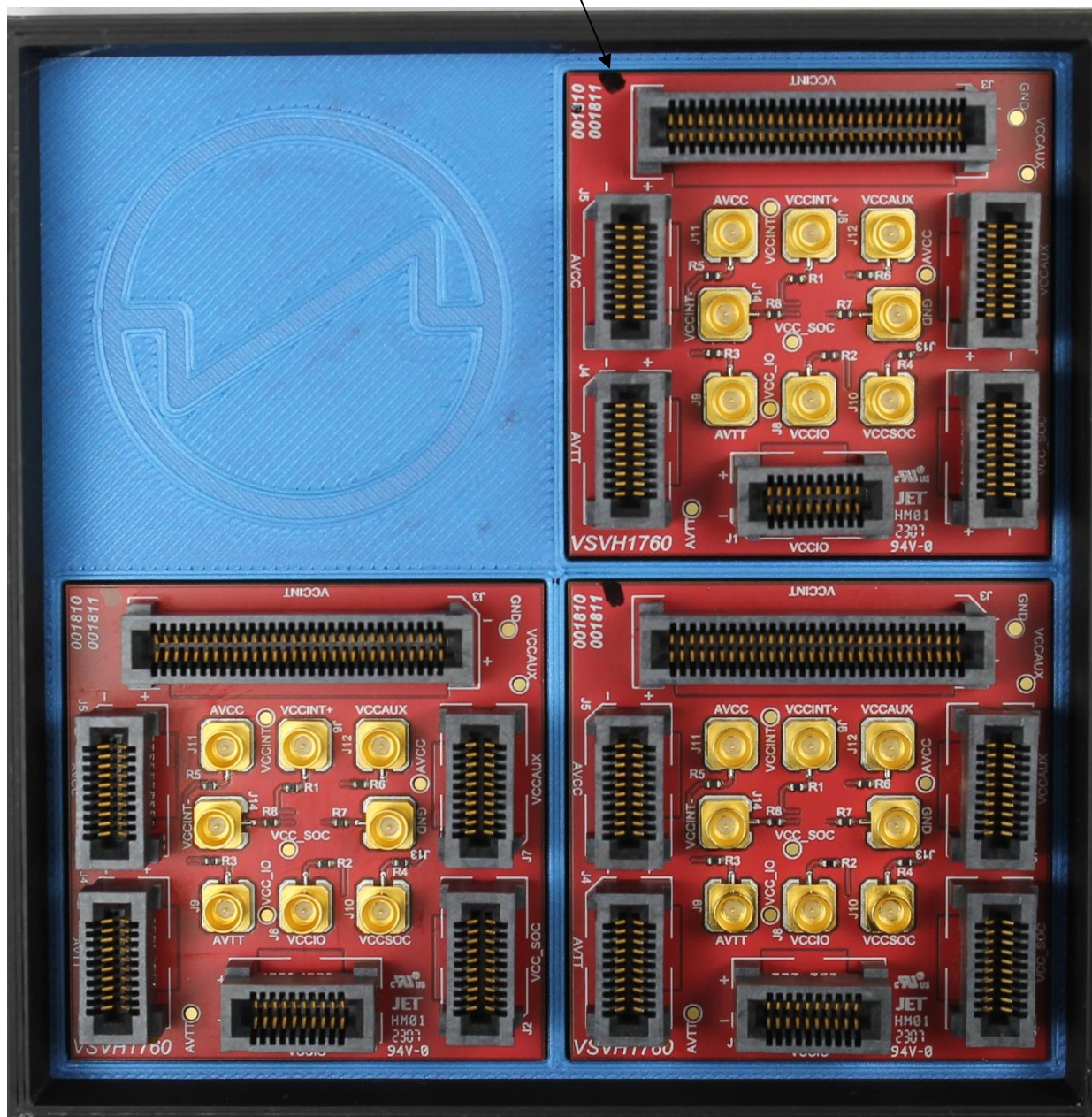
0.92mm BGA Pitch

**Sn96.5-Ag3.0-Cu0.5 0.6mm balls**

## Packing Tray Specs

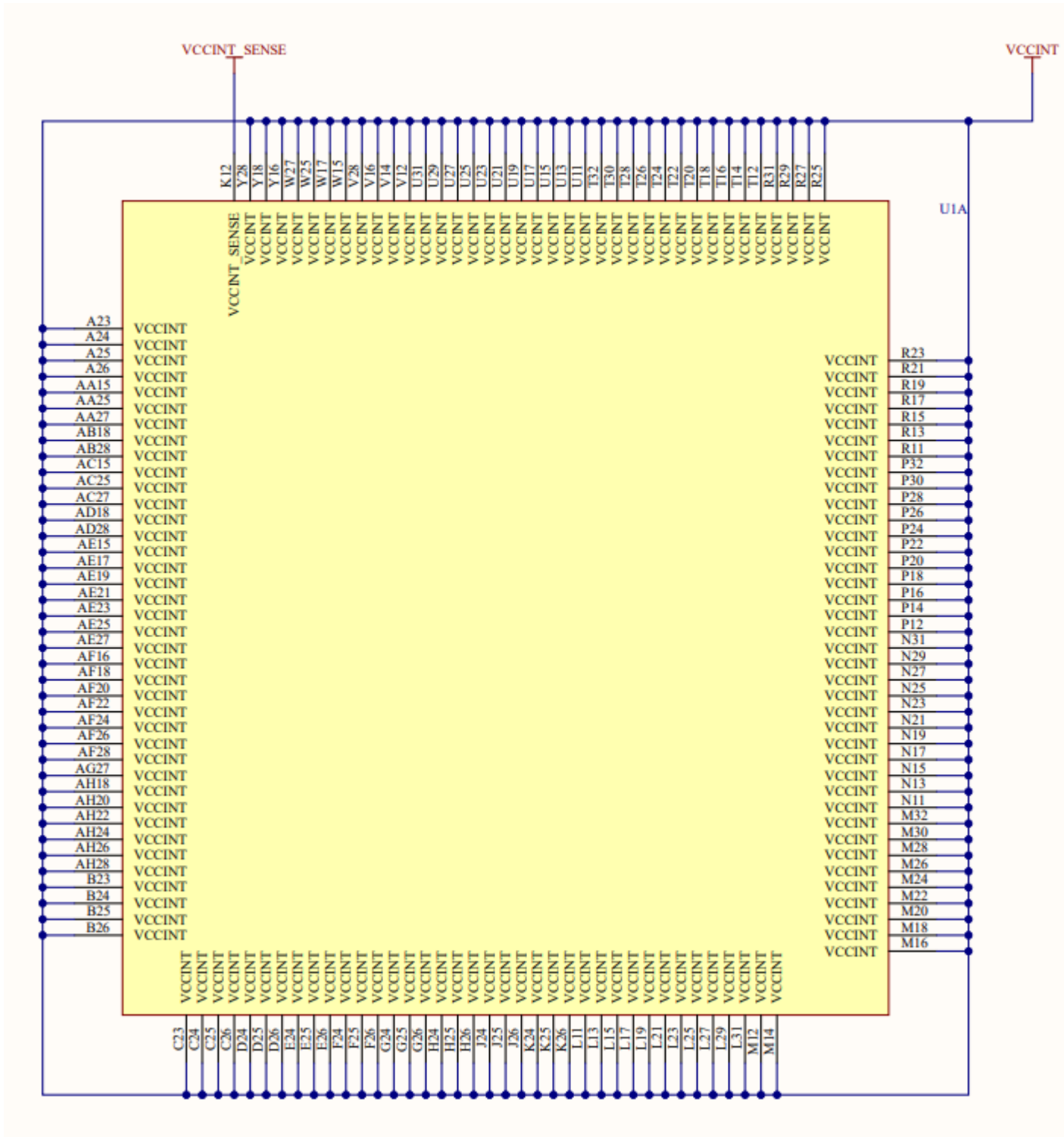
40x40mm package will have a 92x92x15mm tray

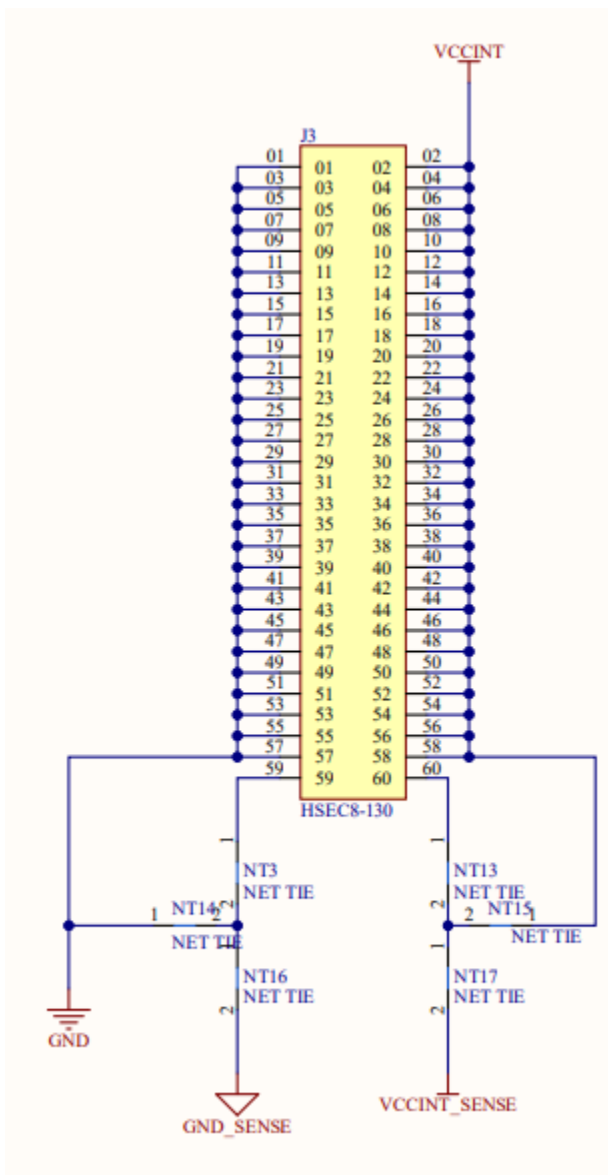
A1 marked - top left corner

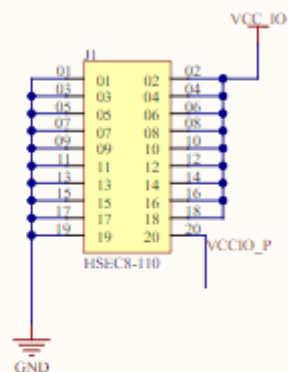
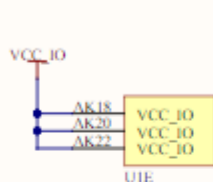




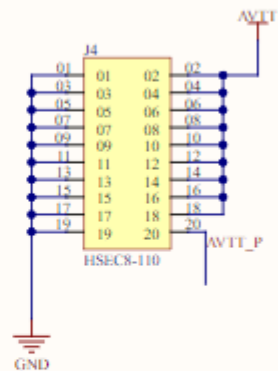
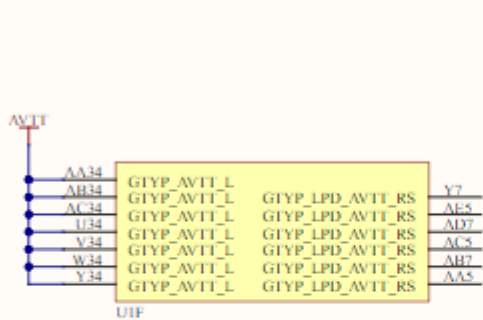
# Schematics



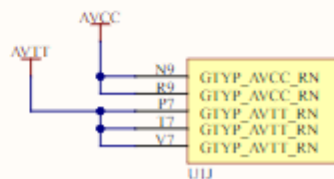




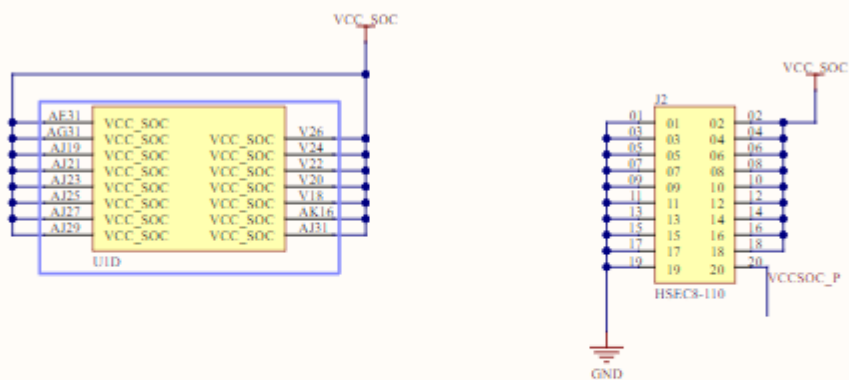
## VCC\_IO



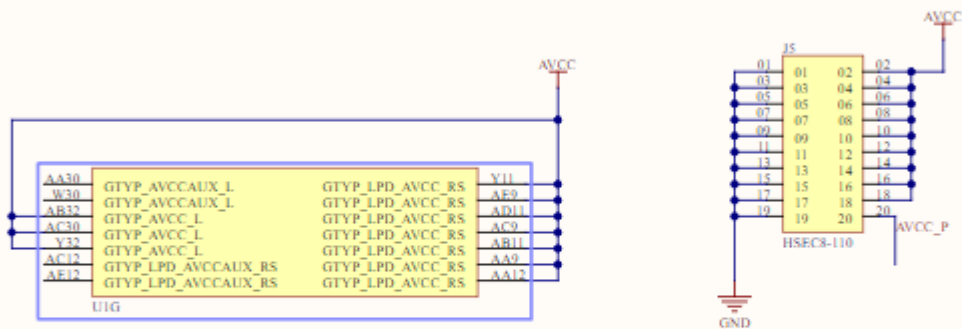
## AVTT







## VCC\_SOC

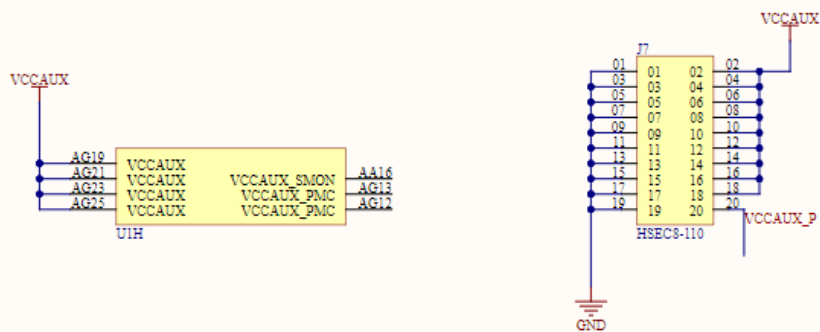


## AVCC

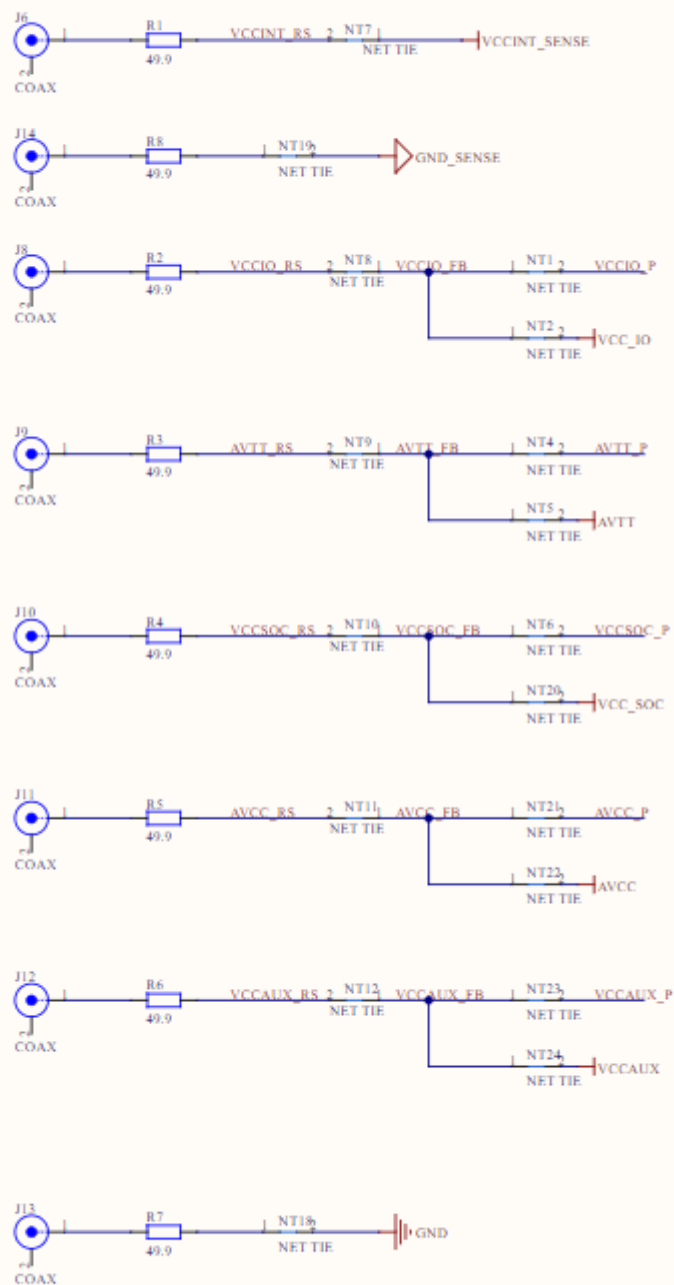
AD16	RSVDGND	VCC_PSPF	AI14
AD17	RSVDGND	VCC_PSPF	AI15
AH14	VCC_BATT	VCC_PSLP	AH17
AB14	VCC_CPMS	VCC_PSLP	AJ16
AD14	VCC_CPMS	VCC_PSLP	AJ17
AE14	VCC_CPMS	VCC_RAM	AB24
Y14	VCC_CPMS	VCC_RAM	AD24
AH12	VCC_FUSE	VCC_RAM	Y24
AH15	VCC_PMC	VP_500	AC17
AI13	VCC_PMC	VP_500	AB16
AI14	VCC_PMC	VREFN_500	AB17
AK15	VCC_PSPF	VREFP_500	AC18

UIH

## VCC MISC



## VCCAUX



# COAX SMP

