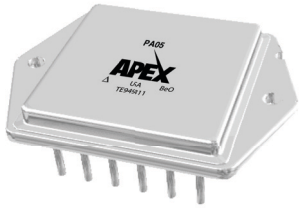
PA05

Power Operational Amplifier

RoHS COMPLIANT

FEATURES



- High Internal Dissipation — 250 Watts
- High Voltage, High Current — 100V, 30A
- High Slew Rate — 100V/µs
- 4 Wire Current Limit Sensing
- Low Distortion
- External Shutdown Control
- Optional Boost Voltage Inputs
- Evaluation Kit — see EK45

APPLICATIONS

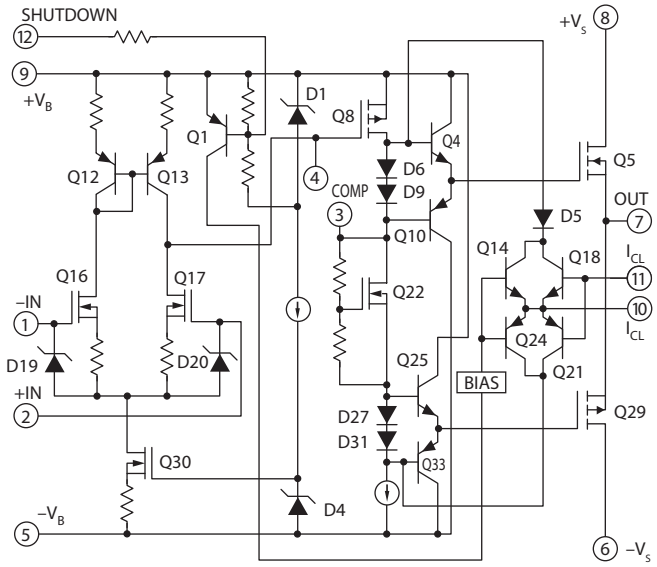
- Linear And Rotary Motor Drives
- Sonar Transducer Driver
- Yoke/magnetic Field Excitation
- Programmable Power Supplies To ±45V
- Audio up to 500W

DESCRIPTION

The PA05 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

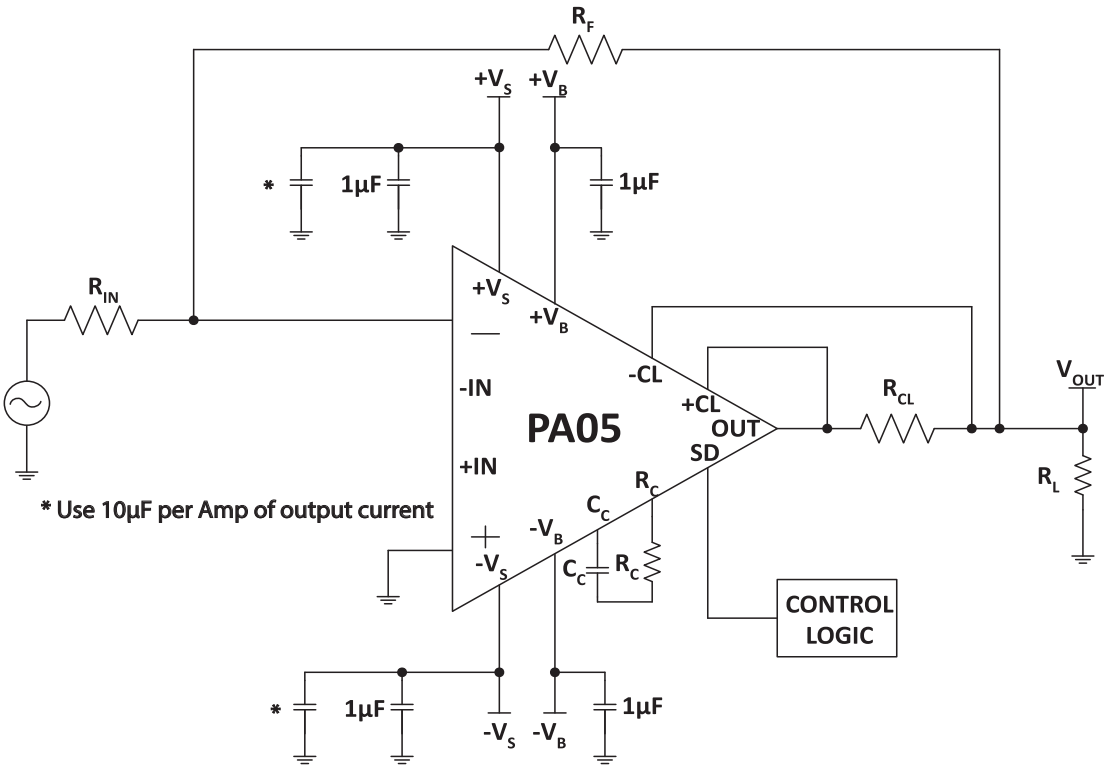
The PA05 is a highly flexible amplifier. The shutdown control feature allows the output stage to be turned off for standby operation or load protection during fault conditions. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors slew rate and bandwidth performance to user needs. A four wire sense technique allows precision current limiting without the need to consider internal or external mΩ parasitic resistance in the output line. The output stage is protected by thermal limiting circuits above junction temperatures of 175°C.

Figure 1: Equivalent Schematic



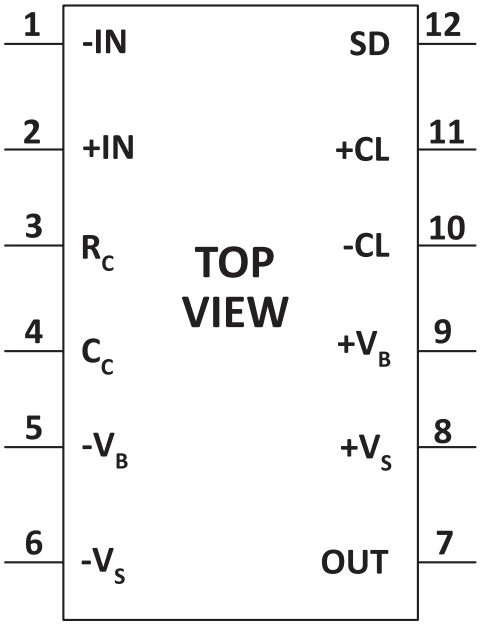
TYPICAL CONNECTION

Figure 2: Typical Connections



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	-IN	The inverting input.
2	+IN	The non-inverting input.
3	R_C	Compensation resistor connection. Select value based on Phase Compensation. See applicable section.
4	C_C	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.
5	$-V_B$	The negative boost supply rail. Short to $-V_S$ if unused. See applicable section.
6	$-V_S$	The negative supply rail.
7	OUT	The output. Connect this pin to load and to the feedback resistors through R_{CL}.
8	$+V_S$	The positive supply rail.
9	$+V_B$	The positive boost supply rail. Short to $+V_S$ if unused. See applicable section.
10	-CL	Connect to the load side of the current limit resistor. Current limit will activate as the voltage across R_{CL} increases.
11	+CL	Connect to the OUT side of the current limit resistor. Current limit will activate as the voltage across R_{CL} increases.
12	SD	The shutdown activation pin. See applicable section.

SPECIFICATIONS

Unless otherwise noted: T_C = 25°C, C_C = 470pF, R_C = 120 Ω. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_B = \pm V_S$.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_s$ to $-V_s$		100	V
Boost Voltage	$\pm V_B$	$-V_s$ - 20	$+V_s$ + 20	V
Output Current, continuous within SOA	I_{OUT}		30	A
Power Dissipation, internal	P_D		250	W
Input Voltage, differential	$V_{IN\ (Diff)}$	-20	20	V
Input Voltage, common mode	V_{CM}	$-V_B$	V_B	V
Temperature, pin solder, 10s			350	°C
Temperature, junction [1]	T_J		175	°C
Temperature, storage		-65	+150	°C
Operating Temperature Range, case	T_c	-55	+125	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.

CAUTION The PA05 is constructed from MOSFET transistors. ESD handling procedures must be observed. The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA05			PA05A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial			5	10		2	5	mV
Offset Voltage vs. temperature	Full temp range		20	50		10	30	µV/°C
Offset Voltage vs. supply			10	30		*	*	µV/V
Offset Voltage vs. power	Full temp range		30			10		µV/W
Bias Current, initial			10	50		5	20	pA
Bias Current vs. supply			0.01			*		pA/V
Offset Current, initial			10	50		5	20	pA
Input Impedance, DC			10^{11}			*		Ω
Input Capacitance			13			*		pF
Common Mode Voltage Range	Full temp range	$\pm V_B - 8$			*			V
Common Mode Rejection, DC	Full temp range, V_{CM} = ±20V	90	100		*	*		dB
Input Noise	100 kHz BW, R_S = 1 kΩ		10			*		µVrms

GAIN

Parameter	Test Conditions	PA05			PA05A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop, @ 15 Hz	Full temp range, C_C = 82pF	94	102		*	*		dB
Gain Bandwidth Product	R_L = 10 Ω		3			*		MHz
Power Bandwidth	R_L = 4 Ω, V_{OUT}= 80V_{P-P}, A_V = –10, C_C = 82pF, R_C= 120 Ω		400			*		kHz
Phase Margin	Full temp range, C_C = 470pF		60			*		°

OUTPUT

Parameter	Test Conditions	PA05			PA05A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing	I_{OUT} = 20A	$\pm V_S$–9.5	$\pm V_S$–8.7		*	*		V
Voltage Swing	V_B =Vs + 5V, I_{OUT} = 30A	$\pm V_S$–5.8	$\pm V_S$–5.0		*	*		V
Current, peak		30			*			A
Settling Time to 0.1%	A_V = +1, 10V step, R_L = 4 Ω		2.5			*		µs
Slew Rate	A_V = –10, C_C = 82pF, R_C = 120 Ω	80	100		*	*		V/µs
Capacitive Load	Full temp range, A_V = +1	2.2			*			nF
Resistance	I_{OUT} = 0, No load, 2 MHz		5			*		Ω
	I_{OUT} = 1A, 2 MHz		2			*		Ω

POWER SUPPLY

Parameter	Test Conditions	PA05			PA05A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage	Full temp range	±15	±45	±50	*	*	*	V
Current, quiescent, boost supply			46	56		*	*	mA
Current, quiescent, total			90	120		*	*	mA
Current, quiescent, total, shut-down			46	56		*	*	mA

THERMAL

Parameter	Test Conditions	PA05			PA05A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case [1]	Full temp range, F>60 Hz		0.3	0.4		*	*	°C/W
Resistance, DC, junction to case	Full temp range, F<60 Hz		0.4	0.5		*	*	°C/W
Resistance, junction to air [2]	Full temp range		12			*		°C/W
Temperature Range, case	Meets full range specs	-25		85	*		*	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
2. The PA05 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.

Note: *The specification of PA05A is identical to the specification for PA05 in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

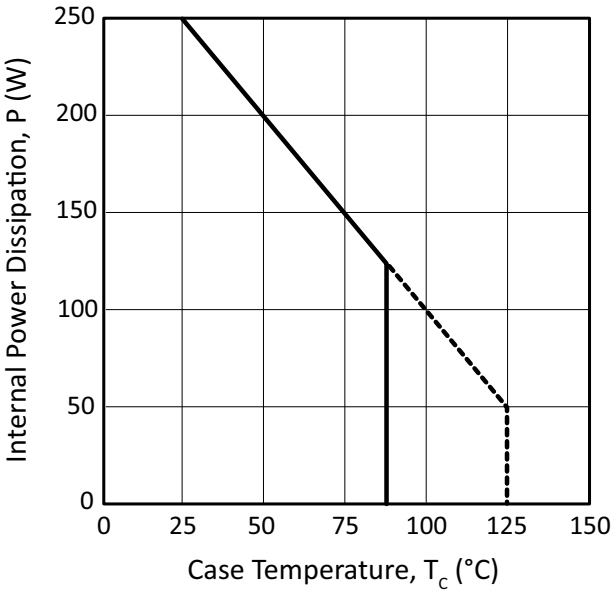


Figure 5: Power Supply Rejection

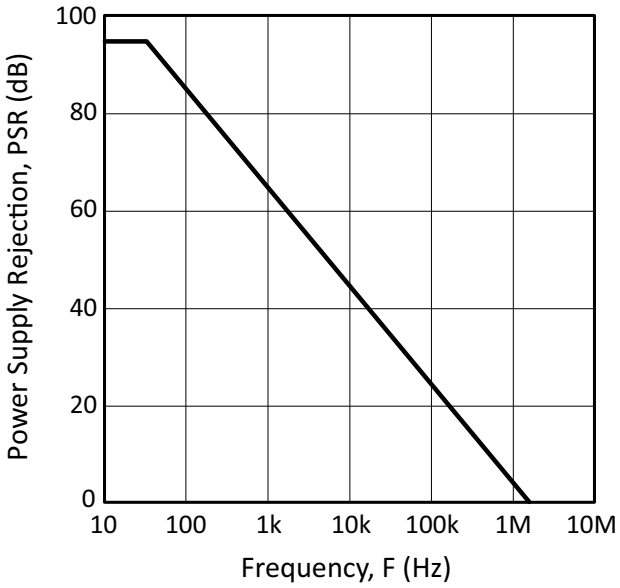


Figure 6: Small Signal Response

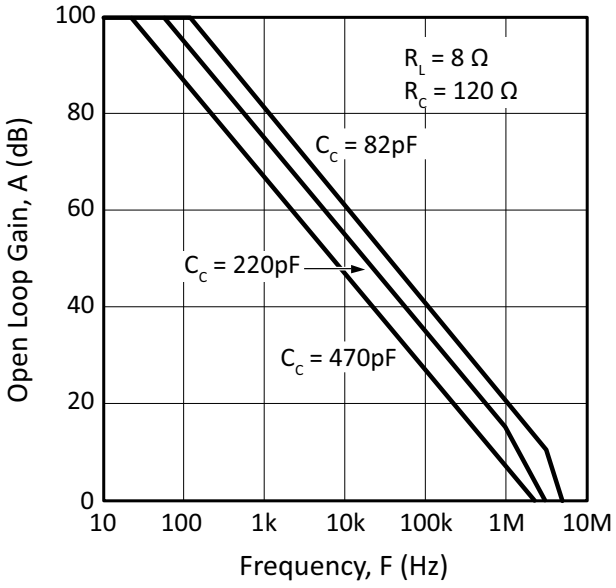


Figure 7: Phase Response

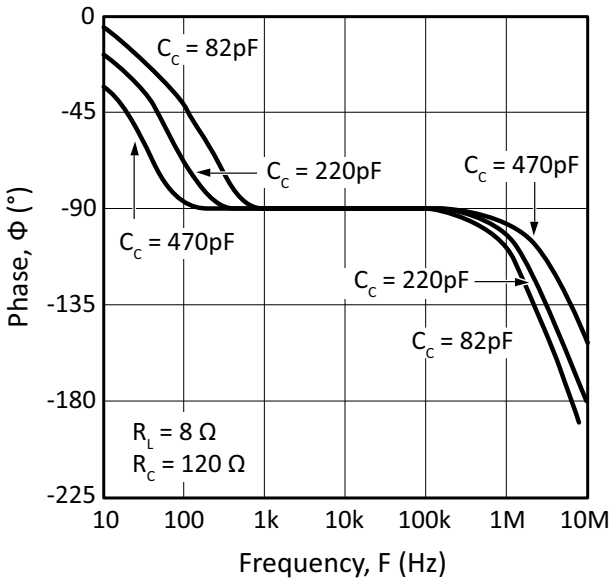


Figure 8: Slew Rate vs. Comp

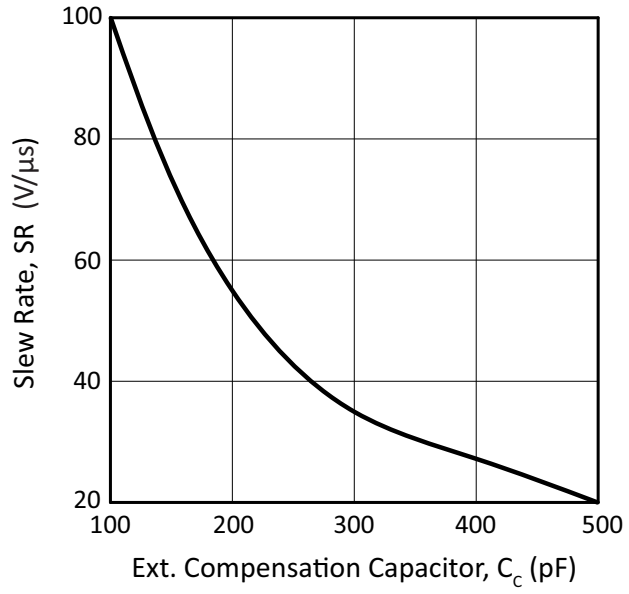


Figure 9: Output Voltage Swing

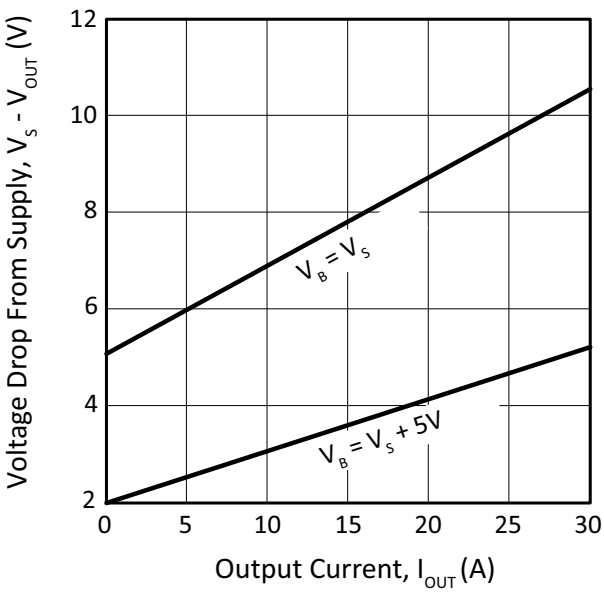


Figure 10: Common Mode Rejection

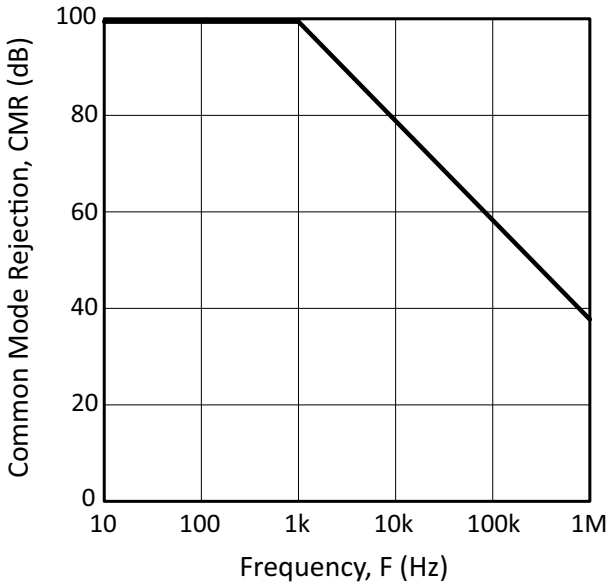


Figure 11: Pulse Response

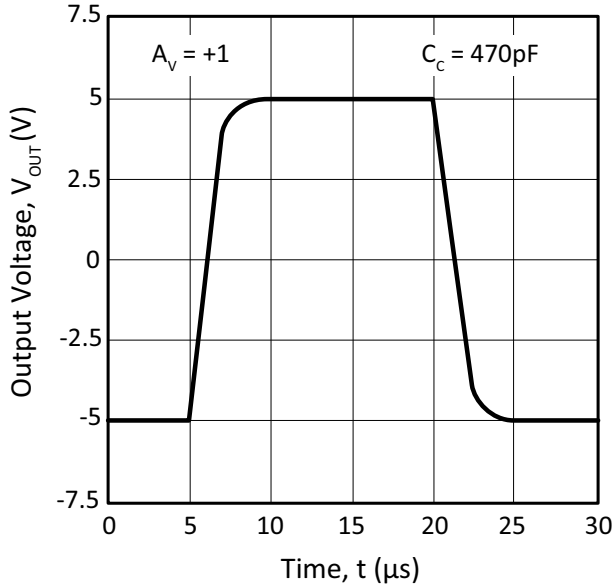


Figure 12: Current Limit

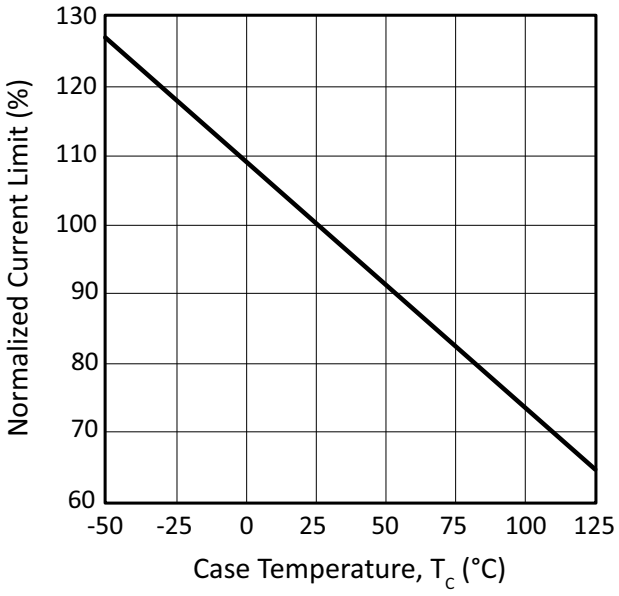


Figure 13: Harmonic Distortion

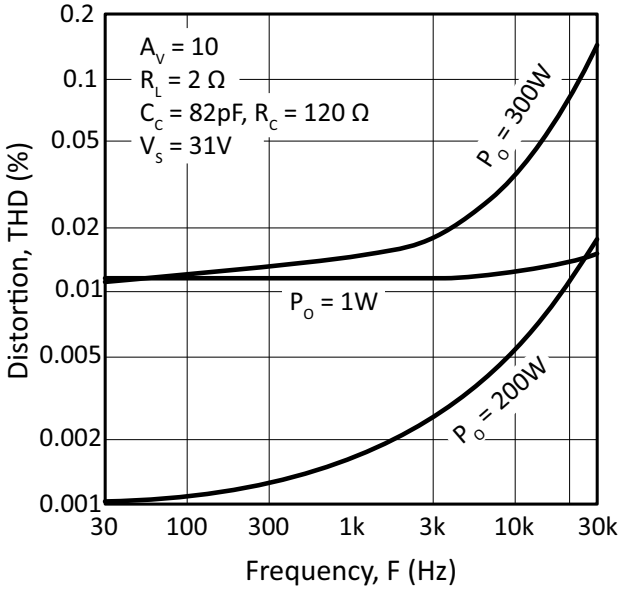


Figure 14: Quiescent Current

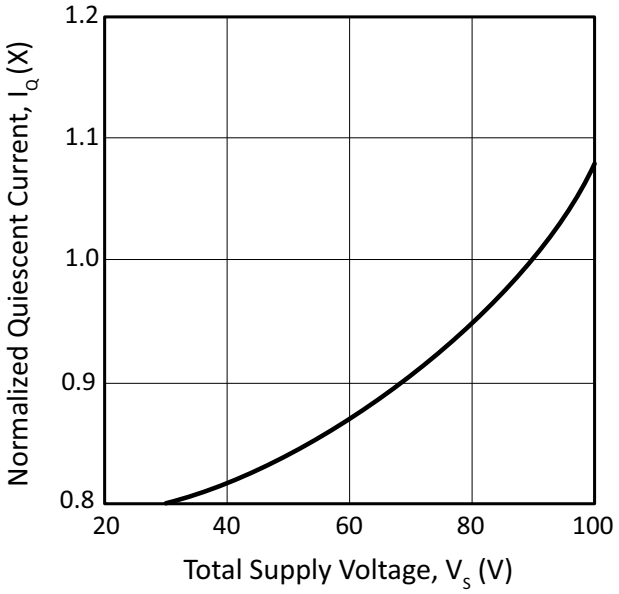
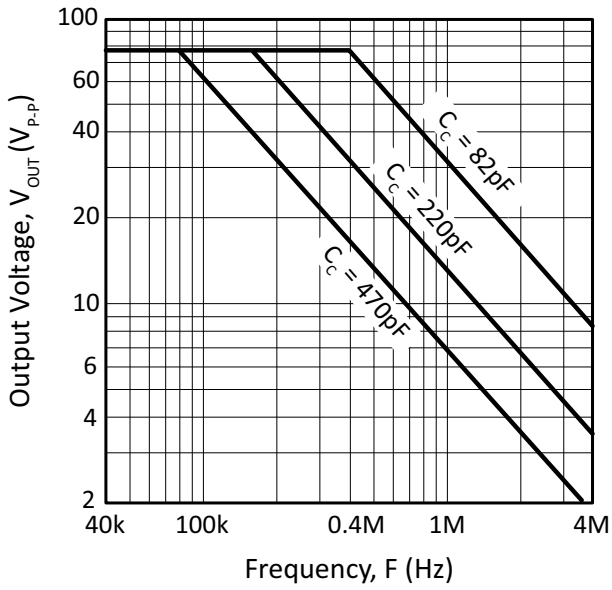


Figure 15: Power Response



SAFE OPERATING AREA (SOA)

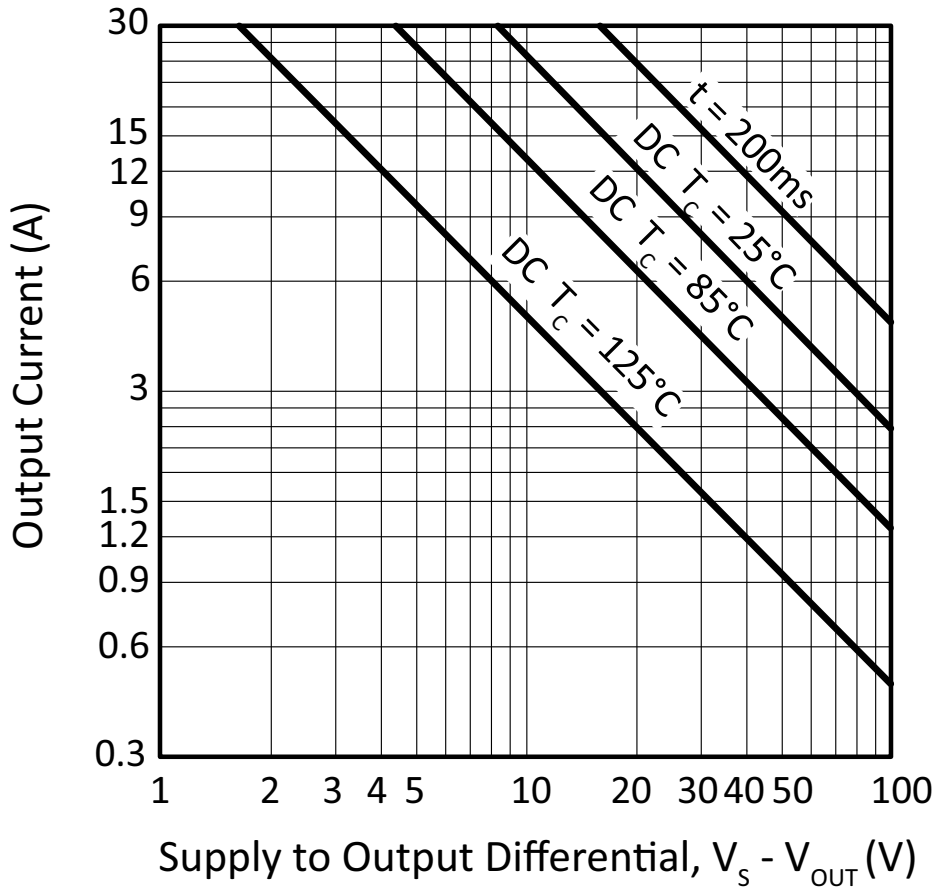
The output stage thermal protection circuit engages when junction temperatures reach approximately 175°C. If the condition remains that caused the shutdown, the amplifier may oscillate in and out of shutdown, creating high peak power stresses reducing the reliability of the device.

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

Note: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

Figure 16: SOA



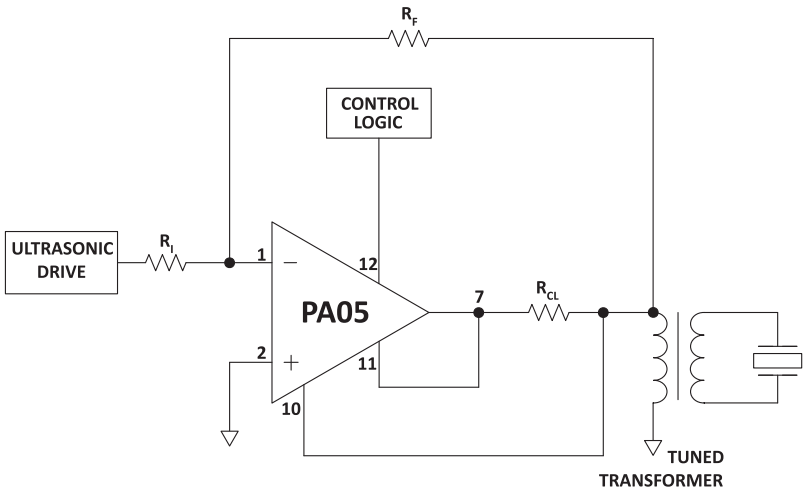
GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

The high power bandwidth of the PA05 allows driving sonar transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the PA05. Control logic turns off the amplifier's output during shutdown.

Figure 17: Typical Application



PHASE COMPENSATION

Gain	C_C*	R_C
1	470pF	120 Ω
>3	220pF	120 Ω
≥10	82pF	120 Ω

C_C rated for full supply voltage

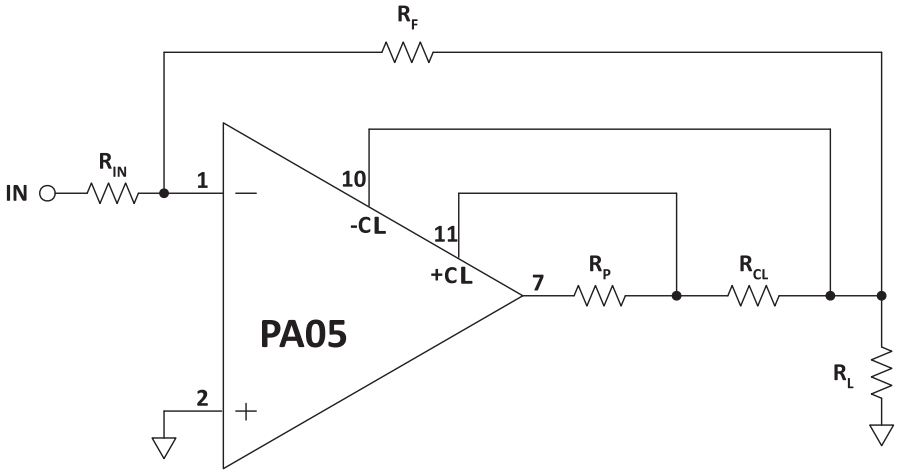
*See Boost Operation paragraph.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly, pin 11 must be connected to the amplifier output side and pin 10 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 18. This connection will bypass any parasitic resistances, R_P formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 18. If current limiting is not used, pins 10 and 11 must be tied to pin 7.
The value of the current limit resistor can be calculated as follows:

$$R_{CL}(\Omega) = \frac{0.7V}{I_{CL}(A)}$$

Figure 18: Current Limit

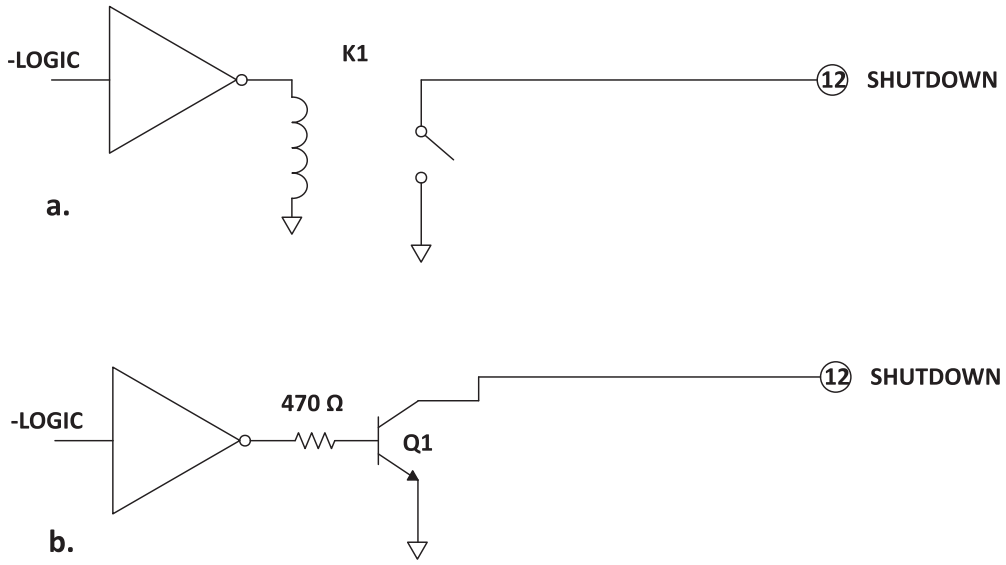


SHUTDOWN OPERATION

To disable the output stage, pin 12 is connected to ground via relay contacts or via an electronic switch. The switching device must be capable of sinking 2mA to complete shutdown and capable of standing off the supply voltage $+V_S$. See Figure 19 for suggested circuits.

From an internal circuitry standpoint, shutdown is just a special case of current limit where the allowed output current is zero. As with current limit, however, a small current does flow in the output during shutdown. A load impedance of 100 Ω or less is required to insure the output transistors are turned off. Note that even though the output transistors are off the output pin is not open circuited because of the shutdown operating current.

Figure 19: Shutdown Operation



BOOST OPERATION

With the V_B feature, the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_B$ (pin 9), and $-V_B$ (pin 5) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 8) and $-V_S$ (pin 6) are connected to the high current output stage. An additional 5V on the V_B pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required, the $+V_B$ and $+V_S$ pins must be strapped together as well as the $-V_B$ and $-V_S$ pins. The V_B pins must not be at a voltage lower than the V_S pins.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 3 and 4. Unity gain stability can be achieved at any compensation capacitance greater than 470 pF with at least 60 degrees of phase margin. At higher gains, more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C and R_C for the application.