PA08 • PA08A

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- Wide Supply Range — ±15V to ±150V
- Programmable Output Current Limit
- Output Current — Up to ±150mA
- Low Bias Current — FET Input

APPLICATIONS

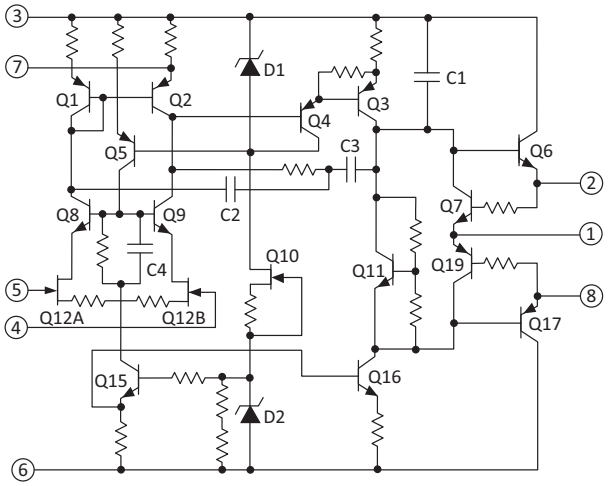
- High Voltage Instrumentations
- Electrostatic Transducers & Deflection
- Programmable Power Supplies up to 290V
- Analog Simulators 4 - 20mA

DESCRIPTION

The PA08 is a high voltage operational amplifier designed for output voltage swings of up to ±145V with a dual (±) supply or 290V with a single supply. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA08 features an unprecedented supply range and excellent supply rejection. The output stage is biased-on for linear operation. Internal phase compensation assures stability at all gain settings. The safe operating area (SOA) can be observed with all types of loads by choosing the appropriate current limiting resistors. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid integrated circuit utilizes beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque will void the product warranty. Please see Application Note 1, “General Operating Considerations.”

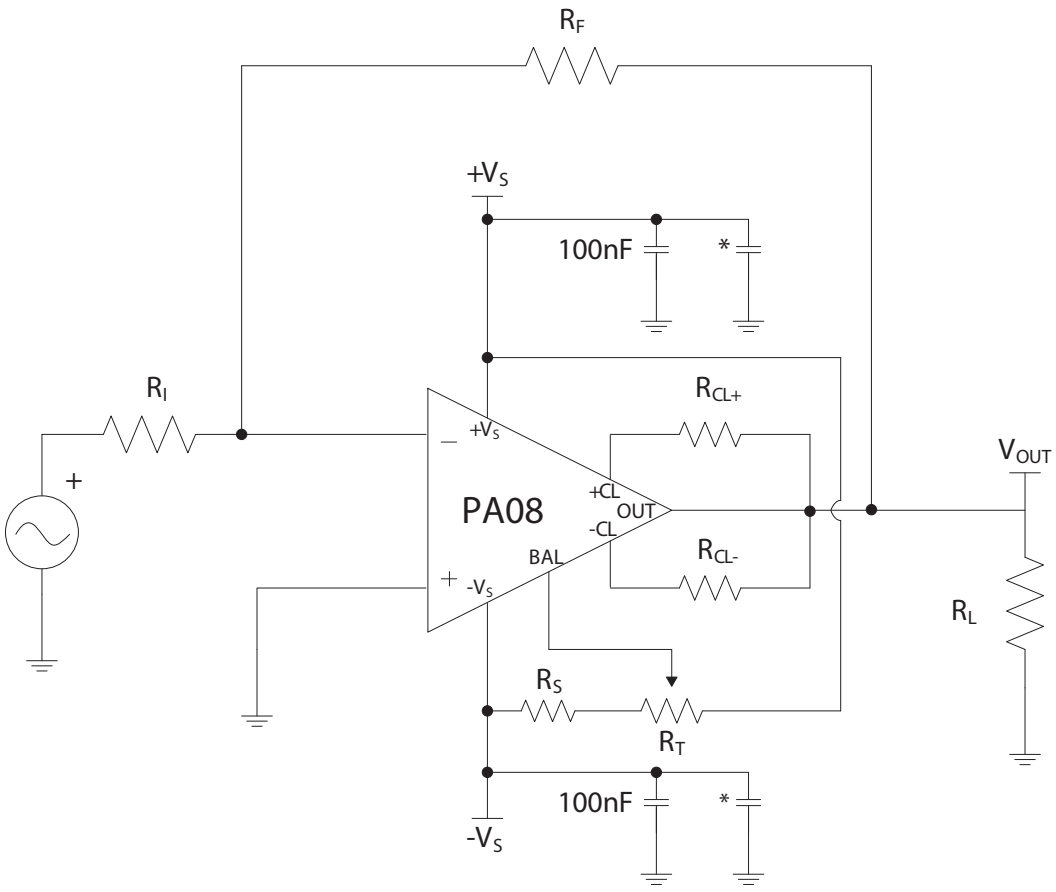
Figure 1: Equivalent Schematic



TYPICAL CONNECTIONS

Figure 2: Typical Connections

$$R_S = (|+V_S| + |-V_S|)\, R_T / 1.6$$

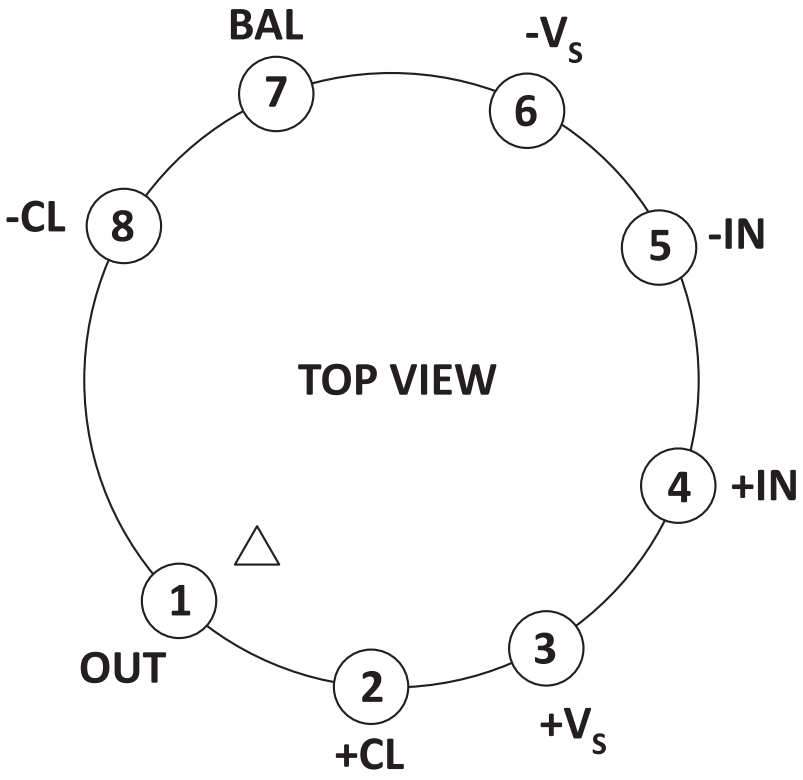


Note: Input offset voltage trim optional. R_T = 10 kΩ MAX.

*Use 10µF per Amp of output current.

PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	OUT	The output. Connect this pin to load and to the feedback resistors.
2	+CL	Connect to the sourcing current limit resistor. Output current flows out of this pin through R_{CL+}. The output pin and the load are connected to the other side of R_{CL+}.
3	+Vs	The positive supply rail.
4	+IN	The non-inverting input.
5	-IN	The inverting input.
6	-Vs	The negative supply rail.
7	BAL	Balance Control pin. Adjusts voltage offset. See applicable section.
8	-CL	Connect to the sinking current limit resistor. Output current flows into this pin through R_{CL-}. The output pin and the load are connected to the other side of R_{CL-}.

SPECIFICATIONS

The power supply voltage specified under typical (TYP) applies unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_S$ to $-V_S$		300	V
Output Current, within SOA	I_O		200	mA
Power Dissipation, internal @ T_C = 25°C	P_D		17.5	W
Input Voltage, differential	$V_{IN\ (Diff)}$	-50	50	V
Input Voltage, common mode	V_{cm}	$-V_S$	V_S	V
Temperature, pin solder, 10s max.			350	°C
Temperature, junction [1]	T_J		175	°C
Temperature Range, storage		-65	+150	°C
Operating Temperature Range, case	T_C	-55	+125	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA08			PA08A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial	T_C =25°C		±0.5	±2		±0.25	±0.5	mV
Offset Voltage vs. Temperature	T_C =-25 to +85°C		±15	±30		±5	±10	µV/°C
Offset Voltage vs. Supply	T_C =25°C		±0.5			*	2	µV/V
Offset Voltage vs. Time	T_C =25°C		±75			*		µV/√kh
Bias Current, initial [1]	T_C =25°C		5	50		3	10	pA
Bias Current vs. Supply	T_C =25°C		0.01			*		pA/V
Offset Current, initial [1]	T_C =25°C		±2.5	±50		±1.5	±10	pA
Input Impedance, DC	T_C =25°C		10^{11}			*		Ω
Input Capacitance	T_C =25°C		4			*		pF
Common Mode Voltage Range[2]	T_C =-25 to +85°C	$\pm V_S$-10			*			V
Common Mode Rejection, DC	T_C =-25 to +85°C, V_{CM}= ±90V		130			*		dB

1. Doubles for every 10°C of temperature increase.
2. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.

GAIN

Parameter	Test Conditions	PA08			PA08A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop Gain @ 10 Hz	T_C = 25°C, R_L= ∞		118			*		dB
Open Loop Gain @ 10 Hz	T_C = 25°C, R_L = 1.2 kΩ	96	111		*	*		dB
Gain Bandwidth Product at 1MHz	T_C = 25°C, R_L = 1.2 kΩ		5			*		MHz
Power Bandwidth	T_C = 25°C, R_L= 1.2 kΩ		90			*		kHz
Phase Margin	T_C =-25 to +85°C		60			*		°

OUTPUT

Parameter	Test Conditions	PA08			PA08A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing [1]	T_C = 25°C, I_O= 150mA	$\pm V_S$-15	$\pm V_S$-8		*	*		V
Voltage Swing [1]	T_C =-25 to +85°C, I_O= ±75mA	$\pm V_S$-10	$\pm V_S$-5		*	*		V
Voltage Swing [1]	T_C =-25 to +85°C, I_O= ±20mA	$\pm V_S$-5	$\pm V_S$-3		*	*		V
Current, peak	T_C = 85°C	150			*			mA
Slew rate	T_C = 25°C		30		20	*		V/µs
Capacitive Load, A_V = 1	T_C =-25 to +85°C			10			*	nF
Capacitive Load, A_V > 4	T_C =-25 to +85°C			SOA			*	
Settling Time to 0.1%	T_C = 25°C, R_L= 1.2 kΩ, 2V step		1			*		µs

1. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.

POWER SUPPLY

Parameter	Test Conditions	PA08			PA08A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage	T_C=-55 to +125°C	±15	±100	±150	*	*	*	V
Current, quiescent	T_C = 25°C		6	8.5		*	*	mA

THERMAL

Parameter	Test Conditions	PA08			PA08A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case[1]	T_C=-55 to +125°C F > 60 Hz		4.26			*		°C/W
Resistance, DC, junction to case	T_C=-55 to +125°C F < 60 Hz		6.22	8.57		*	*	°C/W
Resistance, junction to air	T_C=-55 to +125°C		30			*		°C/W
Temperature Range, case	Meets full range specification	-25		85	*		*	°C

1. Rating applies only if output current alternates between both output transistors at a rate faster than 60 Hz.

Note: * The specification of PA08A is identical to the specification for PA08 in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

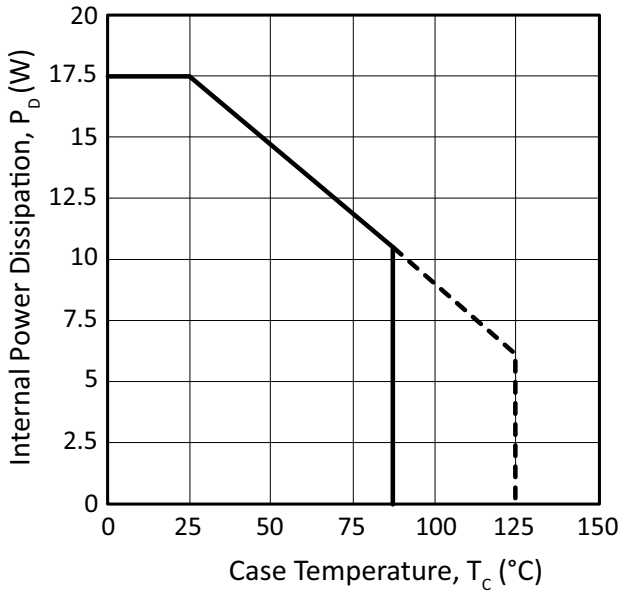


Figure 5: Current Limit

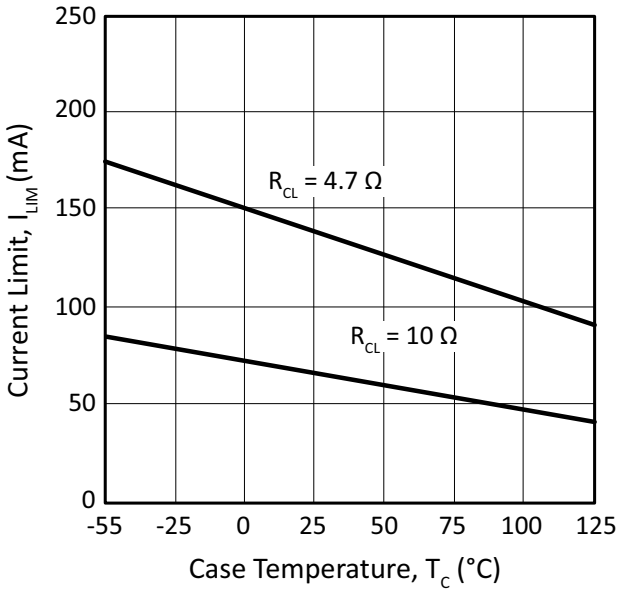


Figure 6: Small Signal Response

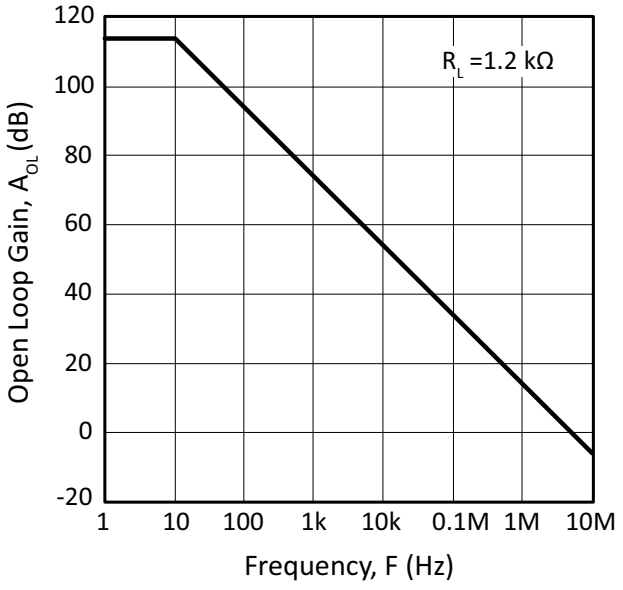


Figure 7: Phase Response

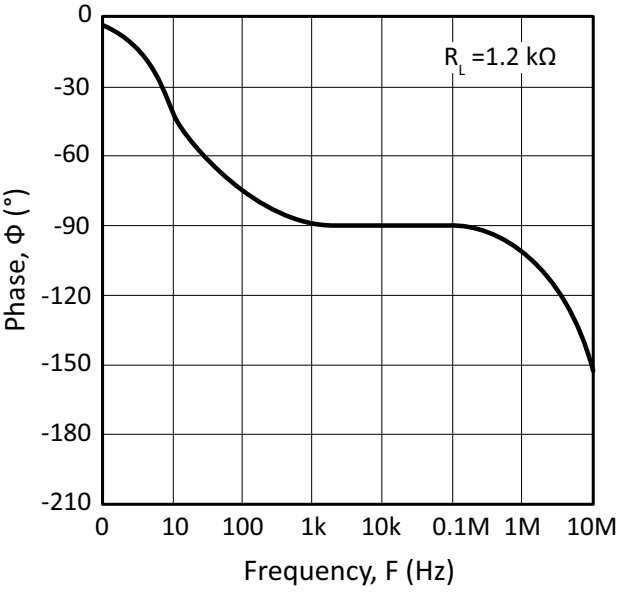


Figure 8: Open Loop Gain

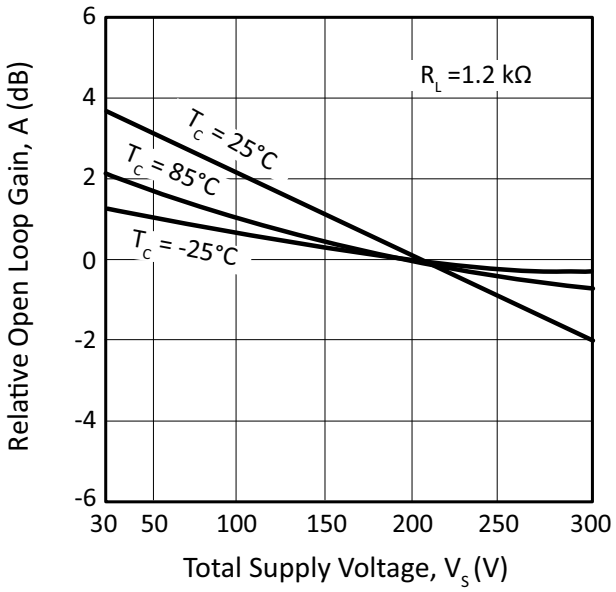


Figure 9: Power Response

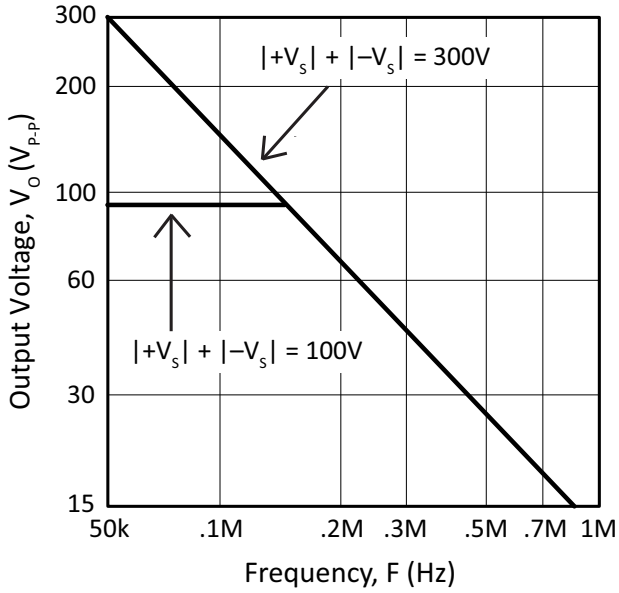


Figure 10: Pulse Response

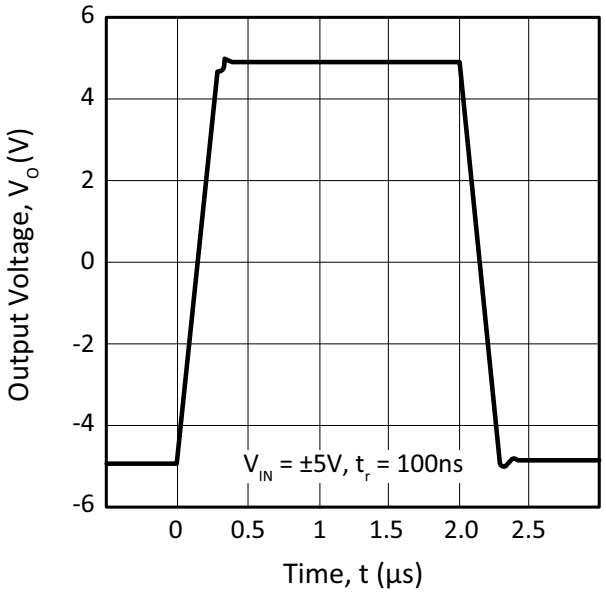


Figure 11: Slew Rate

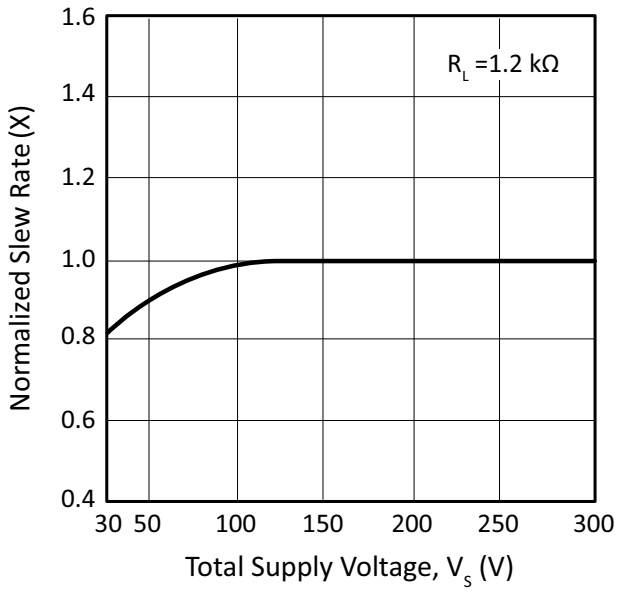


Figure 12: Input Noise

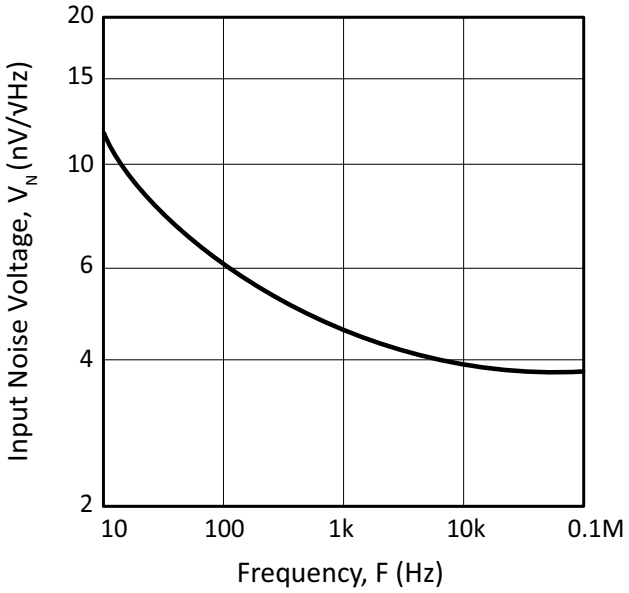


Figure 13: Common Mode Rejection

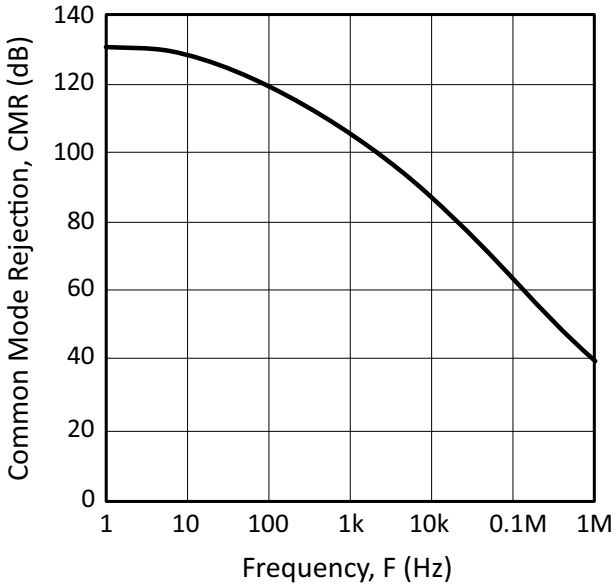


Figure 14: Power Supply Rejection

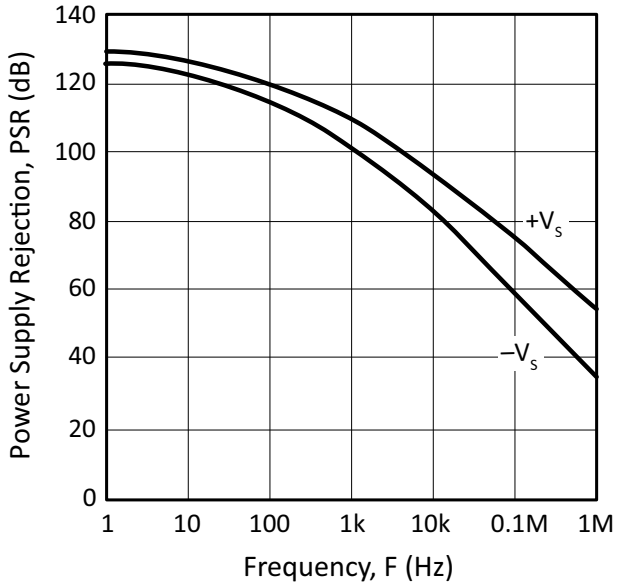
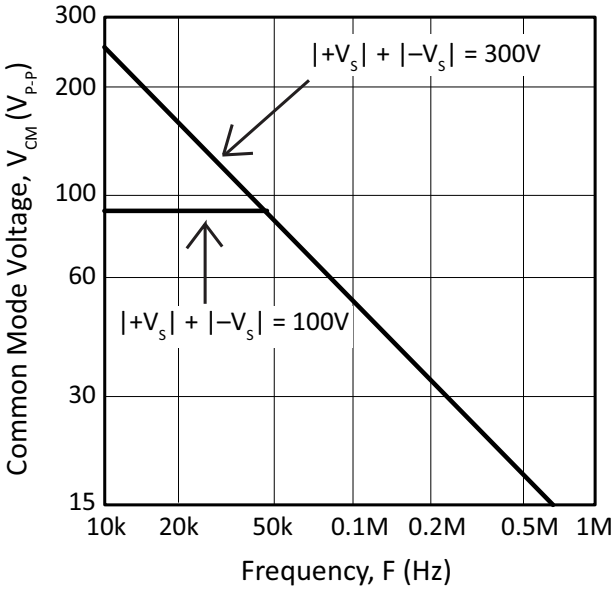


Figure 15: Common Mode Voltage



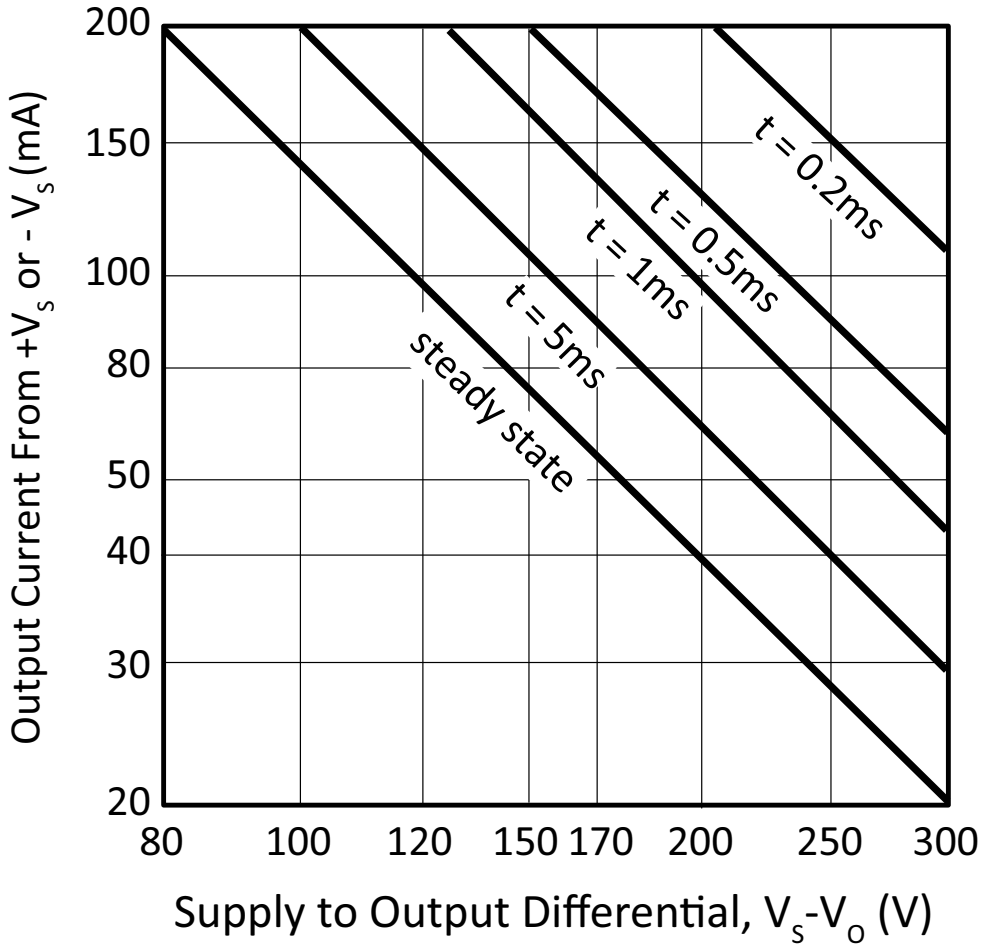
SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has two distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the guidelines on the next page may save extensive analytical efforts.

Figure 16: SOA



1. Under transient conditions, the following capacitive and inductive loads are safe with the current limits set to the maximum:

$\pm V_S$	C (Max)	L (Max)
150V	0.4µF	280 mH
125V	0.9µF	380 mH
100V	2µF	500 mH
75V	10µF	1200 mH
50V	100µF	13 H

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or simple shorts to common if the current limits are set as follows:

$\pm V_S$	Short to C, L, or EMF Load	Short to Common
150V	20mA	67mA
125V	27mA	90mA
100V	42mA	130mA
75V	67mA	200mA
50V	130mA	200mA

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

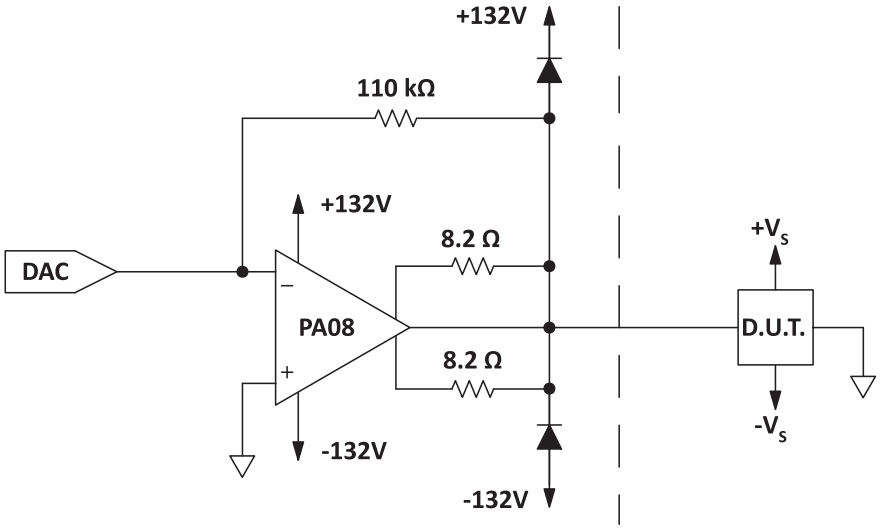
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

Figure 17: Typical Application (ATE Pin Driver)



The PA08 as a pin driver is capable of supplying high test voltages to a device under test (DUT). Due to the possibility of short circuits to any terminal of the DUT, current limit must be set to be safe when limiting with a supply to output voltage differential equal to the amplifier supply plus the largest magnitude voltage applied to any other pin of the DUT. In addition, flyback diodes are recommended when the output of the amplifier exits any equipment enclosure to prevent damage due to electrostatic discharges. Refer to Application Note 7 for details on accuracy considerations of this circuit.

INDUCTIVE LOADS

Two external diodes as shown in Figure 18, are required to protect these amplifiers from flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

INPUT PROTECTION

The input is protected against common mode voltages up to the supply rails and differential voltages up to ±50V. Increased protection against differential input voltages can be obtained by adding 2 resistors, 2 capacitors and 4 diode connected FETs as shown in Figure 19.

Figure 18: Protection, Inductive Load

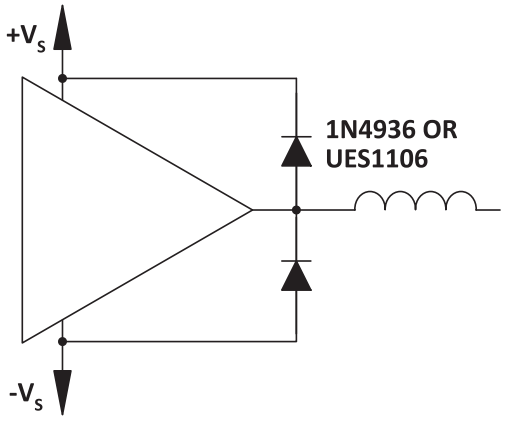
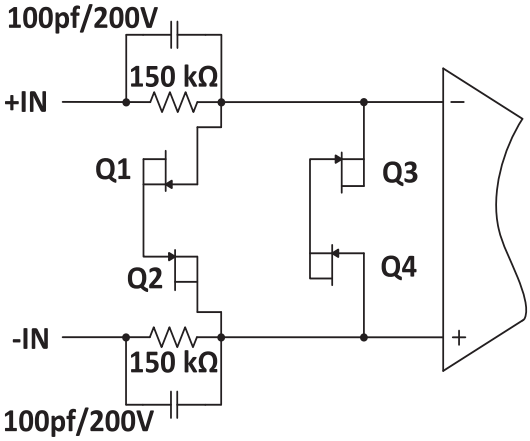


Figure 19: Protection, Overvoltage



CURRENT LIMITING

Proper operation requires the use of two current limit resistors, connected as shown in the typical connection diagram. The minimum value for R_{CL} is 3.24 Ω. However, for optimum reliability it should be set as high as possible. Refer to Application Note 1 and 9 for current limit adjust details.

BALANCE CONTROL (OFFSET NULL)

The input biasing of PA08 can be adjusted externally to provide better input offset voltage (V_{OS}) characteristics on a part-to-part basis. Use the equations in the Typical Connection Diagram (figure 2) to determine values for R_T(trim-pot) and R_S(static resistor). R_S will have a value many times that of R_T, meaning R_S will

experience almost the entire supply voltage. Rate for proper power dissipation. Adjust the wiper on R_T until input offset voltage is reduced to a minimum.

If offset nulling is not required for the application, pin 7 should be left open. Omit R_S and R_T.