PA13 • PA13A

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- Low Thermal Resistance — 1.1°C/W
- Current Foldover Protection
- Excellent Linearity — Class A/B Output
- Wide Supply Range — ±10V to ±45V
- High Output Current — Up to ±15A Peak

APPLICATIONS

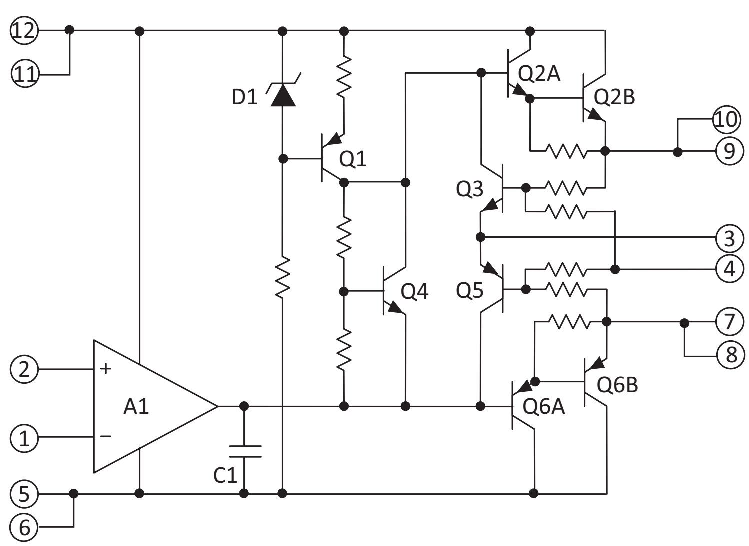
- Motor, Valve and Actuator Control
- Magnetic Deflection Circuits up to 10A
- Power Transducers up to 100 kHz
- Temperature Control up to 360W
- Programmable Power Supplies up to 90V
- Audio Amplifiers up to 120W RMS

DESCRIPTION

The PA13 is a state of the art high voltage, very high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. For continuous operation under load, a heatsink of proper rating is recommended. The PA13 is not recommended for gains below –3 (inverting) or +4 (non-inverting).

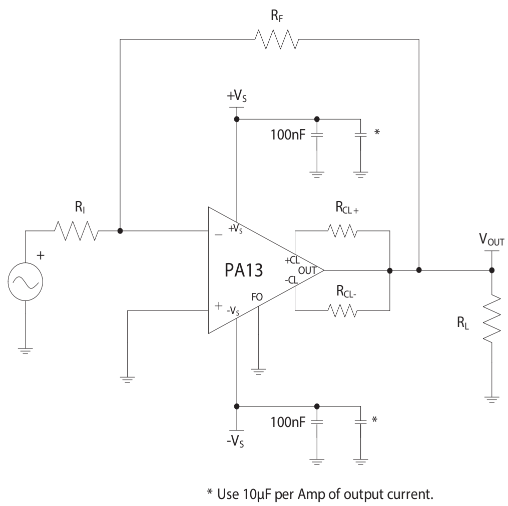
This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 12-pin power SIP is electrically isolated.

Figure 1: Equivalent Schematic



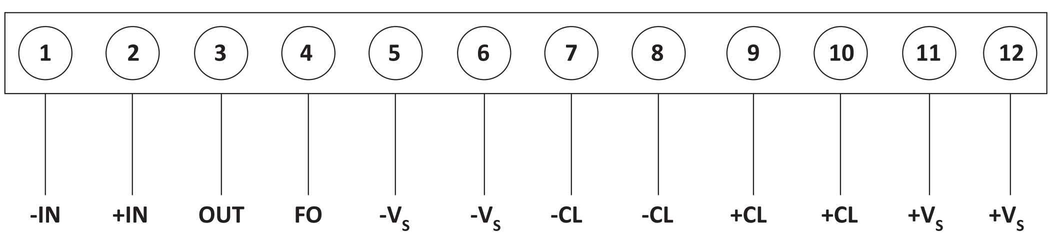
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	-IN	The inverting input.
2	+IN	The non-inverting input.
3	OUT	The output. Connect this pin to load and to the feedback resistors.
4	FO	The fold-over current limit. Connect to ground if desired. See "Current Limiting" section.
5, 6	$-V_S$	The negative supply rail. Pins 5 and 6 are internally connected.
7, 8	-CL	Connect to the sinking current limit resistor. Output current flows into this pin through R_{CL-}. The output pin and the load are connected to the other side of R_{CL-}. Pins 7 and 8 are internally connected.
9, 10	+CL	Connect to the sourcing current limit resistor. Output current flows out of this pin through R_{CL+}. The output pin and the load are connected to the other side of R_{CL+}. Pins 9 and 10 are internally connected.
11, 12	$+V_S$	The positive supply rail. Pins 11 and 12 are internally connected.

SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz. Full temperature range specifications are guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_S$ to $-V_S$		100	V
Output Current, within SOA	I_{OUT}		15	A
Power Dissipation, internal	P_D		135	W
Input Voltage, differential	$V_{IN (Diff)}$	-37	37	V
Input Voltage, common mode	V_{CM}	$-V_S$	V_S	V
Temperature, pin solder, 10s max.			260	°C
Temperature, junction [1]	T_J		175	°C
Temperature Range, storage		-55	+125	°C
Operating Temperature Range, case	T_C	-40	+85	°C

1. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.

CAUTION The substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes

INPUT

Parameter	Test Conditions	PA13			PA13A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial			±2	±6		±1	±4	mV
Offset Voltage vs. temperature	Full temp range		±10	±65		*	±40	μV/°C
Offset Voltage vs. supply			±30	±200		*	*	μV/V
Offset Voltage vs. power			±20			*		μV/W
Bias Current, initial			±12	±30		±10	±20	nA
Bias Current vs. temperature	Full temp range		±50	±500		*	*	pA/°C
Bias Current vs. supply			±10			*		pA/V
Offset Current, initial			±12	±30		±5	±10	nA
Offset Current vs. temperature	Full temp range		±50			*		pA/°C
Input Impedance, DC			200			*		MΩ
Input Capacitance			3			*		pF
Common Mode Voltage Range [1]	Full temp range	$\pm V_S \mp 5$	$\pm V_S \mp 3$		*	*		V
Common Mode Rejection, DC	Full temp range, $V_{CM} = \pm V_S - 6V$	74	100		*	*		dB

1. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.

GAIN

Parameter	Test Conditions	PA13			PA13A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop Gain @ 10 Hz	1 kΩ load		110			*		dB
Open Loop Gain @ 10 Hz	Full temp range, 8 Ω load	96	108		*	*		dB
Gain Bandwidth Product @ 1 MHz	8 Ω load		4		*	*		MHz
Power Bandwidth	8 Ω load	13	20		*	*		kHz
Phase Margin, $A_V = +4$	Full temp range, 8 Ω load		20			*		°

OUTPUT

Parameter	Test Conditions	PA13			PA13A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing [1]	PA13 = 10A, PA13A = 15A	$\pm V_S \mp 6$			*			V
Voltage Swing [1]	I_{OUT} = 5A	$\pm V_S \mp 5$			*			V
Voltage Swing [1]	Full temp range, I_{OUT} = 80mA	$\pm V_S \mp 5$			*			V
Current, peak		10			15			A
Settling Time to 0.1%	2V step		2			*		µs
Slew Rate		2.5	4		*	*		V/µs
Capacitive Load	Full temp range, A_V = 4			1.5			*	nF
Capacitive Load	Full temp range, A_V > 10			SOA			*	

1. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.

POWER SUPPLY

Parameter	Test Conditions	PA13			PA13A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage	Full temp range	±10	±40	±45	*	*	*	V
Current, quiescent			25	50		*	*	mA

THERMAL

Parameter	Test Conditions	PA13			PA13A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case [1]	T_C=-55 to 125°C, F > 60 Hz		0.6	0.7		*	*	°C/W
Resistance, DC, junction to case	T_C=-55 to 125°C		0.9	1.1		*	*	°C/W
Resistance, junction to air	T_C=-55 to 125°C		30			*		°C/W
Temperature Range, case	Meets full range specs	-25		+85	*		*	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: * The specification of PA13A is identical to the specification for PA13 in the applicable column to the left

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

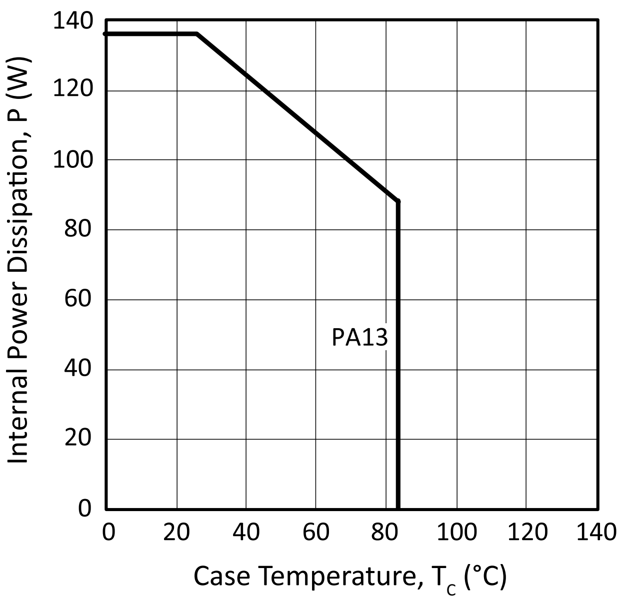


Figure 5: Bias Current

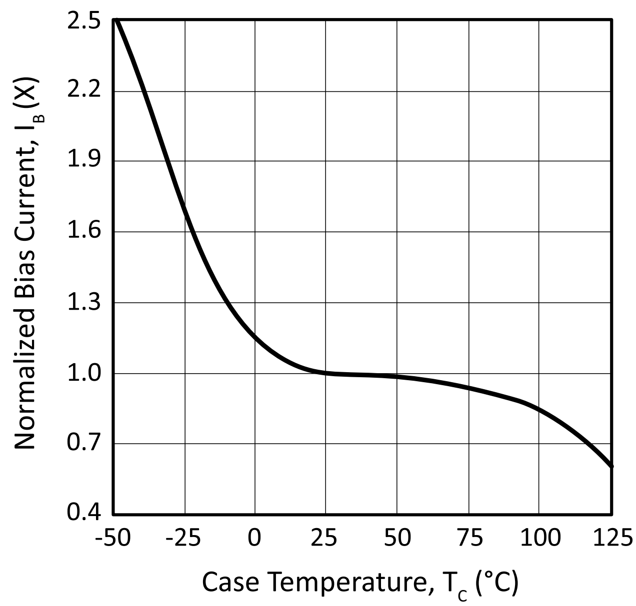


Figure 6: Small Signal Response

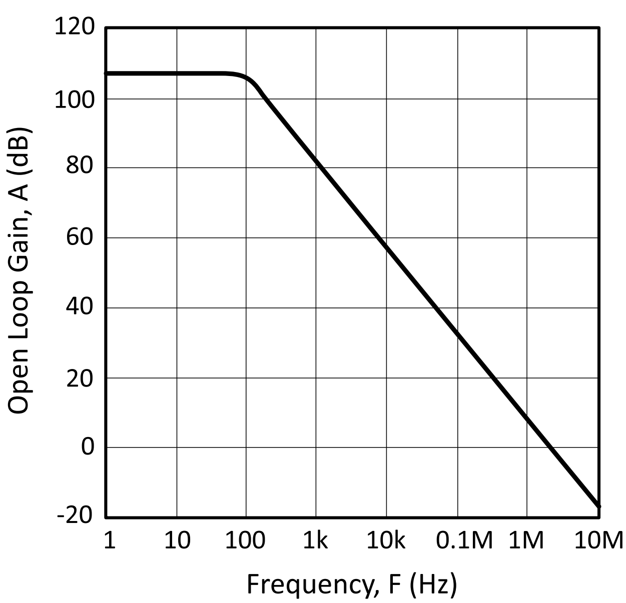


Figure 7: Phase Response

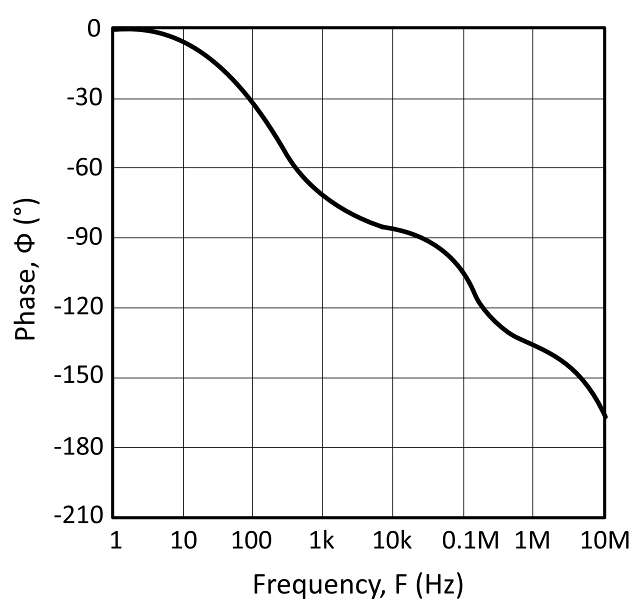


Figure 8: Current Limit

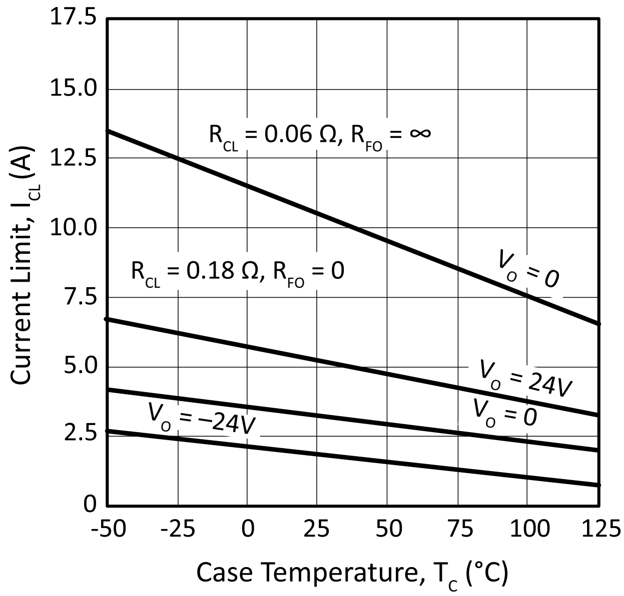


Figure 9: Power Response

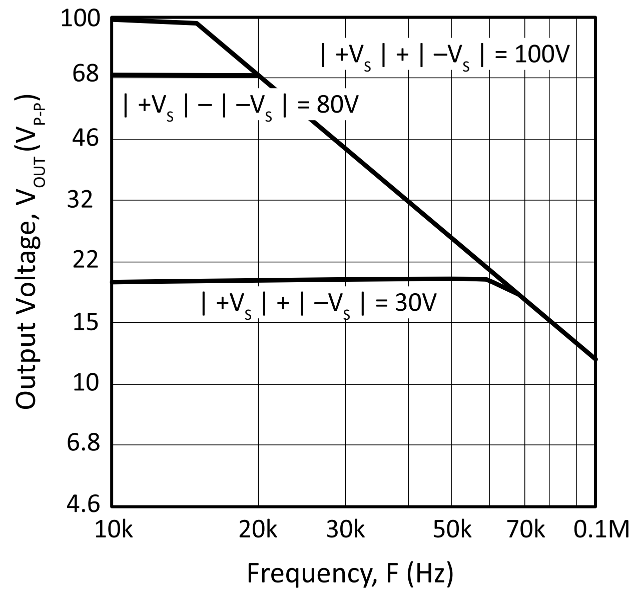


Figure 10: Common Mode Rejection

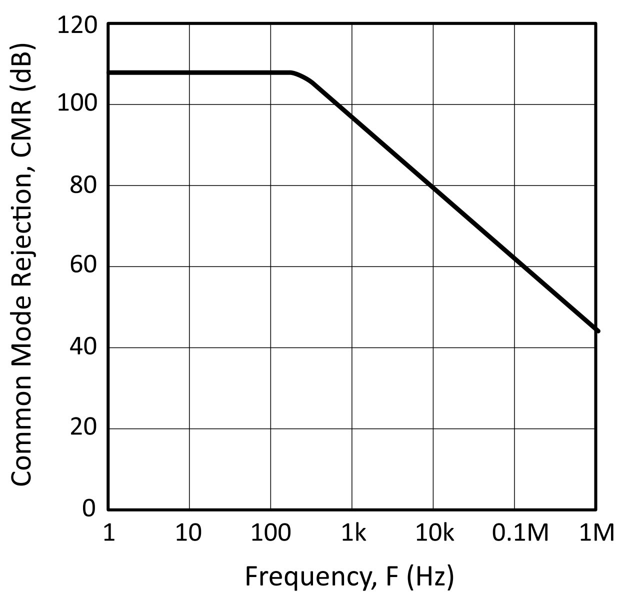


Figure 11: Pulse Response

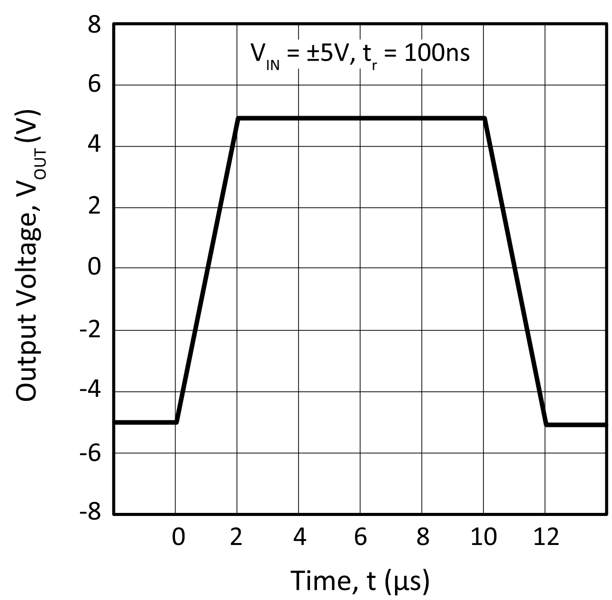


Figure 12: Input Noise

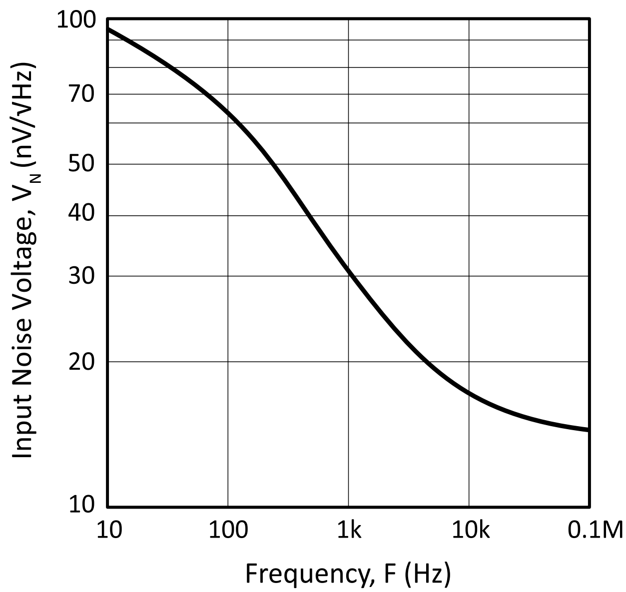


Figure 13: Harmonic Distortion

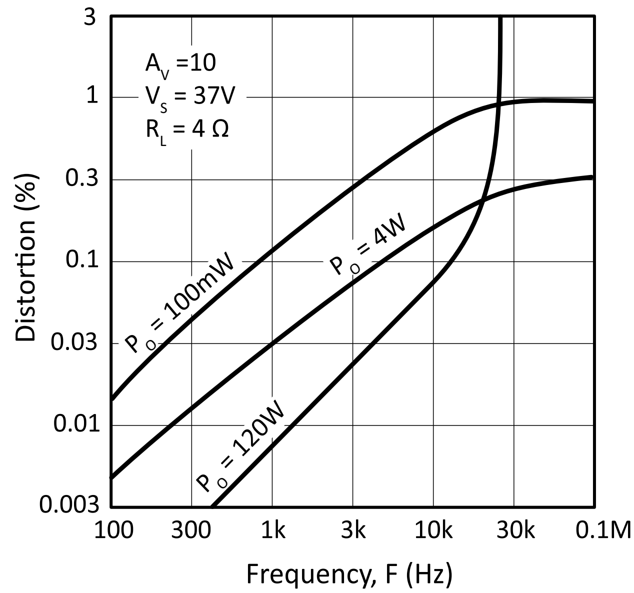


Figure 14: Quiescent Current

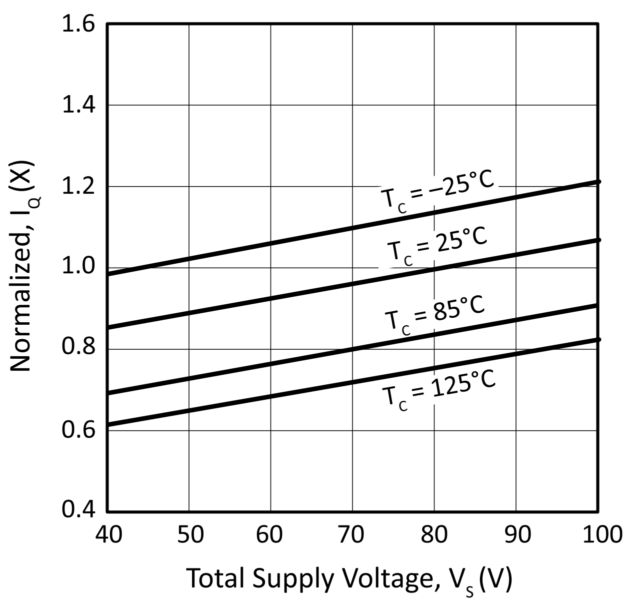
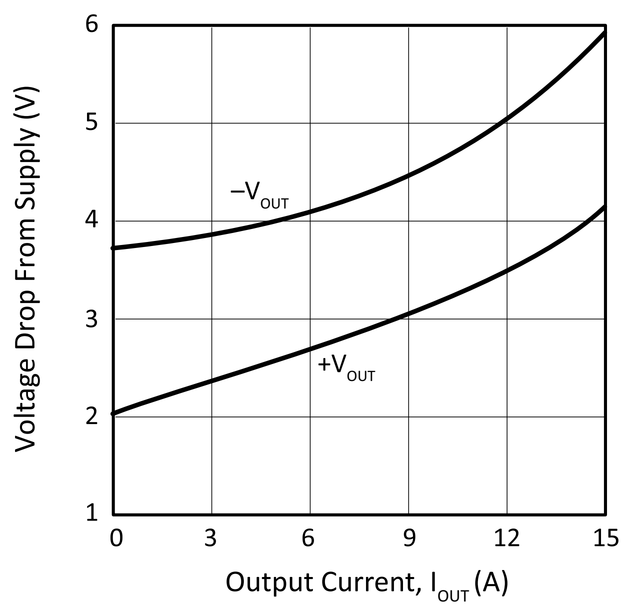


Figure 15: Output Voltage Swing



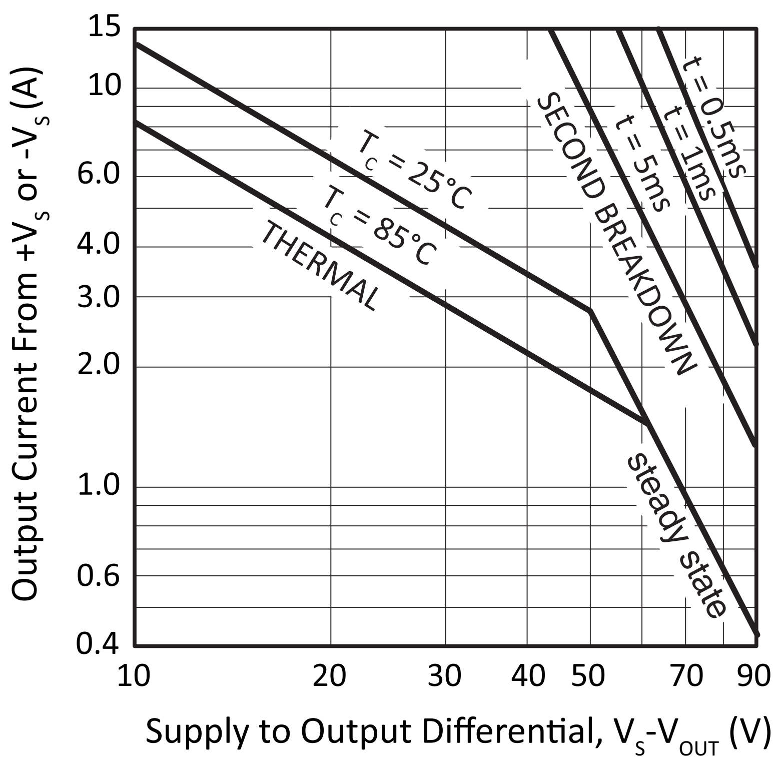
SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the guidelines on the next page may save extensive analytical efforts.

Figure 16: SOA



1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

$\pm V_S$	Capacitive Load		Inductive Load	
	I_{CL} = 5A	I_{CL} = 10A	I_{CL} = 5A	I_{CL} = 10A
50V	200µF	125µF	5 mH	2.0 mH
40V	500µF	350µF	15 mH	3.0 mH
35V	2.0mF	850µF	50 mH	5.0 mH
30V	7.0mF	2.5mF	150 mH	10 mH
25V	25mF	10mF	500 mH	20 mH
20V	60mF	20mF	1,000 mH	30 mH
15V	150mF	60mF	2,500 mH	50 mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 12.5V below the supply rail with I_{CL} = 10A or 27V below the supply rail with I_{CL} = 5A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or common if the current limits are set as follows at T_C = 25°C:

$\pm V_S$	Short to $\pm V_S$ C, L, or EMF Load	Short to Common
45V	0.43A	3.0A
40V	0.65A	3.4A
35V	1.0A	3.9A
30V	1.7A	4.5A
25V	2.7A	5.4A
20V	3.4A	6.7A
15V	4.5A	9.0A

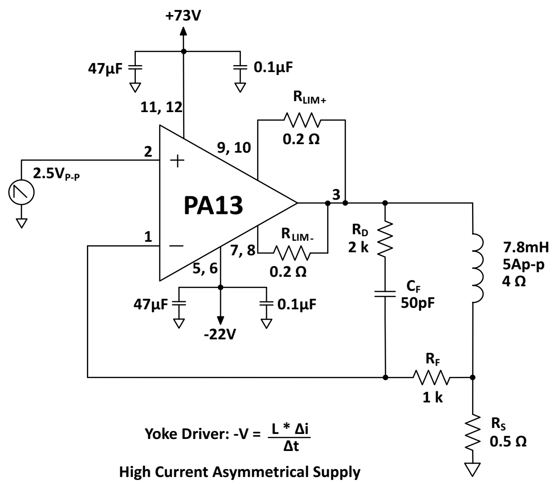
These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology's complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

Figure 17: Typical Application



POWER RATING

Not all vendors use the same method to rate the power handling capability of a Power Op Amp. Apex Microtechnology rates the internal dissipation, which is consistent with rating methods used by transistor manufacturers and gives conservative results. Rating delivered power is highly application dependent and therefore can be misleading. For example, the 135W internal dissipation rating of the PA13 could be expressed as an output rating of 260W for audio (sine wave) or as 440W if using a single ended DC load. Please note that all vendors rate maximum power using an infinite heatsink.

THERMAL STABILITY

Apex Microtechnology has eliminated the tendency of class A/B output stages toward thermal runaway and thus has vastly increased amplifier reliability. This feature, not found in most other Power Op Amps, was pioneered by Apex Microtechnology in 1981 using thermistors which assure a negative temperature coefficient in the quiescent current. The reliability benefits of this added circuitry far outweigh the slight increase in component count.

CURRENT LIMITING

Refer to Application Note 9, "Current Limiting", for details of both fixed and foldover current limit operation. Beware that current limit should be thought of as a ±20% function initially and varies about 2:1 over the range of –55°C to 125°C.

For fixed current limit, leave pin 4 open and use equations 1 and 2.

1.

$$R_{CL}(\Omega) = \frac{0.65V}{I_{CL}(A)}$$

2.

$$I_{CL}(A) = \frac{0.65V}{R_{CL}(\Omega)}$$

Where:

I_{CL} is the current limit in Amperes.

R_{CL} is the current limit resistor in Ohms.

For certain applications, fold-over current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum fold-over slope, ground pin 4 and use equations 3 and 4.

3.

$$I_{CL}(A) = \frac{0.65V + (V_{OUT} \cdot 0.014)}{R_{CL}(\Omega)}$$

4.

$$R_{CL}(\Omega) = \frac{0.65V + (V_{OUT} \cdot 0.014)}{I_{CL}(A)}$$

Where:

V_{OUT} is the output voltage in Volts.

Most designers start with either equation 1 to set R_{CL} for the desired current at 0V out, or with equation 4 to set R_{CL} at the maximum output voltage. Equation 3 should then be used to plot the resulting fold-over limits on the SOA graph. If equation 3 results in a negative current limit, fold-over slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced fold-over slope is desired, this can be achieved by adding a resistor (R_{FO}) between pin 4 and ground. Use equations 5 and 6 with this new resistor in the circuit.

5.

$$I_{CL}(A) = \frac{0.65V + \frac{V_{OUT} \cdot 0.14}{10.14 + R_{FO}}}{R_{CL}(\Omega)}$$

6.

$$R_{CL}(\Omega) = \frac{0.65V + \frac{V_{OUT} \cdot 0.14}{10.14 + R_{FO}}}{I_{CL}(A)}$$

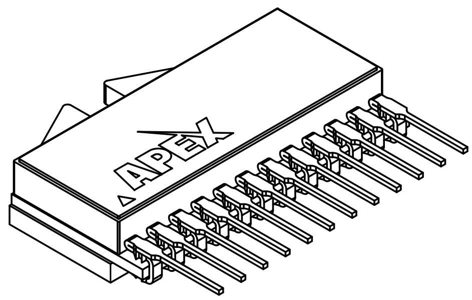
Where:

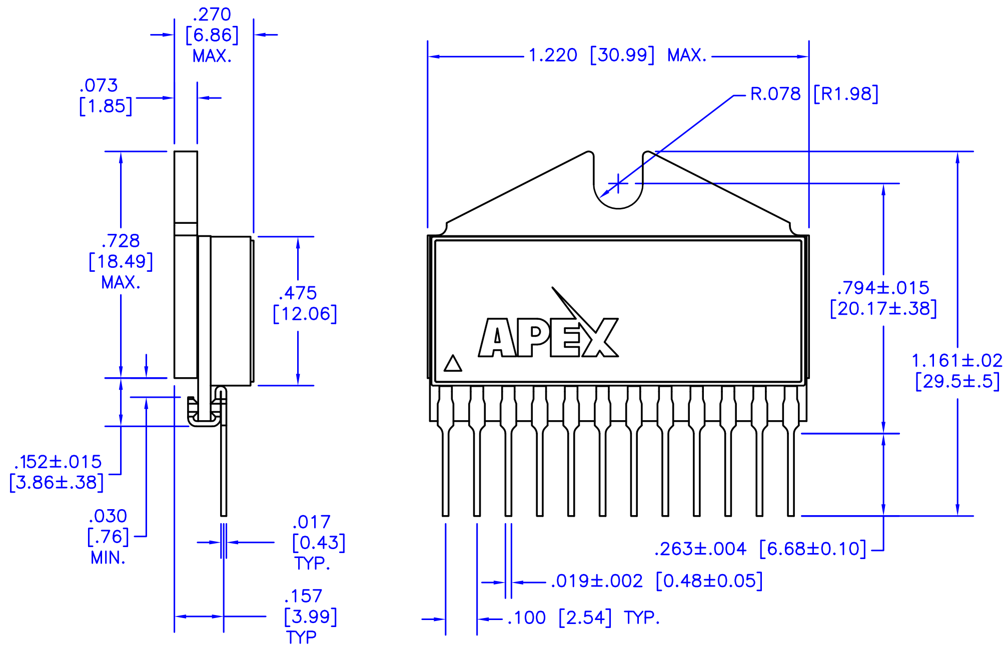
R_{FO} is in kΩ.

PACKAGE OPTIONS

Part Number	Apex Package Style	Description
PA13	DP	12-pin SIP
PA13A	DP	12-pin SIP
PA13EE	EE	12-pin SIP w/ formed leads

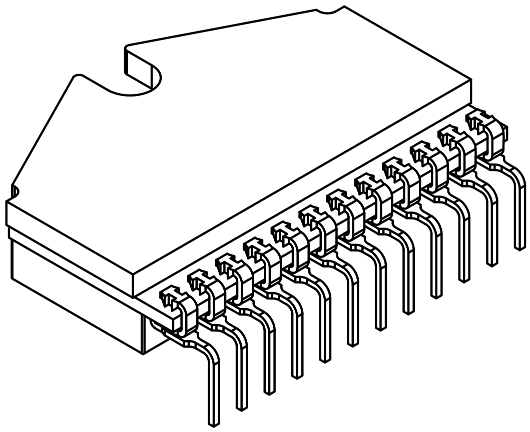
PACKAGE STYLE DP

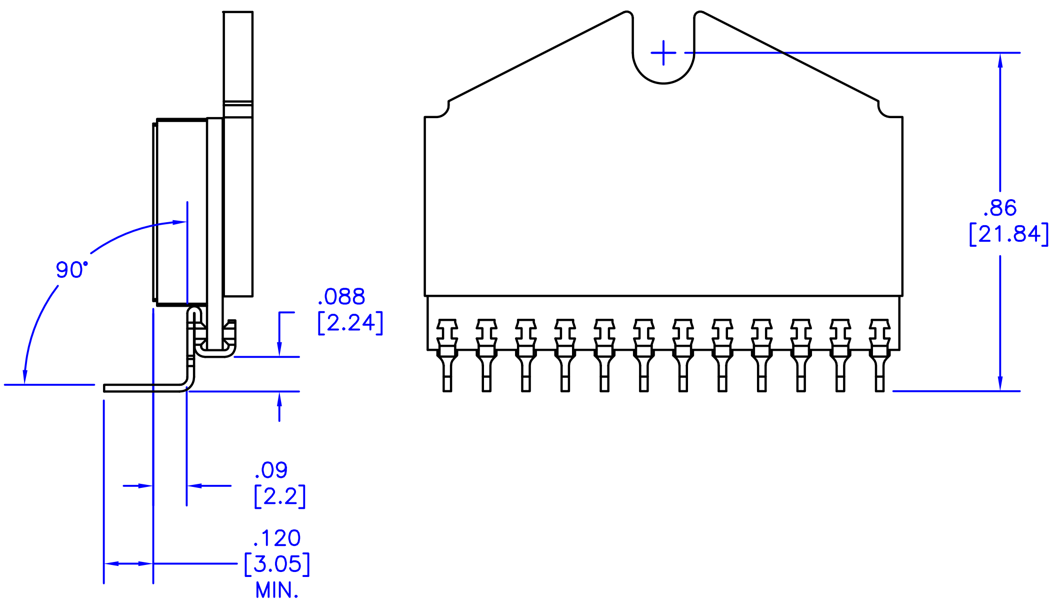




NOTES:
1. Dimensions are inches & [mm].
2. Triangle on lid denotes pin 1.
3. Pins: Alloy 510 phosphor bronze plated with matte tin (150 – 300μ”) over nickel (50 μ” max.) underplate.
4. Package: Vectra liquid crystal polymer, black
5. Epoxy–sealed & ultrasonically welded non–hermetic package.
6. Package weight: .367 oz. [11.41 g]

PACKAGE STYLE EE





NOTES:

1. Dimensions are inches & [mm].
2. For other dimensions and information on this package with unformed leads, see package DP.