PA15FL • PA15FLA

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- High Voltage — 450V (±225V)
- Low Cost
- Low Quiescent Current — 3mA max
- High Output Current — 200mA
- Programmable Current Limit

APPLICATIONS

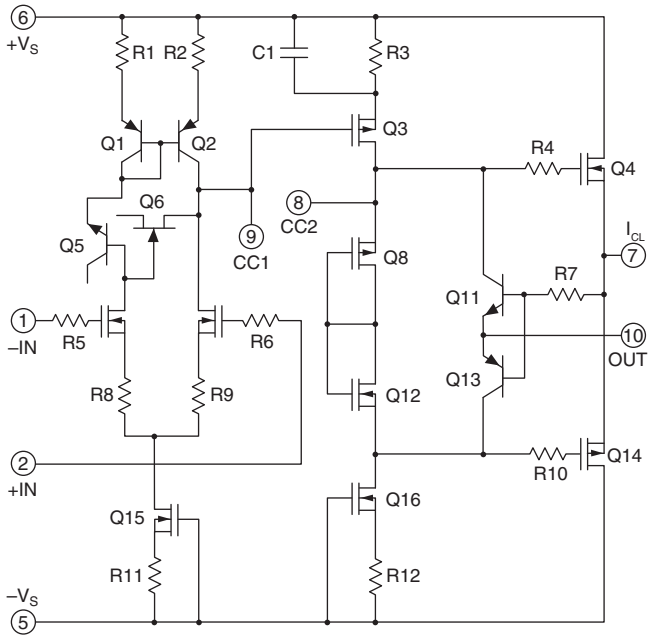
- Piezoelectric Positioning
- High Voltage Instrumentation
- Electrostatic Transducers
- Programmable Power Supplies Up To 440V

DESCRIPTION

The PA15FL is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 200mA and pulse currents up to 350mA into capacitive loads. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET input stage has integrated static and differential mode protection. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. The 10-pin power SIP package is electrically isolated.

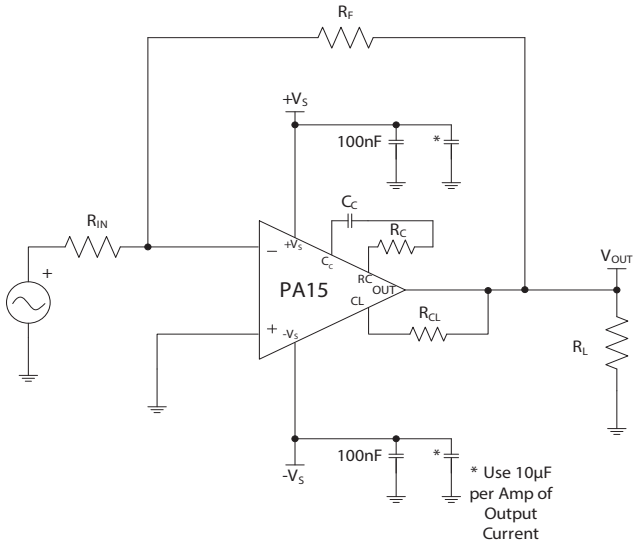
EQUIVALENT SCHEMATIC

Figure 1: Equivalent Schematic



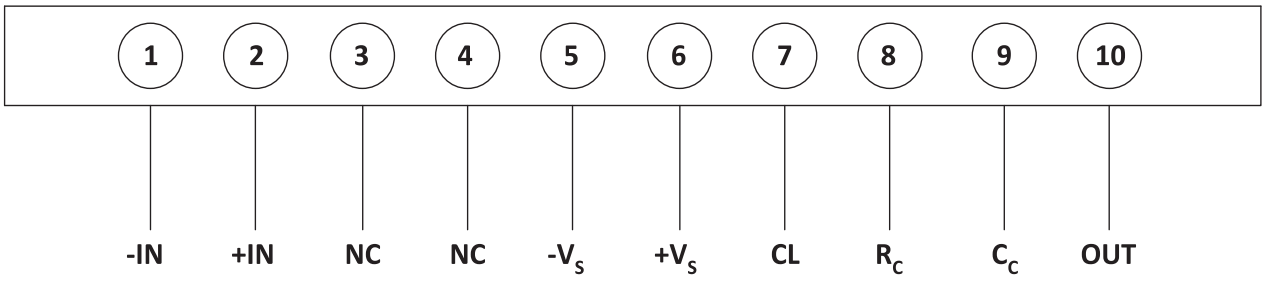
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	-IN	The inverting input.
2	+IN	The non-inverting input.
3, 4	NC	No connection.
5	$-V_S$	The negative supply rail.
6	$+V_S$	The positive supply rail.
7	CL	Connect to the current limit resistor. Output current flows into/out of this pin through R_{CL}. The output pin and the load are connected to the other side of R_{CL}.
8	RC	Compensation resistor connection. Select value based on Phase Compensation. See applicable section.
9	C_C	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.
10	OUT	The output. Connect this pin to load and to the feedback resistors.

SPECIFICATIONS

Unless otherwise noted: T_C = 25°C, compensation = C_C = 33pF, R_C = 1 kΩ, R_{CL} = 0. DC input specifications are ± value given. Power supply voltage is typical rating.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_S$ to $-V_S$		450	V
Output Current, source, sink	I_{OUT}	SEE SOA		mA
Power Dissipation, internal @ T_c = 25°C	P_D		30	W
Input Voltage, differential	$V_{IN\ (Diff)}$	-25	25	V
Input Voltage, common mode	V_{CM}	$-V_S$	V_S	V
Temperature, pin solder, -10s max.			260	°C
Temperature, junction [1]	T_J		150	°C
Temperature Range, storage		-55	125	°C
Operating Temperature Range, case	T_C	-40	85	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

CAUTION The PA15FL is constructed from MOSFET transistors. ESD handling procedures must be observed. The substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA15FL			PA15FLA			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial			2	10		0.5	3	mV
Offset Voltage vs. temperature	Full temp range		15	50		5	20	µV/°C
Offset Voltage vs. supply			10	50		*	*	µV/V
Offset Voltage vs. time			75			*		µV/√kh
Bias Current, initial			200	2000		*	*	pA
Bias Current vs. supply			4			*		pA/V
Offset Current, initial			50	500		30	200	pA
Input Impedance, DC			10^{11}			*		Ω
Input Capacitance			4			*		pF
Common Mode Voltage Range [1]		$\pm V_S$–15			*			V
Common Mode Rejection, DC	V_{CM} = ±90V	80	98		*	*		dB
Noise	10 kHz BW, R_S= 1 kΩ, C_C = open		2			*		µVrms

1. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.

GAIN

Parameter	Test Conditions	PA15FL			PA15FLA			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop, @ 15 Hz	R_L = 2 kΩ, C_C = OPEN	94	111		*	*		dB
Gain Bandwidth Product @ 1 MHz	R_L = 2 kΩ, C_C = OPEN		5.8			*		MHz
Power Bandwidth	R_L = 2 kΩ, C_C = OPEN		24			*		kHz
Phase Margin	Full temp range		60			*		°

OUTPUT

Parameter	Test Conditions	PA15FL			PA15FLA			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing [1]	I_{OUT} = ±200mA	$\pm V_S$–15	$\pm V_S$–10		*	*		V
Current, continuous		±200			*			mA
Slew Rate, A_V = 100	C_C = OPEN		20		20	30		V/µs
Capacitive Load, A_V = +1	Full temp range	100			*			pF
Settling Time to 0.1%	C_C = OPEN, 2V step		2			*		µs
Resistance, no load			50			*		Ω

1. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.

POWER SUPPLY

Parameter	Test Conditions	PA15FL			PA15FLA			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage [1]		±50	±150	±225	*	*	*	V
Current, quiescent			2.0	3.0		*	*	mA

1. Derate max supply rating 0.625 V/°C below 25°C case. No derating needed above 25°C case.

THERMAL

Parameter	Test Conditions	PA15FL			PA15FLA			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC junction to case [1]	Full temp range, f > 60 Hz			2.5			*	°C/W
Resistance, DC junction to case	Full temp range, f < 60 Hz			4.2			*	°C/W
Resistance, junction to air	Full temp range		30			*		°C/W
Temperature Range, case	Meets full range specifications	-25		85	*		*	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: *The specification of PA15FLA is identical to the specification for PA15FL in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

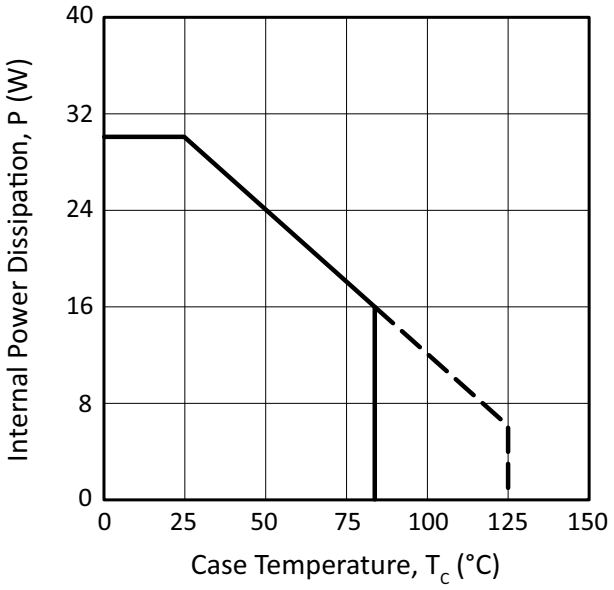


Figure 5: Quiescent Current

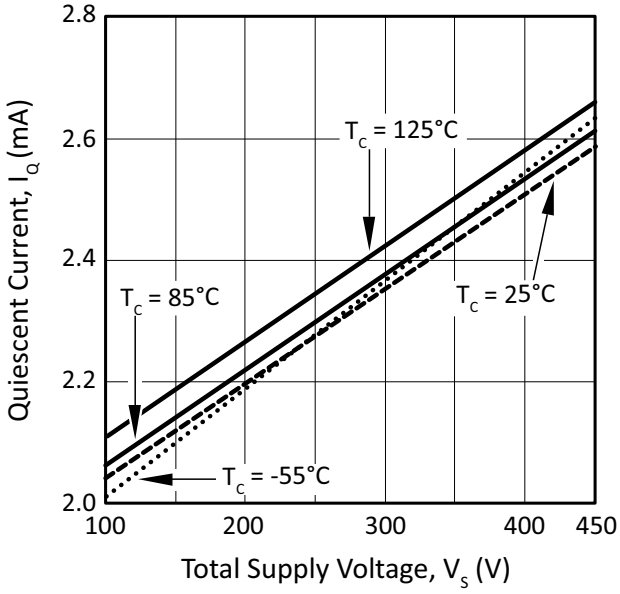


Figure 6: Power Response

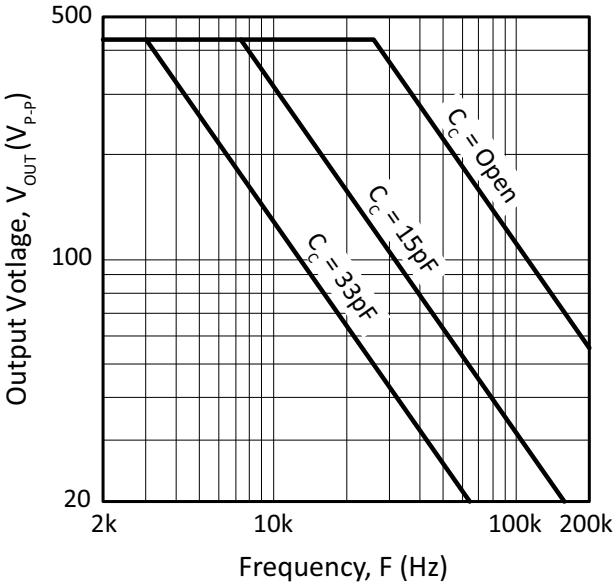


Figure 7: Small Signal Response

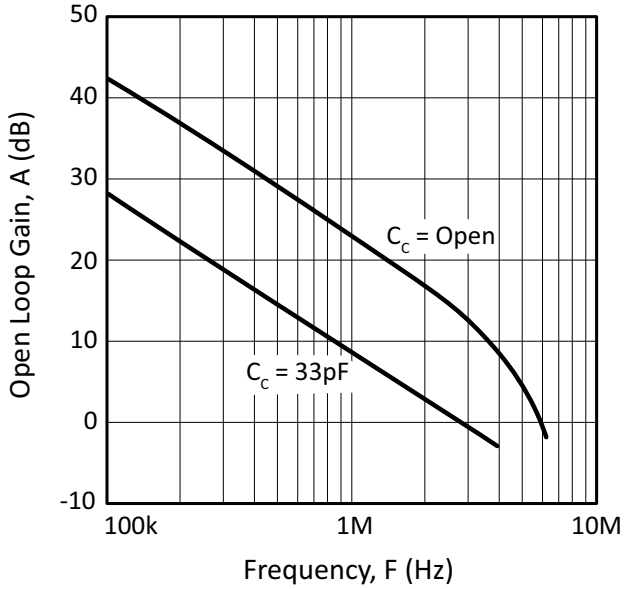


Figure 8: Small Signal Response

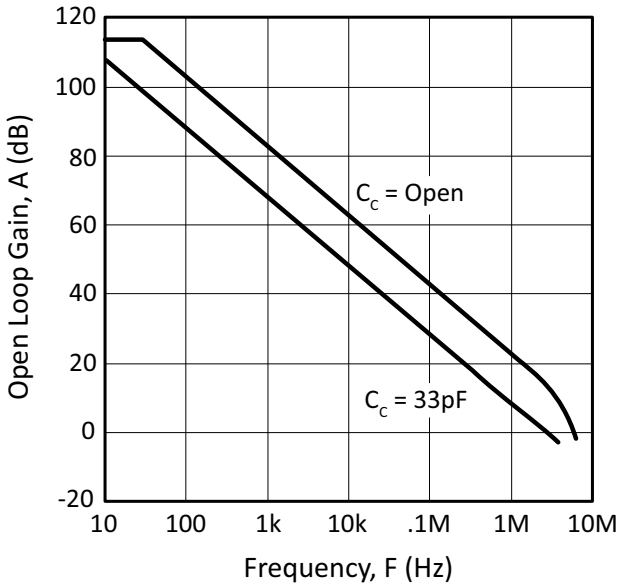


Figure 9: Phase Response

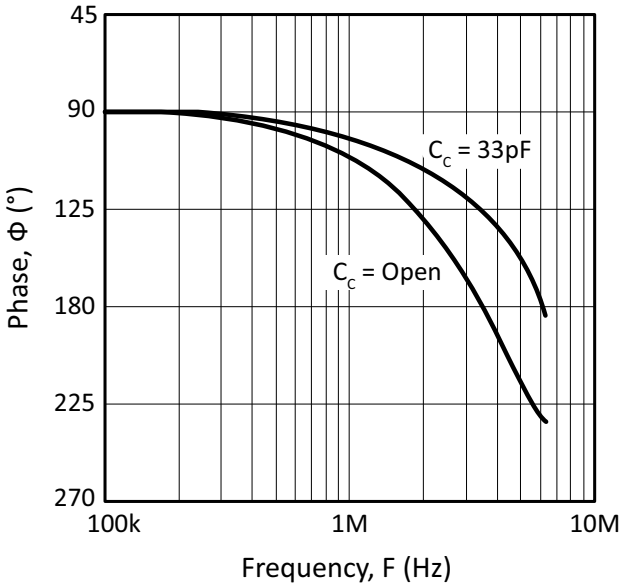


Figure 10: Swing from $+V_S$

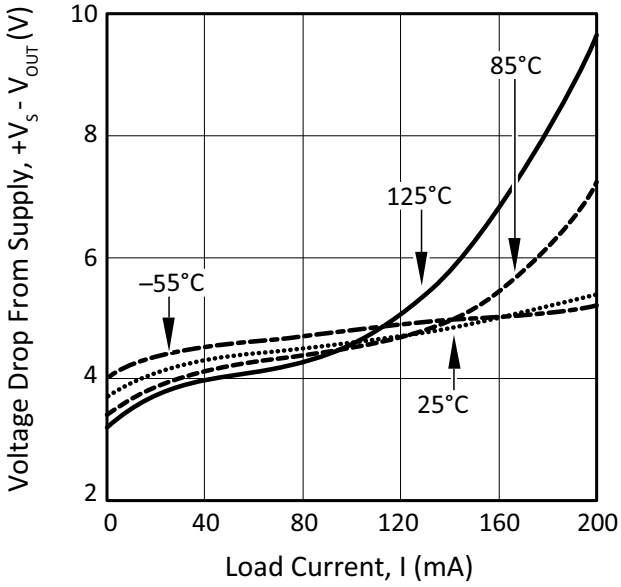


Figure 11: Swing from $-V_S$

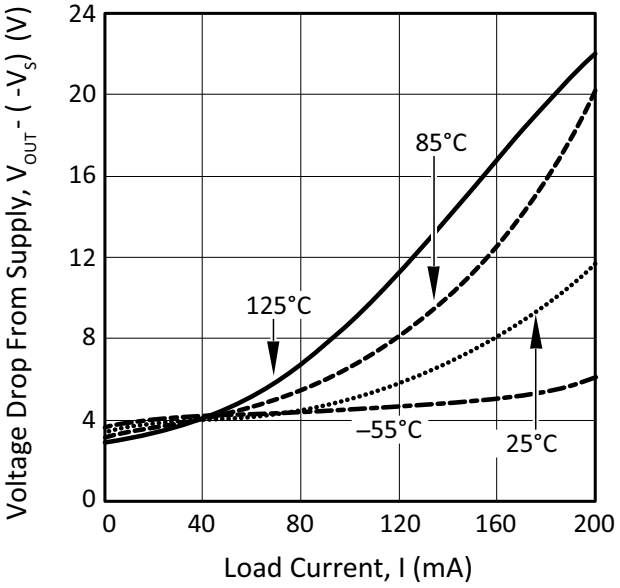


Figure 12: Open Loop Output Impedance

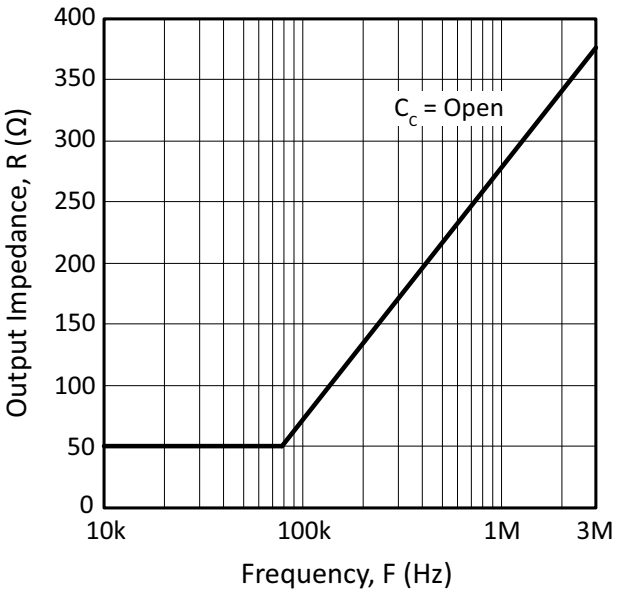


Figure 13: Harmonic Distortion

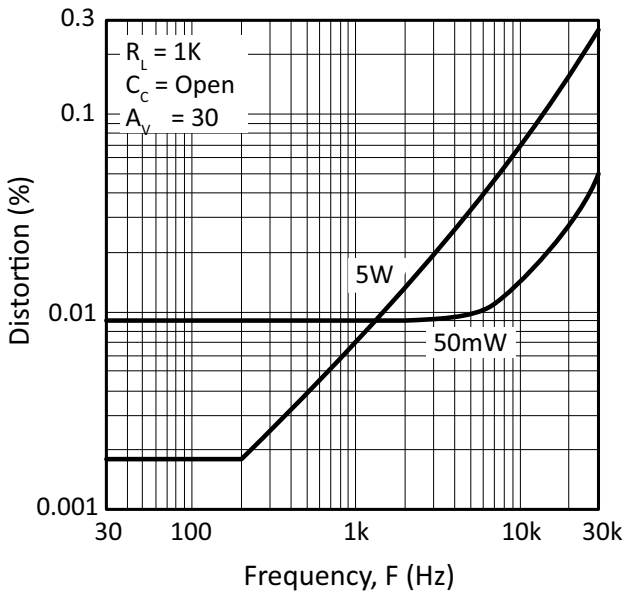


Figure 14: Common Mode Rejection

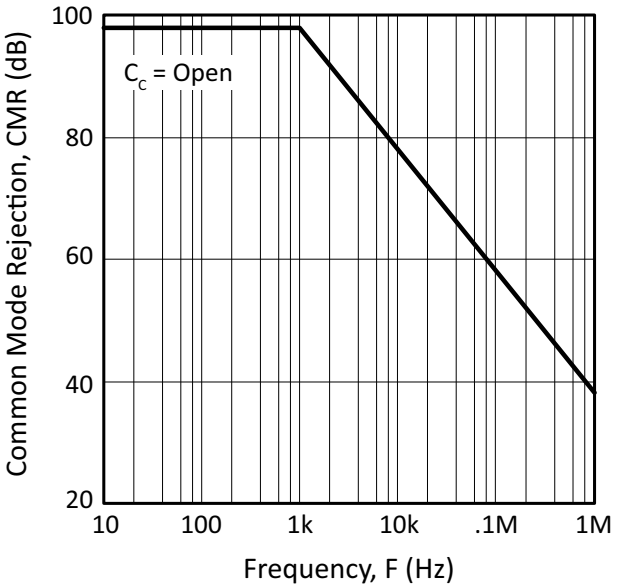
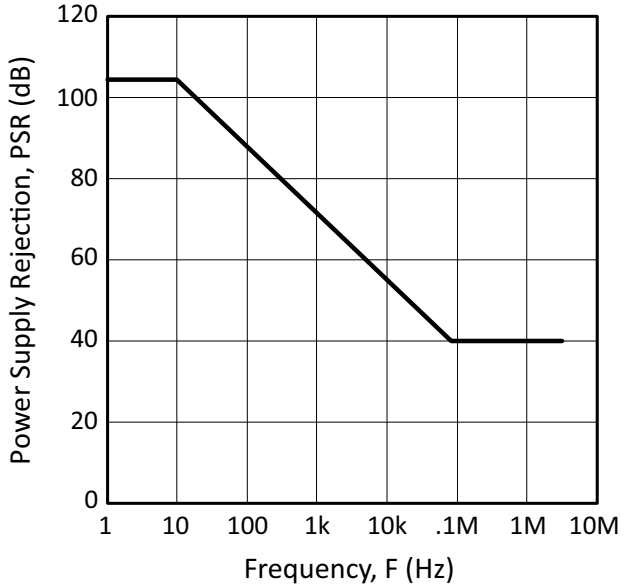


Figure 15: Power Supply Rejection

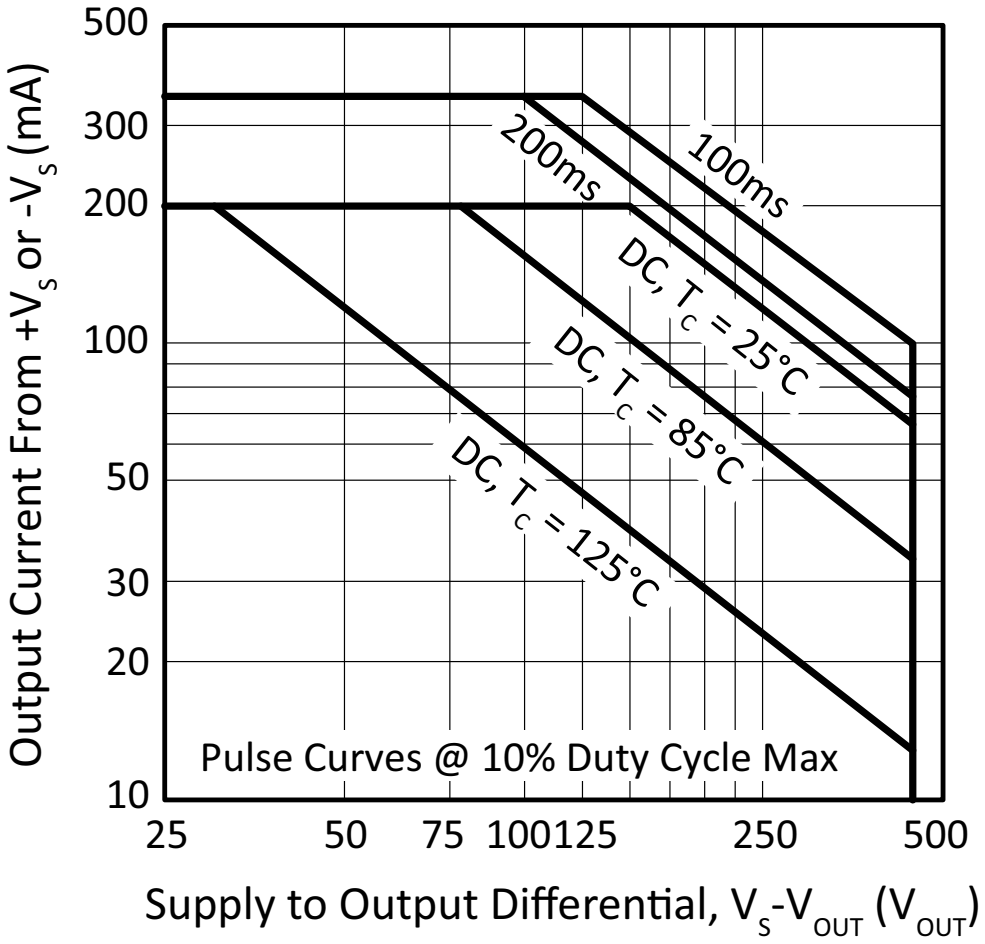


SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

Figure 16: SOA



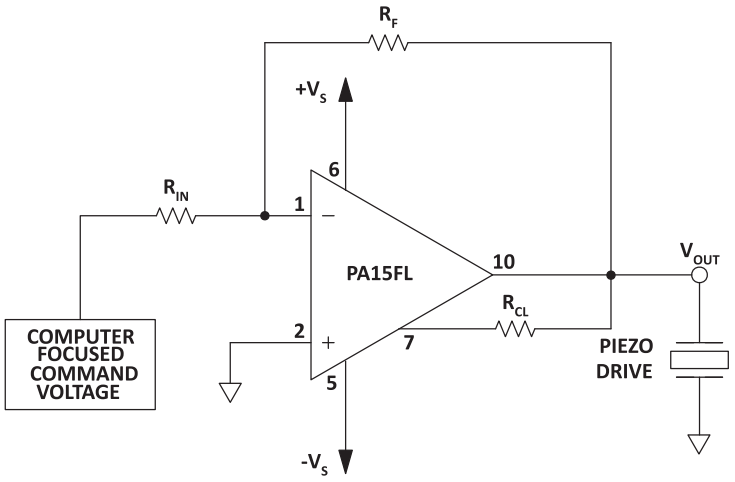
GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA15FL reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

Figure 17: Typical Application (Low Power, Piezoelectric Positioning)



PHASE COMPENSATION

Gain	C_C*	R_C
≥1	33pF	1 kΩ
≥10	OPEN	OPEN

CURRENT LIMIT

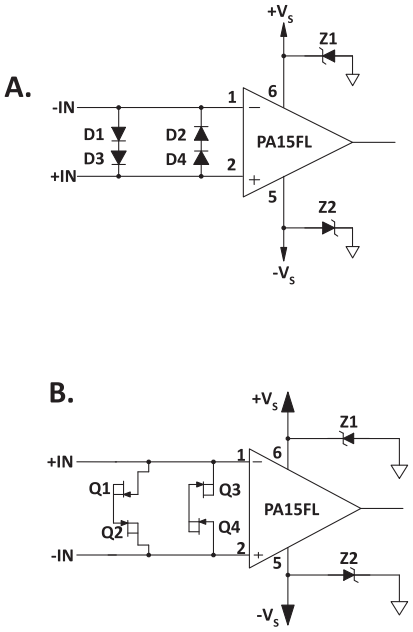
For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 2Ω, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 150Ω.

$$R_{CL}(\Omega) = \frac{0.6V}{I_{CL}(A)}$$

INPUT PROTECTION

Although the PA15FL can withstand differential input voltages up to ±25V, additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1-D4 in Figure 17A). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1-Q4 in Figure 17B). In either case the input differential voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

Figure 18: Overvoltage Protection



POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.
Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail are known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

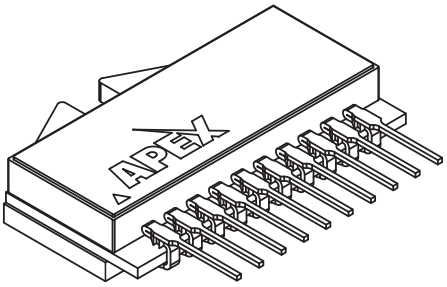
The PA15FL has sufficient phase margin to be stable with most capacitive loads at a gain of 10 or more, using the recommended phase compensation.

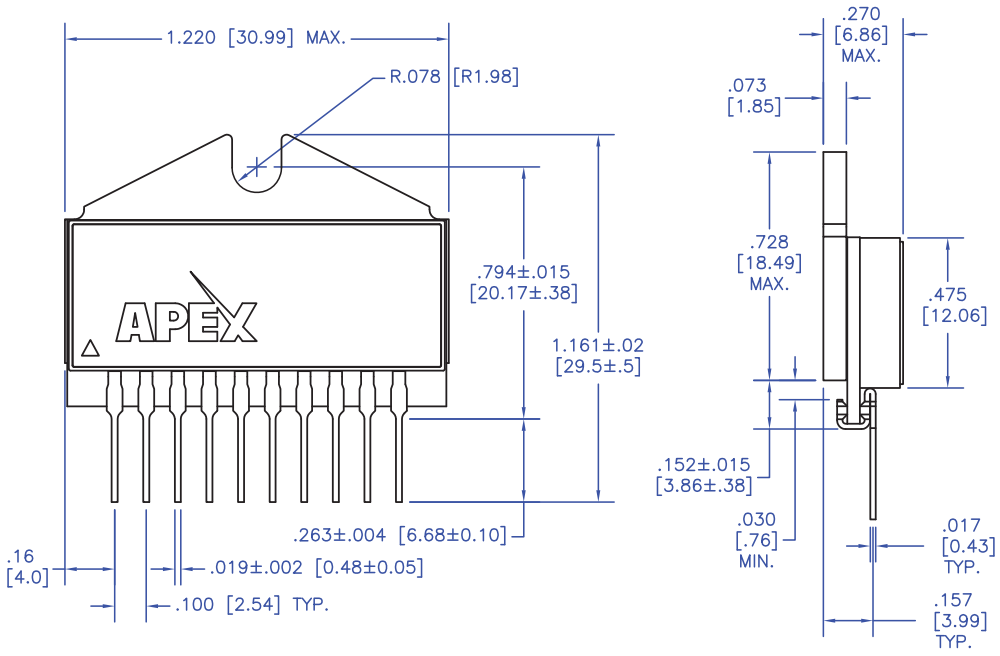
The PA15FL is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 8 and 9 to avoid spurious oscillation.

PACKAGE DESIGN

Part Number	Apex Package Style	Description
PA15AFU	FU	10-Pin SIP w/ formed leads
PA15FL	FL	10-Pin SIP
PA15FLA	FL	10-Pin SIP
PA15FU	FU	10-Pin SIP w/ formed leads

PACKAGE STYLE FL





NOTES:

1. Dimensions are inches & [mm].
2. Triangle on lid denotes pin 1.
3. Pins: Alloy 510 phosphor bronze plated with matte tin (150 – 300µ") over nickel (50 µ" max.) underplate.
4. Package: Vectra liquid crystal polymer, black
5. Epoxy–sealed & ultrasonically welded non–hermetic package.
6. Package weight: .367 oz. [11.41 g]