PA22

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- Up to ±110 V Power Supply
- 12 A Continuous Output Current, Typical
- 250 W Continuous Power Dissipation at T_C = 25 °C
- 4 MHz Gain Bandwidth Product

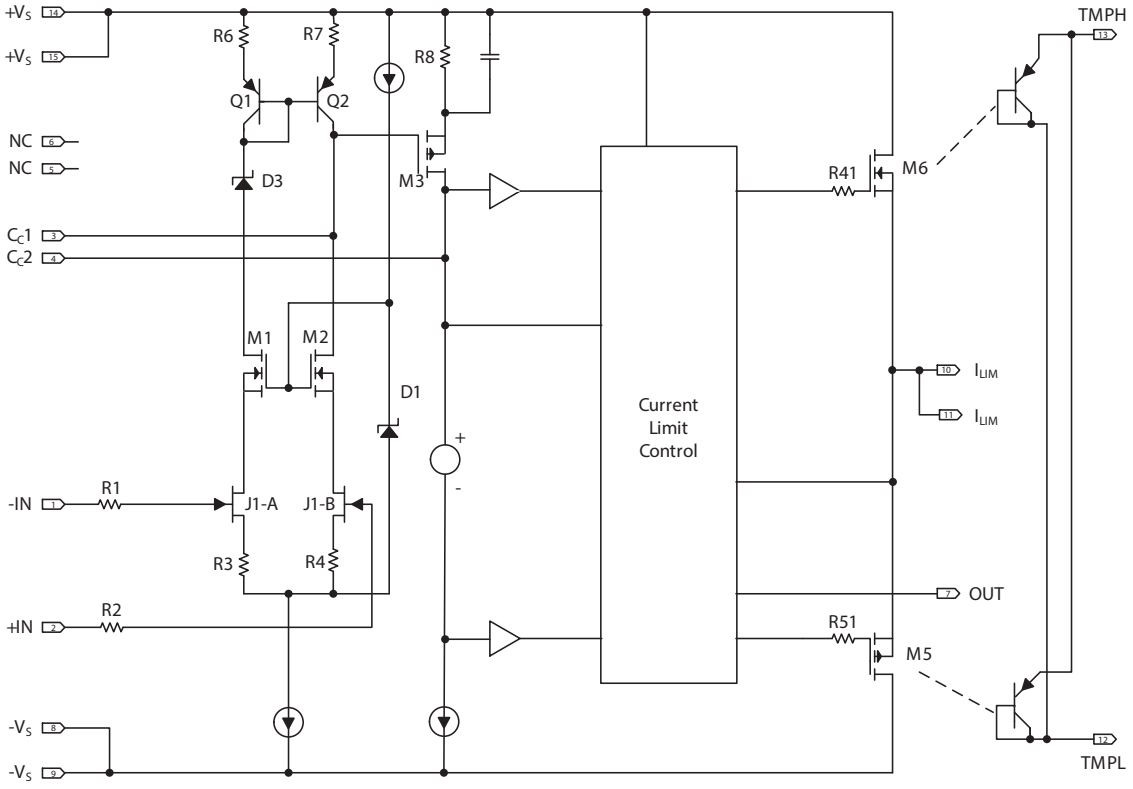
APPLICATIONS

- Programmable Voltage or Current Sources
- Piezo Electric Positioning
- Deformable Mirror Focus
- Electrostatic Transducers

DESCRIPTION

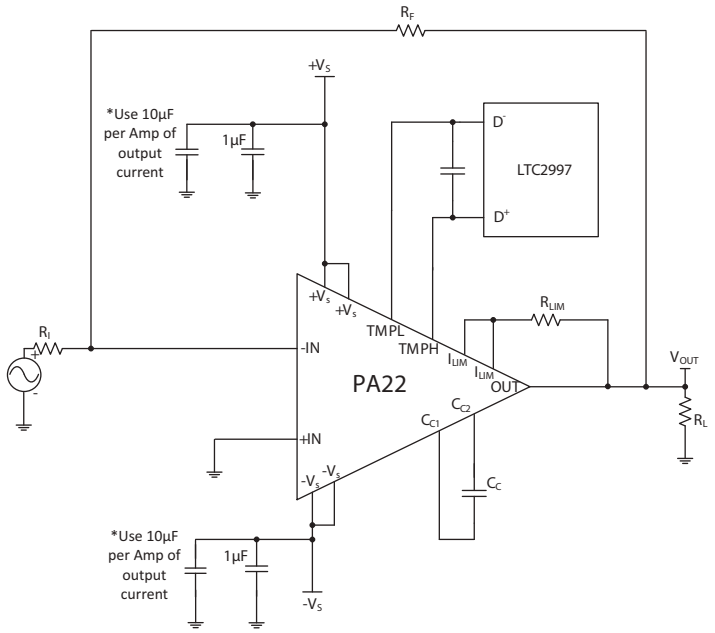
The PA22 linear power operational amplifier is specifically designed for high pulse current applications. With its peak current capability of 13.6 A and internal power dissipation of 250 W, this amplifier offers power density yet unseen in SIP form-factors. Its novel design allows for easy and reliable connection to a heatsink, as well as strong performance even when socketed. This amplifier is equipped with temperature sensing and current limit.

Figure 1: Equivalent Schematic



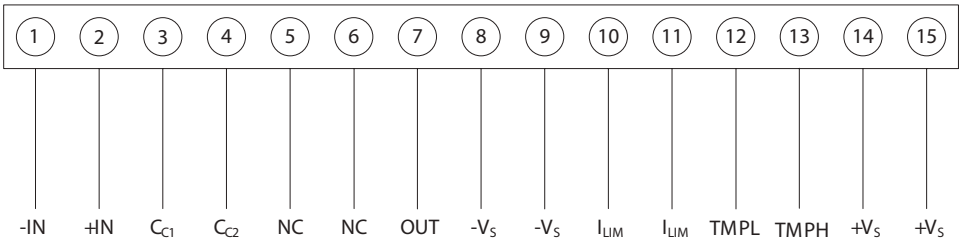
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	-IN	Inverting input
2	+IN	Non-inverting input
3	C_{C1}	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.
4	C_{C2}	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.
7	OUT	The output voltage sense, no current driving capability; connect this pin to the load and the feedback resistors.
8, 9	$-V_S$	The negative supply rail. Pins 8 and 9 are internally connected.
10, 11	I_{LIM}	The output with current driving capability. Connect to the current limit resistor. Output current flows into/out of these pins through R_{LIM}. The output pin and the load are connected to the other side of R_{LIM}. Pins 10 and 11 are internally connected.
12	TMPL	Cathode side of two parallel-connected temperature-sensing transistors, mounted on top of one of the sinking and one of the sourcing output elements. Connect to LTC2997 D- pin for PTAT voltage.
13	TMPH	Anode side of two parallel-connected temperature-sensing transistors, mounted on top of one of the sinking and one of the sourcing output elements. Connect to LTC2997 D+ pin for PTAT voltage.
14, 15	$+V_S$	The positive supply rail. Pins 14 and 15 are internally connected.
5, 6	NC	No Connection

SPECIFICATIONS

Unless otherwise noted: T_C = 25 °C, C_C = 47 pF, $+V_S$ = 100 V, $-V_S$ = -100 V. DC input specifications are +/- value given.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol[1]	Min	Max	Units
Supply Voltage, total	$+V_S$ to $-V_S$	40	250	V
Output Current, peak, within SOA	I_{OUT}		13.6	A
Power Dissipation, internal, continuous[2]	P_D		250	W
Input Voltage, differential	$V_{IN\ (Diff)}$	-25	25	V
Input Voltage, common mode	V_{CM}	$-V_s$	$+V_s$	V
I_{LIM} to OUT Pin Voltage Differential	V_{LIM}	-5	5	V
Temperature, pin solder, 10s			260	°C
Temperature, junction	T_J		150	°C
Temperature Range, storage		-40	+85	°C
Operating Temperature Range, case	T_C	-25	+85	°C

1. $+V_S$ and $-V_S$ denote the positive and negative supply voltages.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.

CAUTION

The PA22 is constructed from MOSFET transistors. ESD handling procedures must be observed. The internal substrate contains Beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850 °C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Offset Voltage, initial			5	20	mV
Offset Voltage vs. Temperature[1]	25 °C to 85 °C		90	250	µV/°C
Offset Voltage vs. Supply			22	50	µV/V
Offset Voltage vs. Time			130		µV/kh
Bias Current, initial[2]			100	2000	pA
Bias Current vs. Supply			4		pA/V
Offset Current, initial			50	2000	pA
Input Impedance, DC			10^{11}		Ω
Input Capacitance			4		pF
Common Mode Voltage Range[1]		$-V_S+15$		$+V_s-15$	V
Common Mode Rejection, DC	V_{CM}= ± 43.5 V	74	108		dB
Noise	10 kHz, R_I=1 kΩ		13		nV/√Hz

1. Guaranteed but not tested.
2. Doubles for every 10 °C of case temperature increase.

GAIN

Parameter	Test Conditions	Min	Typ	Max	Units
Large Signal Bandwidth[1, 2]	A_V=-100, R_{LOAD}= 1 kΩ, V_{OUT}=220 V_{PP}, ±V_S=±125 V		28		kHz
Gain Bandwidth Product	F=1 MHz		5.8		MHz
PSRR, DC	Referred to input	80	104		dB

1. Guaranteed but not tested.
2. Calculated from minimum slew rate.

OUTPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Output Voltage Swing, Sourcing	$\|I_{OUT}\|$=2 A	$+V_S$-7.9	$+V_S$-7		V
	$\|I_{OUT}\|$=10 A	$+V_S$-15	$+V_S$-8.5		V
Output Voltage Swing, Sinking	$\|I_{OUT}\|$=2 A		$-V_S$+7	$-V_S$+7.9	V
	$\|I_{OUT}\|$=10 A		$-V_S$+8.5	$-V_S$+15	V
Current, Continuous, within SOA		10	12		A
Settling Time to 5%[1]	10 V step, A_V=-4 2 A/µs load transient			5	µs
Slew Rate	A_V=-100, R_{LOAD} = 1 kΩ	20	35		V/µs
Current Limit vs. Temperature	R_{LIM}=0.2 Ω, T_C=25 °C to 85 °C		3.5		%

1. Guaranteed but not tested.

POWER SUPPLY

Parameter	Test Conditions	Min	Typ	Max	Units
Supply Voltage ($+V_S$, $-V_S$)		46	200	220	V
Current, quiescent	220 V supply		45	55	mA

THERMAL

Parameter	Test Conditions	Min	Typ	Max	Units
Resistance, AC, Junction to case	F≥60 Hz		0.35		°C/W
Resistance, DC, junction to case	F<60 Hz		0.5		°C/W
Resistance, Junction to Air	Full temp range		12		°C/W
Temperature Range, Case	Meet full range specs	-25		+85	°C
Temperature Sense Diode Temp. Coefficient			-2		mV/°C

Figure 4: Power Derating

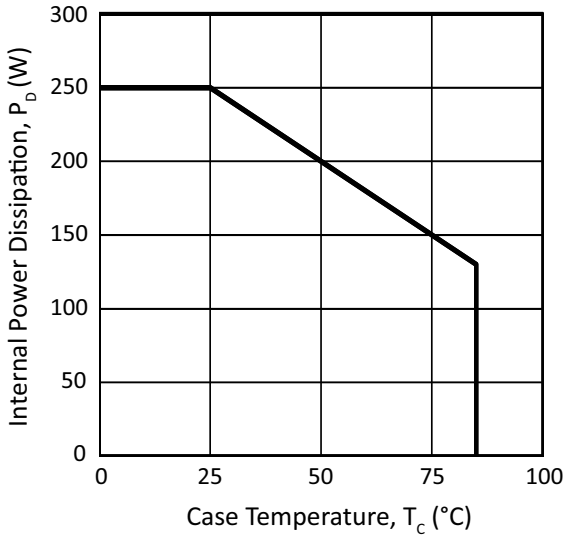


Figure 5: Power Response

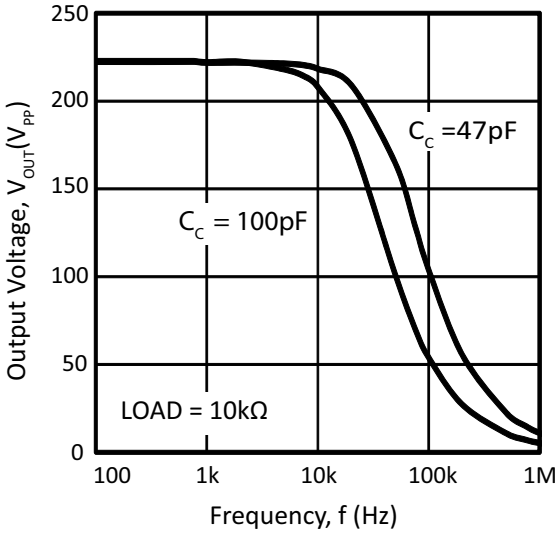


Figure 6: Phase Response

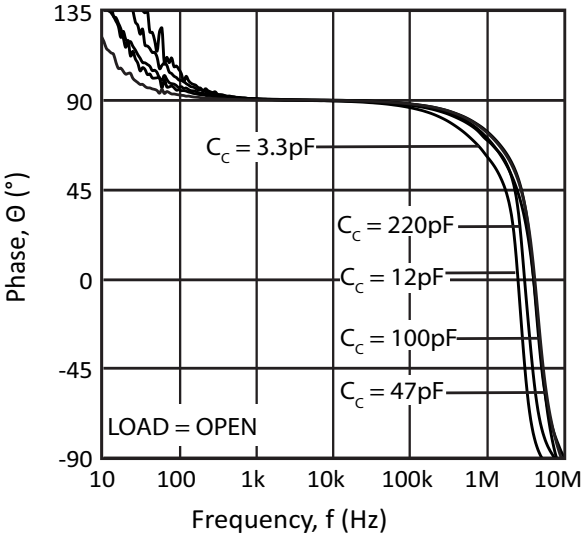


Figure 7: Small Signal Response

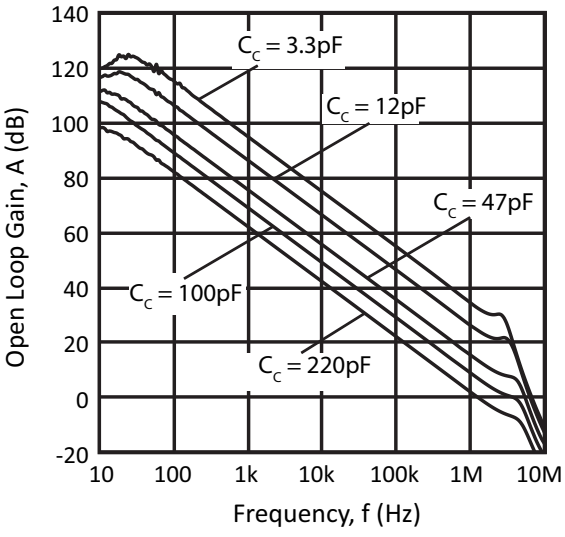


Figure 8: Output Voltage Swing

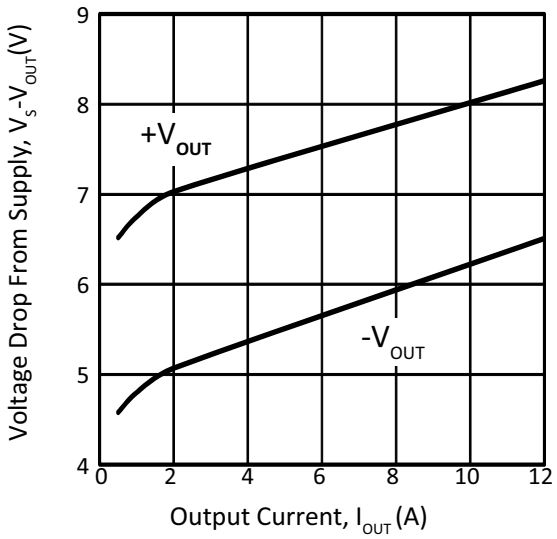


Figure 9: Quiescent Current

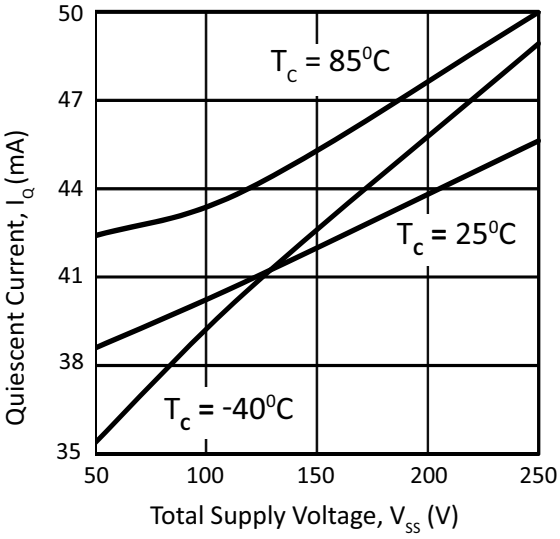


Figure 10: Power Supply Rejection

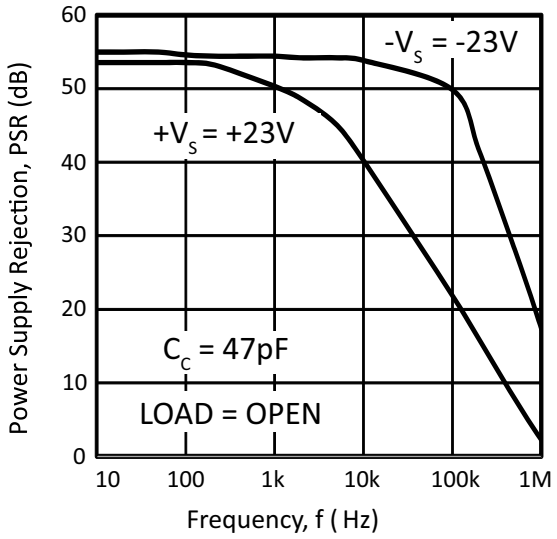


Figure 11: Power Supply Rejection

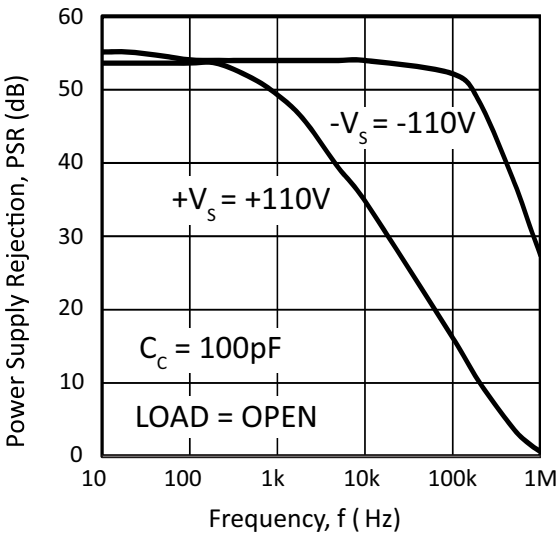


Figure 12: Step Response

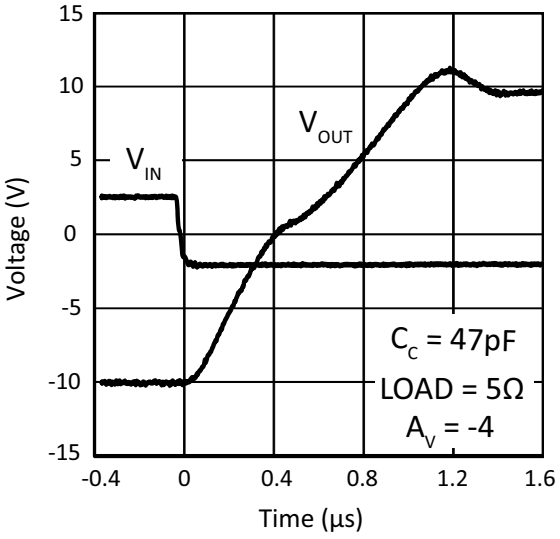


Figure 13: Pulse Response

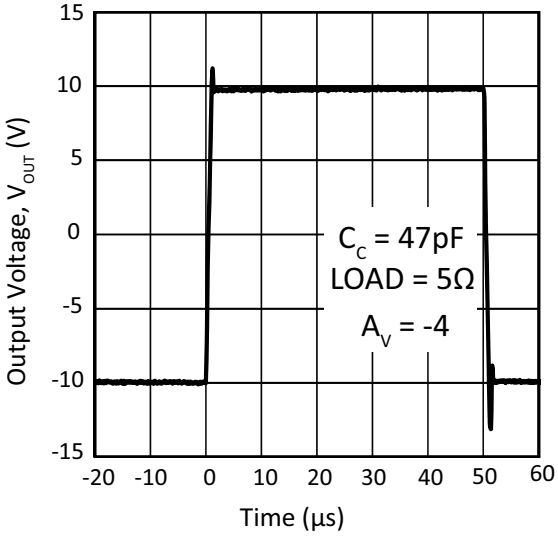
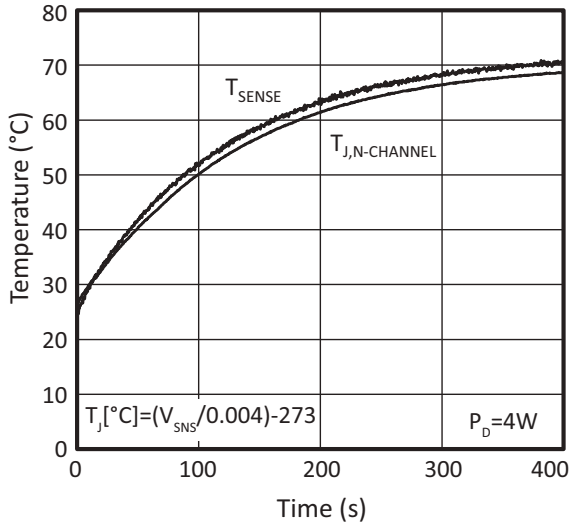


Figure 14: Temp Sense vs Time



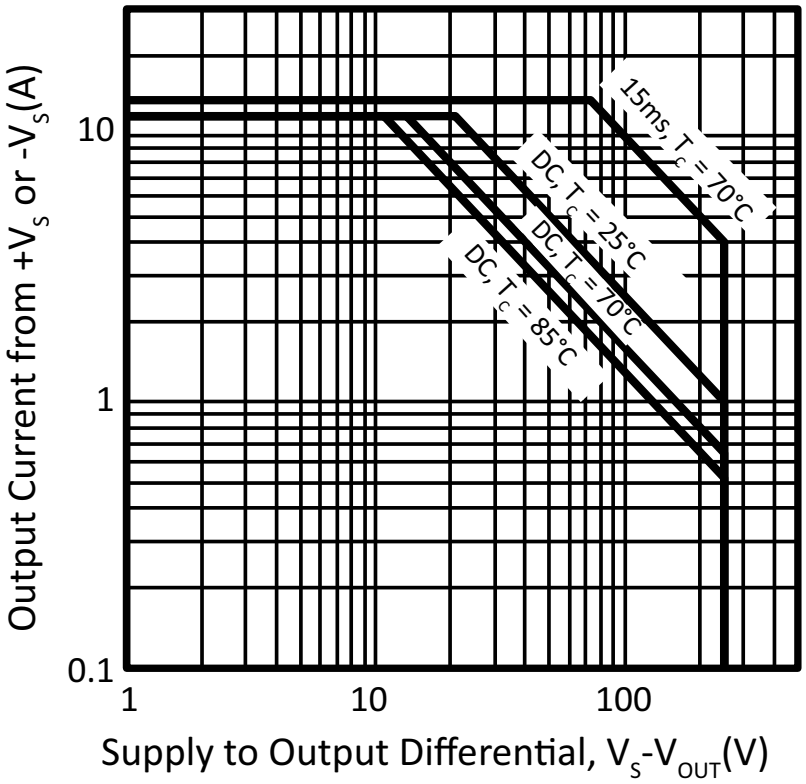
GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, and Technical Seminar Workbook, and Evaluation Kits.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of the PA22 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Figure 15). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback conditions, external fast-recovery diodes must be used.

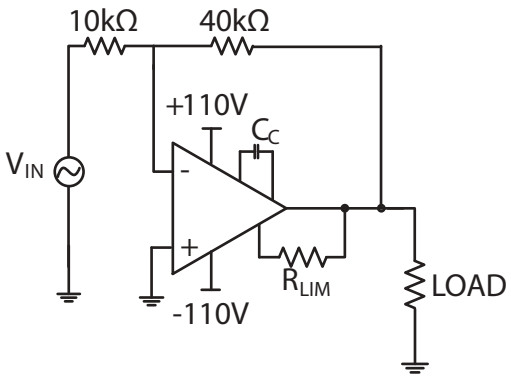
Figure 15: Safe Operating Area (SOA)



TYPICAL APPLICATION

In Figure 16, PA22 is used in an inverting gain of 4 for a programmable voltage source application.

Figure 16: Typical Application Schematic



CURRENT LIMIT

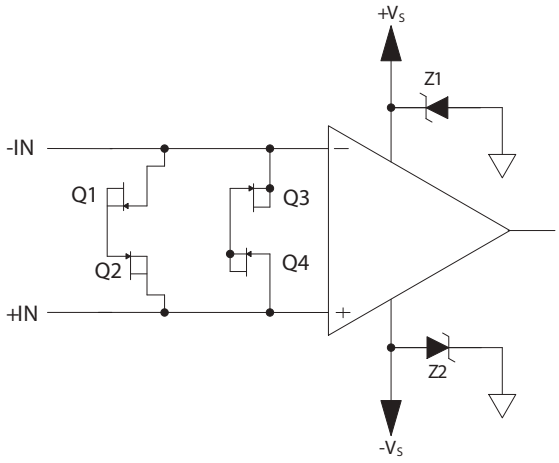
For proper operation, the current limit resistor (R_{LIM}) must be connected as shown in the external connection diagram. For optimum reliability, the resistor value should be set as high as possible. The value is calculated as follows. The current limit function can be disabled by shorting the I_{LIM} pin to the OUT pin. When current limit is active, an internal bias current of 20 mA typical will be shunted through R_{LIM} into the load. The lowest practical current limit level will be 20 mA.

$$I_{LIM} = \frac{0.65\,V}{R_{LIM}} + \begin{pmatrix} 20mA, I_{OUT} \geq 0A \\ -10mA, I_{OUT} < 0A \end{pmatrix}$$

OVERVOLTAGE PROTECTION

Although the PA22 can withstand differential input voltages up to ±25 V, additional external protection is recommended. In most applications, 1N4148 signal diodes connected series anti-parallel across the input pins is sufficient. In more demanding applications where bias current is important, diode-connected JFETs such as 2N4416 will be required. See Q1 through Q4 in Figure 17. In either case, the differential input voltage will be clamped to ±1.4 V. This is usually sufficient overdrive to produce the maximum power bandwidth. Some applications will also need over voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zener diodes clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zener diodes are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals, as well as line regulation. See Z1 and Z2 in Figure 17.

Figure 17: Overvoltage Protection



POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins. Apex recommends to use electrolytic capacitors of 10 µF or greater per output amp. As additional prevention of local parasitic oscillation in the output stage of the PA22, Apex advises to place high quality ceramic capacitors (X7R) of 0.1 µF or greater in parallel to the electrolytic capacitors.

PHASE COMPENSATION

The external compensation capacitor C_C is connected between pins 3 and 4. Unity gain stability can be achieved with any capacitor value larger than 220 pF for a minimum phase margin of 45° driving resistive loads. At higher gains, more phase shift can usually be tolerated, and the compensation capacitor value can be reduced to result in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C for the application. An NPO (COG) type capacitor rated for the full supply voltage (250 V) is required.

TEMPERATURE SENSE

PA22 offers accurate junction-temperature sense. This uses two parallel bipolar transistors mounted directly on top of select power die for near-junction temperature measurement. Connect pins 12 and 13 to the D- and D+ pins of LTC2997 (or similar device), respectively. The LTC2997 will properly bias the bipolar transistors and translate the signal to a Proportional To Absolute Temperature (PTAT) voltage. Apex does not recommend reading temperature without an LTC2997 or similar device.

PACKAGE OPTIONS

Part Number	Apex Package Style	Description
PA22	LL	15-Pin Power SIP

PACKAGE OUTLINE (STYLE LL)

NOTES:
1. Dimensions are in inches & [mm].
2. Triangle on lid denotes Pin 1.
3. Pins: Alloy 510 phosphor bronze plated with matte tin (150-300u") over nickel (500u" max.) underplate.
4. Epoxy-sealed & ultrasonically welded non-hermetic package.
5. Creepage distance between I/O pin pads: 0.050 inches.
6. The exposed substrate contains BeO. Do not crush, machine or subject to temperatures in excess of 850° C to avoid generating toxic fumes.