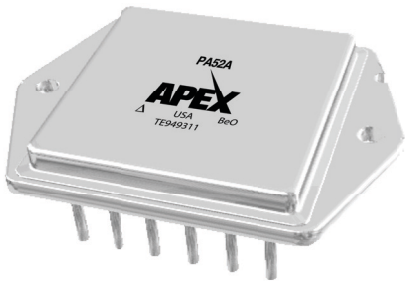
PA52 • PA52A

Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- High Internal Dissipation — 400W
- High Current — 40A Continuous, 80A Peak
- High Slew Rate — 50V/µs
- Optional Boost Voltage Inputs



APPLICATIONS

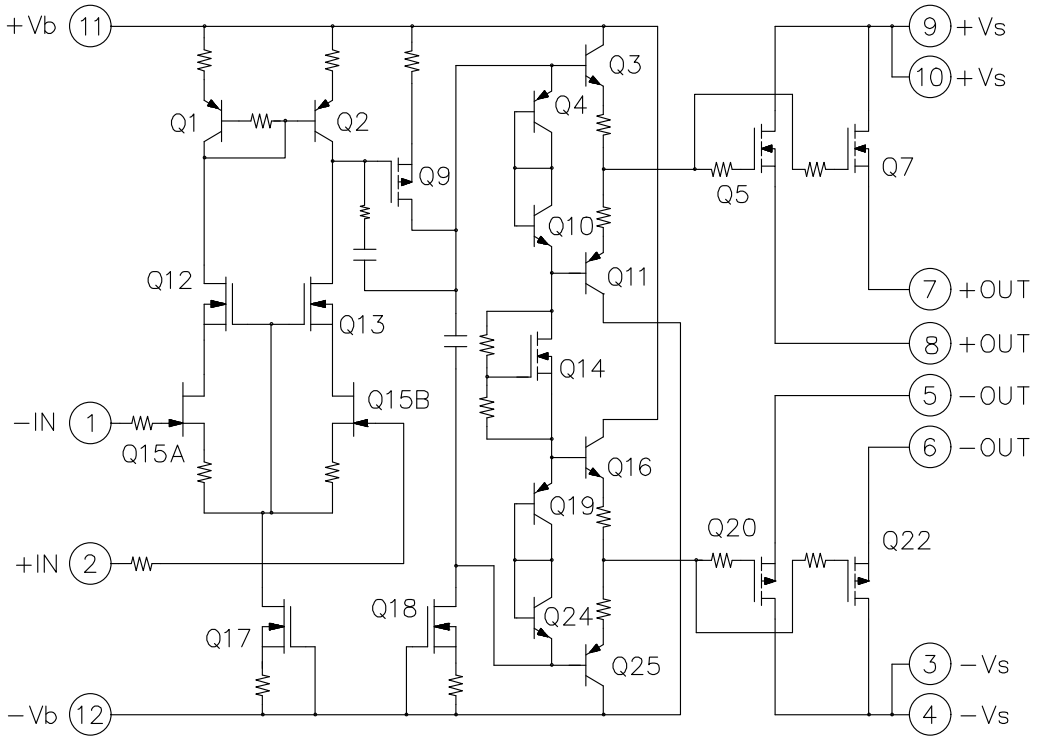
- Semi-conductor Testing
- Brushless DC Motor Drive
- Voltage Controlled Current Source
- Electromagnetic Driver

DESCRIPTION

The PA52 is a MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation.

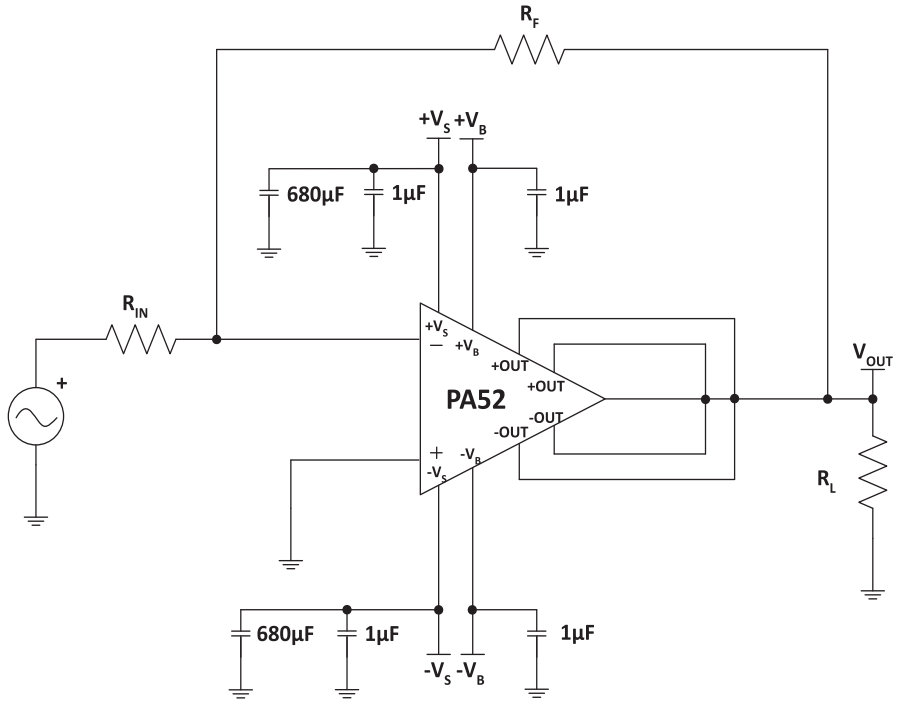
The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see Application Note 1, “General Operating Considerations”.

Figure 1: Equivalent Schematic



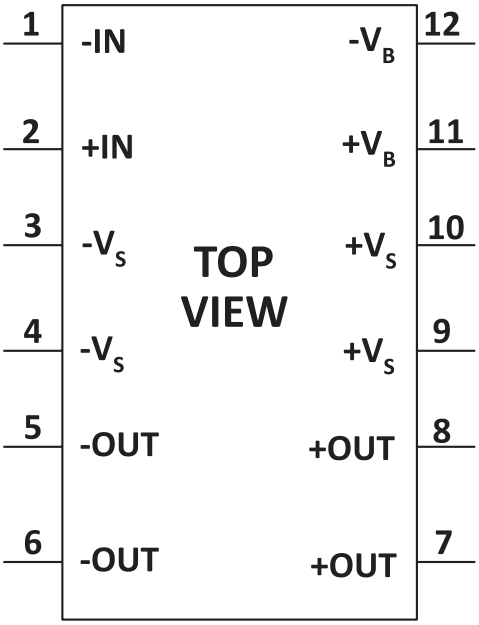
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	-IN	The inverting input.
2	+IN	The non-inverting input.
3, 4	$-V_S$	The negative supply rail. Pins 3 and 4 are internally connected.
5, 6	-OUT	The negative output. Pins 5 and 6 are not internally connected. Short pins 5, 6, 7, and 8.
7, 8	+OUT	The positive output. Pins 7 and 8 are not internally connected. Short pins 5, 6, 7, and 8.
9, 10	$+V_S$	The positive supply rail. Pins 9 and 10 are internally connected.
11	$+V_B$	The positive boost supply rail. Short to $+V_S$ if unused. See applicable section.
12	$-V_B$	The negative boost supply rail. Short to $-V_S$ if unused. See applicable section.

SPECIFICATIONS

Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_B = \pm V_S$.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, $+V_S$ To $-V_S$	$+V_S$ to $-V_S$		200	V
Boost Voltage, $+V_B$ To $-V_B$			230	V
Output Current, within SOA	I_{OUT}		80	A
Power Dissipation, internal	P_D		400	W
Input Voltage, differential	$V_{IN\ (Diff)}$	-20	20	V
Input Voltage, common mode	V_{CM}	$-V_B$	$+V_B$	V
Temperature, pin solder, 10s			350	°C
Temperature, junction [1]	T_J		150	°C
Temperature, storage		-65	+150	°C
Operating Temperature Range, case	T_C	-55	+125	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.

CAUTION The PA52 is constructed from MOSFET transistors. ESD handling procedures must be observed. The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA52			PA52A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial			5	10		2	5	mV
Offset Voltage vs. temperature	Full temp range		20	50		*	*	µV/°C
Offset Voltage vs. supply			10	30		*	*	µV/V
Bias Current, initial			10	50		*	*	pA
Bias Current vs. supply			0.01			*		pA/V
Offset Current, initial			10	50		*	*	pA
Input Impedance, DC			10^{11}			*		Ω
Input Capacitance			13			*		pF
Common Mode Voltage Range	Full temp range	$-V_B$ +12 $+V_B$ -14			*			V
Common Mode Rejection, DC	Full temp range, V_{CM}= ±20V	90	100			*	*	dB
Input Noise	100 kHz BW, R_S=1 kΩ		10			*		µVrms

GAIN

Parameter	Test Conditions	PA52			PA52A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop, @ 15 Hz	Full temp range	94	102		*	*		dB
Gain Bandwidth Product	R_L=10 Ω		3			*		MHz
Power Bandwidth	R_L = 4 Ω, V_{OUT}=180V_{P-P}, A_V= -10 Full temp range		90			*		kHz

OUTPUT

Parameter	Test Conditions	PA52			PA52A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing	I_{OUT} = 40A	$\pm V_S \pm 9.5$	$\pm V_S \pm 8.0$		*	*		V
Voltage Swing, PA52	$\pm V_B = \pm V_S \pm 10V$, I_{OUT}=40A	$\pm V_S \pm 5.8$	$\pm V_S \pm 4.0$					V
Voltage Swing, PA52A	$\pm V_B = \pm V_S \pm 10V$, I_{OUT}=50A				$\pm V_S \pm 5.8$	$\pm V_S \pm 5.0$		V
Current, peak	3ms 10% Duty Cycle	80			*			A
Settling Time to 0.1%	A_V = -10, 10V Step, R_L=4 Ω		1			*		µs
Slew Rate	A_V=-10	50			*			V/µs
Resistance	I_{OUT}=0, No Load, 2 MHz		2.5			*		Ω

POWER SUPPLY

Parameter	Test Conditions	PA52			PA52A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage, $\pm V_B$	Full temp range	+14,-12	±30	±115	*	*	*	V
Voltage, $\pm V_S$	Full temp range	±3		±100	*		*	V
Current, quiescent, boost supply			26	32		*	*	mA
Current, quiescent, total			30	36		*	*	mA

THERMAL

Parameter	Test Conditions	PA52			PA52A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case [1]	Full temp range, F > 60 Hz		0.2	0.25		*	*	°C/W
Resistance, DC, junction to case	Full temp range, F > 60 Hz		0.25	0.31		*	*	°C/W
Resistance, junction to air	Full temp range		12			*		°C/W
Temperature Range, case	Meets full range specification	-25		85	*		*	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: *The specification of PA52A is identical to the specification for PA52 in applicable column to the left

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

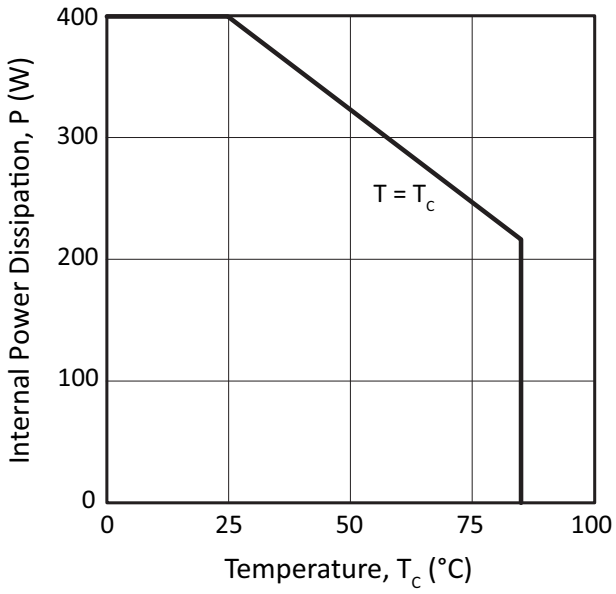


Figure 5: Power Supply Rejection

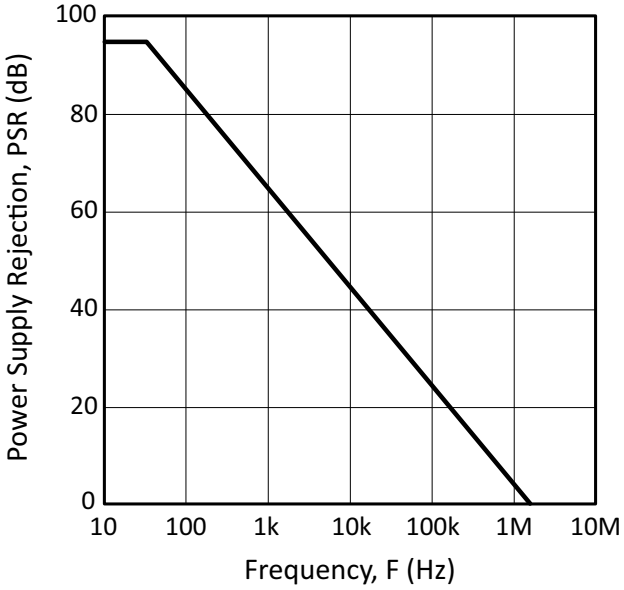


Figure 6: Small Signal Gain

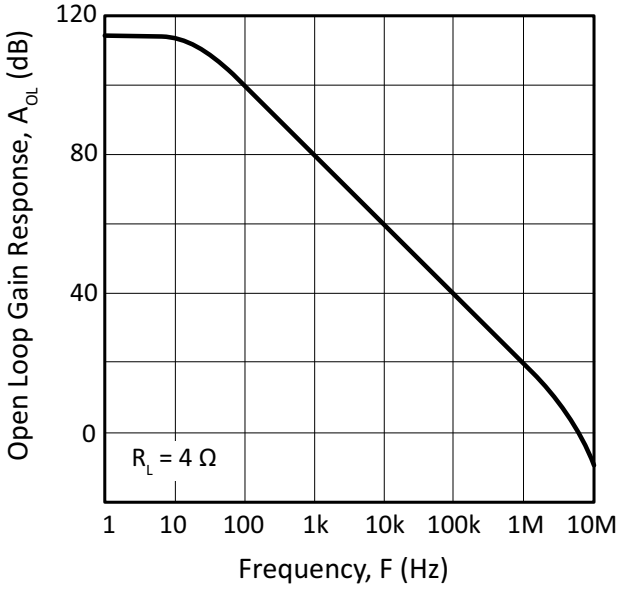


Figure 7: Small Signal Phase

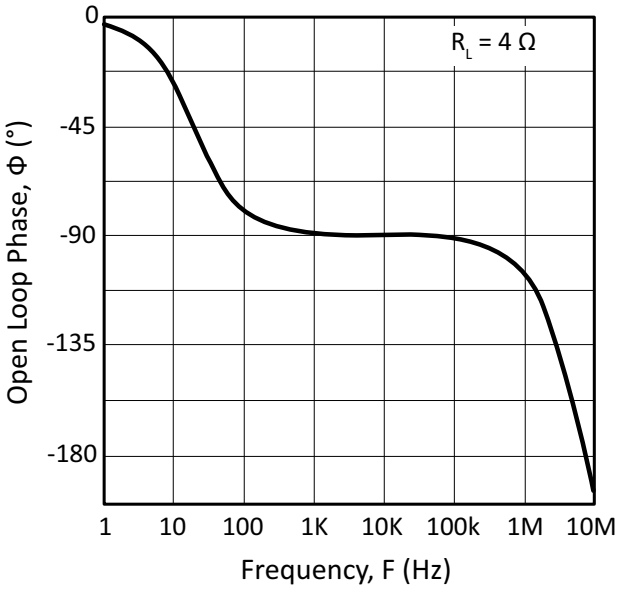


Figure 8: Output Voltage Swing

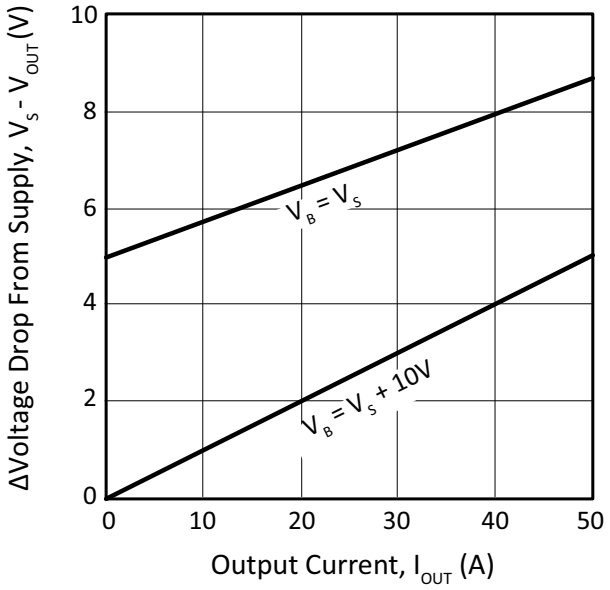


Figure 10: Power Response

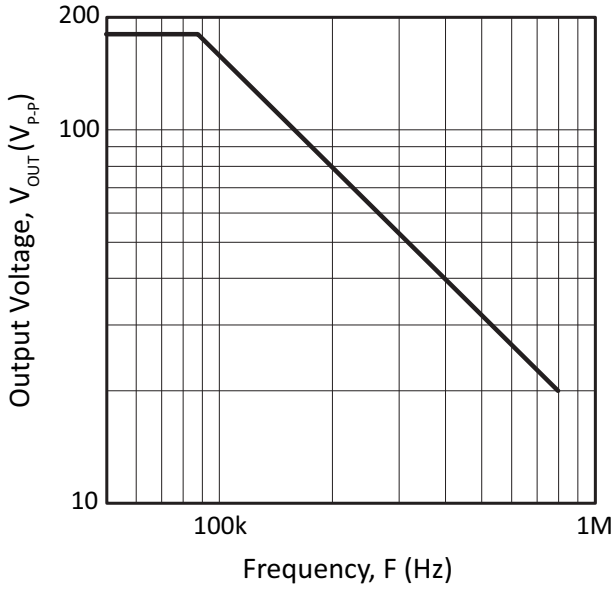


Figure 9:

Figure 11: Common Mode Rejection

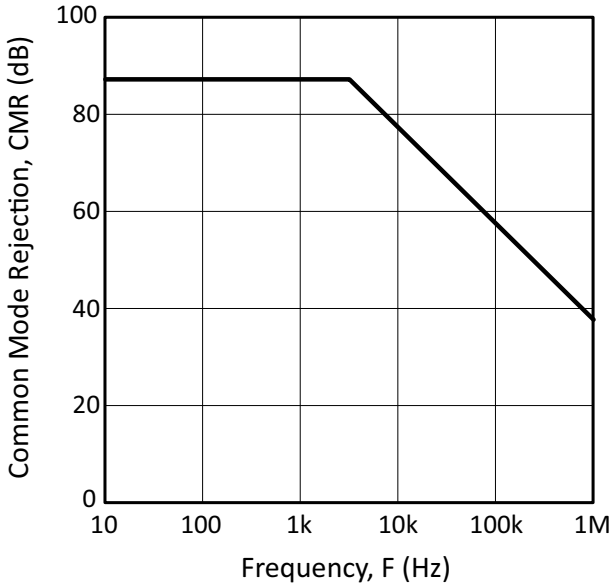
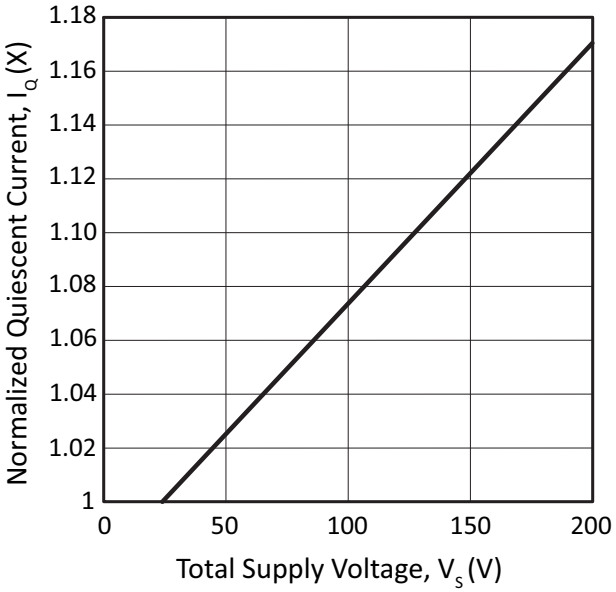
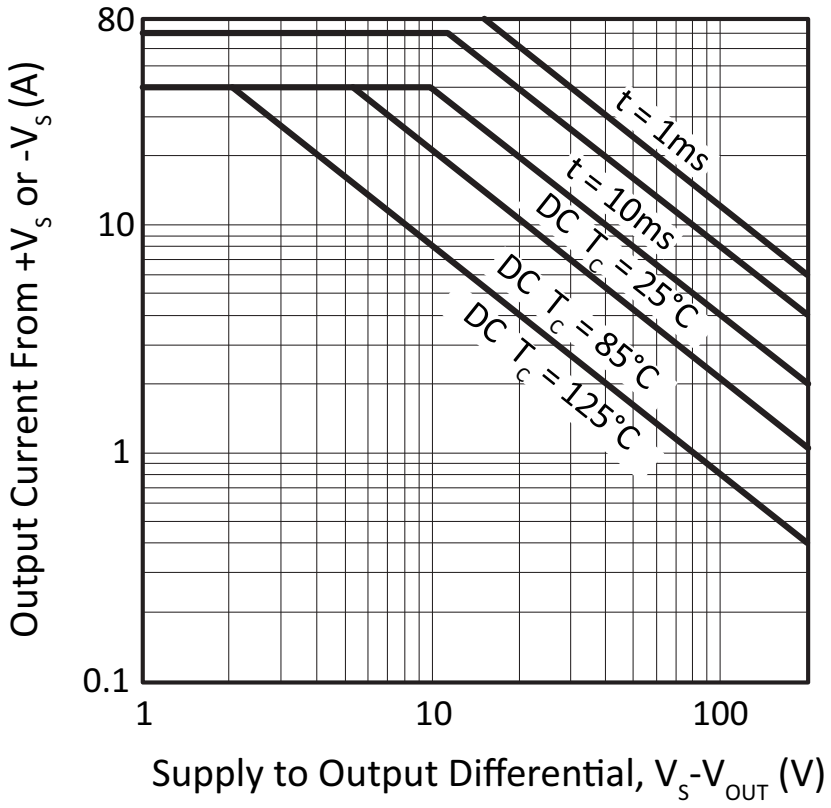


Figure 12: Quiescent Current



SAFE OPERATING AREA (SOA)

Figure 13: SOA



GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

CURRENT LIMIT

There is no internal circuit provision for current limit in the PA52. However, the PA52 circuit board in the PA52 evaluation kit does provide a means whereby the output current can be sensed. An external circuit current limit can thereby be implemented if needed.

BOOST OPERATION

With the V_B feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier’s high current output stage. $+V_B$ (pin 11) and $–V_B$ (pin 12) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 9,10) and $–V_S$ (pin 3,4) are connected to the high current output stage. An additional 10V on the V_B pins is sufficient to allow the small signal stages to drive the output transistors into

saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_B$ and $+V_S$ pins must be strapped together as well as the $–V_B$ and $–V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

Compensation is internally fixed for a gain of 3 or more and is not adjustable by the user. The PA52 therefore is not unity gain stable.

POWER SUPPLY BYPASSING

Proper and sufficient power supply bypassing is crucial to proper operation of the PA52. Bypass the $+V_B$ and $-V_B$ supply pins with a minimum 0.1µF ceramic capacitors directly at the supply pins. On the $+V_S$ and $-V_S$ pins use a combination of ceramic and electrolytic capacitors. Use 1µF ceramic capacitors and an electrolytic capacitor at least 10µF for each amp of output current required.