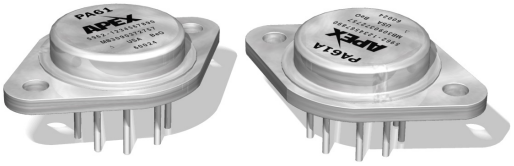
PA61 • PA61A

Power Operational Amplifiers

RoHS COMPLIANT

FEATURES



- Wide Supply Range — ±10 to ±45V
- High Output Current — ±10A Peak
- Low Cost — Class "C" Output Stage
- Low Quiescent Current — 3mA

APPLICATIONS

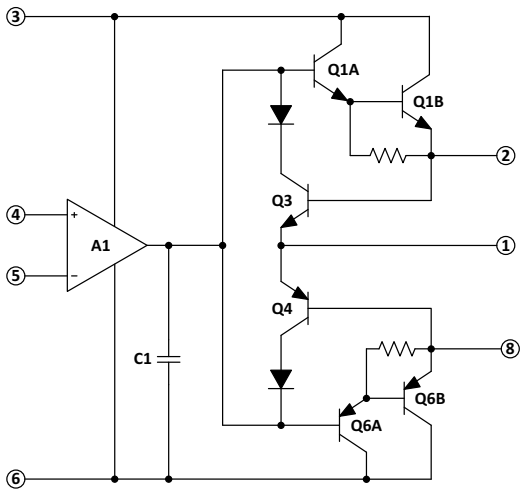
- Programmable Power Supply
- Motor/Syncro Driver
- Valve And Actuator Control
- DC or AC Power Regulator
- Fixed Frequency Power Oscillator

DESCRIPTION

The PA61 and PA61A are high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary emitter follower output stage is the simple class C type and optimized for low frequency applications where crossover distortion is not critical. These amplifiers are not recommended for audio, transducer or deflection coil drive circuits above 1 kHz or when distortion is critical. The safe operating area (SOA) is fully specified and can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

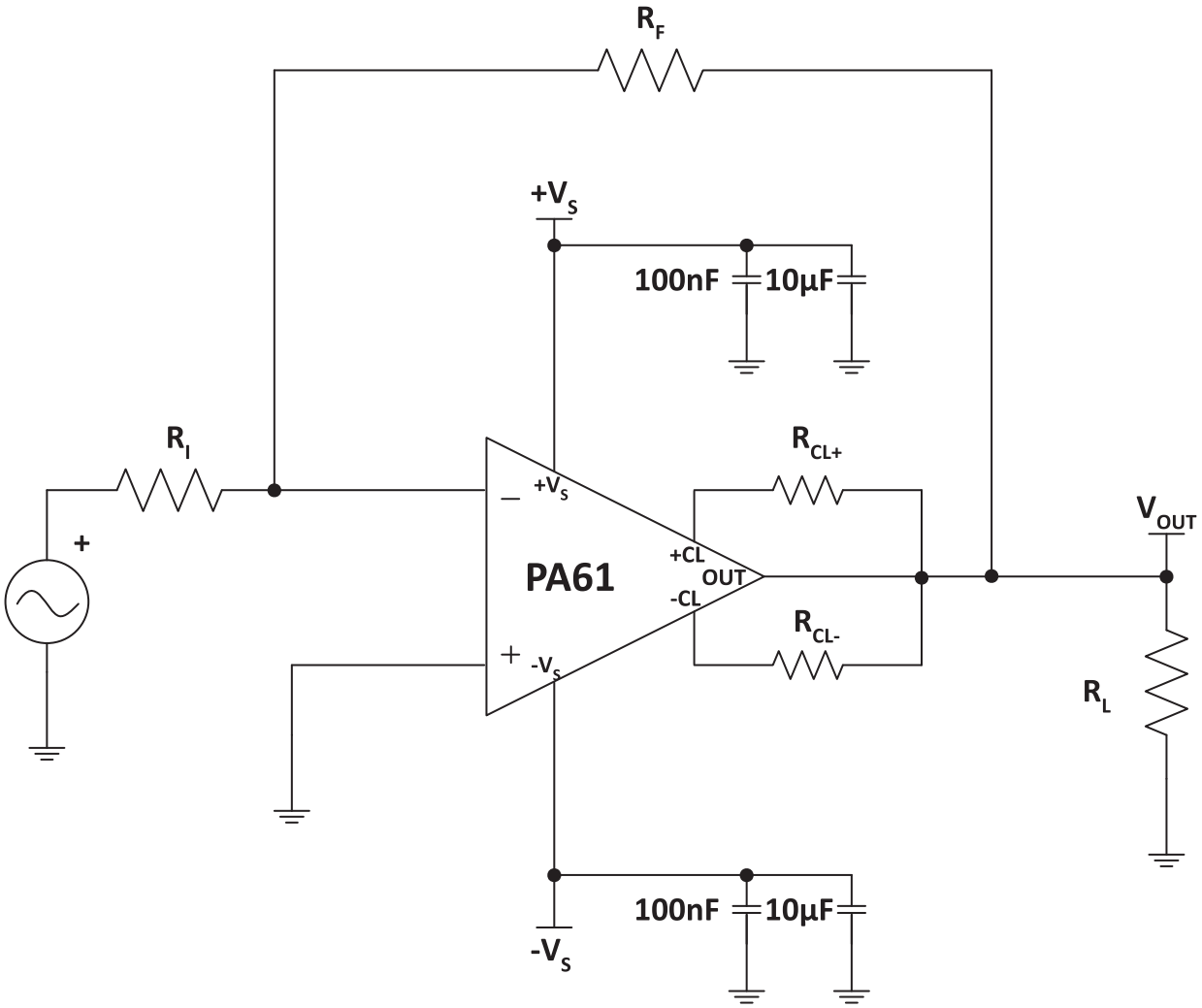
This hybrid circuit utilizes thick film conductors, ceramic capacitors, and semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed. The use of compressible thermal washers and/or improper mounting torque voids the product warranty. Please see Application Note 1, "General Operating Considerations".

Figure 1: Equivalent Schematic



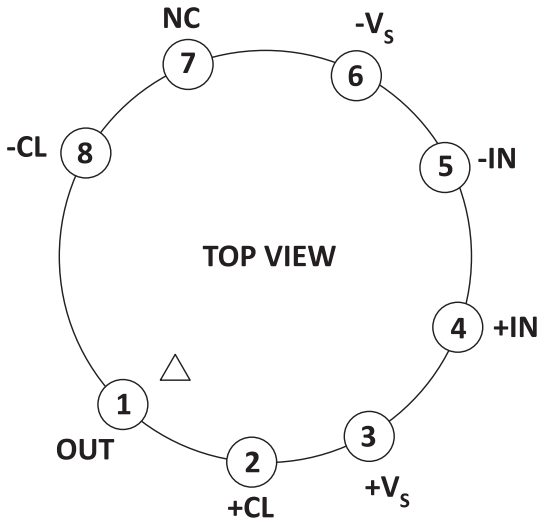
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	OUT	The output. Connect this pin to load and to the feedback resistors.
2	+CL	Connect to the sourcing current limit resistor. Output current flows into/out of this pin through R_{CL+}. The output pin and the load are connected to the other side of R_{CL+}.
3	-Vs	The positive supply rail.
4	+IN	The non-inverting input.
5	-IN	The inverting input.
6	-Vs	The negative supply rail.
7	NC	No connection.
8	-CL	Connect to the sinking current limit resistor. Output current flows into/out of this pin through R_{CL-}. The output pin and the load are connected to the other side of R_{CL-}.

SPECIFICATIONS

The power supply voltage for all specifications is the TYP rating unless noted as a test condition.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_S$ to $-V_S$		90	V
Output Current, within SOA	I_O		10	A
Power Dissipation, internal	P_D		97	W
Input Voltage, differential	$V_{IN\ (Diff)}$		±37	V
Input Voltage, common mode	V_{cm}		$\pm V_S$	V
Temperature, pin solder, 10s max.			350	°C
Temperature, junction [1]	T_J		200	°C
Temperature Range, storage		-65	+150	°C
Operating Temperature Range, case	T_C	-55	+125	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA61			PA61A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial	T_C = 25°C		±2	±6		±1	±4	mV
Offset Voltage vs. Temperature	Specified temp range		±10	±65		*	±40	µV/°C
Offset Voltage vs. Supply	T_C = 25°C		±30	±200		*	*	µV/V
Offset Voltage vs. Power	T_C = 25°C		±20			*		µV/W
Bias Current, initial	T_C = 25°C		12	30		10	20	nA
Bias Current vs. Temperature	Specified temp range		±50	±500		*	*	pA/°C
Bias Current vs. Supply	T_C = 25°C		±10			*		pA/V
Offset Current, initial	T_C = 25°C		±12	±30		±5	±10	nA
Offset Current vs. Temperature	Specified temp range		±50			*		pA/°C
Input Impedance, DC	T_C = 25°C		200			*		MΩ
Input Capacitance	T_C = 25°C		3			*		pF
Common Mode Voltage Range [1]	Specified temp range	$\pm V_S - 5$	$\pm V_S - 3$		*	*		V
Common Mode Rejection, DC [1]	Specified temp range	74	100		*	*		dB

1. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.

GAIN

Parameter	Test Conditions	PA61			PA61A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop @ 10 Hz	Full temp range, full load	96	108		*	*		dB
Gain Bandwidth Product @ 1 MHz	T_C = 25°C, full load		1			*		MHz
Power Bandwidth	T_C = 25°C, I_O = 8A, $V_O = 40V_{PP}$	10	16		*	*		kHz
Phase Margin	Full temp range		45			*		°

OUTPUT

Parameter	Test Conditions	PA61			PA61A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing [1]	T_C=25°C, I_O=10A	$\pm V_S$–7	$\pm V_S$–5		$\pm V_S$–6	*		V
Voltage Swing [1]	Full temp range, I_O = 4A	$\pm V_S$–6	$\pm V_S$–4		*	*		V
Voltage Swing [1]	Full temp range, I_O = 68mA	$\pm V_S$–5			*			V
Current	T_C = 25°C	±10			*			A
Settling Time to 0.1%	T_C=25°C, 2V step		2			*		µs
Slew Rate	T_C=25°C, R_L=6 Ω	1.0	2.8		*	*		V/µs
Capacitive Load, unit gain	Full temp range			1.5			*	nF
Capacitive Load, gain > 4	Full temp range			SOA			*	

1. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.

POWER SUPPLY

Parameter	Test Conditions	PA61			PA61A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage	Full temp range	±10	±32	±45	*	*	*	V
Current, quiescent	T_C = 25°C		3	10		*	*	mA

THERMAL

Parameter	Test Conditions	PA61			PA61A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case [1]	F > 60 Hz		1.0	1.2		*	*	°C/W
Resistance, DC, junction to case	F < 60 Hz		1.5	1.8		*	*	°C/W
Resistance, junction to air			30			*		°C/W
Temperature Range, case	Meets full range specs	-25	25	+85	*	*	*	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: * The specification of PA61A is identical to the specification for PA61 in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

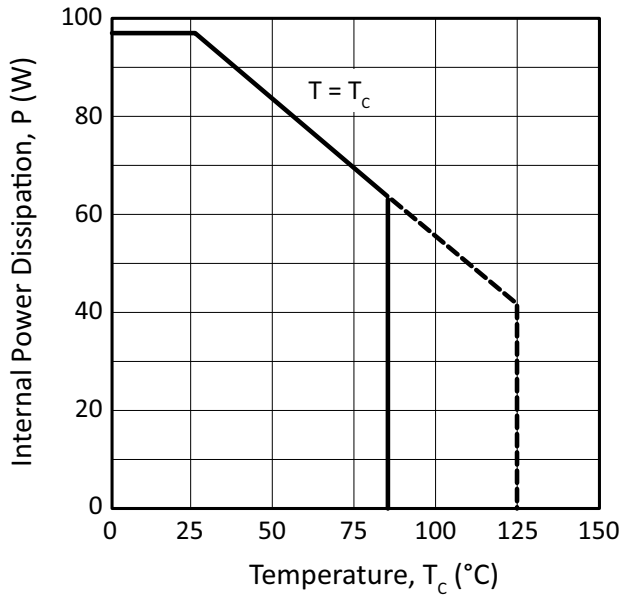


Figure 5: Output Voltage Swing

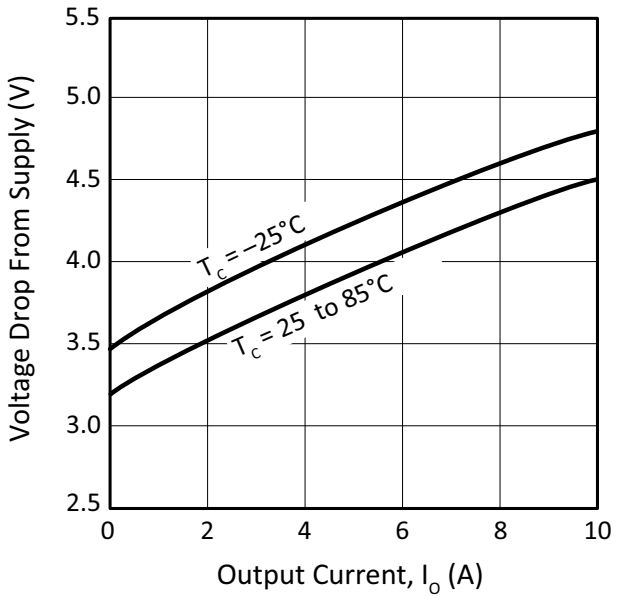


Figure 6: Small Signal Response

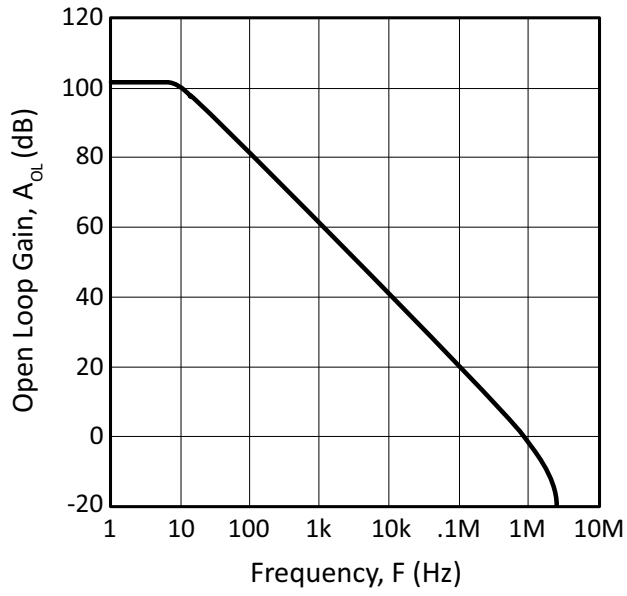


Figure 7: Phase Response

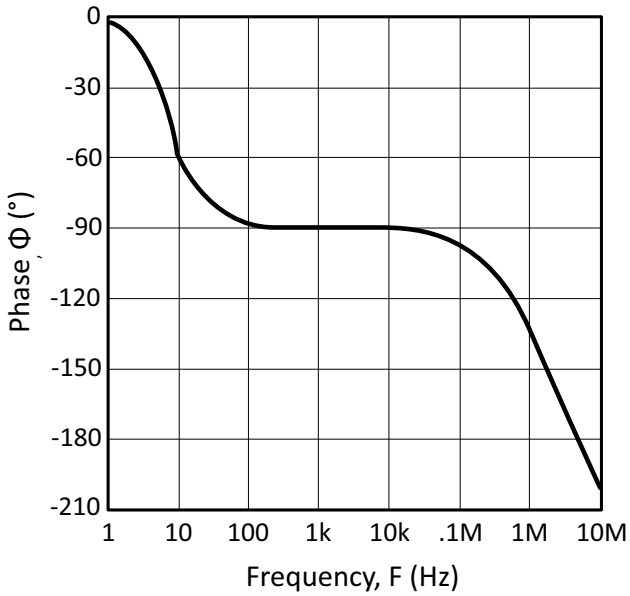


Figure 8: Current Limit

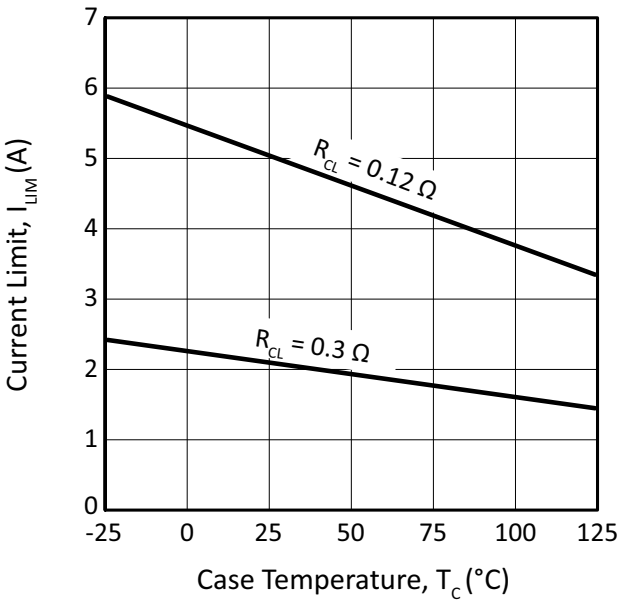


Figure 9: Power Response

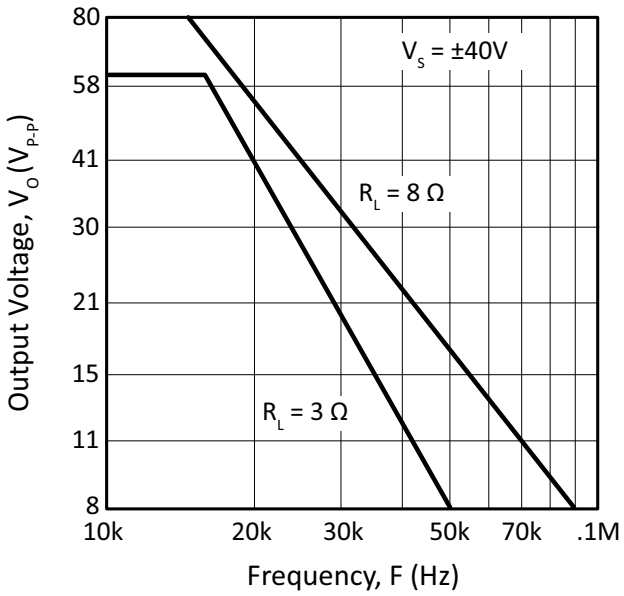


Figure 10: Pulse Response

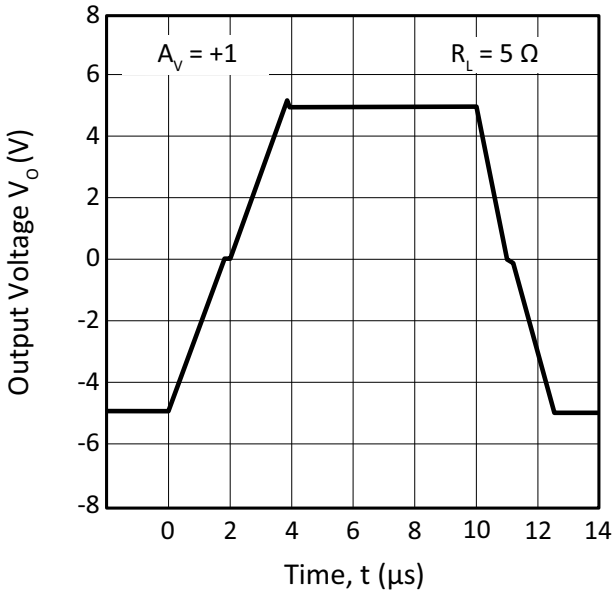


Figure 11: Common Mode Rejection

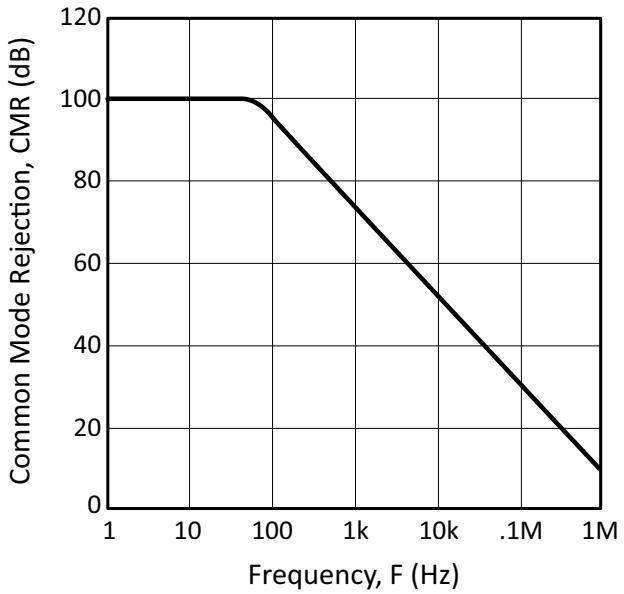


Figure 12: Bias Current

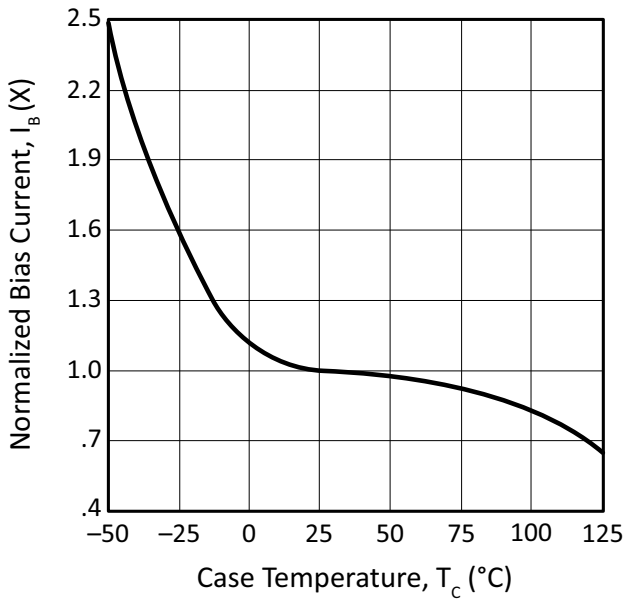


Figure 13: Harmonic Distortion

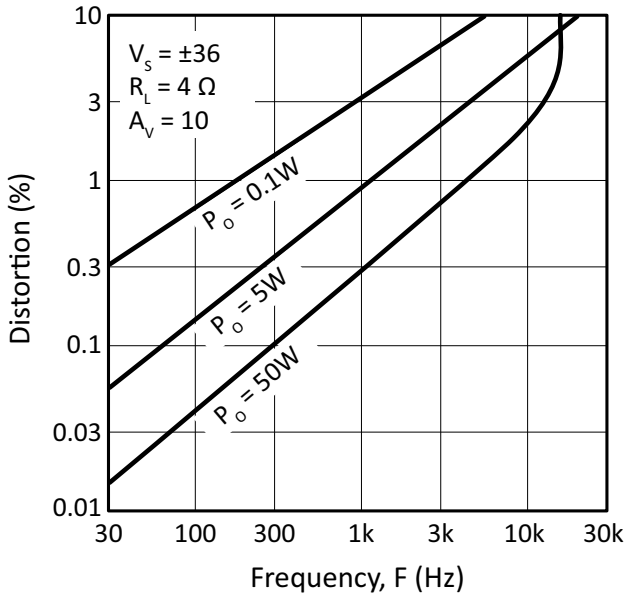


Figure 14: Quiescent Current

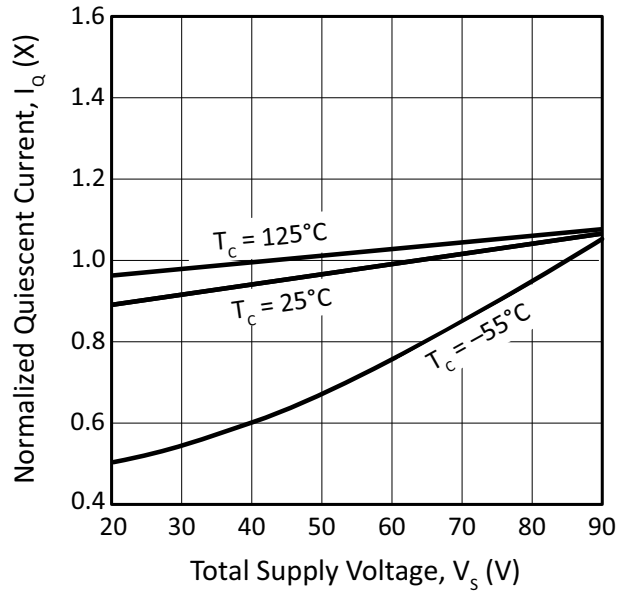
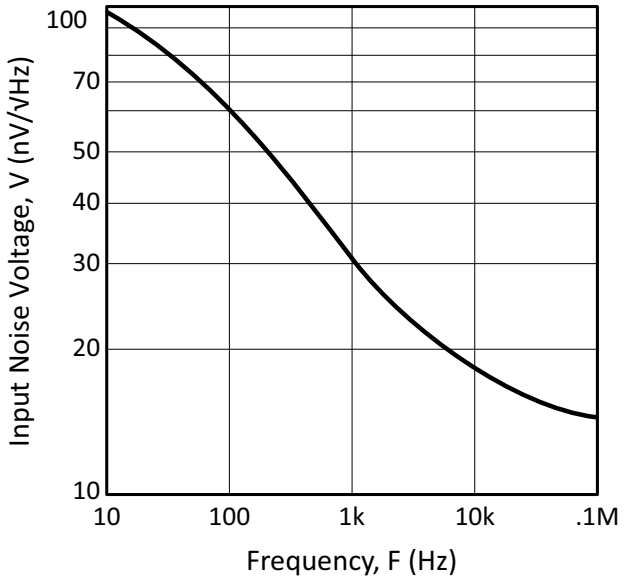


Figure 15: Input Noise



SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximum are safe:

$\pm V_S$	Capacitive Load		Inductive Load	
	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
45V	200 F	150 F	8 mH	2.8 mH
40V	400 F	200 F	11 mH	4.3 mH
35V	800 F	400 F	20 mH	5.0 mH
30V	160 F	800 F	35 mH	6.2 mH
25V	5mF	2.5mF	50 mH	15 mH
20V	10mF	5mF	400 mH	20 mH
15V	20mF	10mF	**	100 mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 10A or 15V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Second breakdown effect imposes no limitation but thermal limitations must still be observed.

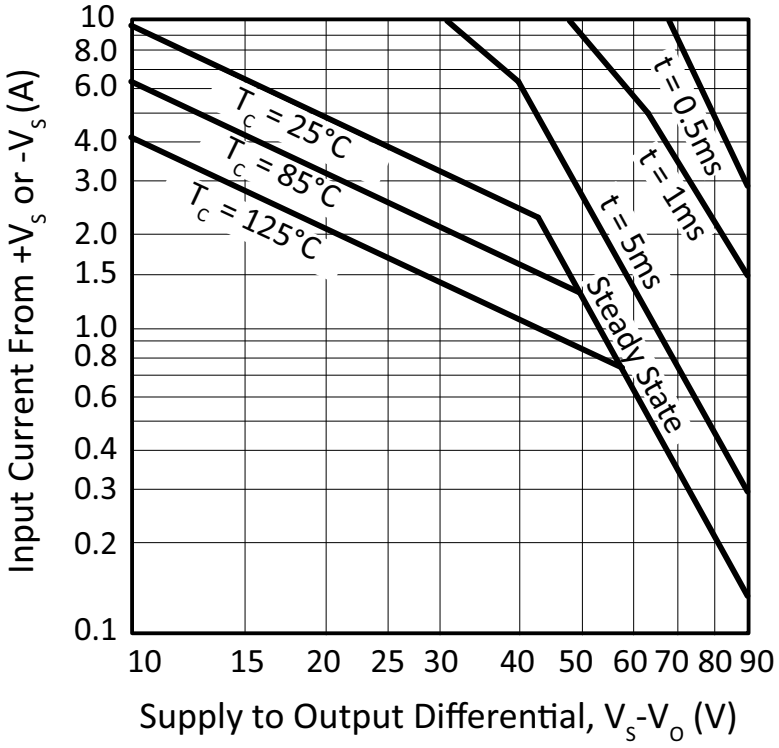
2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C = 85°C.

$\pm V_S$	Short to $\pm V_S$ C, L, or EMF Load	Short to Common
45V	0.1A	1.3A
40V	0.2A	1.5A
35V	0.3A	1.6A
30V	0.5A	2.0A
25V	1.2A	2.4A
20V	1.5A	3.0A
15V	2.0A	4.0A

* These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

Figure 16: SOA



GENERAL

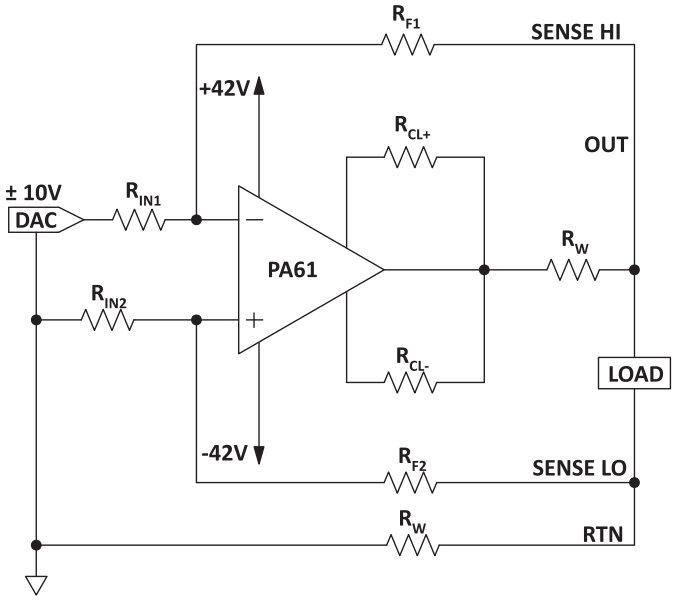
Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

Due to its high current drive capability, PA61 applications often utilize remote sensing to compensate IR drops in the wiring. The importance of remote sensing increases as accuracy requirements, output currents, and distance between amplifier and load go up. The circuit above shows wire resistance from the PA61 to the load and back to the local ground via the power return line. Without remote sensing, a 7.5A load current across only 0.05 ohm in each line would produce a 0.75V error at the load.

With the addition of the second ratio matched R_F/R_{IN} pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop. Therefore, as long as the Power Op Amp has the voltage drive capability to overcome the IR losses, accuracy remains the same. Application Note 7 presents a general discussion of PPS circuits.

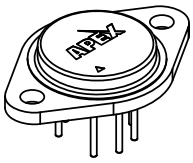
Figure 17: Typical Application (Programmable Power Supply With Remote Sensing)

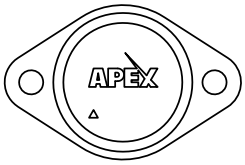


PACKAGE OPTIONS

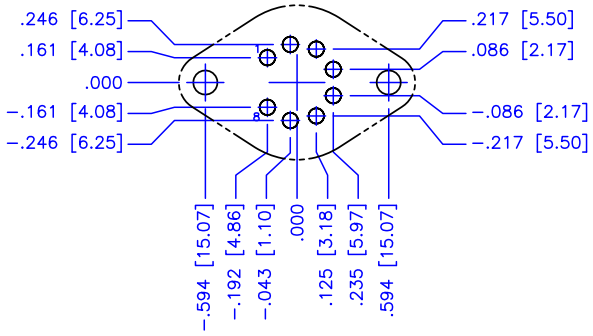
Part Number	Apex Package Style	Description
PA61	CE	8-pin TO-3
PA61A	CE	8-pin TO-3

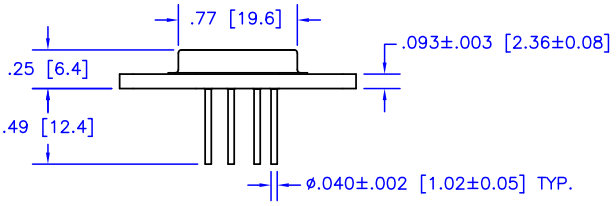
PACKAGE STYLE CE

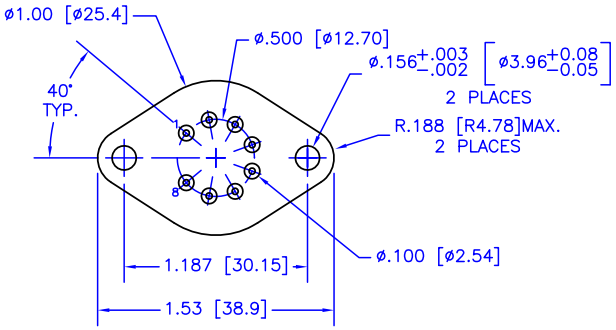




Ordinate dimensions for CAD layout







NOTES:

1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Header flatness within pin circle is .0005" TIR, max.
4. Header flatness between mounting holes is .0015" TIR, max.
5. Standard pin material: Solderable nickel–plated Alloy 52.
6. Header material: Nickel–plated cold–rolled steel.
7. Welded hermetic package seal
8. Isolation: 500 VDC any pin to case.
9. Package weight: .53 oz [15 g]