PA88 • PA88A

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- High Voltage— 450V (±225V)
- Low Quiescent Current — 2mA
- Output Current— 100mA
- Programmable Current Limit
- Low Bias Current — FET Input

APPLICATIONS

- Piezoelectric Positioning
- High Voltage Instrumentation
- Electrostatic Transducers
- Programmable Power Supplies up to 440V

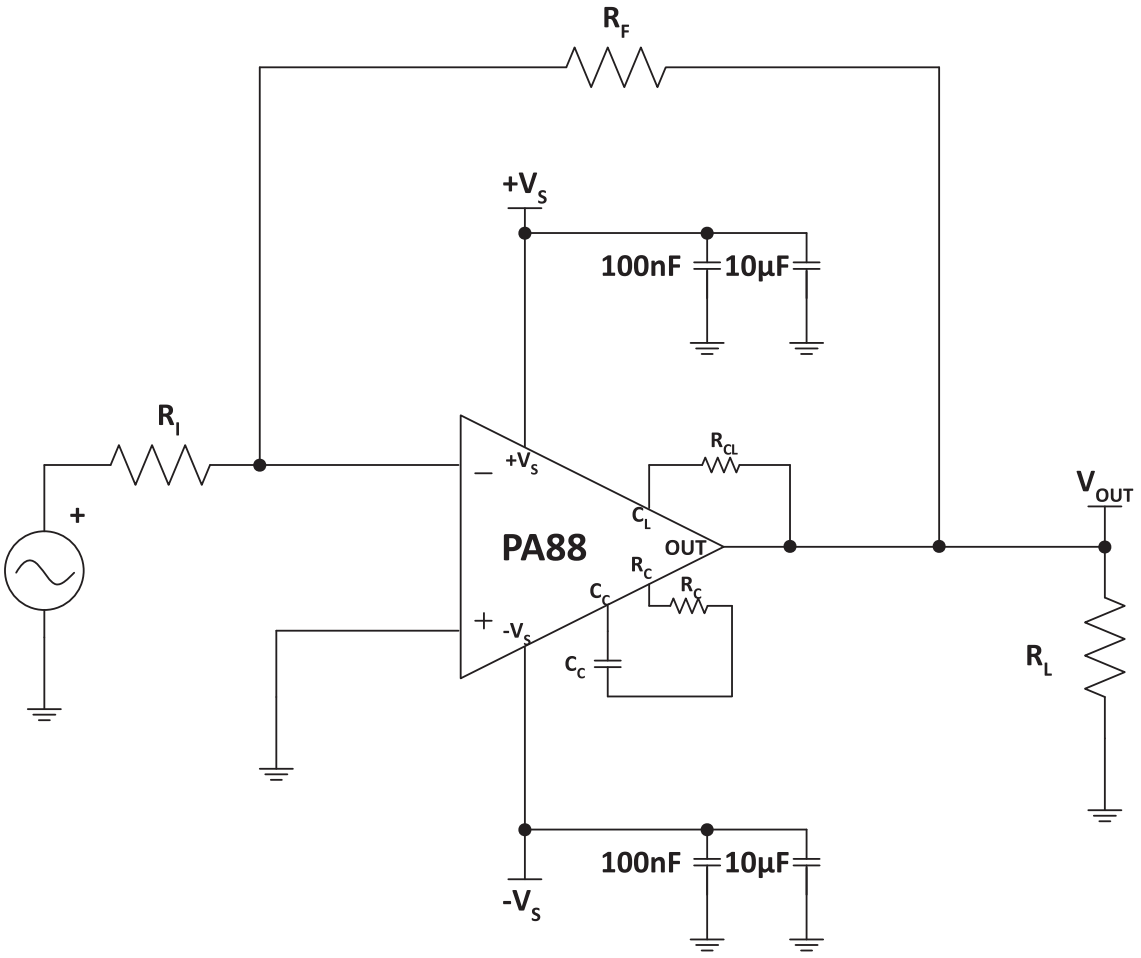
DESCRIPTION

The PA88 is a high voltage, low quiescent current MOSFET operational amplifier designed for output currents up to 100mA. Output voltages can swing up to ±215V with a dual supply and up to +440 volts with a single supply. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a bootstrapped zener-MOSFET current source. As a result, the PA88 features an unprecedented supply range and excellent supply rejection. The MOSFET output stage is biased on for linear operation. External compensation provides user flexibility.

This hybrid circuit utilizes beryllia (BeO) substrates, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque will void the product warranty. Please see Application Note 1, “General Operating Considerations.”

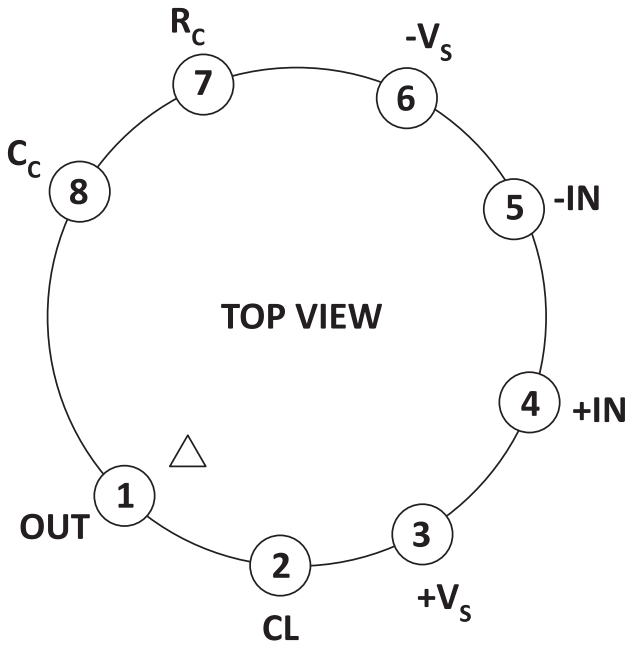
TYPICAL CONNECTION

Figure 1: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 2: External Connections



Pin Number	Name	Description
1	OUT	The output. Connect this pin to load and to the feedback resistors.
2	CL	Connect to the current limit resistor. Output Current flows into/out of these pins through R_{CL}. The output pin and the load are connected to the other side of R_{CL}.
3	+Vs	The positive supply rail.
4	+IN	The non-inverting input.
5	-IN	The inverting input.
6	-Vs	The negative supply rail.
7	RC	Compensation resistor connection. Select value based on Phase Compensation. See applicable section.
8	CC	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.

SPECIFICATIONS

Unless otherwise noted: T_C = 25°C, compensation = C_C = 68pF, R_C = 100 Ω. DC input specifications are ± value given. Power supply voltage is typical rating.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, $+V_S$ To $-V_S$	$+V_S$ to $-V_S$		450	V
Output Current	I_O	See SOA		
Power Dissipation, continuous @ T_c = 25°C	P_D		15	W
Input Voltage, differential	$V_{IN\ (Diff)}$		±25	V
Input Voltage, common mode	V_{cm}		$\pm V_S$	V
Temperature, pin solder - 10s max.			350	°C
Temperature, junction [1]	T_J		150	°C
Temperature, storage		-65	+150	°C
Operating Temperature Range, case	T_C	-55	+125	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

INPUT

Parameter	Test Conditions	PA88			PA88A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial			0.5	2		0.25	0.5	mV
Offset Voltage vs. Temperature	Full temp range		10	30		5	10	µV/°C
Offset Voltage vs. Supply			1	5		*	*	µV/V
Offset Voltage vs. Time			75			*		µV/√kh
Bias Current, initial [1]			5	50		3	10	pA
Bias Current vs. Supply			0.01			*		pA/V
Offset Current, initial [1]			2.5	100		3	20	pA
Input Impedance, DC			10^{11}			*		Ω
Input Capacitance			4			*		pF
Common Mode Voltage Range[2]		$\pm V_S$–15			*			V
Common Mode Rejection, DC	V_{CM} = ±90V	90	110		*	*		dB
Noise	100 kHz BW, R_S=1 kΩ, C_C=15pf		2			*		µVrms

1. Doubles for every 10°C of temperature increase.
2. $+V_S$ and $–V_S$ denote the positive and negative power supply rail respectively.

GAIN

Parameter	Test Conditions	PA88			PA88A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop, @ 15 Hz	R_L= 2 kΩ, C_C= OPEN	96	111		*	*		dB
Gain Bandwidth Product @ 1 MHz	R_L = 2 kΩ, C_C = 15pf, R_C = 100 Ω		2.1			*		MHz
Power Bandwidth	R_L = 2 kΩ, C_C = 15pf, R_C = 100 Ω		6			*		kHz
Phase Margin	Full temp range		60			*		°

OUTPUT

Parameter	Test Conditions	PA88			PA88A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing [1]	Full temp range, I_O = ±75mA	$\pm V_S$–16	$\pm V_S$–14		*	*		V
Voltage Swing [1]	Full temp range, I_O = ±20mA	$\pm V_S$–10	$\pm V_S$–5.2		*	*		V
Current, continuous	T_C = 85°C	±100				*		mA
Slew Rate, A_V = 20	C_C = 15pf, R_C = 100 Ω		8			*		V/µs
Slew Rate, A_V = 100	C_C = OPEN		30			*		V/µs
Capacitive Load, A_V = +1	Full temp range	470			*			pF
Settling Time to 0.1%	C_C = 15pf, R_C = 100 Ω, 2V step		10			*		µs
Resistance, no load	R_{CL} = 0		100			*		Ω

1. $+V_S$ and $–V_S$ denote the positive and negative power supply rail respectively.

POWER SUPPLY

Parameter	Test Conditions	PA88			PA88A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage[1]		±15	±200	±225	*	*	*	V
Current, quiescent,			1.7	2		*	*	mA

1. Derate max supply rating 0.625 V/°C below 25°C case. No derating needed above 25°C case.

THERMAL

Parameter	Test Conditions	PA88			PA88A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case[1]	Full temp range, F > 60 Hz			5			*	°C/W
Resistance, DC, junction to case	Full temp range, F < 60 Hz			8.3			*	°C/W
Resistance, junction to air	Full temp range		30			*		°C/W
Temperature Range, case	Meets full range specifications	-25		+85	*		*	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

CAUTION The PA88 is constructed from MOSFET transistors. ESD handling procedures must be observed. The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

TYPICAL PERFORMANCE GRAPHS

Figure 3: Power Derating

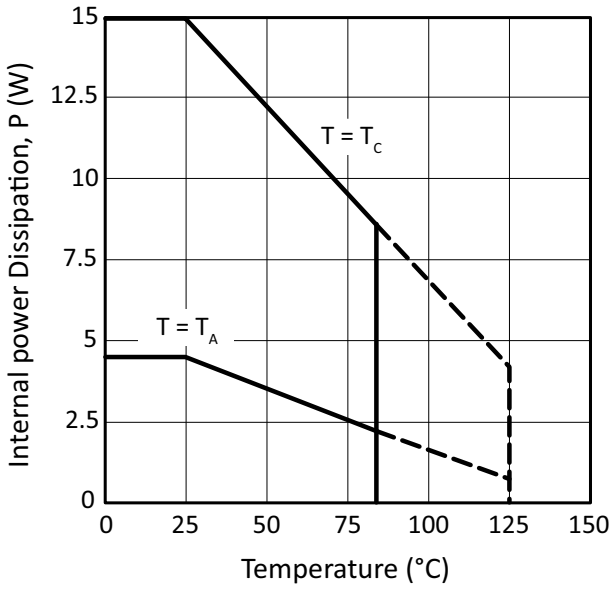


Figure 4: Quiescent Current

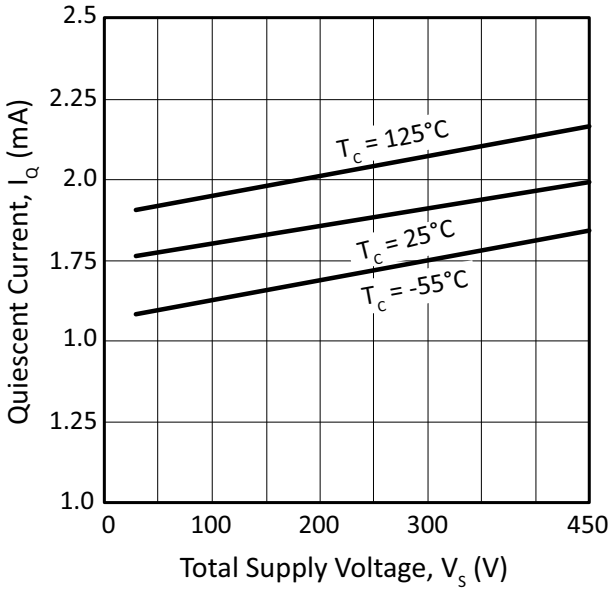


Figure 5: Small Signal Response

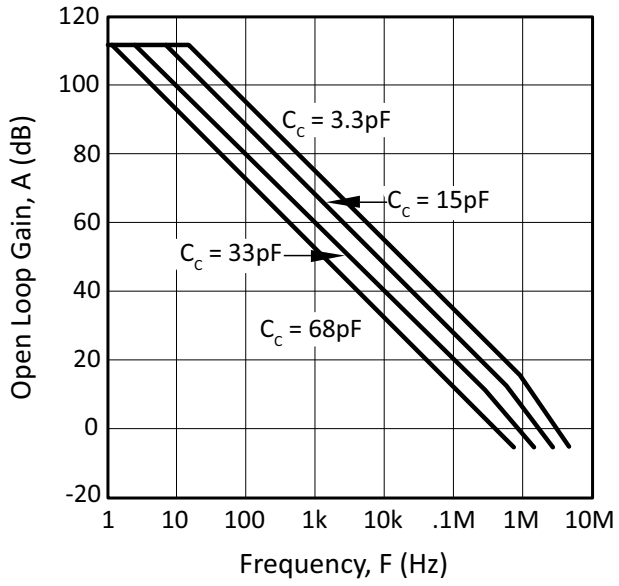


Figure 6: Phase Response

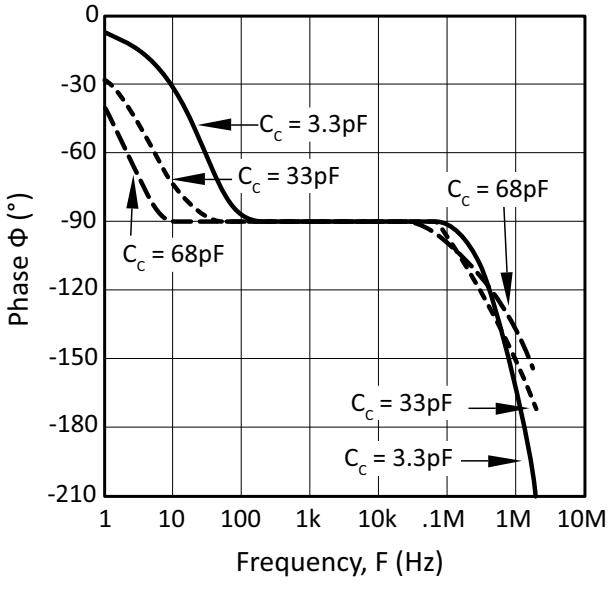


Figure 7: Output Voltage Swing

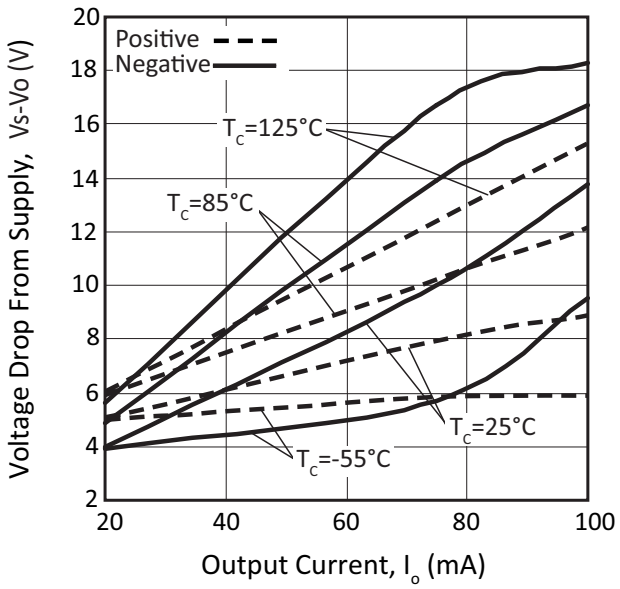


Figure 8: Power Response

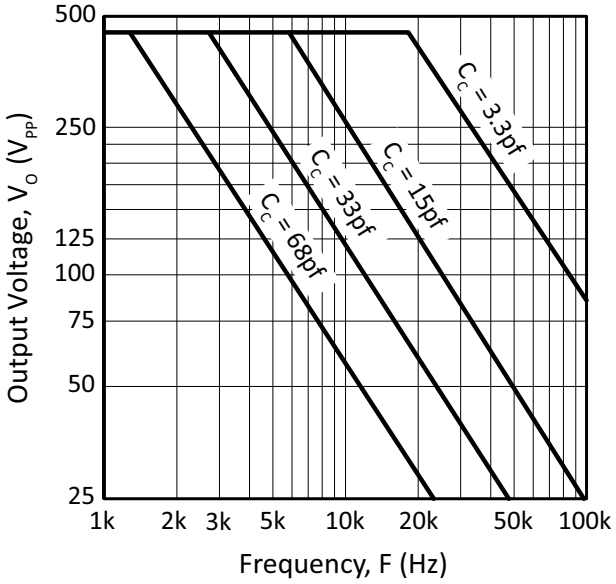


Figure 9: Slew Rate

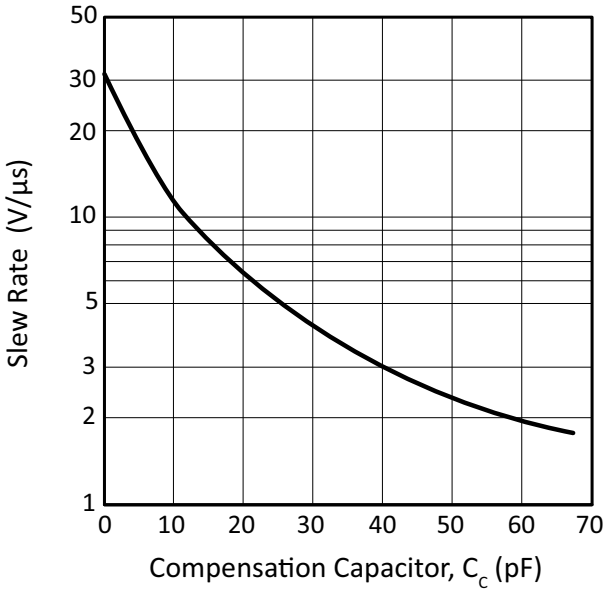


Figure 10: Harmonic Distortion

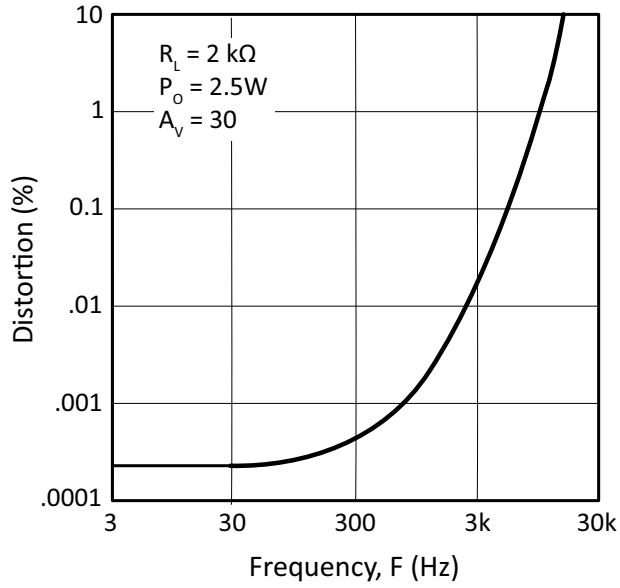


Figure 11: Input Noise

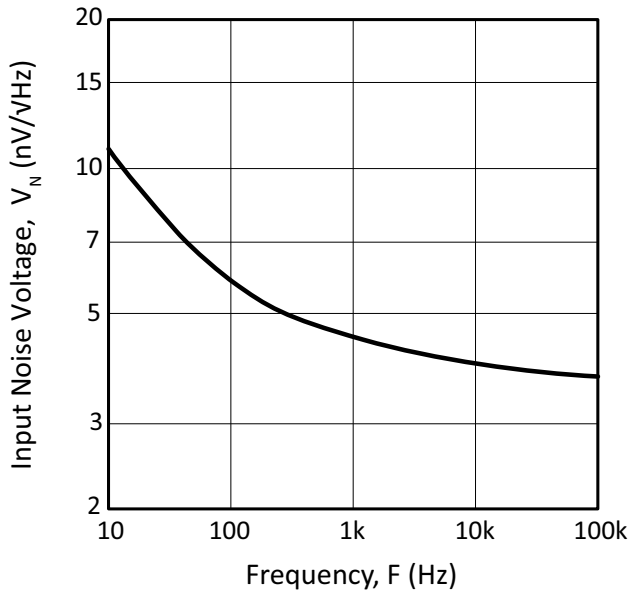


Figure 12: Common Mode Rejection

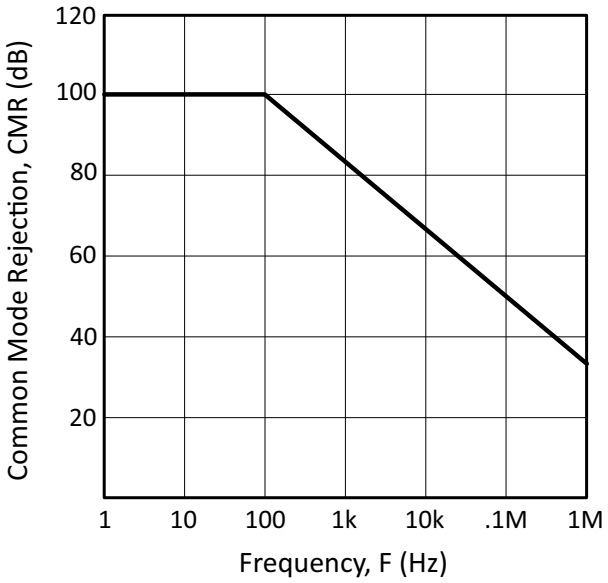


Figure 13: Power Supply Rejection

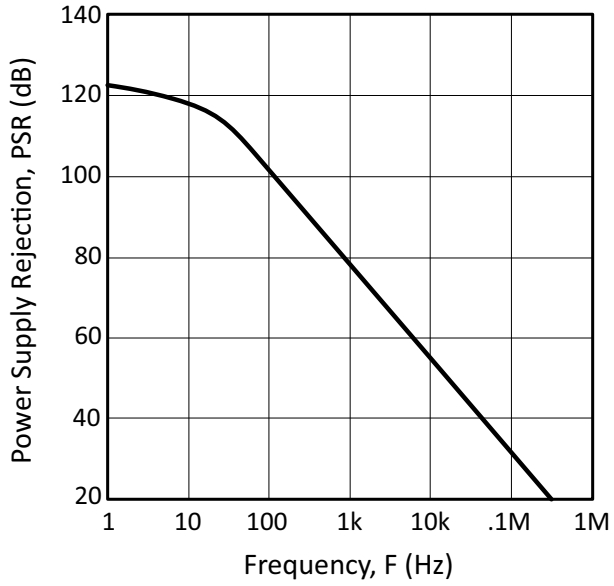
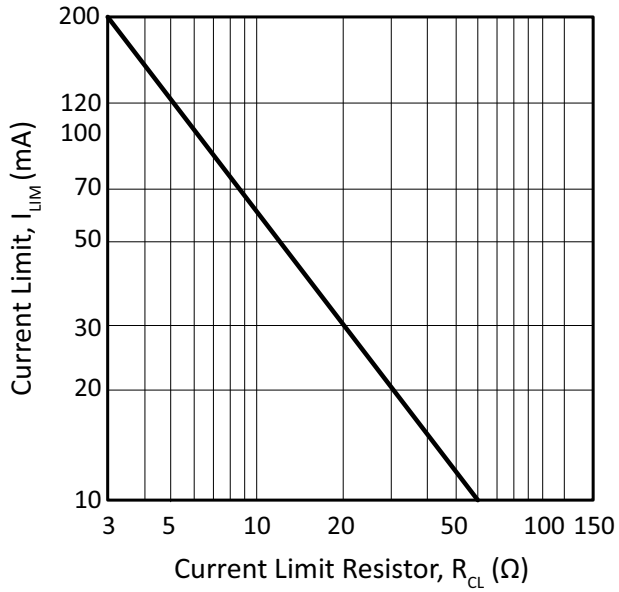


Figure 14: Current Limit



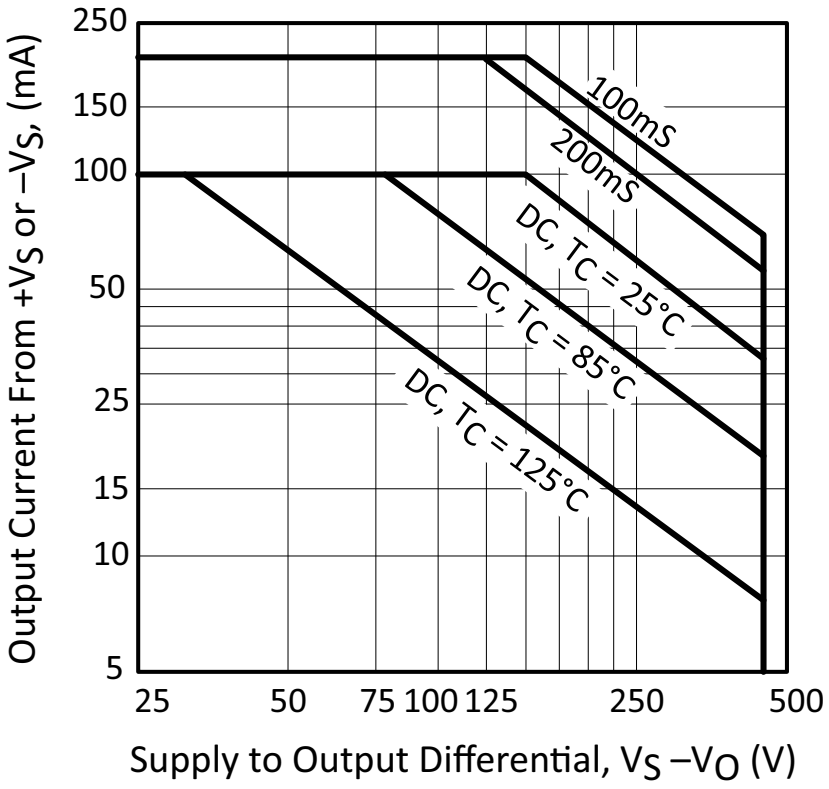
SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

Note: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

Figure 15: SOA



GENERAL

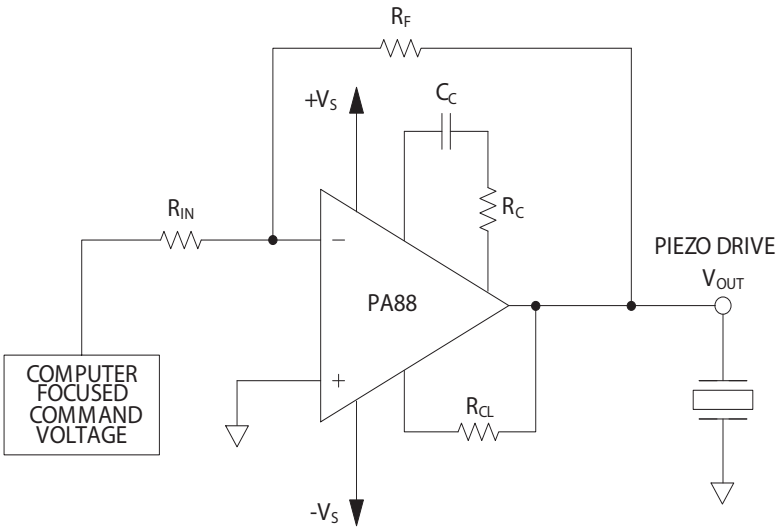
Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA88’s advantage of low quiescent power consumption reduces the costs of power supplies and cooling, while providing the interface between the computer and the high voltage drive to the piezo positioners.

Figure 16: Typical Application



PHASE COMPENSATION

Gain	C_C*	R_C
1	68pf	100Ω
10	33pf	100Ω
20	15pf	100Ω
100	15pf	---

*C_C Rate for full supply voltage

STABILITY

The PA88 has sufficient phase margin to be stable with most capacitive loads at a gain of 4 or more, using the recommended phase compensation.

The PA88 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 7 and 8 to avoid spurious oscillation.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the typical connection diagram. The minimum value is 3.5 Ω, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 150 Ω.

$$R_{CL}(\Omega) = \frac{0.7V}{I_{LIM}(A)}$$

INPUT PROTECTION

Although the PA88 can withstand differential input voltages up to ±25V, additional external protection is recommended, and required at total supply voltages above 300 volts. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1, D2 in Figure 17a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1, Q2 in Figure 17b). In either case the input differential voltage will be clamped to ± 0.7V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

Figure 17: Overvoltage Protection