# PA92

## *High Voltage Power Operational Amplifiers*

RoHS COMPLIANT

### FEATURES

- High Voltage — 400V (±200V)
- Low Quiescent Current — 10mA
- High Output Current — 4A
- Programmable Current Limit

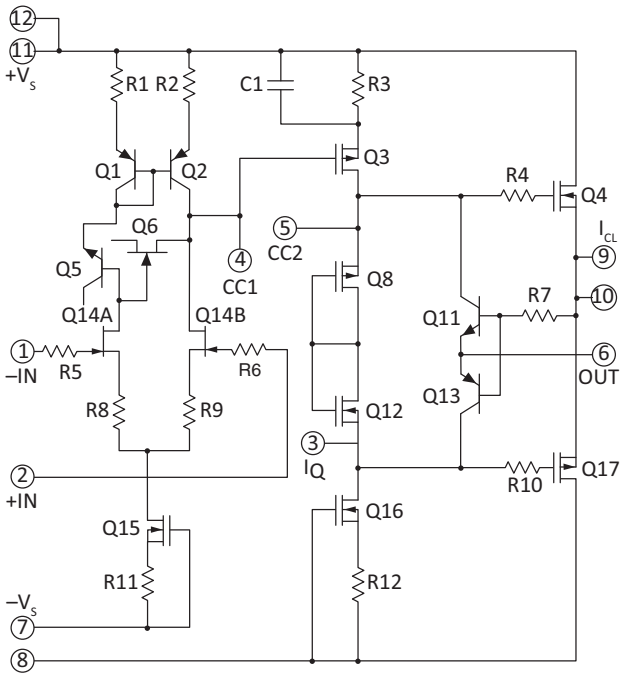

### APPLICATIONS

- Piezoelectric Positioning
- High Voltage Instrumentation
- Electrostatic Transducers
- Programmable Power Supplies up to 390V

### DESCRIPTION

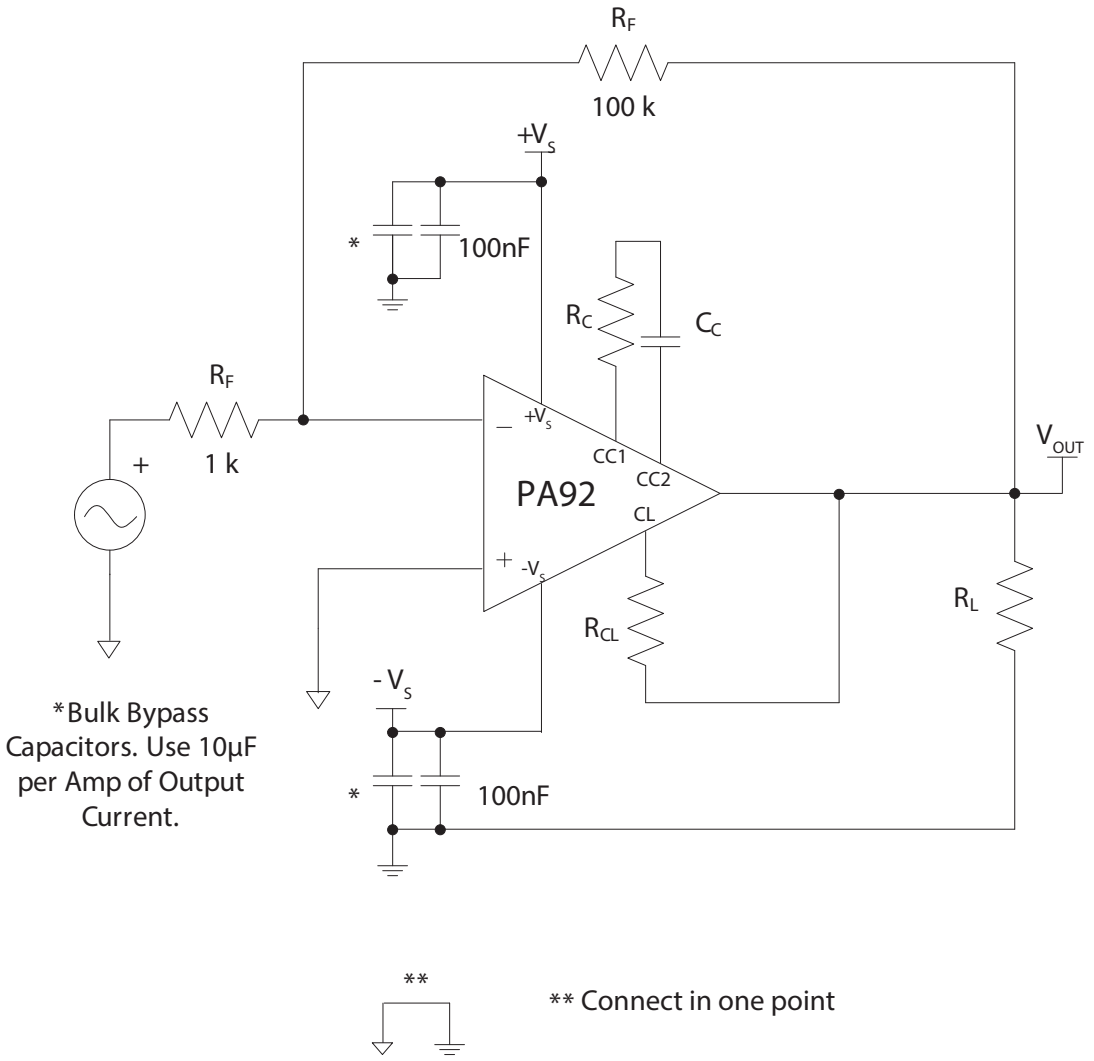
The PA92 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 4A and pulse currents up to 7A. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. Apex Microtechnology's Power SIP uses a minimum of board space allowing for high density circuit boards. The Power SIP is electrically isolated.

**Figure 1: Equivalent Schematic**



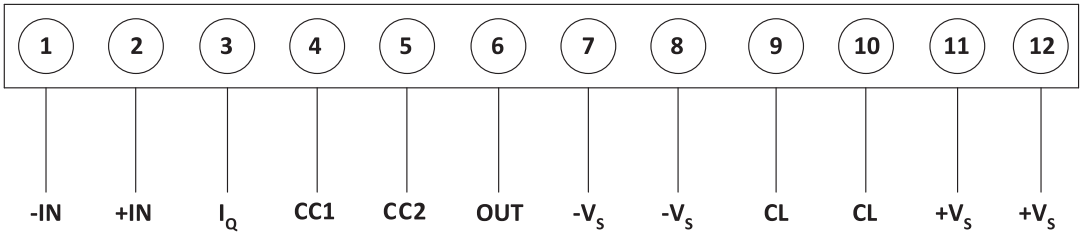
## TYPICAL CONNECTION

**Figure 2: Typical Connection**



## PINOUT AND DESCRIPTION TABLE

**Figure 3: External Connections**




| Pin Number | Name | Description |
|---|---|---|
| 1 | -IN | The inverting input. |
| 2 | +IN | The non-inverting input. |
| 3 | IQ | Quiescent current reduction pin. Connect to pin 5 to disable the AB bias. See applicable section. |
| 4 | CC1 | Compensation resistor connection. Select value based on Phase Compensation. See applicable section. |
| 5 | CC2 | Compensation capacitor connection. Select value based on Phase Compensation. See applicable section. |
| 6 | OUT | The output. Connect this pin to load and to the feedback resistors. |
| 7, 8 | $-V_S$ | The negative supply rail. Pins 7 and 8 are internally connected. |
| 9, 10 | CL | Connect to the current limit resistor. Output current flows into/out of these pins through $R_{CL}$. The output pin and the load are connected to the other side of $R_{CL}$. Pins 9 and 10 are internally connected. |
| 11, 12 | $+V_S$ | The positive supply rail. Pins 11 and 12 are internally connected. |

## SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and $T_C$ = 25°C.

### *ABSOLUTE MAXIMUM RATINGS*

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Supply Voltage, total | $+V_S$ to $-V_S$ | | 400 | V |
| Output Current, source, sink, peak, within SOA | $I_{OUT}$ | | 7 | A |
| Power Dissipation, continuous @ $T_c$ = 25°C | $P_D$ | | 80 | W |
| Input Voltage, differential | $V_{IN\ (Diff)}$ | -20 | 20 | V |
| Input Voltage, common mode | $V_{CM}$ | $-V_S$ | $+V_S$ | V |
| Temperature, pin solder, 10s max. | | | 260 | °C |
| Temperature, junction [1] | $T_J$ | | 150 | °C |
| Temperature Range, storage | | -55 | +125 | °C |
| Operating Temperature Range, case | $T_C$ | -40 | +85 | °C |

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.

**CAUTION** The PA92 is constructed from MOSFET transistors. ESD handling procedures must be observed. The substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

### *INPUT*

| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Offset Voltage, initial | | | 2 | 10 | mV |
| Offset Voltage vs. Temperature | Full temp range | | 15 | 50 | µV/°C |
| Offset Voltage vs. Supply | | | 10 | 25 | µV/V |
| Offset Voltage vs. Time | | | 75 | | µV/kh |
| Bias Current, initial | | | 200 | 2000 | pA |
| Bias Current vs. Supply | | | 4 | | pA/V |
| Offset Current, initial | | | 50 | 500 | pA |
| Input Impedance, DC | | | $10^{11}$ | | Ω |
| Input Capacitance | | | 4 | | pF |
| Common Mode Voltage Range [1] | | $\pm V_S \mp 15$ | | | V |
| Common Mode Rejection, DC | $V_{CM}$ = ±90V | 80 | 98 | | dB |
| Noise | 100 kHz BW, $R_S$ = 1 kΩ, $C_C$ = 10pF | | 1 | | µV RMS |

1. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.

### GAIN

| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Open Loop @ 15 Hz | $R_L$ = 2 kΩ, $C_C$ = 10pF | 94 | 111 | | dB |
| Gain Bandwidth Product @ 1 MHz | $R_L$ = 2 kΩ, $C_C$ = 10pF | | 18 | | MHz |
| Power Bandwidth | $R_L$ = 2 kΩ, $C_C$ = 10pF | | 30 | | kHz |
| Phase Margin | Full temp range | | 60 | | ° |

### OUTPUT

| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Voltage Swing [1] | $I_{OUT}$ = 4A | $\pm V_S \mp 12$ | $\pm V_S \mp 10$ | | V |
| Current, continuous | | 4 | | | A |
| Slew Rate, $A_V$ = 100 | $C_C$ = 10pF | | 50 | | V/µs |
| Capacitive Load, $A_V$ = +1 | Full temp range | 1 | | | nF |
| Settling Time to 0.1% | $C_C$ = 10pF, 2V step | | 1 | | µs |
| Resistance, no load | | | 10 | | Ω |

1. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.

### POWER SUPPLY

| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Voltage [1] | | ±50 | ±150 | ±200 | V |
| Current, quiescent | | | 10 | 14 | mA |

1. Derate max supply rating 0.625 V/°C below 25°C case. No derating needed above 25°C case.

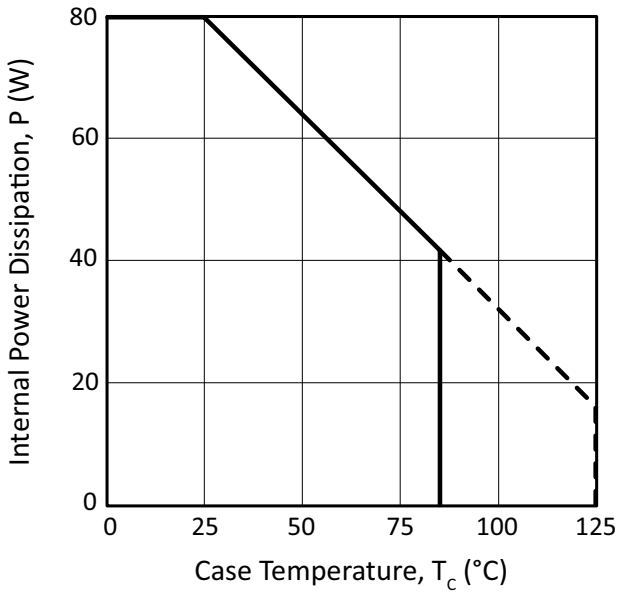
### THERMAL

| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Resistance, AC, junction to case [1] | Full temp range, F > 60 Hz | | | 1 | °C/W |
| Resistance, DC, junction to case | Full temp range, F < 60 Hz | | | 1.5 | °C/W |
| Resistance, junction to air | Full temp range | | 30 | | °C/W |
| temperature range, case | Meets full range specs | -25 | | +85 | °C |

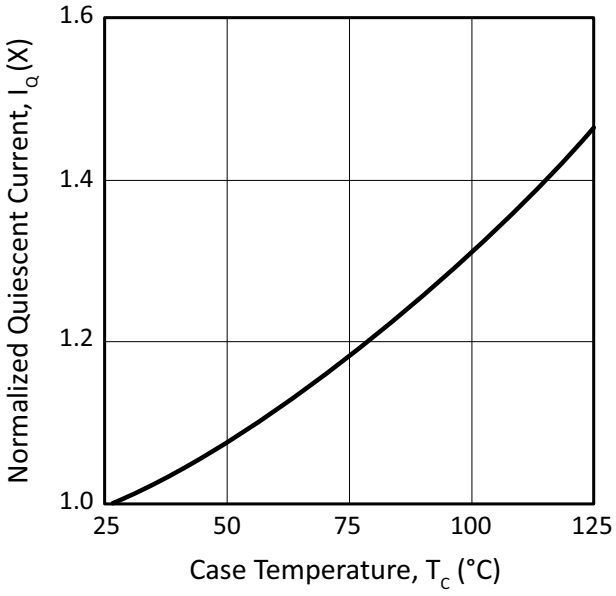
1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

## TYPICAL PERFORMANCE GRAPHS

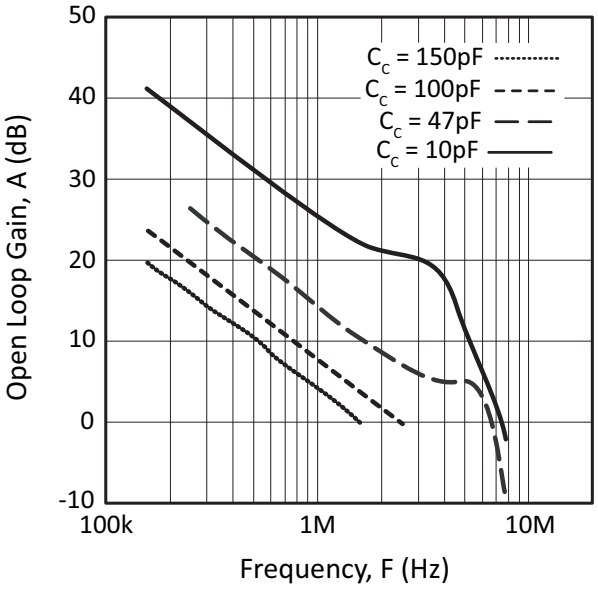
### Figure 4: Power Derating




### Figure 5: Normalized Quiescent Current




### Figure 6: Small Signal Response




### Figure 7: Phase Response

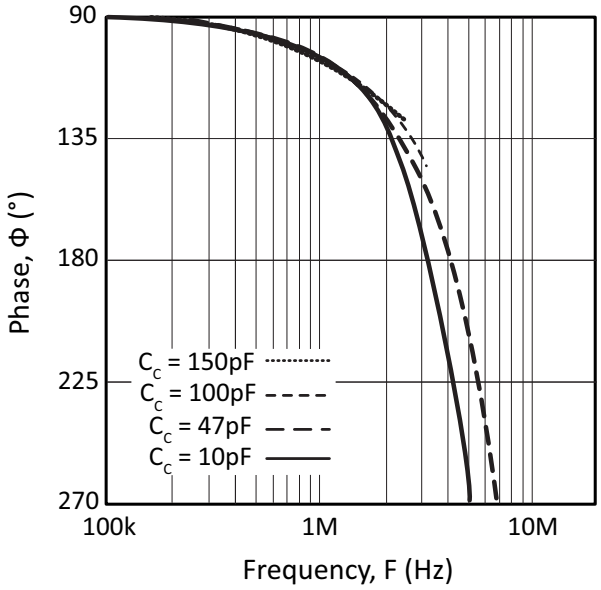


**Figure 8: Output Voltage Swing**

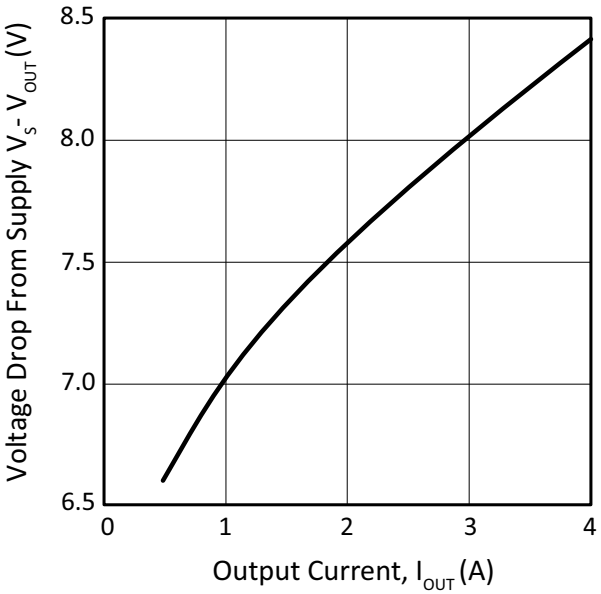



**Figure 9: Power Response**

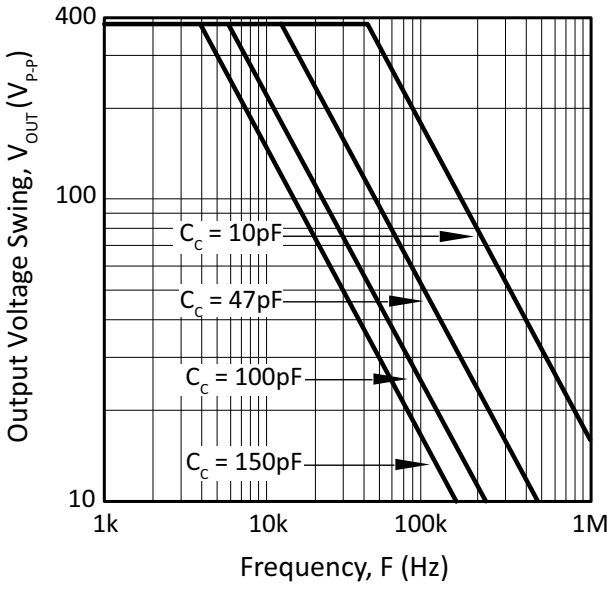



**Figure 10: Slew Rate**

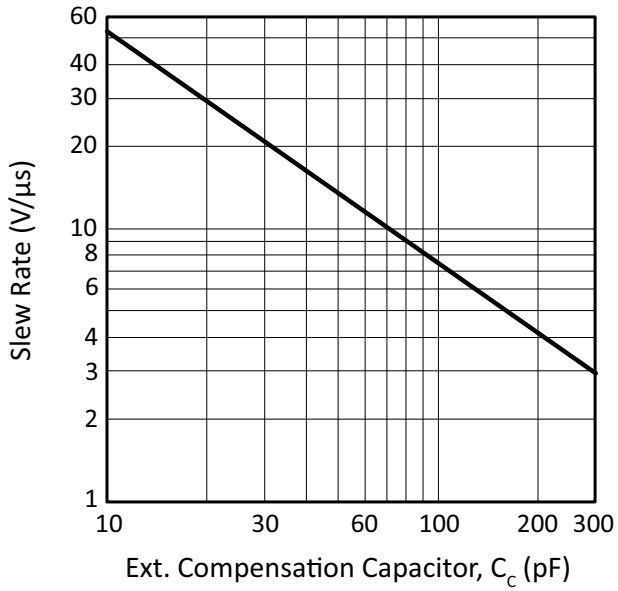



**Figure 11: Harmonic Distortion**

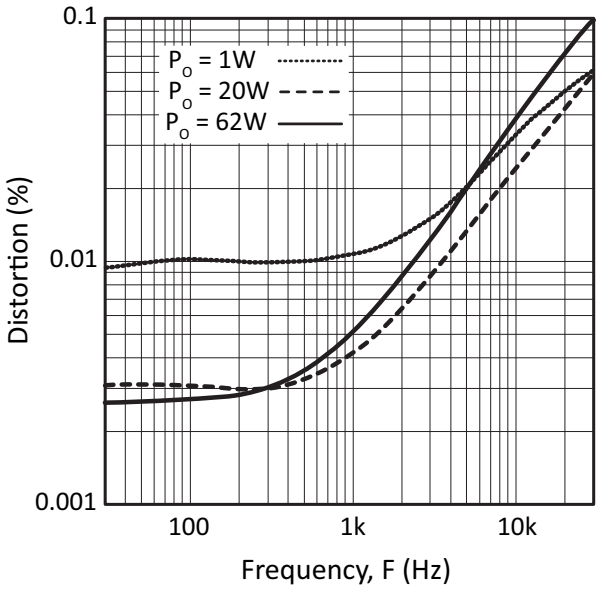


**Figure 12: Input Noise Voltage**

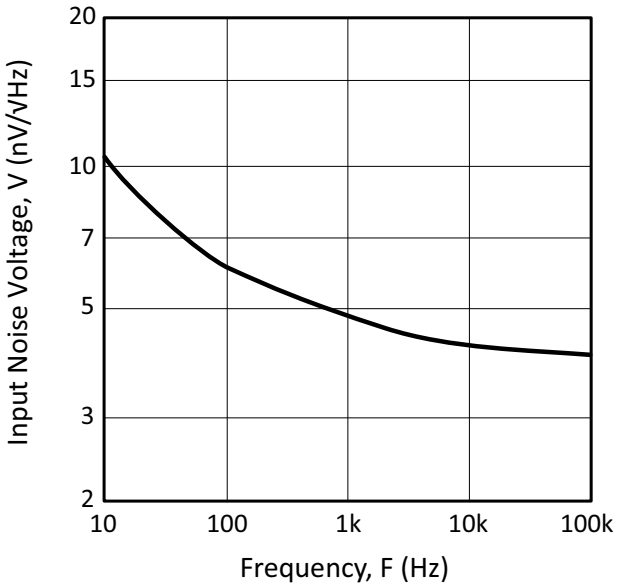
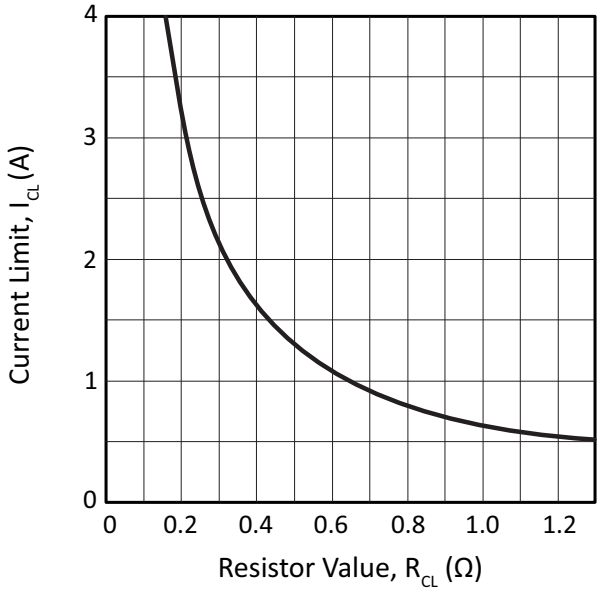



**Figure 13: Current Limit**



## SAFE OPERATING AREA (SOA)

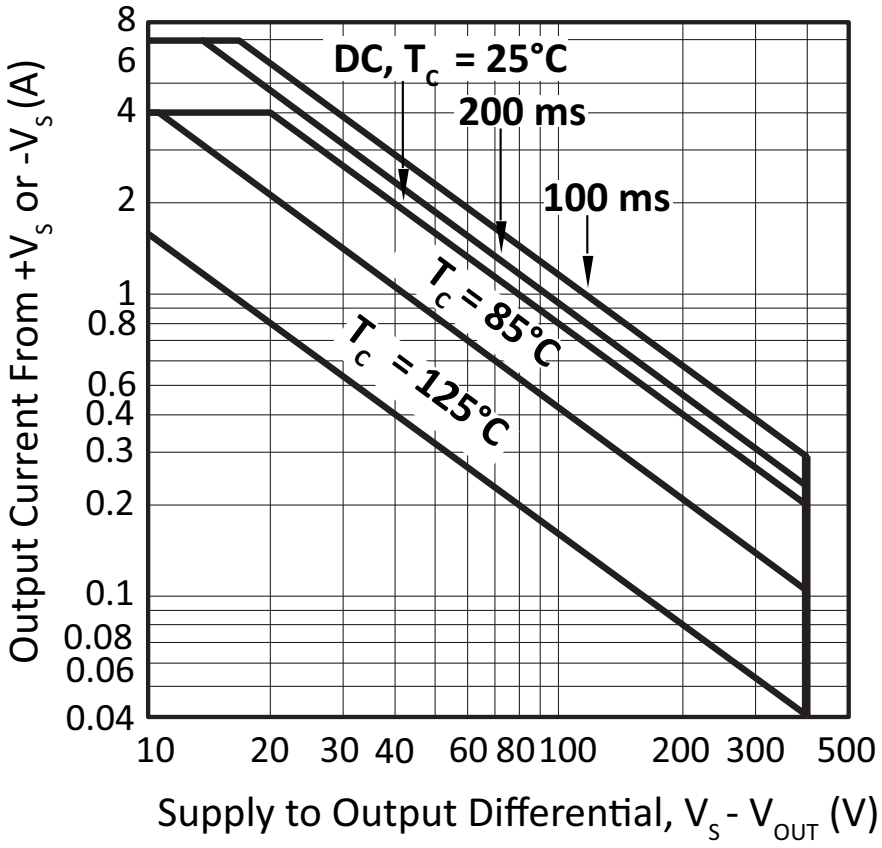
The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

**Note:** The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

**Figure 14: SOA**



## GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

## PHASE COMPENSATION

| Gain | $C_C$* | $R_C$ |
|---|---|---|
| ≥1 | 150pF | 100 Ω |
| ≥2 | 100pF | 100 Ω |
| ≥3 | 47pF | 0 Ω |
| ≥12 | 10pF | 0 Ω |

*$C_C$ Never to be <10pF. $C_C$ to be rated for the full supply voltage $+V_S$ to $-V_S$. Use ceramic NPO (COG) type.

## CURRENT LIMIT

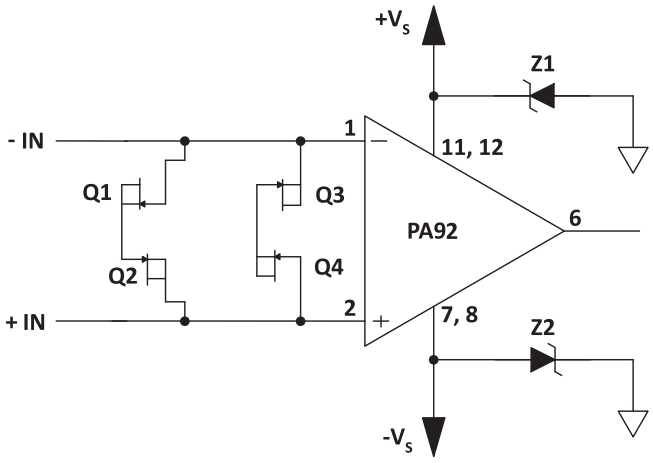
For proper operation, the current limit resistor ($R_{CL}$) must be connected as shown in the typical connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 16 Ω.

$$R_{CL}(\Omega) = \frac{0.65V}{I_{CL}(A)}$$

## INPUT PROTECTION

Although the PA92 can withstand differential voltages up to ±20V, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 15). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

**Figure 15: Overvoltage Protection**



## POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 315. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail are known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

## STABILITY

The PA92 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor $C_C$ must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network $C_CR_C$ must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

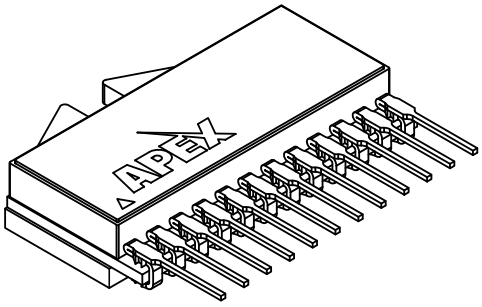
## QUIESCENT CURRENT REDUCTION

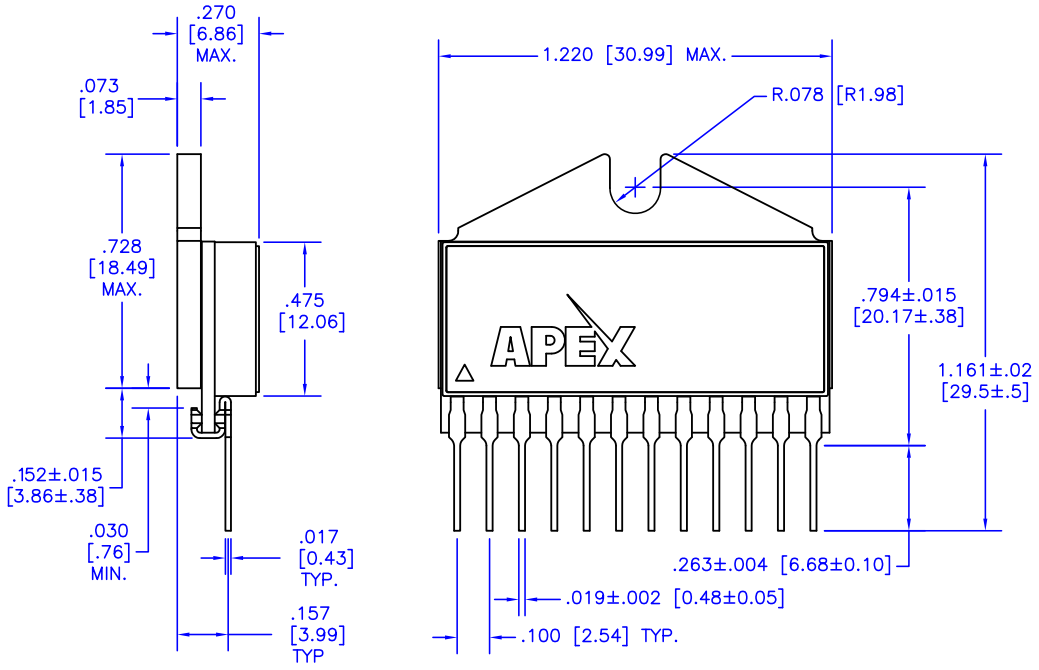
When pin 3 ($I_Q$) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This lowers quiescent power but also raises distortion since the output stage is then class C biased. The output stage bias current is nominally set at 1mA. Pin 3 may be left open if not used.

## PACKAGE DESIGN

| Part Number | Apex Package Style | Description |
|---|---|---|
| PA92 | DP | 12-Pin SIP |
| PA92EE | EE | 12-Pin SIP w/ formed leads |

***PACKAGE STYLE DP***






**NOTES:**

1. Dimensions are inches & [mm].
2. Triangle on lid denotes pin 1.
3. Pins: Alloy 510 phosphor bronze plated with matte tin (150 – 300µ") over nickel (50 µ" max.) underplate.
4. Package: Vectra liquid crystal polymer, black
5. Epoxy–sealed & ultrasonically welded non–hermetic package.
6. Package weight: .367 oz. [11.41 g]