PAC5232EVK1

Power Application Controllers

PAC5232EVK1 User's Guide

www.active-semi.com

Copyright © 2017 Active-Semi, Inc.

CONTENTS

OVERVIEW

Active-Semi's PAC5232EVK1 development platform is a complete hardware solution enabling users not only to evaluate the PAC5232 device, but also develop power applications revolving around this powerful and versatile Cortex M0 based microcontroller. The module contains a PAC5232 Power Application Controller (MCU) and all the necessary circuitry to properly energize the MCU and its internal peripherals once power is applied.

To aid in the application development the PAC5232EVK1 offers access to each and every one of the PAC5232 device's signals by means of a series of male header connectors.

The PAC5232EVK1 grants access to an external USB to UART module enabling users to connect the evaluation module to a PC computer through a conventional Virtual Comm Port which can then be used in the communication efforts by taking advantage of the PAC5232's UART interface. Graphical User Interface (GUI) software suites can be employed to externally control particular application's features.

Finally, the PAC5232EVK1 module gives access to the PAC5232's SWD port allowing users to both program their application to the device's FLASH memory, as well as debugging the application in real time. The 4 pin connector based SWD port is compatible with a fair number of debugger/programmer modules widely available.

Active-Semi's PAC5232EVK1 evaluation kit consists of the following:

- PAC5232EVK1 Body module
- PAC5232EVK1 User's Guide
- Schematics, BOM and Layout Drawings

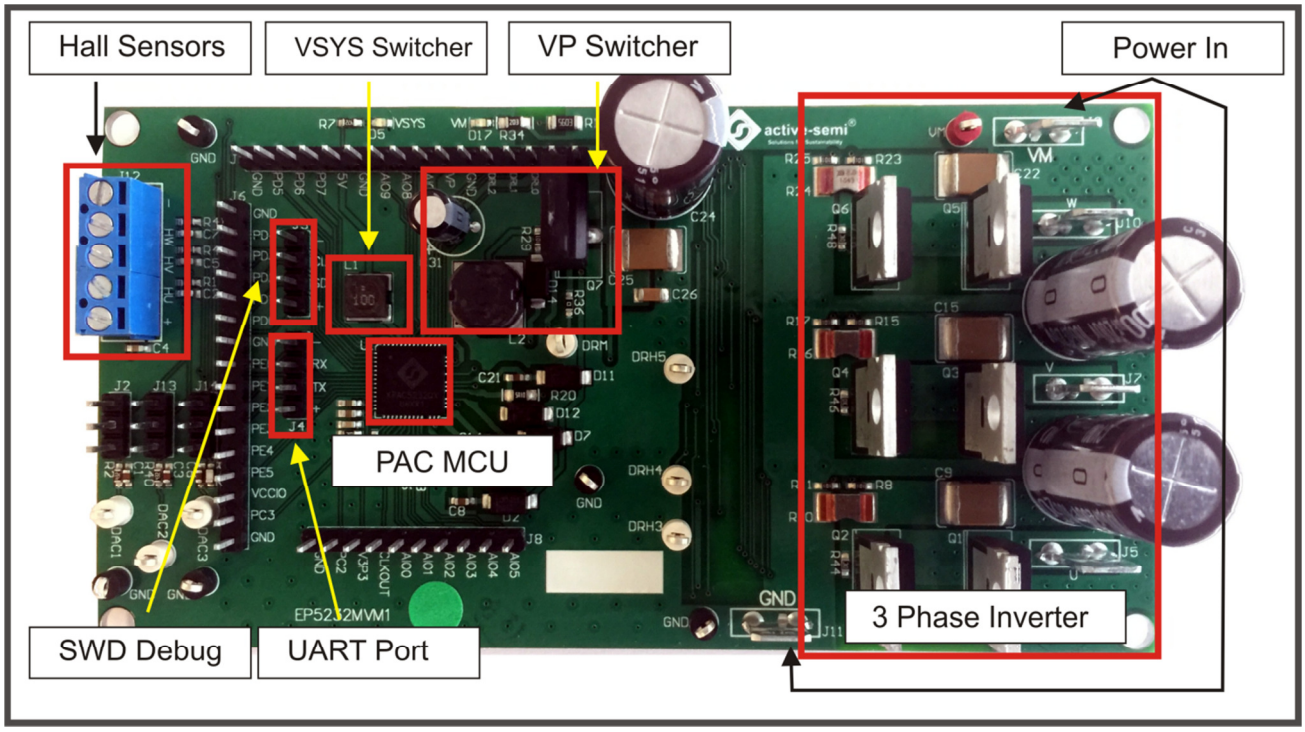


Figure 1: PAC5232EVK1 Block Diagram

Solution Benefits:

- Ideal for high voltage (up to 200V Abs Max) general purpose power applications and controllers
- Single-IC PAC5232 with 12 PWM outputs, 9 ADC inputs, I2C, UART, SPI and GPIO.
- Gate driving for up to three half H Bridge (tri phase) inverter.
- Schematics, BOM, Layout drawings available

The following sections provide information about the hardware features of Active-Semi's PAC5232EVK1 turnkey solution.

PAC5232EVK1 RESOURCES

Pinout and Signal Connectivity

The following diagram shows the male header pinout for the PAC5232EVK1 evaluation module, as seen from above:

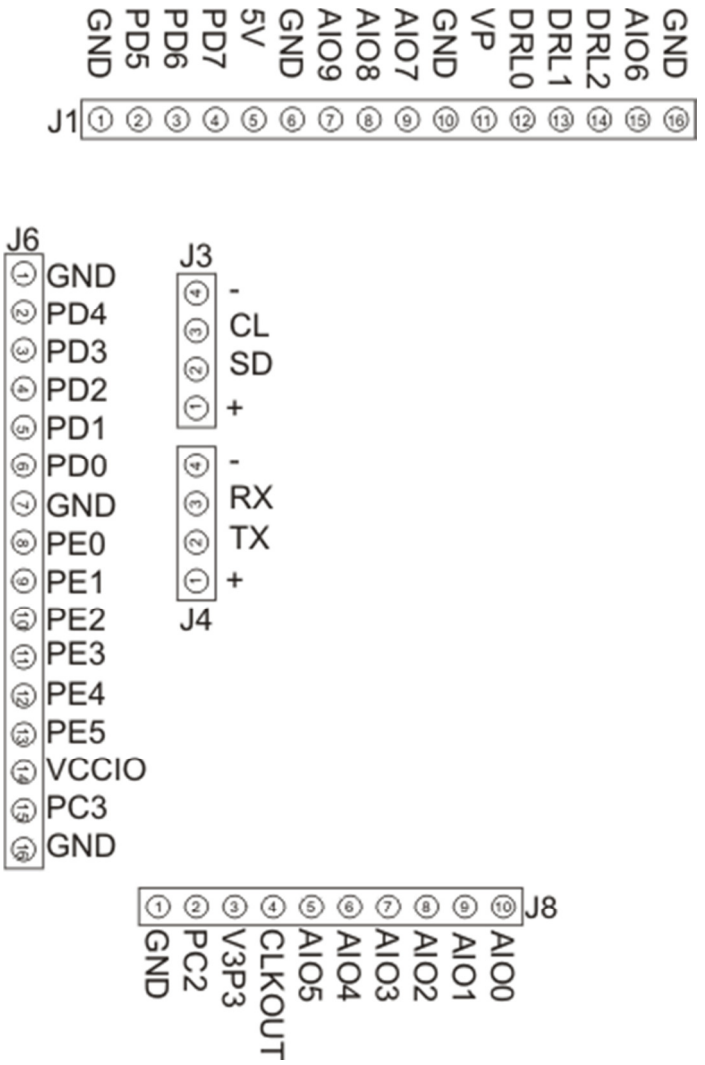


Figure 2 PAC5232EVK1 Headers and Test Stakes Pinout

Power Input

Power to the PAC5232EVK1 evaluation module can be applied to the J9 (VIN) and J11 (GND) spade connectors. Power to the PAC5232EVK1 evaluation module should not exceed 200V.

The PAC5232EVK1 is optimized to operate with voltages ranging from 25V to 80V. When the VIN input voltage goes above 25V, the system exits UVLO protection and all subsystems, including voltage regulators, analog front end and microcontroller, are enabled.

LED's

When an operational voltage is applied, LED D5 will light up. This is the LED which notifies VSYS (5V) rail is up and running. VP (12V gate drive), 3.3V (for analog circuitry) and 1.8V (for CPU core) regulators will also be operating at this point in time. Module is ready for use.

The following table shows the available LEDs and their associated diagnostic function.

LED	Description
D5	VSYS (5V). Lights up when the PAC5232 device is successfully powered up by VIN.
D17	VIN. Lights up as VIN voltage is applied.

SWD Debugging

Connector J3 offers access to the PAC5232 SWD port lines.

J3 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	SD	SWD Serial Data
3	CL	SWD Serial Clock
4	-	GND (System Ground)

Serial Communications

Connector J4 offers access to the PAC5232 UART port lines.

J4 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	TX	MCU Transmit Line
3	RX	MCU Receive Line
4	-	GND (System Ground)

Hall Sensor

Connector J2 offers access to the PAC5232 resources on PORTD utilized for hall sensor based commutation. These resources can be made available by selecting the Hall Sensor option within the J2/J13/J14 jumper selection.

J12 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	Hall Sensor U	PORTD2 (PWMB0 function)
3	Hall Sensor V	PORTD3 (PWMB1 function)
4	Hall Sensor W	PORTD7 (PWMD0 function)
5	GND	GND (System Ground)

Hall Sensor / DAC Selection Jumpers

Three pin jumpers J2/J13/J14 are used to select whether the PD3/PD3/PD7 resources are employed as Hall Sensor Inputs or PWM DAC outputs.

Jumper	Resource	Connected To
J2 1-2	PORTD2 (PWMB0 function)	Hall Sensor U
J2 2-3	PORTD2 (PWMB0 function)	PWM DAC 1 (TP6)
J13 1-2	PORTD3 (PWMB1 function)	Hall Sensor V
J13 2-3	PORTD3 (PWMB1 function)	PWM DAC 2 (TP8)
J14 1-2	PORTD7 (PWMD0 function)	Hall Sensor W
J14 2-3	PORTD7 (PWMD0 function)	PWM DAC 3 (TP9)

PAC5232EVK1 SETUP

The setup for the PAC5232EVK1 evaluation module requires up to four simple connections.

1. Connect the VIN power source via spade tab connectors J9 and J11. As VIN power is applied, the LED D17 will light up. If VIN voltage is larger than 25V, the PAC5232's Configurable Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D5 lighting up.
2. Connect the 3 Phase BLDC/PMSM motor via spade tab connectors J5 (PHASE U), J7 (PHASE V) and J10 (PHASE W).
3. If Serial Communications are desired, connect the USB to UART module 4 pin connection to J4.
4. For debugging/programming, connect a suitable USB SWD module to J3 by using a standard 4 wire cable.

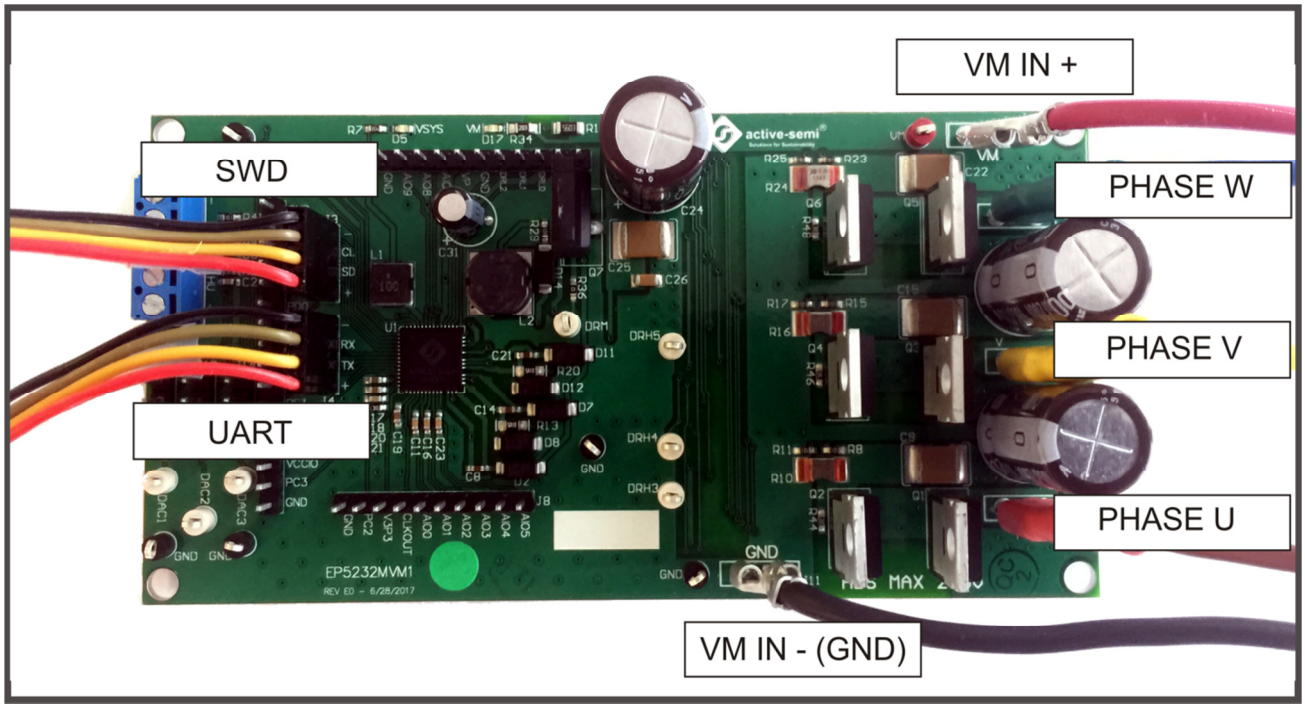


Figure 7: PAC5232EVK1 Evaluation Module Connections

POWER CONSIDERATIONS

Maximum Current and Voltage

The PAC5232EVK1 evaluation module was designed to operate with voltages in the 80V to 120V range. Transients can go to as high as 200V (Abs Max).

The recommended operating current is 10A RMS per phase. Higher currents could be achieved, albeit the user is responsible of applying different techniques to handle the increased thermal dissipation constraints. Please see the “Increasing Output Power” section for more information on how to achieve higher current loading.

SENSE Resistors

The SENSE resistors utilized to digitize motor winding current will determine how much current the three phase inverter will be able to handle. The PAC5232EVK1 module ships with 0.01 Ohm 3W SENSE resistors. For higher current handling, a smaller SENSE resistor could be employed.

The equation utilized to compute maximum tri phase inverter leg current is:

$$I_{MAX} = \sqrt{\frac{P_{TOTAL}}{R_{SENSE}}}$$

Users are encouraged to modify SENSE resistor value according to their application. The following table *showcases different resistance values, maximum currents and suggested part numbers.*

Resistance (Ω)	Rated Power (W)	Maximum RMS Current (A)	Part Number
0.01	3	17.3	CRA2512-FZ-R010ELF
0.002	5	50	CSS2H-2512K-2L00F

NOTE: For increased current handling, adding thermal heat sinking must be considered.

Power FETs

The PAC5232EVK1 ships with six IRFB4227PBF TO-220 Power FETs. These power switches are rated at 200V and 130A. RDSON is about 0.020 Ohms. In order to obtain the maximum performance out of these components, some form of heat sinking is required. The evaluation module ships without a heat radiation device. The appendix offers guidelines the measurements users can employ to fabricate their own version of a simple metal heat plate.

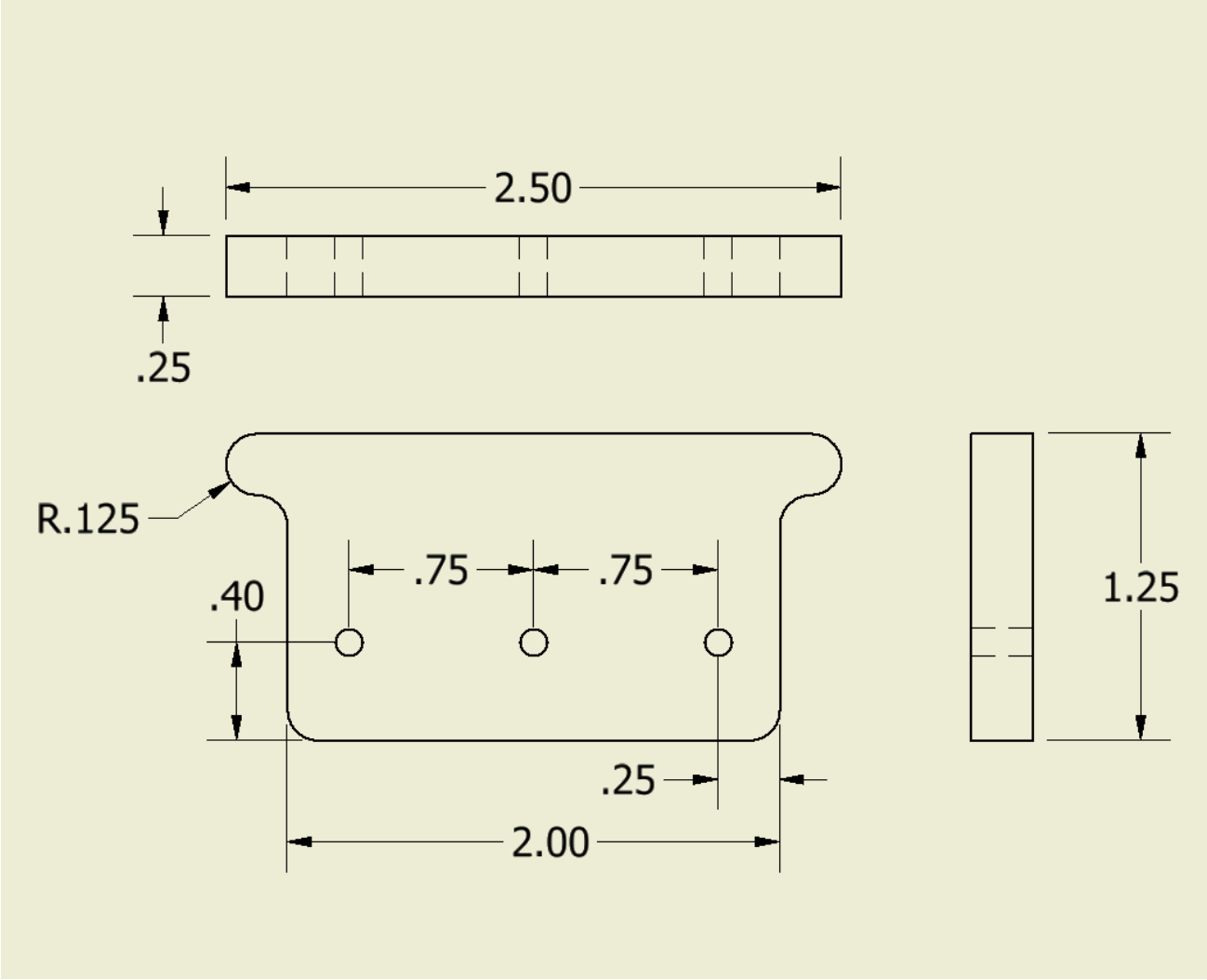
Users are also encouraged to modify the evaluation module by exchanging power switches with other components offering better thermal performance. Power FETs designed with a lower RDSON would tend to require less heat sinking. Traditionally, such FETs would have a lower maximum voltage, but for applications requiring smaller voltages, this may be an acceptable venue.

INCREASING OUTPUT POWER (APPENDIX)

In this section we provide different techniques which must be employed when wanting to drive higher then 10A per phase loads. As depicted in previous sections, the user will be responsible of selecting a proper SENSE resistor, suitable power FET, adding heat sinking and in some cases, some extra clamping.

Suggested Heat Sink Profile

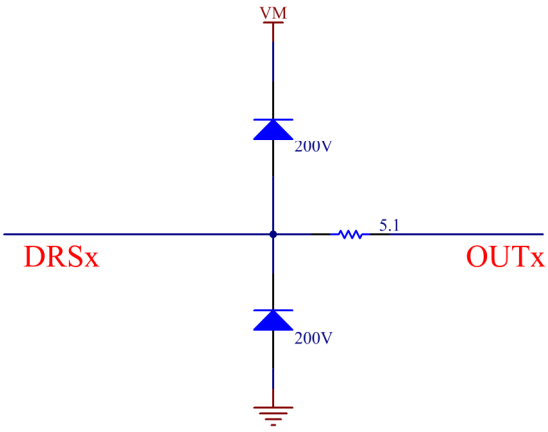
The following drawing offers guidelines in a shape which could be utilized to fabricate a heat radiator. This heat sinking metal plate is intended to be bolted into the power FETs through the usage of gap pads and insulating washers.



Clamping Mechanisms

When current load increases, destructive voltage transients can be observed. These transients are usually prevalent during dead time, when current must find an asynchronous path (e.g. FET body diodes) to continue its flow. Controlling these transients is of uttermost importance to protect both the power switches as well as the PAC5232 pre drive power stage block.

Adding DRS Clamps



The PAC5232EVK1 evaluation module already incorporates a series of clamps put in place to protect the DRSx terminal from negative transients at the phase outputs. However, under high current scenarios, it is plausible to see large positive transients. It is recommended to place a similar diode from DRS to VM in order to clamp the PHASE output to VM.