PAC5256EVK1

Power Application Controllers

PAC5256EVK1 User's Guide

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OVERVIEW

Active-Semi's PAC5256EVK1 development platform is a complete hardware solution enabling users not only to evaluate the PAC5256 device, but also develop power applications revolving around this powerful and versatile Cortex M0 based microcontroller. The module contains a PAC5256 Power Application Controller (MCU) and all the necessary circuitry to properly energize the MCU and its internal peripherals once power is applied.

To aid in the application development the PAC5256EVK1 offers access to each and every one of the PAC5256 device's signals by means of a series of female header connectors.

The PAC5256EVK1 also contains access to an external USB to UART module enabling users to connect the evaluation module to a PC computer through a conventional Virtual Comm Port which can then be used in the communication efforts by taking advantage of the PAC5256's UART interface. Graphical User Interface (GUI) software suites can be employed to externally control particular application's features.

Finally, the PAC5256EVK1 module gives access to the PAC5256's SWD port allowing users to both program their application into the device's FLASH memory, as well as debugging the application in real time. The 4 pin connector based SWD port is compatible with a fair number of debugger/programmer modules widely available.

Active-Semi's PAC5256EVK1 evaluation kit consists of the following:

- PAC5256EVK1 Evaluation module
- PAC5256EVK1 User's Guide
- Schematics, BOM and Layout Drawings

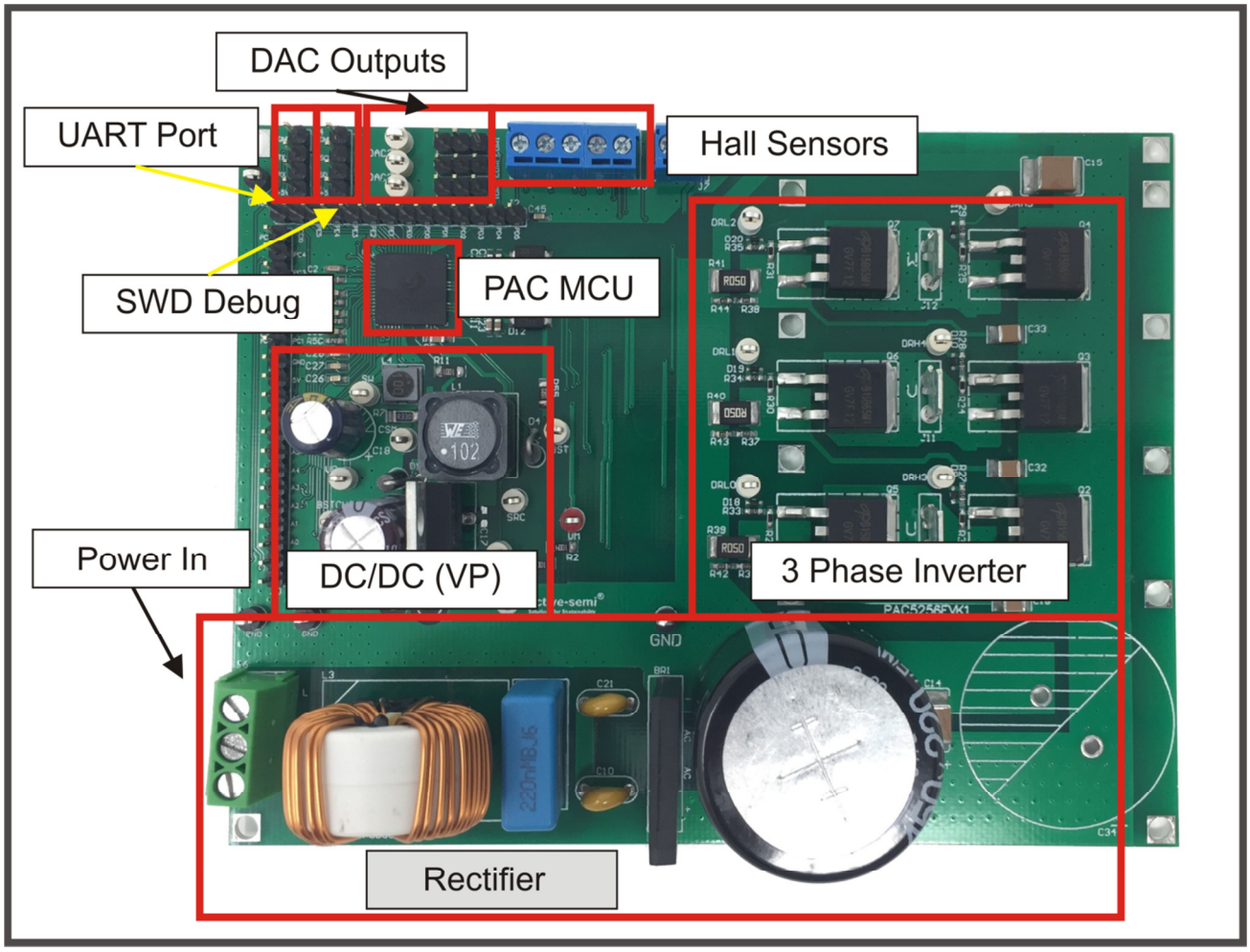

Figure 1: PAC5256EVK1 Block Diagram

Solution Benefits:

- Ideal for High Voltage (110/220 VAC nominal, up to 450VDC Abs Max) general purpose power applications and controllers
- Single-IC PAC5256 with 10 PWM outputs, 10 ADC inputs, I2C, UART, SPI and GPIO.
- Gate driving for up to three half H Bridge (tri phase) inverter.
- Three PWM DAC's for real time debugging.
- Hall Sensor Interface for sensored applications.
- Current and Voltage sensing for sensorless applications.
- Schematics, BOM, Layout drawings available

The following sections provide information about the hardware features of Active-Semi's PAC5256EVK1 turnkey solution.

PAC5256EVK1 RESOURCES

Pinout and Signal Connectivity

The following diagram shows the male header pinout for the PAC5256EVK1 evaluation module, as seen from above:

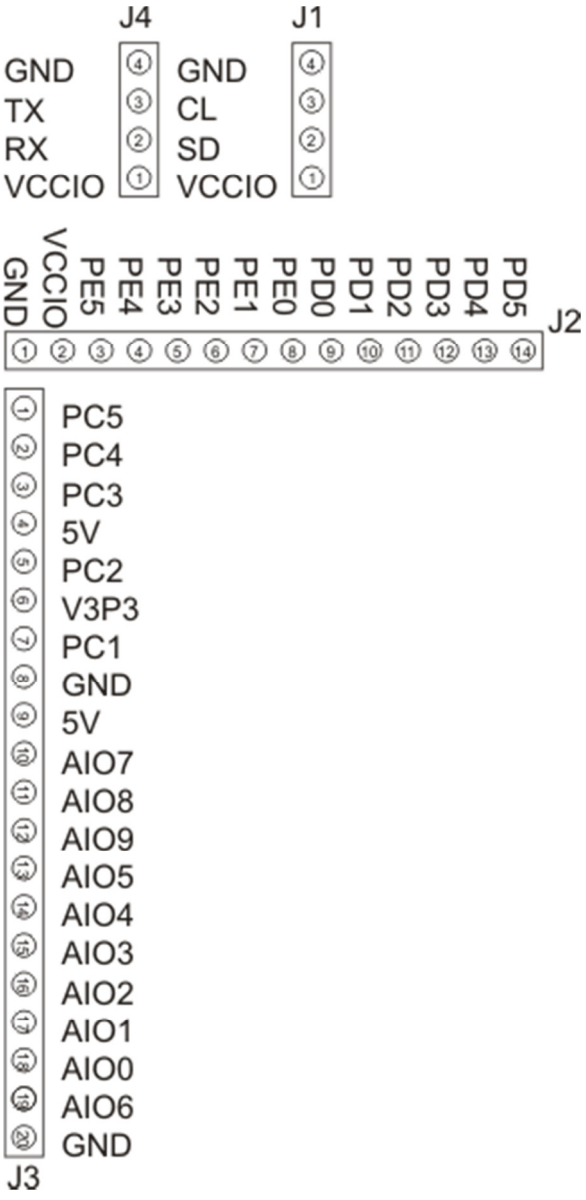

Figure 2 PAC5256EVK1 Headers and Test Stakes Pinout

Power Input

Power to the PAC5256EVK1 evaluation module can be applied to the J6 three position terminal block connector. Power to the PAC5256EVK1 evaluation module should not exceed 240 VAC (450 VDC Abs Max).

The PAC5256EVK1 is optimized to operate with voltages ranging from 110 VAC to 220 VAC Nominal. When the rectified input voltage (VM) goes above around 85 VDC, the system's High Voltage Buck Converter is powered up and the device exits UVLO protection. At this time all subsystems, including internal voltage regulators, analog front end and microcontroller, are enabled.

LED's

When an operational voltage is applied, LED D2 will light up. This is the LED which notifies VSYS (5V) rail is up and running. VP (12V gate drive), 3.3V (for analog circuitry) and 1.8V (for CPU core) regulators will also be operating at this point in time. Module is ready for use.

The following table shows the provided LED and its associated diagnostic function.

LED	Description
D2	VSYS (5V). Light up when the PAC5256 device is successfully powered up by VM.

SWD Debugging

Connector J1 offers access to the PAC5256 SWD port lines.

J1 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	SD	SWD Serial Data
3	CL	SWD Serial Clock
4	-	GND (System Ground)

Serial Communications

Connector J4 offers access to the PAC5256 UART port lines.

J4 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	TX	MCU Transmit Line
3	RX	MCU Receive Line
4	-	GND (System Ground)

Hall Sensor / DAC Interface

Terminal Block J15 offers access to the PAC5256 resources on PORTD utilized for hall sensor based commutation. These resources can be alternatively utilized as PWM DAC outputs for in real time debugging. Jumpers JMP1/2/3 are used to select the preferred function.

NOTE: 2 pin shunts must be placed on the JMP1/2/3 in order for the respective PORTD resources to be made available.

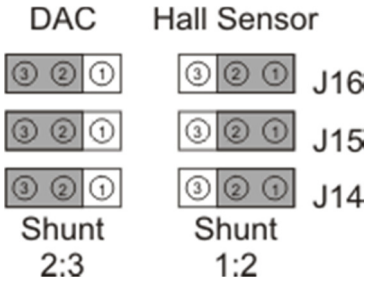

Figure 3 DAC / Hall Sensor Jumper Selection

Jumper JMP1/2/3	Description
1:2	Hall Sensor Functionality
2:3	DAC Functionality

NOTE: J15 functionality is only available when jumpers JMP1/2/3 have been shunted on the Hall Sensor respective position.

J15 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	Hall Sensor U	PORTD2
3	Hall Sensor V	PORTD3
4	Hall Sensor W	PORTD4
5	GND	GND (System Ground)

NOTE: Test stakes DAC1/2/3 are only available when jumpers JMP1/2/3 have been shunted on the DAC respective position

Test Stake	Description
DAC 1	PORTD2
DAC 2	PORTD3
DAC 3	PORTD4

PAC5256EVK1 SETUP

The setup for the PAC5256EVK1 evaluation module requires up to four simple connections.

1. Connect the 3 Phase BLDC/PMSM motor via space tab connectors PHASE U, PHASE V and PHASE W.
2. If Serial Communications are desired, connect the USB to UART module 4 pin connection to J4.
3. For debugging/programming, connect a suitable USB SWD module to J1 by using a standard 4 wire cable.
4. Connect the line voltage power source via three prong terminal block connector J6. For most systems, only connecting to the Live and Neutral terminals is sufficient.
5. **NOTE**: Due to the high voltage nature of this board, it is highly recommended for all connections to be made prior to applying power. Once rectified input voltage goes above 85VDC, the PAC5256's Multi Mode Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D2 lighting up.

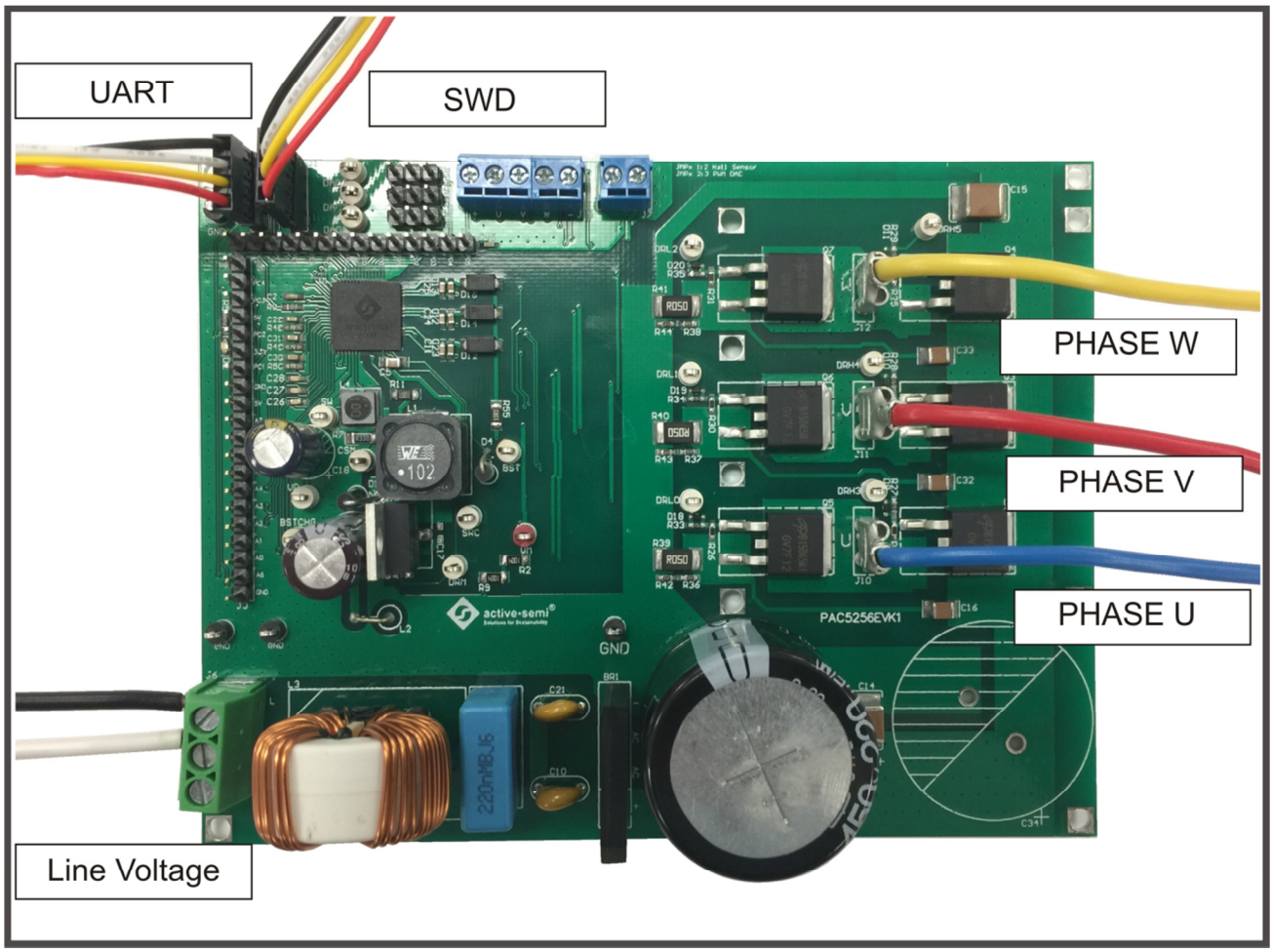

Figure 7: PAC5256EVK1 Evaluation Module Connections