PAC5532[A,B]
Data Sheet

Power Application Controller®

Multi-Mode Power Manager™

Configurable Analog Front End™

Application Specific Power Drivers™

Arm® Cortex®-M4F Controller Core

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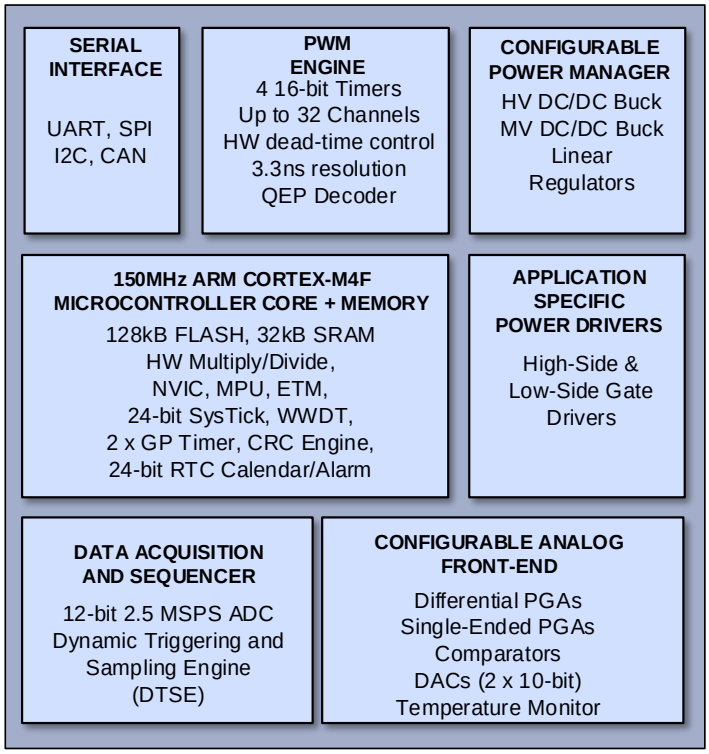
1 GENERAL DESCRIPTION

The PAC5532 is a Power Application Controller® (PAC) product that is optimized for high-speed BLDC motor control. The PAC5532 integrates a 150MHz Arm® Cortex®-M4F 32-bit microcontroller core with Active-Semi's proprietary highly configurable Power manager, Active-Semi's proprietary and patent-pending Configurable Analog Front-End™ and Application Specific Power Drivers™ to form the most compact microcontroller-based power and motor control solution available.

The PAC5532 features 128kB of embedded FLASH, 32kB of SRAM memory, a 2.5MSPS analog-to-digital converter (ADC) with programmable auto-sampling of up to 24 conversion sequences, 3.3V IO, flexible clock control system, PWM and general-purpose timers and several serial communications interfaces.

The Configurable Power Manager (CPM) provides "all-in-one" efficient power management solution for multiple types of power sources. It features a configurable high-voltage switching supply controller capable of operating a buck converter, a configurable medium-voltage switching regulator, and four linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are 180V power drivers designed for half bridge, H-bridge, 3-phase, and general-purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals.

Figure 1-1. PAC5532 Power Application Controller



The PAC5532 is available in a 51-pin, 8x8mm TQFN package.

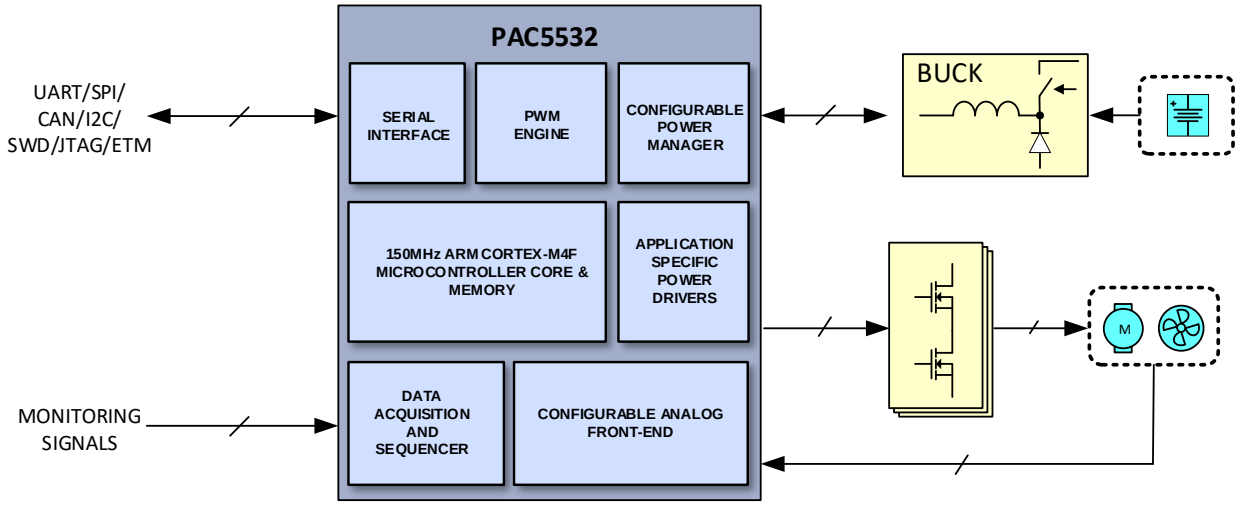
2 PAC FAMILY APPLICATIONS

The PAC5532 is ideal for battery powered applications between 48V and 120V.

Target applications for this device include:

- Power Tools
- Garden Tools
- Motor Controllers
- Drone/RC
- E-Bike
- E-Vehicle
- Ped-Electric Bikes
- Light HEV

Figure 2-1. Simplified Application Diagram



3 PRODUCT SELECTION SUMMARY

Table 3-1 Product Selection Summary

PART NUMBER	PIN PKG	POWER MANAGER		CONFIGURABLE ANALOG FRONT END					APPLICATION SPECIFIC POWER DRIVERS			MICROCONTROLLER					PRIMARY APPLICATION
		INPUT VOLTAGE	DC/DC	DIFF-PGA	PGA	COMPARATOR	DAC	ADC CHANNEL	VBST/VSRC	POWER DRIVER	PWM CHANNEL	SPEED (MHz)	FLASH (kB)	SRAM (kB)	GPIO	COMM	
PAC5532 PAC5532A PAC5532B	51L 8x8 QFN	25V-160V	Y	3	4	10	2	13	160V	3 LS (2A) 3 HS (2A)	6@VP 16@VCCIO	150	128	32	29	UART SPI I2C CAN SWD JTAG ETM	3 half-bridge 3 phase control BEMF Trapezoidal or FOC

Notes: DIFF-PGA = differential programmable gain amplifier; HS = high-side, LS = low-side, PGA = programmable gain amplifier, VSRC = Bootstrap Voltage Source

4 ORDERING INFORMATION

Table 4-1 Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
PAC5532QX	-40°C to 125°C	51L 8x8 QFN	51 + Exposed Pad	Tray (4900 piece)
PAC5532AQX				Tray (4900 piece)
PAC5532AQX-T				Tape and Reel (3000 piece)
PAC5532BQX-T				Tape and Reel (3000 piece)

5 FEATURES

5.1 Feature Overview

- **Configurable Power Manager**
  - High-voltage buck switching supply controller
    - Input Voltage: 25V – 160V
    - Configurable Output Voltage: 12V or 15V
  - 5V medium-voltage switching supply regulator
  - 4 Linear regulators with power and hibernate management
  - Power and temperature monitor, warning, fault detection
- **Proprietary Configurable Analog Front-End**
  - 10 Analog Front-End IO pins
  - 3 Differential Programmable Gain Amplifiers
  - 4 Single-ended Programmable Gain Amplifiers
  - Programmable Over-Current Protection
  - 10 Comparators
  - 2 10-bit DACs
- **Proprietary Application Specific Power Drivers**
  - 3 180V high-side gate drivers with 2A gate driving capability
  - 3 low-side gate drivers with 2A gate driving capability
  - Configurable propagation delay and fault protection
- **3.3V I/Os**
- **150MHz Arm® Cortex®-M4F 32-bit Microcontroller Core**
  - Single-cycle 32-bit x 32-bit hardware multiplier
  - 32-bit hardware divider
  - DSP Instructions and Saturation Arithmetic Support
  - Integrated sleep and deep sleep modes
  - Single-precision Floating Point Unit (FPU)
  - 8-region Memory Protection Unit (MPU)
  - Nested Vectored Interrupt Controller (NVIC) with 32 Interrupts with 8 levels of priority
  - 24-Bit SysTick Timer
  - Wake-up Interrupt Controller (WIC) allowing power-saving sleep modes
  - Clock-gating allowing low-power operation
  - Embedded Trace Macrocell (ETM) for in-system debugging at real-time without breakpoints
- **Memory**
  - 128kB FLASH
  - 32kB SRAM with ECC
  - 2 x 1kB INFO FLASH area for manufacturing information
  - 1 x 1kB INFO FLASH area for user parameter storage and application configuration or code
  - Code Protection
- **Analog to Digital Converter (ADC)**
  - 12-bit resolution
  - 2.5MSPS
  - Programmable Dynamic Triggering and Sampling Engine (DTSE)

- **I/O**
  - 16 general-purpose I/Os with tri-state, pull-up, pull-down and dedicated I/O supply
  - 7 I/Os can be configured as ADC input or digital I/O
    Configurable weak pull-up and pull-down
  - Configurable drive strength (6mA to 25mA minimum)
  - Dedicated Integrated IO power supply (3.3V)
  - Flexible peripheral MUX allowing each IO pin to be configured with one of up to 8 peripheral functions
  - Flexible Interrupt Controller
- **Flexible Clock Control System (CCS)**
  - 300MHz PLL from internal 1.25% oscillator
  - 20MHz Ring Oscillator
  - 20MHz External Clock Input
- **Timing Generators**
  - Four 16-bit timers with up to 32 PWM/CC blocks
    - 16 Programmable Hardware Dead-time generators
    - Up to 300MHz input clock for high-resolution PWM
  - 16-bit Windowed Watchdog Timer (WWDT)
  - 24-bit Real-time Clock (RTC) with Calendar and Alarm Functions
  - 24-bit SysTick Timer
  - 2 x 24-bit General-purpose count-down timers with interrupt
  - Wake-up timer for sleep modes from 0.125s to 8s
- **Communication Peripherals**
  - 2 x USART
    - SPI or UART modes
    - SPI Master/Slave, up to 25MHz
    - UART, up to 1Mbps
  - I2C Master/Slave
  - CAN 2.0A/B Controller
  - Single Wire Debugger (SWD)
  - JTAG
  - Embedded Trace Macrocell (ETM)
- **4-Level User-Configurable Code Protection**
- **96-bit Unique ID**
- **CRC Engine**
  - Offloads software for communications and safety protocol through hardware acceleration
  - Configurable Polynomial (CRC-16 or CRC-8)
  - Configurable Input Data Width, Input and Output Reflection
  - Programmable Seed Value

6 ABSOLUTE MAXIMUM RATINGS

The table below shows the absolute maximum ratings for this device.

To prevent damage to the device, do not exceed these limits. Exposure to the absolute maximum rating conditions for long periods of time may affect device reliability.

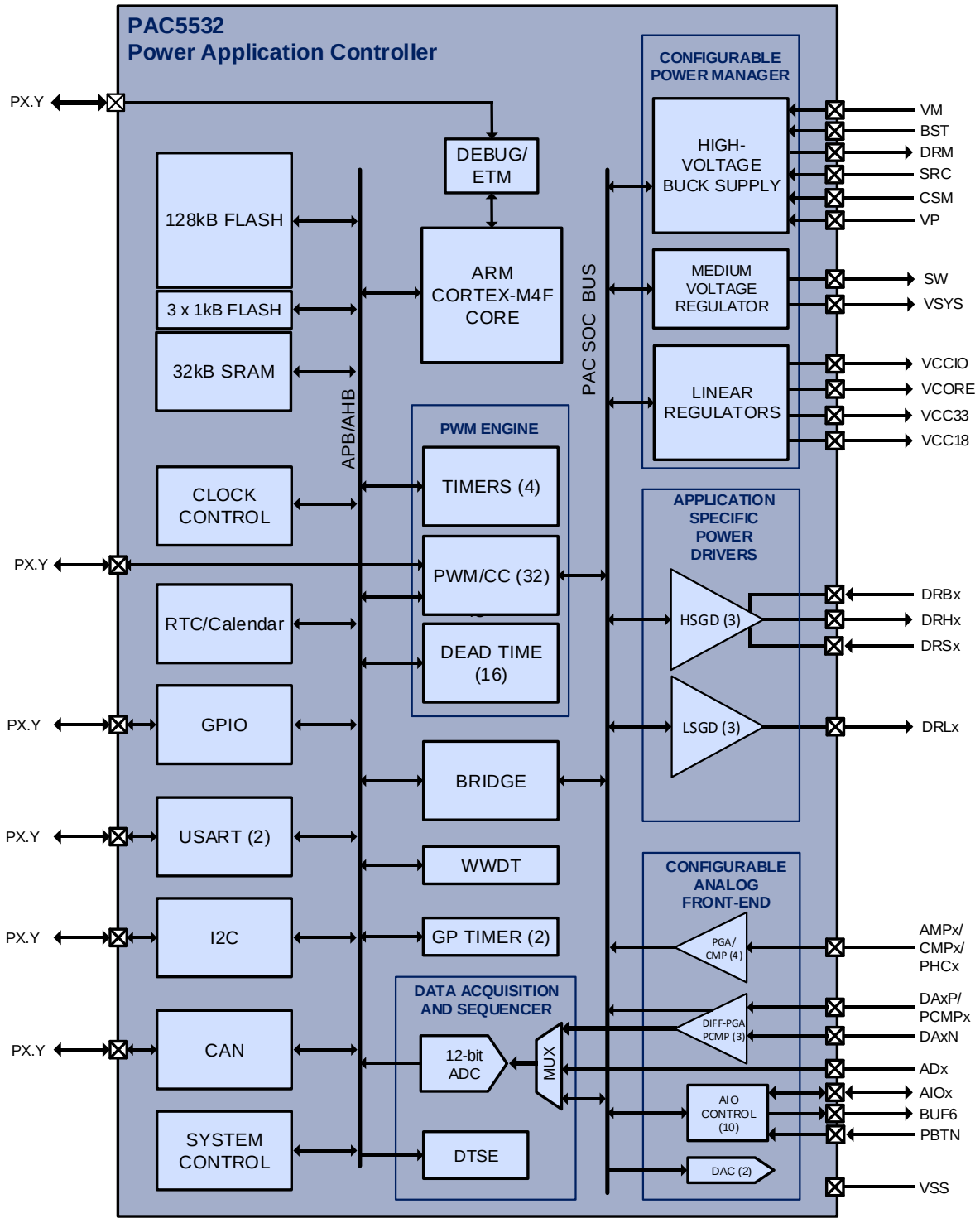
The device is not guaranteed to function properly outside of the operating conditions.

Table 6-1 Absolute Maximum Ratings

PARAMETER		VALUE	UNIT
VM to VSS		-0.3 to 160	V
BST to VSS		-0.3 to 180	V
BST to SRC		-0.3 to 20	V
SRC to VSS		-10 to VM + 15	V
DRM to SRC		-0.3 to 20	V
VP to VSS		-0.3 to 20	V
SW to VSS		-0.3 to V_P + 0.3	V
CSM to VP		-0.3 to 0.3	V
VSYS, AIO6 to VSS		-0.3 to 6	V
AIO<9:7>, AIO<5:0> to VSS		-0.3 to V_{SYS} + 0.3	V
PC<x>, PE<x>, PF<x> to VSS		-0.3 to V_{CCIO} + 0.3	V
PC<x>, PE<x>, PF<x> pin injection current		25	mA
PC<x>, PE<x>, PF<x> sum of all pin injection current		50	mA
VCC33, VCCIO to VSS		-0.1 to 4.1	V
VCORE to VSS		-0.1 to 1.44	V
VCC18 to VSS		-0.1 to 2.5	V
DRL0, DRL1, DRL2 to VSS		-0.3 to V_P + 0.3	V
DRB3, DRB4, DRB5 to VSS		-0.3 to 180	V
DRS3, DRS4, DRS5 to VSS		-10 to VM + 15	V
DRB3 to DRS3, DRB4 to DRS4, DRB5 to DRS5		-0.3 to 20	V
DRH3 to DRS3, DRH4 to DRS4, DRH5 to DRS5		-0.3 to V_{DRBx} + 0.3	V
VSS RMS Current		0.2	A_{RMS}
Operating ambient temperature range (T_A)		-40 to 125	°C
Electrostatic Discharge (ESD)	Human body model (JEDEC)	2	kV
	Charge device model (JEDEC)	1	kV

7 ARCHITECTURAL BLOCK DIAGRAM

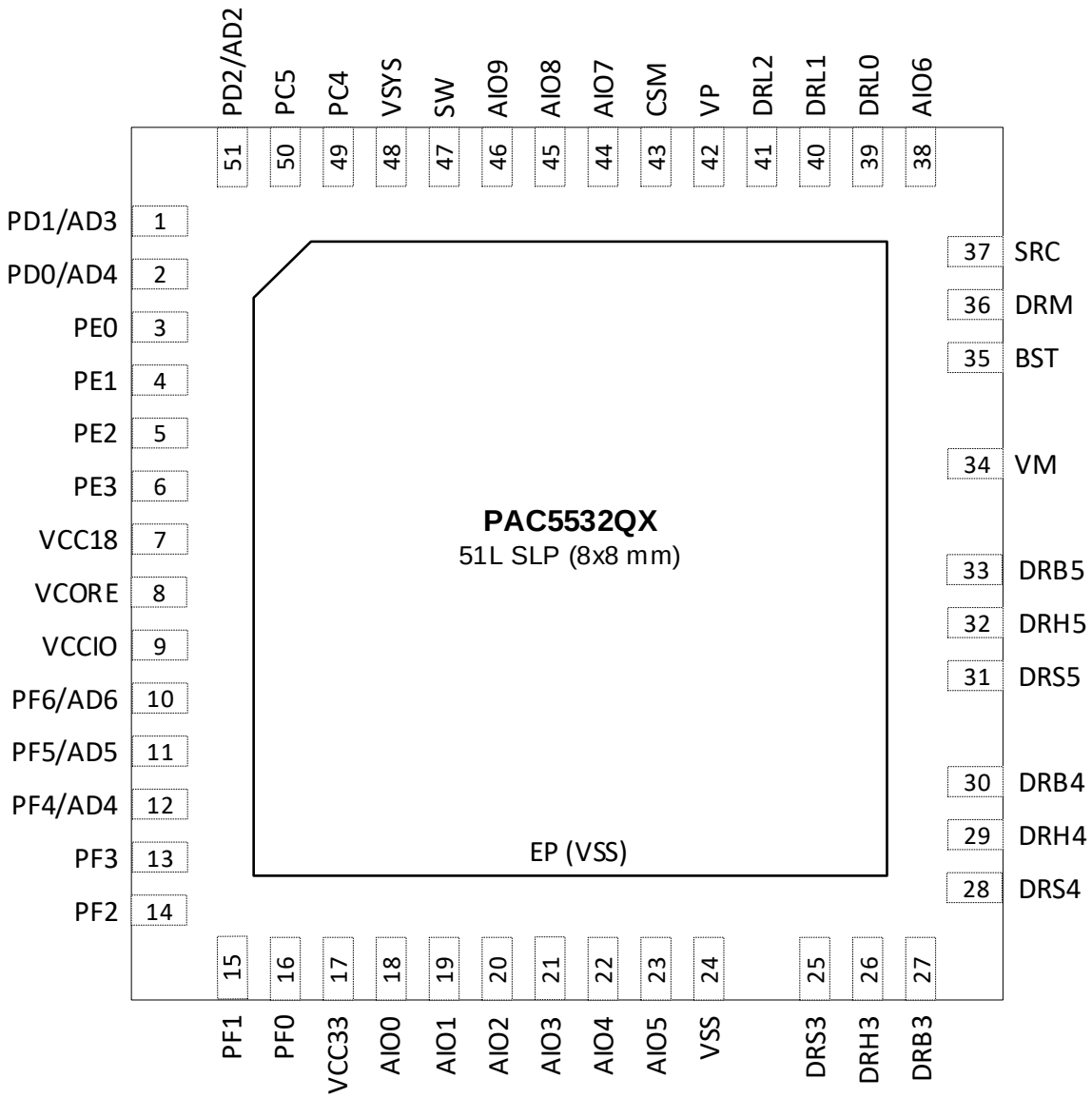
Figure 7-1 Architectural Block Diagram



9 PIN CONFIGURATION

9.1 PAC5532QX

Figure 9-1 PAC5532QX Pin Diagram



10 PIN DESCRIPTION

10.1 Power and Ground Pin Description

Table 10-1 Power and Ground Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VCC18	7	Power	Internally generated digital I/O 1.8V power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CC18} to V_{SSA}.
VCORE	8	Power	Internally generated 1.2V core power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CORE} to V_{SSA}.
VCCIO	9	Power	Internally generated digital I/O 3.3V power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CCIO} to V_{SSA}.
VCC33	17	Power	Internally generated 3.3V power supply. Connect to a 2.2µF or higher value ceramic capacitor from V_{CC33} to V_{SSA}.
VSS	24	Power	Ground.
VM	34	Power	High-Voltage Buck Regulator supply controller input. Connect a 1µF or higher value ceramic capacitor, or a 0.1µF ceramic capacitor in parallel with a 10µF or higher electrolytic capacitor from VM to VSS. This pin requires good capacitive bypass to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
BST	35	Power	High-Voltage Buck Regulator bootstrap input. Connect a 2.2µF or higher value ceramic capacitor from BST to SRC with a shorter than 10mm trace from the pin.
DRM	36	Power	High-Voltage Buck Regulator Switching supply driver output. Connect to the base or gate of the external N-channel MOSFET.
SRC	37	Power	High-Voltage Buck Regulator Source. Connect to the source of the high-side power MOSFET of the high-voltage buck regulator.
VP	42	Power	Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 10µF ceramic capacitor in parallel with a 100µF aluminum capacitor from V_P to V_{SS} for voltage loop stabilization. If the switching frequency of the HV-BUCK is >= 200kHz, then the 100µF aluminum capacitor can be replaced with 47µF, but the efficiency will be worse. This pin requires good capacitive bypassing to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
CSM	43	Power	High-Voltage Buck Regulator Switching supply current sense input. Connect to the positive side of the current sense resistor.
SW	47	Power	Switch node for the medium-voltage buck regulator.
VSYS	48	Power	5V System power supply. Connect to a 22µF/10V (20%) or higher ceramic capacitor from V_{SYS} to V_{SS}.
EP (VSS)	EP	Power	Exposed pad. Must be connected to V_{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking.

10.2 Signal Manager Pin Description

Table 10-2 Signal Manager Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
AIO0	18	AIO0	I/O	Analog front end I/O 0.
		DA0N	Analog	Differential PGA 10 negative input.
AIO1	19	AIO1	I/O	Analog front end I/O 1.
		DA0P	Analog	Differential PGA 10 positive input.
AIO2	20	AIO2	I/O	Analog front end I/O 2.
		DA1N	Analog	Differential PGA 32 negative input.
AIO3	21	AIO3	I/O	Analog front end I/O 3.
		DA1P	Analog	Differential PGA 32 positive input.
AIO4	22	AIO4	I/O	Analog front end I/O 4.
		DA2N	Analog	Differential PGA 54 negative input.
AIO5	23	AIO5	I/O	Analog front end I/O 5.
		DA2P	Analog	Differential PGA 54 positive input.
AIO6	38	AIO6	I/O	Analog front end I/O 6.
		AMP6	Analog	PGA input 6.
		CMP6	Analog	Comparator input 6.
		BUF6	Analog	Buffer output 6.
		PBTN	Analog	Push button input.
AIO7	44	AIO7	I/O	Analog front end I/O 7.
		AMP7	Analog	PGA input 7.
		CMP7	Analog	Comparator input 7.
		PHC7	Analog	Phase comparator input 7.
AIO8	45	AIO8	I/O	Analog front end I/O 8.
		AMP8	Analog	PGA input 8.
		CMP8	Analog	Comparator input 8.
		PHC8	Analog	Phase comparator input 8.
AIO9	46	AIO9	I/O	Analog front end I/O 9.
		AMP9	Analog	PGA input 9.
		CMP9	Analog	Comparator input 9.
		PHC9	Analog	Phase comparator input 9.

10.3 Driver Manager Pin Description

Table 10-3 Driver Manager Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DRS3	25	Analog	High-side gate driver source 3.
DRH3	26	Analog	High-side gate driver 3.
DRB3	27	Analog	High-side gate driver bootstrap 3.
DRS4	28	Analog	High-side gate driver source 4.
DRH4	29	Analog	High-side gate driver 4.
DRB4	30	Analog	High-side gate driver bootstrap 4.
DRS5	31	Analog	High-side gate driver source 5.
DRH5	32	Analog	High-side gate driver 5.
DRB5	33	Analog	High-side gate driver bootstrap 5.
DRL0	39	Analog	Low-side gate driver 0.
DRL1	40	Analog	Low-side gate driver 1.
DRL2	41	Analog	Low-side gate driver 2.

10.4 I/O Ports Pin Description

Table 10-4 I/O Ports Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION[1]
PD1/AD3	1	PD1	I/O	I/O port PD1.
		AD3	Analog Input	ADC channel ADC3.
PD0/AD4	2	PD0	I/O	I/O port PD0.
		AD4	Analog Input	ADC channel ADC4.
PE0	3	PE0	I/O	I/O port PE0.
PE1	4	PE1	I/O	I/O port PE1.
PE2	5	PE2	I/O	I/O port PE2.
PE3	6	PE3	I/O	I/O port PE3.
PF6/AD6	10	PF6	I/O	I/O port PF6.
		AD6	Analog Input	ADC channel ADC6.
PF5/AD5	11	PF5	I/O	I/O port PF5.
		AD5	Analog Input	ADC channel ADC5.
PF4/AD4	12	PF4	I/O	I/O port PF4.
		AD4	Analog Input	ADC channel ADC4.
PF3	13	PF3	I/O	I/O port PF3.
PF2	14	PF2	I/O	I/O port PF2.
PF1	15	PF1	I/O	I/O port PF1.
PF0	16	PF0	I/O	I/O port PF0.
PC4	49	PC4	I/O	I/O port PC4.
PC5	50	PC5	I/O	I/O port PC5.
PD2/AD2	51	PD2	I/O	I/IO port PD2.
		AD2	Analog Input	ADC channel ADC2.

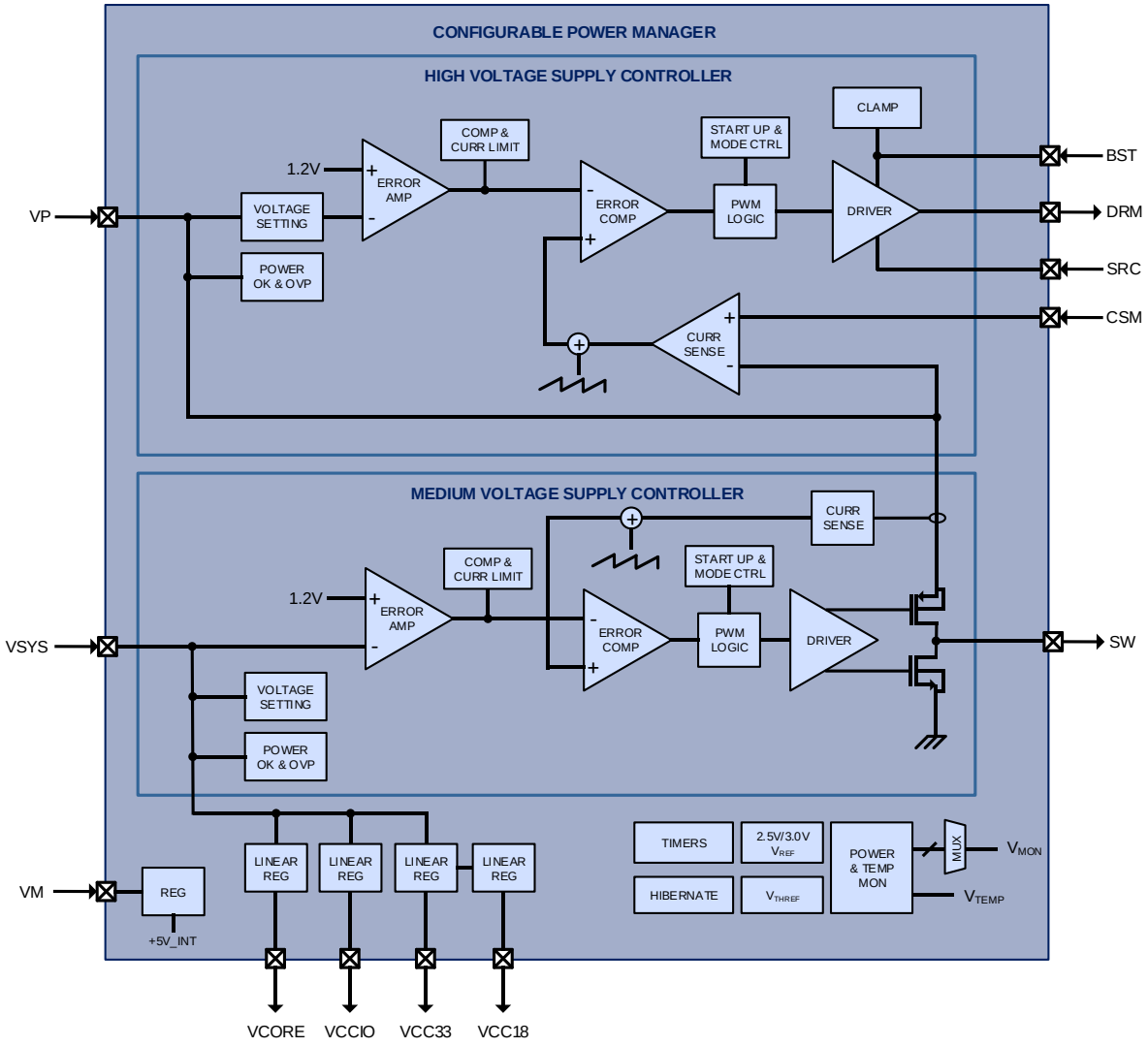
[1] For a full description of all of the pin configurations for each digital I/O, see the Digital Peripheral MUX in the PAC55XX Family User Guide.

11 CONFIGURABLE POWER MANAGER (CPM)

11.1 Features

- 160V Buck DC/DC Controller (HV Buck)
  - 25V – 160V input
- 5V Switching Regulator (MV Buck)
- 4 linear regulators with power and hibernate management, including V_{REF} for ADC
- Power and temperature monitor, warning, and fault detection

Figure 11-1 CPM Block Diagram



11.2 Functional Description

The Configurable Power Manager (Figure 11-1) is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a high-voltage power supply controller that is used to convert power from a DC input source to generate a main supply output V_P. There is also an integrated medium-voltage buck DC/DC regulator to generate V_{SYS}.

Four other linear regulators provide V_{CCIO}, V_{CC33}, V_{CC18} and V_{CORE} supplies for 3.3V I/O, 3.3V mixed signal, MCU FLASH and 1.2V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

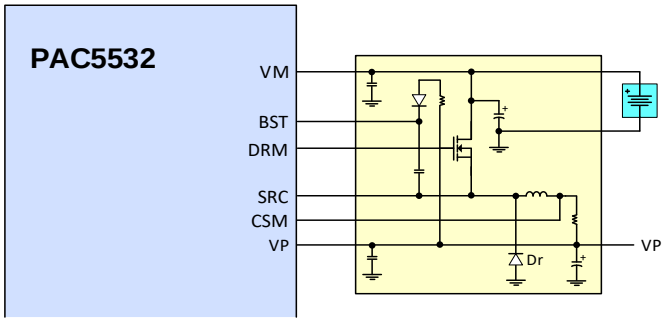
11.3 High-Voltage Supply Controller (HV-BUCK)

The PAC5532 contains a High-Voltage Supply Controller for a Buck DC/DC. This power supply is used to supply the various regulators in the PAC5532, as generating the V_P gate drive voltage for the Application Specific Driver Manager (ASPD).

The HV-BUCK controller drives an external power MOSFET for pulse-width modulation switching of an inductor or transformer for power conversion. The VM is the HV-BUCK supply controller input. The DRM output drives the gate of the N-CH MOSFET between the V_M on state and V_{SS} off state at proper duty cycle and switching frequency to ensure that the main supply voltage V_P is regulated. The gate of the high-side power MOSFET is connected to the DRM pin and the source of the high-side power MOSFET is connected to SRC.

The V_P regulation voltage is initially set to 15V during start up, and can be reconfigured to be 15V by the microcontroller after initialization. When V_P is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise V_P. Conversely, when V_P is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower V_P. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. The inductor current signal is sensed differentially between the CSM pin and V_P, and has a peak current limit threshold of 0.2V.

Figure 11-2 HV-BUCK Example



The switching frequency and output voltage of the HV-BUCK can be reconfigured by the MCU. The switching frequency can be configured to be between 50kHz and 400kHz and the gate drive output voltage can be configured to either 12V or 15V to work for a range of MOSFET or IGBT based inverters.

The Rectifier Diode (Dr) must be a low QRR diode.

11.3.1 HV-BUCK Re-start Handling

The HV-BUCK has a safety re-start mechanism that protects the device and external components in case of a DC/DC failure. This mechanism samples VM and VP when the MV-BUCK is re-started and may insert a delay before it allows the power supply to be re-started, in case of some type of short or damage with the power supply components on the PCB.

The re-start handling operates as described below.

In PAC5532, if the DC/DC has been disabled due to VM falling below $V_{UVLOF;VM}$, VM is sampled and if VM > 10V, then a 350ms delay is inserted, before sampling VM again and attempting a re-start of the DC/DC. Once the delay has expired and VM > $V_{UVLOR;VM}$, then the DC/DC will re-start. If VM falls below 8V, the DC/DC will re-start as an initial start-up without the 350ms delay.

In PAC5532A or PAC5532B, if the DC/DC has been disabled due to VM falling below $V_{UVLOF;VM}$, VM is sampled and as soon as VM > $V_{UVLOR;VM}$, then the DC/DC will re-start. In this case, there is no delay before the re-start of the DC/DC.

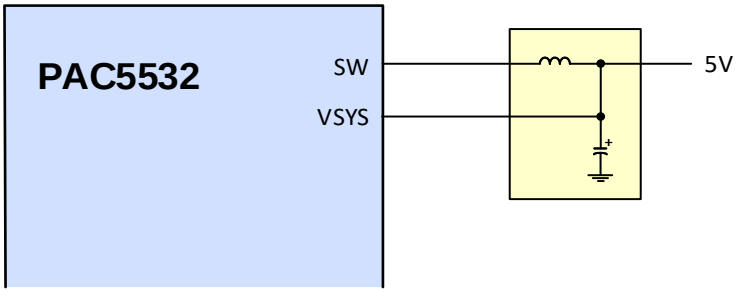
In both PAC5532, PAC5532A or PAC5532B, if VM is > VM UVLO falling ($V_{UVLOF;VM}$) but VP < VP UVLO falling ($V_{UVLOF;VP}$) then the DC/DC is disabled and a 350ms delay is inserted. After this delay, the DC/DC is re-started.

11.4 Medium-Voltage Buck Regulator (MV-BUCK)

The PAC5532 contains a Medium-Voltage Buck Switching Regulator that generates a 5V, 200mA supply for the device, as well as PCB functions.

The SW pin is the switch node of the Buck regulator. The Power MOSFET is integrated, so connect this pin to VSYS through an external inductor. The VSYS pin is the 5V regulator output, which should be bypassed to ground.

Figure 11-3 MV-BUCK Switching Regulator Example

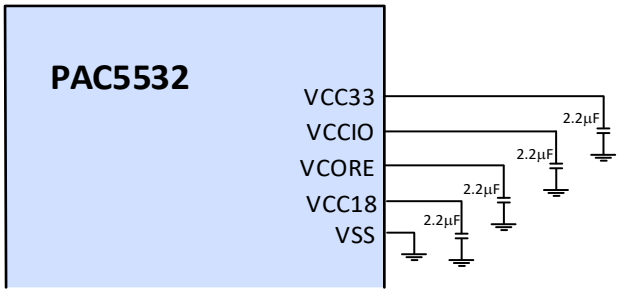


The output of VSYS is fixed at 5V and the switching frequency is 1.33MHz. This regulator supplies at least 200mA. This buck regulator offers better thermal and efficiency performance.

11.5 Linear Regulators

The CPM includes four additional linear regulators. VSYS supplies these three regulators. Once VSYS is above 4.5V, the four additional linear regulators for VCCIO, VCC33, VCC18 and VCORE supplies sequentially power up.

Figure 11-4 Linear Regulators Example

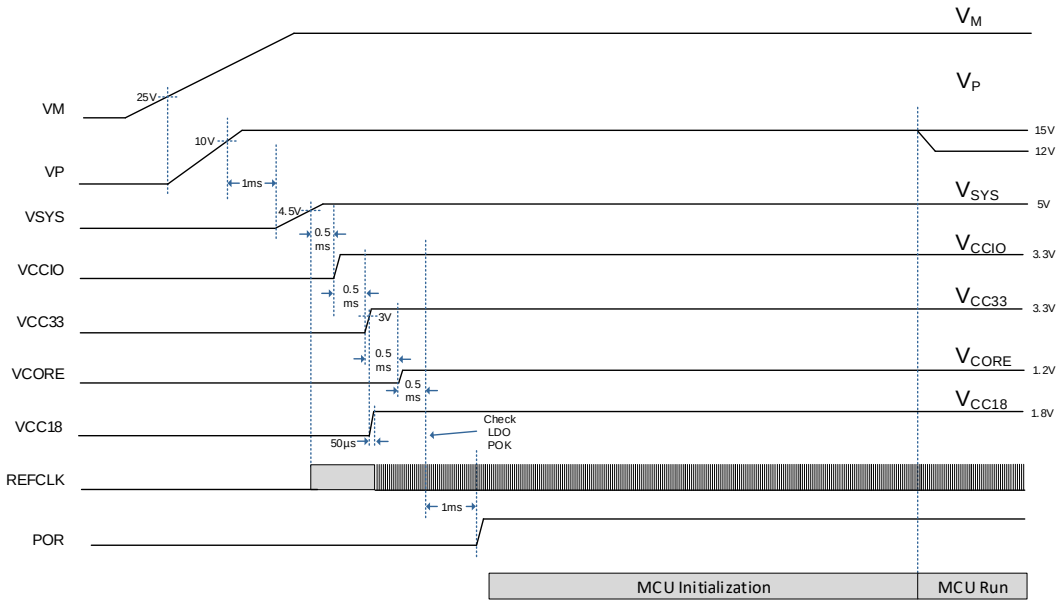


The figure above shows typical circuit connections for the linear regulators. The VCCIO regulator generates a dedicated 3.3V supply for IO. The VCC33 and VCORE regulators generate 3.3V and 1.2V, respectively. When VSYS and the four LDOs above are all above their respective power good thresholds, and the configurable power on reset duration has expired, the microcontroller is initialized.[2]

11.6 Power-up Sequence

The CPM follows a typical power up sequence as shown in Figure 11-5 below.

Figure 11-5 Power-Up Sequence



[2] Note that the VCORE LDO may not have any additional load on it from the PCB. The only components connected to VCORE should be a bypass capacitor to ground.

A typical sequence begins with motor power supply (VM) being applied and rising to 25V. When VM rises to 25V, the HV-BUCK controller is started and VP starts to rise. When VP rises over the UVLO rising threshold, then there is a 1ms delay and then the MV-BUCK is enabled. When VSYS rises to 4.5V, then there is a 0.5ms delay and the VCCIO LDO is enabled. Then there is a 0.5ms delay and the VCC33 LDO is enabled. After the VCC33 LDO reaches 3V, then VCC18 LDO is enabled. Also 0.5ms after the VCC33 LDO is enabled, the VCORE LDO is enabled.

There is then a 0.5ms delay and the power good threshold of all LDOs is checked. If all are OK, then there is an additional 1ms delay, then the POR signal is asserted to the MCU and it begins executing firmware.

During the firmware initialization process, the MCU may change the VP output voltage setting from the default value of 15V to 12V.

11.7 Hibernate Mode

The IC can go into an ultra-low power hibernate mode via the microcontroller firmware or via the optional push button (PBTN, see *Push Button* description in *Configurable Analog Front End*). In hibernate mode, only a minimal amount (typically 19µA at 56V) of current is used by V_M, and the CPM controller and all internal regulators are shut down to eliminate power drain from the output supplies. The system exits hibernate mode after a wake-up timer duration (configurable from 125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the microcontroller is reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

11.8 Power and Temperature Monitor

Whenever any of the V_{SYS}, V_{CCIO}, V_{CC33}, V_{CC18} or V_{CORE} power supplies falls below their respective power good threshold voltage, a fault event is detected and the microcontroller is reset. The microcontroller stays in the reset state until V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CORE} supply rails are all good again and the reset time has expired. A microcontroller reset can also be initiated by a maskable temperature fault event that occurs when the IC temperature reaches 165°C. The fault status bits are persistent during reset, and can be read by the microcontroller upon re-initialization to determine the cause of previous reset.

A power monitoring signal V_{MON} is provided onto the ADC pre-multiplexer for monitoring various internal power supplies. V_{MON} can be set to be one of the following monitored supplies: V_{CORE}, 0.4•V_{CORE}, 0.4•V_{CC33}, 0.4•V_{CCIO}, 0.4•V_{SYS}, VPTAT[3] or 0.1•V_P.

[3] VPTAT is voltage proportional with absolute temperature from the temperature sensing circuit. The VPTAT voltage can be sampled by the ADC through the voltage monitoring MUX. See the PAC5532 Device User Guide for more information.

For power and temperature warning, an IC temperature warning event at 140°C are provided as a maskable interrupt to the microcontroller. This warning allows the microcontroller to safely power down the system.

In addition to the temperature warning interrupt and fault reset, a temperature monitor signal is provided onto the ADC pre-multiplexer for IC temperature measurement.

This value has a compensation coefficient available in INFO FLASH that can be used to obatin an accurate temperature. The parameter VT300K will be stored in INFO FLASH and will indicate the compensation factor.

The die temperature in degrees Kelvin can then be obatined by the following formula:

T_{KELVIN} = 300 * (VPTAT + 0.075) / (VT300K + 0.075)

For information on on the location of this temperature coefficient, see the PAC5532 Device User Guide.

11.9 Voltage Reference

The reference block includes a 1.2V high-precision reference voltage used internally and for all the LDOs. There is also a high-accuracy 2.5V/3.0V programmable reference for the ADC V_{REF} on the MCU. There is also a 4-level programmable threshold voltage V_{THREF} (0.1V, 0.2V, 0.5V, and 1.25V).

11.10 Electrical Characteristics

Table 11-1 High-Voltage Buck Controller Electrical Characteristics

(V_M = 30V, V_P = 12V and T_J = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{HIB;VM}$	V_M hibernate mode supply current	Hibernate mode, VM = 56V		19	26	µA
		Hibernate mode, VM = 80V		22.5		µA
$V_{UVLOR;VM}$	V_M UVLO rising		23	25	27	V
$V_{UVLOF;VM}$	V_M UVLO hysteresis			8		V
$V_{REF;VP}$	V_P output regulation voltage	Set to 12V	-5%	12	-5%	V
$k_{POKR;VP}$	V_P power OK threshold	V_P rising		91		%
$k_{POKF;VP}$		V_P falling		87		%
$k_{OVPR;VP}$	V_P OV protection threshold	V_P rising, blanking = 10□s		130		%
$t_{ONMIN;DRM}$	DRM minimum on time		90	200	300	ns
$t_{OFFMIN;DRM}$	DRM minimum off time		390	600	1150	ns
$V_{UVLOR;VP}$	V_P UVLO rising			10		V
$V_{UVLOF;VP}$	V_P UVLO falling			8		V
$V_{CSM;ILIM}$	CSM current limit threshold		-12%	0.2	12%	V
$F_{S;DRM}$	Switching frequency	Frequency setting: 50kHz, 100kHz (default), 200kHz, 400kHz	-5		5	%
$I_{SOURCE;DRM}$	DRM output high source current			100		mA
$I_{SINK;DRM}$	DRM output low sink current			200		mA
	HV-BUCK inductor value			100		□H
I_{DSG}	Discharge current			10		mA
V_{VM}	Motor voltage range		0		160	V
$V_{SRC;VSS}$	SRC to ground range		-10		VM + 10	V
$V_{SRC;VM}$	SRC to VM range				10	V
$V_{BST;VSS}$	BST to ground range				175	V

Table 11-2 Medium-Voltage Buck Controller Electrical Characteristics

(V_M = 30V, V_P = 12V and T_J = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{VSYS}	V_{SYS} output voltage accuracy		-3%	5	3%	V
F_{SW}	Switching frequency		-5%	1.33	5%	MHz
$I_{VSYS;LIM}$	V_{SYS} current limit		420		550	mA
I_{VSYS}	V_{SYS} output current	V_{SYS} > 3V	200			mA
		V_{SYS} < 2.5V	100			mA
$V_{POK;VSYS}$	V_{SYS} power OK threshold	Rising	4.25	4.5	4.75	V
		Falling		4.2		V
	V_{SYS} power OK blanking delay			10		µs
	MV-BUCK inductor value	Current rating of at least 750mA	6.8 – 20%		10 + 20%	µH
$V_{UVLO;VSYS}$	V_{SYS} UVLO	Rising		4.5		V
		Falling		4.2		V
$V_{OVP;VSYS}$	V_{SYS} OVP	Rising		5.5		V
		Falling		5.2		V

Table 11-3 Linear Regulators Electrical Characteristics

(V_P = 12V and T_A = -40°C to 125°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CCIO}	V_{CCIO} output voltage	Load = 1mA	-3%	3.3	3%	V
V_{CC33}	V_{CCIO} output voltage	Load = 1mA	-3%	3.3	3%	V
V_{CORE}[4]	V_{CORE} output voltage	Load = 1mA	-3%	1.2	3%	V
V_{CC18}	V_{CC18} output voltage			1.8		V
$I_{LIM;VCCIO}$	V_{CCIO} current limit		40	65		mA
$I_{LIM;VCC33}$	V_{CC33} current limit		40	65		mA
$I_{LIM;VCORE}$	V_{CORE} current limit		40	65		mA
	LDO current fold back			50		%
$t_{POK;BLANK}$	Power OK blanking delay	V_{CCIO}, V_{CC33}, V_{CORE}		10		µs
R_{DISCH}	Output discharge resistance	LDO off		300		Ohm
C_{VCCIO}	VCCIO stable output capacitance		1		4.7	µF
C_{VCC33}	VCC33 stable output capacitance		1		4.7	µF
C_{VCORE}	VCORE stable output capacitance		1		4.7	µF
C_{VCC18}	VCC18 stable output capacitance		1		4.7	µF
$t_{POK;VCC18}$	VCC18 power OK time	C_{VCC18} = 1µF			50	µs
$V_{LDO;POK}$	LDO power OK rising threshold	Hysteresis = 10%	85	90	95	%

[4] Note that the VCORE LDO may not have any other loads. The only connection to the VCORE pin should be a bypass capacitor to ground.

11.11 Typical Performance Characteristics

(T_A = 25ºC unless otherwise specified)

Figure 11-6 VDDIO LDO Voltage vs. Current

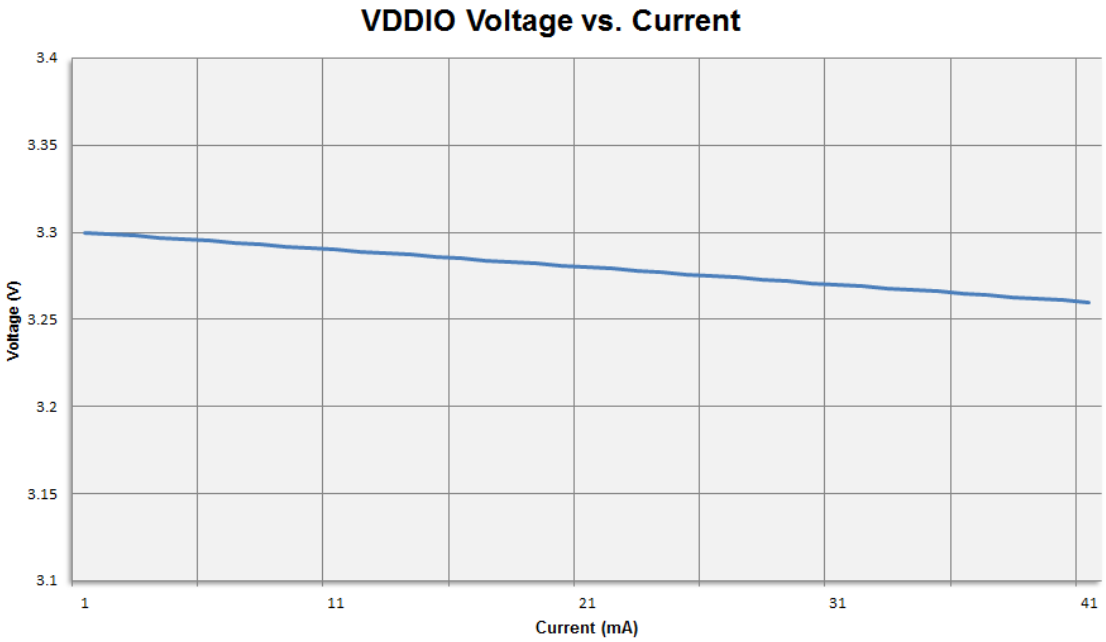


Figure 11-7 VCC33 LDO Voltage vs. Current

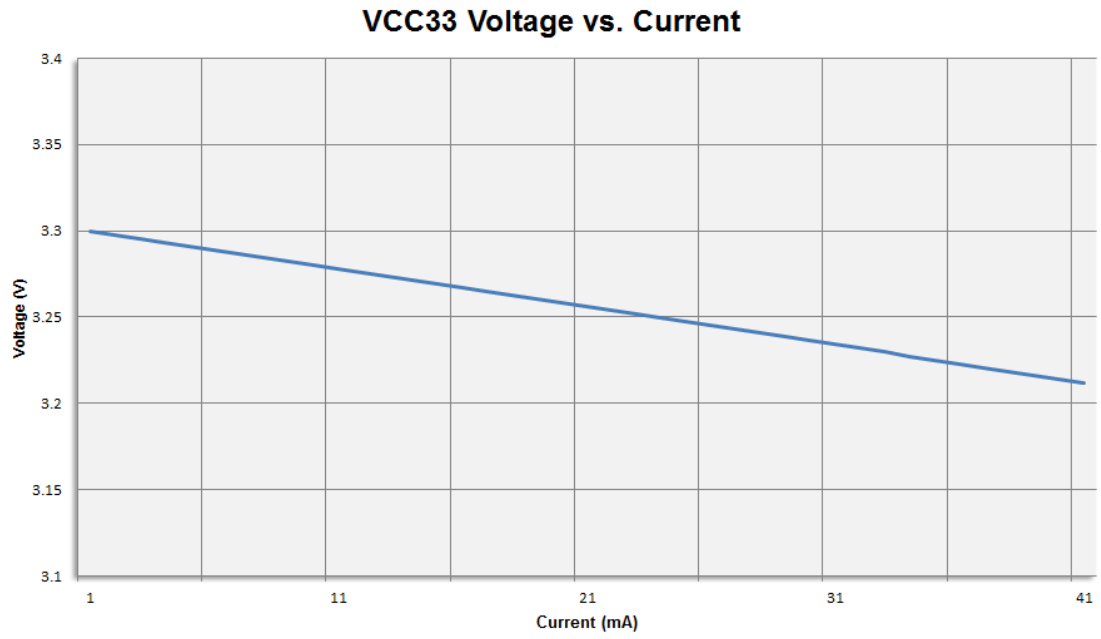
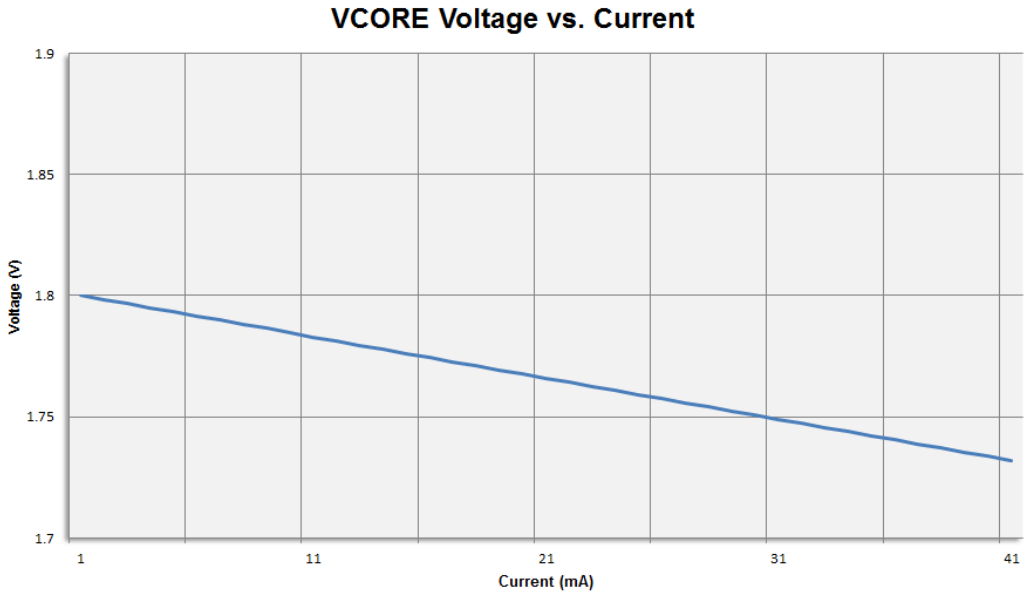


Figure 11-8 VCORE LDO Voltage vs. Current



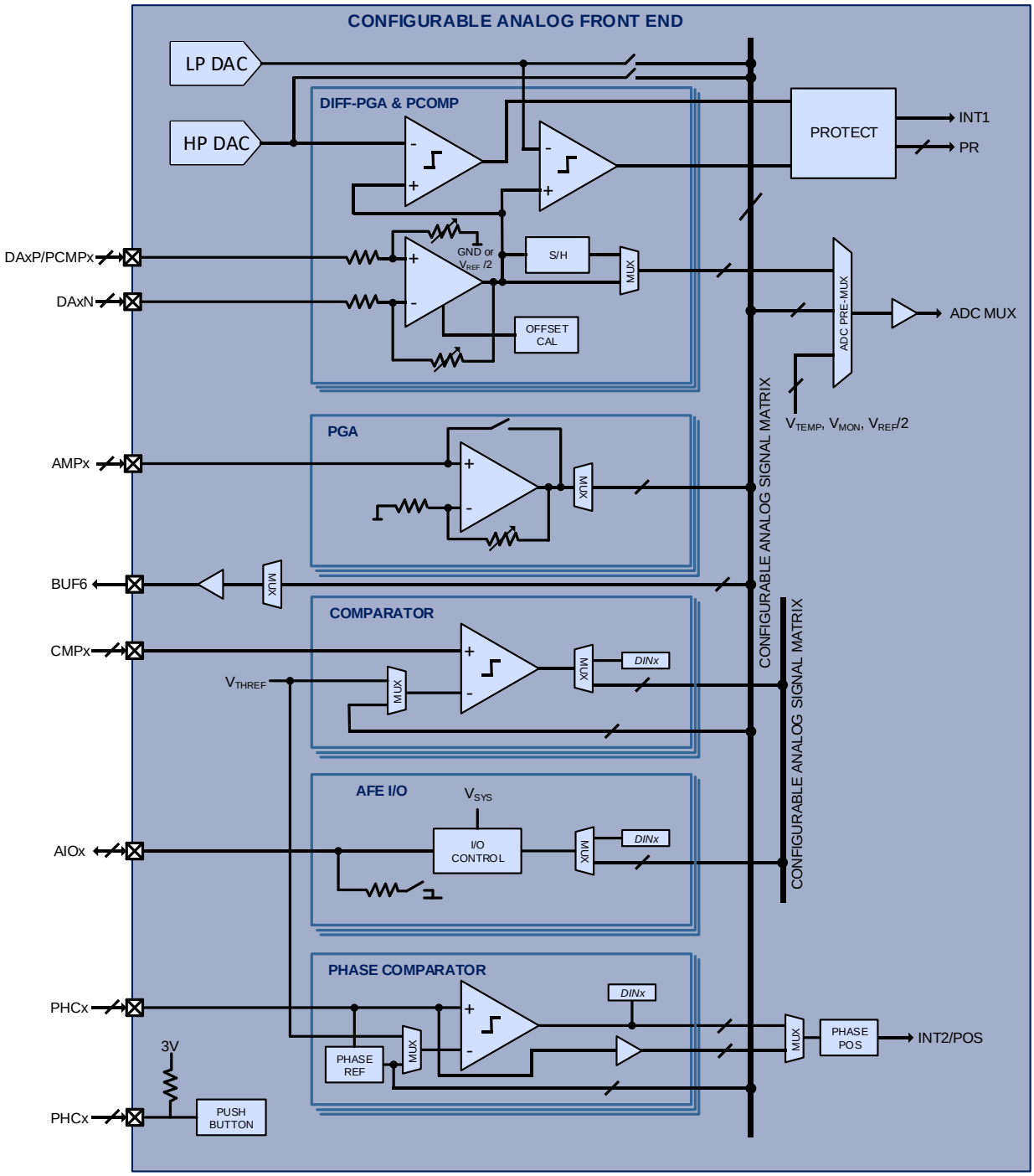
12 CONFIGURABLE ANALOG FRONT END (CAFE)

12.1 Features

- 10 Configurable Analog I/O signals
  - Gain mode, comparator mode, I/O mode, special mode
- 3 High-Performance, Configurable Differential Amplifiers
- 4 High-Performance, Configurable Single-Ended Amplifiers
- Two high-speed comparators with protection functions
- Phase to phase, phase to center-tap modes
- Bi-directional, asymmetric configurable comparator hysteresis
- Push-button input for entering/exiting hibernate mode

12.2 Block Diagram

Figure 12-1 Configurable Analog Front End



12.3 Functional Description

The device includes a Configurable Analog Front End (CAFE, Figure 12-1) accessible through 10 analog and I/O pins. These pins can be configured to form flexible interconnected circuitry made up of 3 differential programmable gain amplifiers, 4 single-ended programmable gain amplifiers, 4 general purpose comparators, 3 phase comparators, 2 protection comparators, and one buffer output. These pins can also be programmed as analog feed-through pins, or as analog front end I/O pins that can function as digital inputs or digital open-drain outputs. The PAC proprietary configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push button function is provided for optional push button on, hibernate, and off power management function.

12.4 Differential Programmable Gain Amplifier (DA)

The DAxP and DAxN pin pair are positive and negative inputs, respectively, to a differential programmable gain amplifier. The differential gain can be programmable to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x for zero ohm signal source impedance. The differential programmable gain amplifier has -0.3V to 2.5V input common mode range, and its output can be configured for routing directly to the ADC pre-multiplexer, or through a sample-and-hold circuit synchronized with the ADC auto-sampling mechanism. Each differential amplifier is accompanied by offset calibration circuitry, and two protection comparators for protection event monitoring. The programmable gain differential amplifier is optimized for use with signal source impedance lower than 500Ω and with matched source impedance on both positive and negative inputs for minimal offset. The effective gain is scaled by 13.5k / (13.5k + R_{SOURCE}), where R_{SOURCE} is the matched source impedance of each input.

12.5 Single-Ended Programmable Gain Amplifier (AMP)

Each AMPx input goes to a single-ended programmable gain amplifier with signal relative to V_{SS}. The amplifier gain can be programmed to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x, or as analog feed-through. The programmable gain amplifier output is routed via a multiplexer to the configurable analog signal matrix CASM.

12.6 General Purpose Comparator (CMP)

The general purpose comparator takes the CMPx input and compares it to either the programmable threshold voltage (V_{THREF}) or a signal from the configurable analog signal matrix CASM. The comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed via a multiplexer to either a data input bit or the configurable digital signal matrix CDSM. Each general purpose comparator has two mask bits to prevent or allow rising or falling edge of its output to trigger second microcontroller interrupt INT2, where INT2 can be configured to active protection event PR.

12.7 Phase Comparator (PHC)

The phase comparator takes the PHCx input and compares it to either the programmable threshold voltage (V_{THREF}) or a signal from the configurable analog signal matrix CASM. The comparison signal can be set to a phase reference signal generated by averaging the PHCx input voltages. In a three-phase motor control application, the phase reference signal acts as a virtual center tap for BEMF detection. The PHCx inputs are optionally fed through to the CASM. The PHC inputs can be compared to the virtual center-tap, or phase to phase for the most efficient BEMF zero-cross detection.

The phase comparator signals can also be configured to the other two phase comparators (between AIO7, AIO8 and AIO9), to perform phase to phase comparisons.

The comparator blanking time is configurable. The blanking time configuration supports bi-directional and asymmetric configurations, which enables hysteresis for rising and falling signals.

The phase comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed to a data input bit and to the phase/position multiplexer synchronized with the auto-sampling sequencers.

12.8 Protection Comparator (PCMP)

Two protection comparators are provided in association with each differential programmable gain amplifier, with outputs available to trigger protection events and accessible as read-back output bits. The HP comparator compares the amplifier output to the 10-bit HP DAC output voltage, with full scale voltage of 2.5V. The limit protection (LP) comparator compares the differential programmable gain amplifier output to the 10-bit LP DAC output voltage, with full scale voltage of 2.5V.

Each protection comparator has a mask bit to prevent or allow it to trigger the main microcontroller interrupt INT1. Each protection comparator also has one mask bit to prevent or allow it to activate protection event PR. These two protection events can be used directly by protection circuitry in the Application Specific Power Drivers (ASPD) to protect devices being driven.

12.9 Analog Output Buffer (BUF)

A subset of the signals from the configurable analog signal matrix CASM can be multiplexed to the BUF6 pin for external use. The buffer offset voltage can be minimized with the built-in swap function.

12.10 Analog Front End I/O (AIO)

The PAC5532 has 10 AIOx pins that are available. In the analog front end I/O mode, the pin can be configured to be a digital input or digital open-drain output. The AIOx input or output signal can be set to a data input or output register bit, or multiplexed to one of the signals in the configurable digital signal matrix CDSM. The signal can be set to active high (default) or active low, with V_{SYS} supply rail. Where $AIO_{6,7,8,9}$ supports microcontroller interrupt for external signals. Each has two mask bits to prevent or allow rising or falling edge of its corresponding digital input to trigger second microcontroller interrupt INT2.

12.11 Push Button (PBTN)

The push button PBTN, when enabled, can be used by the MCU to detect a user active-low push button event and to put the system into an ultra-low-power hibernate mode. Once the system is in hibernate mode, PBTN can be used to wake up the system.

In addition, PBTN can also be used as a hardware reset for the microcontroller when it is held low for longer than 8s during normal operation. The PBTN input is active low and has a 55kΩ pull-up resistor to 3V.

12.12 HP DAC and LP DAC

The 10-bit HP DAC can be used as the comparison voltage for the high-speed protection (HP) comparators, or routed for general purpose use via the AB2 signal in the CASM. The HP DAC output full scale voltage is 2.5V.

The 10-bit LP DAC can be used as the comparison voltage for the limit protection (LP) comparators, or routed for general purpose use via the AB3 signal in the CASM. The LP DAC output full scale voltage is 2.5V.

12.13 ADC Pre-Multiplexer

The ADC pre-multiplexer is a 16-to-1 multiplexer that selects between the 3 differential programmable gain amplifier outputs, AB1 through AB9, temperature monitor signal (V_{TEMP}), power monitor signal (V_{MON}), and offset calibration reference (V_{REF} / 2). The ADC pre-multiplexer can be directly controlled or automatically scanned by the auto-sampling sequencer.

When the ADC pre-multiplexer is automatically scanned, the unbuffered or sensitive signals should be masked by setting appropriate register bits.

12.14 Configurable Analog Signal Matrix (CASM)

The CASM has 12 general purpose analog signals labeled AB1 through AB9 that can be used for:

- Routing the single-ended programmable gain amplifier or analog feed-through output to AB1 through AB9
- Routing an analog signal via AB1, AB2, or AB3 to the negative input of a general purpose comparator or phase comparator
- Routing the 10-bit HP DAC output to AB2
- Routing the 10-bit LP DAC output to AB3
- Routing analog signals via AB1 through AB12 to the ADC pre-multiplexer
- Routing phase comparator feed-through signals to AB7, AB8, and AB9, and averaged voltage to AB1

12.15 Configurable Digital Signal Matrix (CDSM)

The CDSM has 7 general purpose bi-directional digital signals labeled DB1 through DB7 that can be used for:

- Routing the AIOx input to or output signals from DB1 through DB7
- Routing the general purpose comparator output signals to DB1 through DB7

12.16 Cycle-by-cycle Current Limit

The PAC5532 contains hardware support for cycle by cycle current limit. The user may configure this feature to use the LPCOMP DAC as the current threshold. The CAFE will automatically perform duty cycle truncation to lower current at any time the associated phase current is greater than the setting of the LPCOMP DAC.

12.17 Temperature Protection

The PAC5532 contains an internal temperature sensor that detects temperature warnings and faults.

When the device temperature reaches the temperature warning threshold (140ºC), the device sets an over-temperature warning condition. The user may configure a mask-able interrupt the MCU for this condition.

When the device temperature reaches the temperature fault threshold (165 ºC), the device is shut down. There is no interrupt for this condition.

For more details on the register settings for over-temperature protection see the PAC5532 User Guide and related application notes.

12.18 Electrical Characteristics

Table 12-1 Differential Programmable Gain Amplifier (DA) Electrical Characteristics (AIO<5:0>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;DA}$	Input common mode range		-0.3		2.5	V
$V_{OLR;DA}$	Output linear range		0.1		V_{SYS} – 0.1	V
$V_{SHR;DA}$	Sample and hold range		0.1		3.5	V
$I_{CC;DA}$	Operating supply current	Each enabled amplifier		150		µA
$V_{OS;DA}$	Input offset voltage	Gain = 8x	-8		8	mV
$k_{CMRR;DA}$	Common mode rejection ratio		50	80		dB
	Slew rate	Gain = 8x	10			V/µs
$R_{INDIF;DA}$	Differential input impedance			27		kΩ
$t_{ST;DA}$	Settling time	To 1% of final value			360	ns
$A_{VZI;DA}$	Differential amplifier gain (zero ohm source impedance)	Gain = 1x		1		
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{DAxP}=V_{DAxN}=0V, T_A = 25°C		8		
			-2		2	%
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		

Table 12-2 Single-Ended Programmable Gain Amplifier (AMP) Electrical Characteristics (AIO<9:6>)

(V_{SYS} = 5V, V_{CCIO} = 3.3V and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;AMP}$	Input common mode range		0		V_{SYS}	V
$V_{OLR;AMP}$	Output linear range		0.1		V_{SYS} – 0.1	V
$I_{CC;AMP}$	Operating supply current	Each enabled amplifier		80	120	µA
$V_{OS;AMP}$	Input offset voltage	Gain = 8x	-10		10	mV
	Slew rate	Gain = 1x	10			V/µs
$t_{ST;AMP}$	Settling time	To 1% of final value			360	ns
$A_{V;AMP}$	Amplifier gain	Gain = 1x		1		%
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{AMPx}=125mV, T_A = 25°C		8		
			-2		2	
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		
$t_{ST;AMP}$	Settling time	To 1% of final value			350	ns

Table 12-3 General Purpose Comparator (CMP) Electrical Characteristics (AIO<9:6>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;CMP}$	Input common mode range		0		V_{SYS}	V
$I_{CC;CMP}$	Operating supply current	Each enabled comparator		35		µA
$V_{OS;CMP}$	Input offset voltage		-10		10	mV
$V_{HYS;CMP}$	Hysteresis			22		mV
$t_{DEL;CMP}$	Comparator delay				1	µs
$t_{DELMODE;CMP}$	Mode change blanking delay			10		µs

Table 12-4 Phase Comparator (PHC) Electrical Characteristics (AIO<9:6>)

(V_{SYS} = 5V, V_{CC33} = 3.3V and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;PHC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;PHC}$	Operating supply current	Each enabled comparator		35		µA
$V_{OS;PHC}$	Input offset voltage		-10		10	mV
$V_{HYS;PHC}$	Hysteresis			23		mV
$t_{DEL;PHC}$	Comparator delay	10mV difference input			1	µs

Table 12-5 Special Mode Electrical Characteristics (AIO<9:7>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;SPEC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;SPEC}$	Operating supply current	Each enabled comparator		80	120	µA
$V_{HSYS;SPEC}$	Comparator Hysteresis, HYSMODE = 0	AIO<9:7>HYS = 00b (0mV)		0		mV
		AIO<9:7>HYS = 01b (6mV)	4	6	8	mV
		AIO<9:7>HYS = 10b (12mV)	9	12	15	mV
		AIO<9:7>HYS = 11b (24mV)	18	24	30	mV
	Comparator Hysteresis, HYSMODE = 1	AIO<9:7>HYS = 00b (0mV)		0		mV
		AIO<9:7>HYS = 01b (24mV)	18	24	30	mV
		AIO<9:7>HYS = 10b (48mV)	36	48	60	mV
		AIO<9:7>HYS = 11b (96mV)	72	96	120	mV

Table 12-6 Special Mode Electrical Characteristics (AIO6)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;SPEC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;SPEC6}$	Operating supply current			60		µA
$V_{INOFF;SPEC6}$	Input offset voltage		-20		20	mV
$I_{OUT;SPEC6}$	Output current			2		mA

Table 12-7 Analog Front End (AIO) Electrical Characteristics (AIO<9:0>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{AIO}	Pin voltage range		0		5	V
$V_{IH;AIO}$	High-level input voltage		2.2			V
$V_{IL;AIO}$	Low-level input voltage				0.8	V
$R_{PD;AIO}$	Pull-down resistance	Input mode		1		MΩ
$V_{OL;AIO}$	Low-level output voltage	I_{AIOx}=7mA, open-drain output mode			0.3	V
$I_{OL;AIO}$	Low-level output sink current	V_{AIOx} = 0.4V, open-drain output mode	6	14		mA
$I_{LK;AIO}$	High-level output leakage current	V_{AIOx} = 5V, open-drain output mode		0	10	µA

Table 12-8 Push Button (PBTN) Electrical Characteristics (AIO6)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I;PBTN}$	Input voltage range		0		5	V
$V_{IH;PBTN}$	High-level input voltage		2.2			V
$V_{IL;PBTN}$	Low-level input voltage				0.8	V
$R_{PU;PBTN}$	Pull-up resistance	To 3V, push-button input mode		50		kΩ

Table 12-9 HP DAC and LP DAC Electrical Characteristics

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DACREF}	DAC reference voltage	TA = 25°C	-0.5%	2.5	0.5%	V
		TA = -40°C to 125°C	-0.9%	2.5	0.9%	
	HP 10-bit DAC INL		-2		2	LSB
	HP 10-bit DAC DNL		-1		1	LSB
	LP 10-bit DAC INL		-2		2	LSB
	LP 10-bit DAC DNL		-1		1	LSB

Table 12-10 Temperature Protection

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{WARN}	Temperature warning threshold			140		ºC
$T_{WARN;HYS}$	Temperature warning hysteresis			10		ºC
$T_{WARN;BLANK}$	Temperature warning blanking			10		µs
T_{FAULT}	Temperature fault threshold			165		ºC
$T_{FAULT;HYS}$	Temperature fault hysteresis			10		ºC
$T_{FAULT;BLANK}$	Temperature fault blanking			10		µs

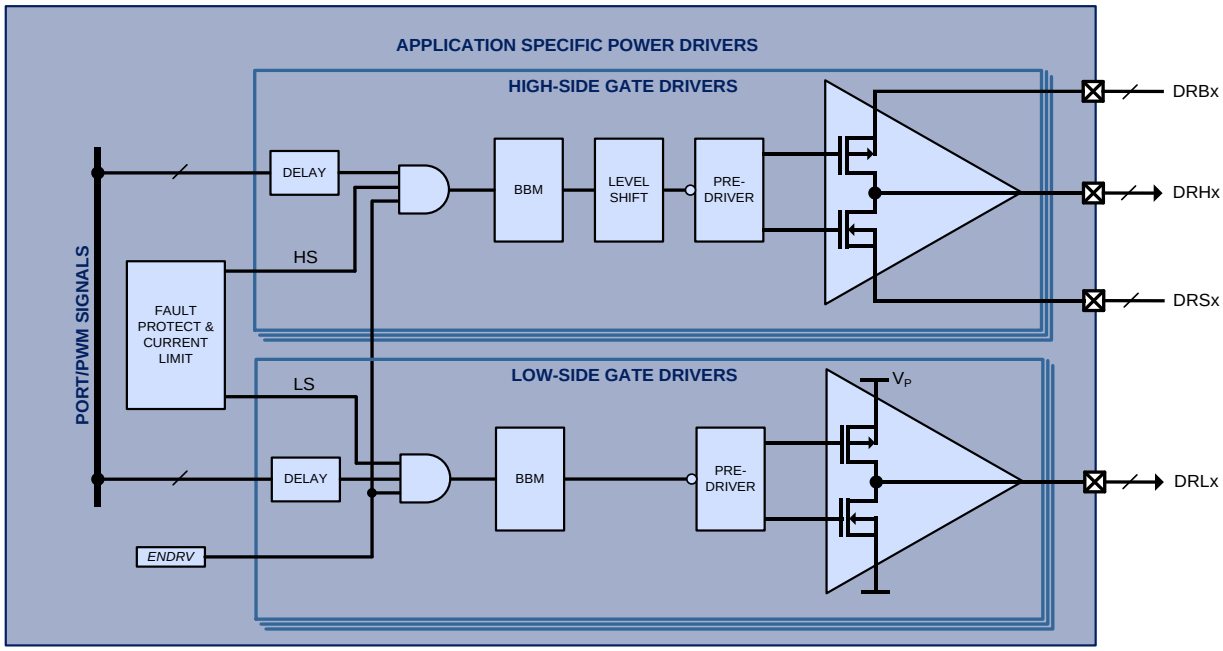
13 APPLICATION SPECIFIC POWER DRIVERS (ASPD)

13.1 Features

- 3 low-side and 3 high-side gate drivers
- 2A sink/source gate driving capability
- Configurable propagation delays
- Fast fault protection
- Cycle-by-cycle current limit function
- Configurable driver break-before-make (BBM) safety function

13.2 Block Diagram

Figure 13-1 Application Specific Power Drivers



13.3 Functional Description

The Application Specific Power Drivers (ASPD, Figure 13-1) module handles power driving for power and motor control applications. The ASPD contains three low-side gate drivers (DRLx), three high-side gate drivers (DRHx). Each gate driver can drive an external MOSFET or IGBT switch in response to high-speed control signals from the microcontroller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

Figure 13-2 below shows typical gate driver connections and Table 13-1 shows the ASPD available resources. The ASPD gate drivers support up to a 180V source supply.

Figure 13-2 Typical Gate Driver Connections

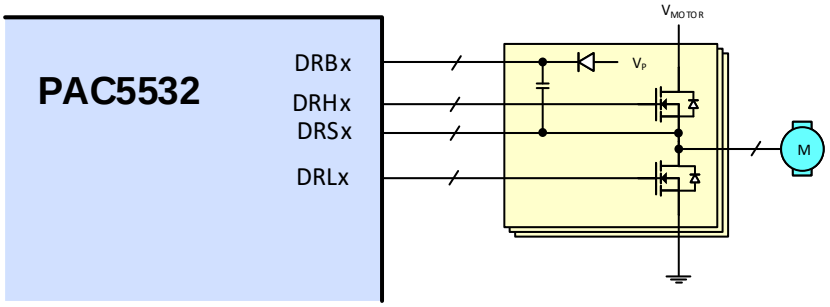


Table 13-1 Power Driver Resources by Part Numbers

PART NUMBER	LOW-SIDE GATE DRIVER		HIGH-SIDE GATE DRIVER		
	DRLx	SOURCE/SINK CURRENT	DRHx	SOURCE/BOOTSTRAP SUPPLY	SOURCE/SINK CURRENT
PAC5532	3	2A/2A	3	165V/180V	2A/2A

The ASPD includes built-in configurable fault protection for the internal gate drivers.

13.4 Low-Side Gate Driver

The DRLx low-side gate driver drives the gate of an external MOSFET or IGBT switch between the low-level power ground rail and high-level V_P supply rail. The DRLx output pin has sink and source output current capability of 2A. Each low-side gate driver is controlled by a microcontroller port signal with 4 configurable levels of propagation delay.

13.5 High-Side Gate Driver

The DRHx high-side gate driver drives the gate of an external MOSFET or IGBT switch between its low-level DRSx driver source rail and its high-level DRBx bootstrap rail. The DRSx pin can go up to 160V steady state (VM + 15V maximum). The DRHx output pin has sink and source output current capability of 2A.

The DRBx bootstrap pin can have a maximum operating voltage of 15V relative to the DRSx pin, and up to 175V steady state. The DRSx pin can have a maximum operating voltage of 10V relative to the VM pin. The DRSx pin is designed to tolerate momentary switching negative spikes down to -10V without affecting the DRHx output state. Each high-side gate driver is controlled by a microcontroller port signal with 4 configurable levels of propagation delay.

For bootstrapped high-side operation, connect an appropriate capacitor between DRBx and DRSx and a properly rated bootstrap diode from V_P to DRBx. To operate the DRHx output as a low-side gate driver, connect its DRBx pin to V_P and its DRSx pin to V_{SS}.

13.6 Power Drivers Control

All power drivers are initially disabled from power-on-reset. To enable the power drivers, the MCU must first enable the ASPD block. The gate drivers are controlled by the microcontroller ports and/or PWM signals with configurable delays as shown in Table 13-2 Power Driver Propagation Delay.

Refer to the PAC55XX Family User Guide and PAC5532 Device User Guide for additional information on power drivers control programming.

Table 13-2 Power Driver Propagation Delay

DRLx	DRHx
135ns	155ns

13.7 Gate Driver Fault Protection

The ASPD incorporates a configurable fault protection mechanism using protection signal from the Configurable Analog Front End (CAFE), designated as protection event 1 (PR) signal. The DRL0/DRL1/DRL2 drivers are designated as low-side group 1. The DRH3/DRH4/DRH5 gate drivers are designated as high-side group 1. The PR signal from the CAFE can be used to disable low-side group 1, high-side group 1, or both depending on the PR mask bit settings.

13.8 Electrical Characteristics

Table 13-3 Gate Driver Electrical Characteristics

(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Low-Side Gate Drivers (DRLx pins)						
$V_{OH;DRL}$	High-level output voltage	I_{DRLx} = -50mA	V_P-0.3			V
$V_{OL;DRL}$	Low-level output voltage	I_{DRLx} = 50mA			0.3	V
$I_{OHPK;DRL}$	Output high source current	10µs pulse		2		A
$I_{OLPK;DRL}$	Output low sink current	10µs pulse		2		A
High-Side Gate Drivers (DRHx, DRBx and DRSx pins)						
V_{DRS}	Level-shift driver source voltage range		-10		VM + 10	V
V_{DRB}	Bootstrap pin voltage range	Relative to V_{DRS}	10		20	V
		Relative to VSS			175	V
$V_{UVLO;DRB}$	Bootstrap UVLO threshold	V_{DRBx} rising	8.5			V
		Hysteresis		1		V
$I_{BS;DRB}$	Bootstrap supply current	Current from DRBx to DRSx		28		µA
$I_{OS;DRB}$	Offset supply current	Current from DRBx to ground		10		µA
$V_{OH;DRH}$	High-Level output voltage	I_{DRHx} = -50mA	V_{DRBx}-0.3			V
$V_{OL;DRH}$	Low-level output voltage	I_{DRHx} = 50mA			V_{DRSx}+0.3	V
$I_{OHPK;DRH}$	Output high source current	10µs pulse		2		A
$I_{OLPK;DRL}$	Output low sink current	10µs pulse		2		A
High-Side and Low-Side Gate Driver Propagation Delay						
t_{PD}	Propagation Delay[5]	Delay setting 00b	-50%	Delay + 0	50%	ns
		Delay setting 01b	-50%	Delay + 50	50%	ns
		Delay setting 10b	-50%	Delay + 100	50%	ns
		Delay setting 11b	-50%	Delay + 200	50%	ns

[5] Delay from Table 13-2 Power Driver Propagation Delay

14 SOC CONTROL SIGNALS

The MCU has access to the Analog Sub-system on the PAC5532 through certain digital peripherals. The functions that the MCU may access from the Analog Sub-System are:

- High-side and Low-side Gate Drivers
- SPI Interface for Analog Register Access
- ADC EMUX
- Analog Sub-system Interrupts

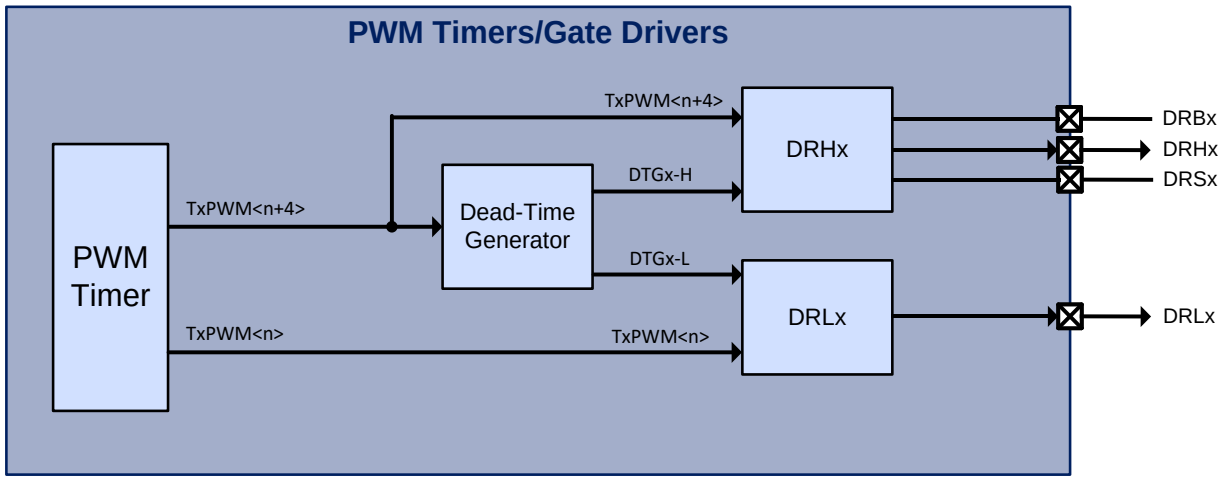
14.1 High-side and Low-Side Gate Drivers

The high-side and low-side gate drivers on the PAC5532 are controlled by PWM outputs of the timer peripherals on the MCU. The timer peripheral generates the PWM output. The PWM timer may be configured to generate a complementary PWM output (high-side and low-side gate drive signals) with hardware controlled dead-time.

These signals are sent to the gate drivers in the Analog Sub-system that create the high and low side gate drivers for the external inverter.

The user may choose to enable or not enable the DTG (Dead-time Generator). The diagram below shows the block diagram of the PWM timer, DTG and ASPD gate drivers.

Figure 14-1 SOC Signals for Gate Drivers



Each timer peripheral that drives the DTG and ASPD Gate Drivers has two PWM outputs that are connected to the gate drivers: TxPWM<n> and TxPWM<n+4>. If the Dead-Time Generator is disabled TxPWM<n> is connected to the DRLx gate driver output and TxPWM<n+4> is connected to the DRHx gate driver output.

If the DTG is enabled, the TxPWM<n+4> is used to generate the complementary high-side and low-side output (DTGx-H and DTGx-L). DTGx-H is connected to the DRHx output and DTGx-L is connected to the DRLx output.

The MCU allows flexibility the assignment of PWM outputs to ASPD gate drivers. The tables below shows which PWM outputs are available for each gate driver.

For applications that drive half-bridge or full-bridge topologies, the DTG will be enabled to allow a complementary output with dead-time insertion.

Table 14-1 PWM to ASPD Gate Driver Options (DTG Enabled)

Gate Driver	PWM Input Options
DRH3/ DRL0	TAPWM4 TBPWM4 TCPWM0 TCPWM4 TDPWM4
DRH4/ DRL1	TAPWM5 TBPWM5 TCPWM1 TCPWM5 TDPWM5
DRH5/ DRL0	TAPWM6 TBPWM6 TCPWM2 TCPWM6 TDPWM6

For applications that are not driving half-bridge topologies, the DTG is disabled and the PWM outputs are directly connected to the gate drivers.

Table 14-2 PWM to ASPD Gate Driver Options (DTG Disabled)

Gate Driver	PWM Input Options
DRH3	TAPWM4 TBPWM4 TCPWM0 TCPWM4 TDPWM4
DRH4	TAPWM5 TBPWM5 TCPWM1 TCPWM5 TDPWM5
DRH5	TAPWM6 TBPWM6 TCPWM2 TCPWM6 TDPWM6

DRL0	TAPWM0 TBPWM0 TCPWM0 TDPWM0
DRL1	TAPWM1 TBPWM1 TCPWM1 TDPWM1
DRL2	TAPWM2 TBPWM2 TCPWM2 TDPWM2

14.2 SPI SOC Bus

The SPI SOC bus is used for reading and writing registers in the Analog Sub-System. The PAC5532 allows both USARTA and USARTB to be used as the SPI master to read and write registers in the Analog Sub-System.

The table below shows which peripherals and which IO pins should be used for this interface.

Table 14-3 SPI SOC Bus Connections

SPI Signal	USART Signal	IO Pin
SCLK	USASCLK	PA3
	USBSCLK	PA3
MOSI	USAMOSI	PA4
	USBMOSI	PA4
MISO	USAMISO	PA5
	USBMISO	PA5
SS	USASS	PA6
	USBSS	PA6

14.3 ADC EMUX

The ADC EMUX is a write-only serial bus that the ADC DTSE uses for instructing the CAFE to perform MUX changes, activate Sample and Hold, etc.

The table below shows the MCU pins that are used by the ADC EMUX in the PAC5532.

Table 14-4 SPI SOC Bus Connections

EMUX Signal	Description	IO Pin
EMUXC	EMUX Clock	PA2
EMUXD	EMUX Data	PA1

14.4 Analog Interrupts

The Analog sub-system has two interrupts that it can generate for different conditions. The table below shows the two different interrupts, the interrupt conditions and the IO pin that the interrupts are connected to.

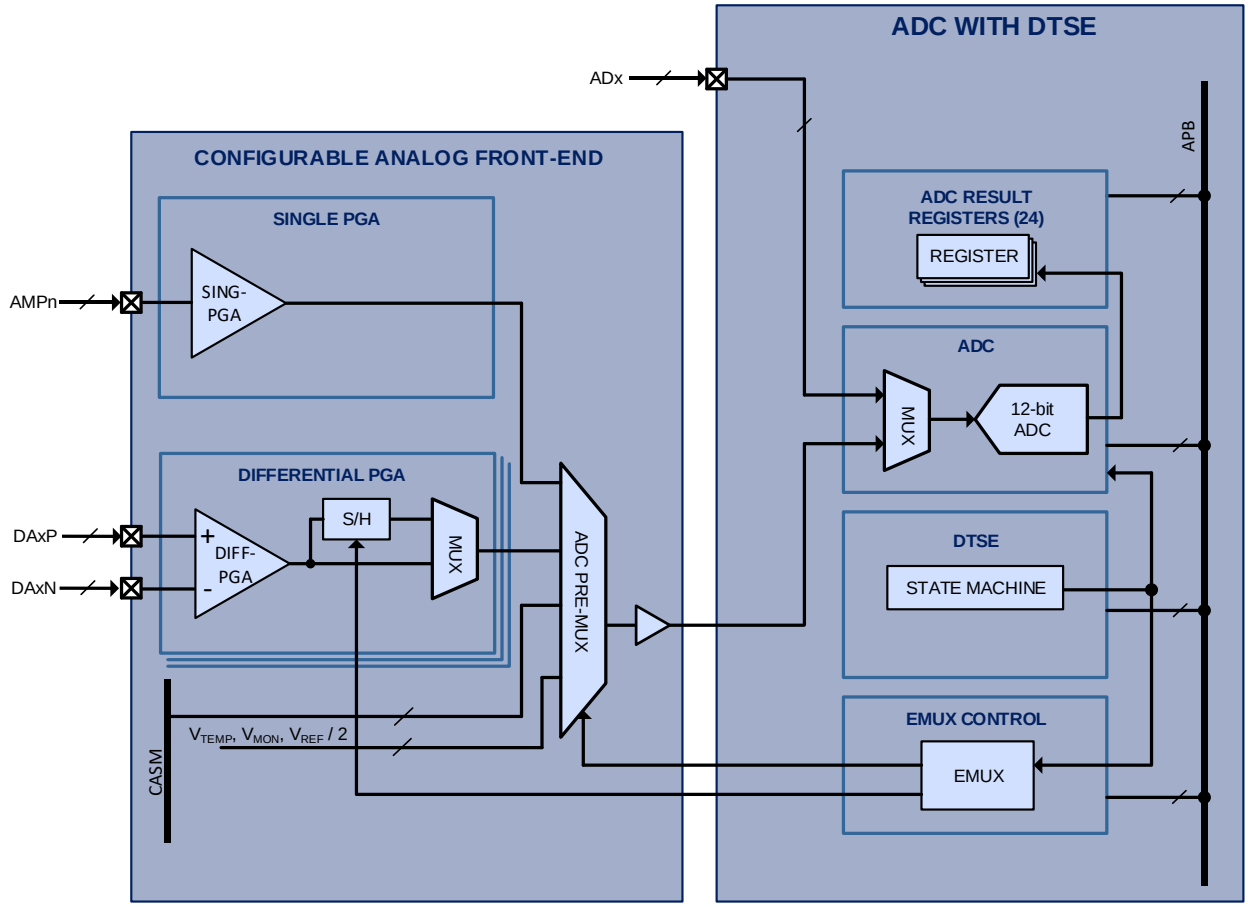
Table 14-5 Analog Interrupts

Analog IRQ	Interrupt Conditions	IO Pin
nIRQ1	HPCOMP/LPCOMP Comparator Protection for Over-current and Over-Voltage events	PA7
nIRQ2	BEMF and Special Mode Comparator, including phase to phase comparator, AIO6/AIO7/AIO8/AIO9 interrupt	PA0

15 ADC/DTSE

15.1 ADC Block Diagram

Figure 15-1 ADC with DTSE



15.2 Functional Description

15.2.1 ADC

The analog-to-digital converter (ADC) is a 12-bit successive approximation register (SAR) ADC with 400ns conversion time and up to 2.5 MSPS capability. The integrated analog multiplexer allows selection from up to 8 direct ADx inputs, and from up to 10 analog inputs signals in the Configurable Analog Front End (CAFE), including up to 3 differential input pairs as well as temperature and V_{REF} / 2.

The ADC contains a power down mode, and the user may configure the ADC to interrupt the MCU for the completion of a conversion when in manual mode. The ADC may be configured for either repeating or non-repeating conversions or conversion sequences.

15.2.2 ADC Conversion Timing

The ADC supports two modes for individual conversions: standard and enhanced[6]. The timing diagrams for each of these modes is shown below.

Figure 15-2 ADC Conversion Timing Diagram (standard)

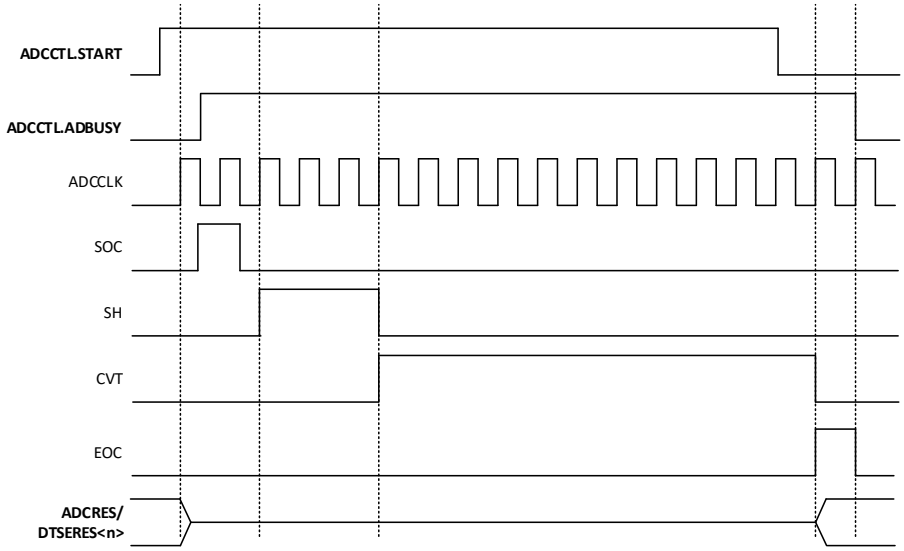
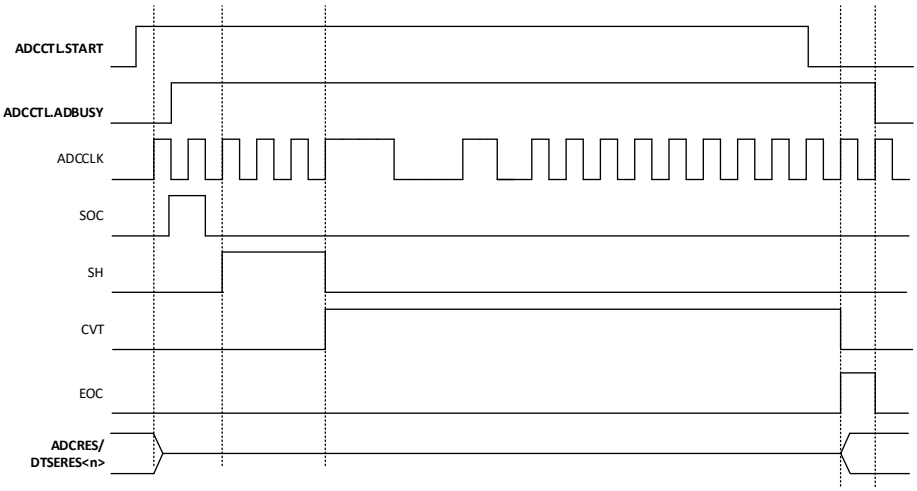


Figure 15-3 ADC Conversion Timing Diagram (enhanced)



[6] Enhanced ADC conversion mode is not available in VER1 of the PAC55XX MCU.

15.2.3 Dynamic Triggering and Sample Engine

The Dynamic Triggering and Sample Engine (DTSE) is a highly-configurable automatic sequencer that allows the user to configure automatic sampling of their application-specific analog signals without any interaction from the micro-controller core. The DTSE also contains a pseudo-DMA engine that copies each of up to 24 conversion results to dedicated memory space and can interrupt the MCU when complete.

The DTSE has up to 32 input triggers, from PWM Timers A, B, C and D for either the rising, falling or rising and falling PWM edges. The user may also force any trigger sequence by writing a register via firmware. The user can configure the DTSE to chain from 1 to 24 conversions to any PWM trigger.

The DTSE has a flexible interrupt structure that allows up to 24 interrupts to be configured at the completion of any individual conversion. The user may configure one of four different IRQ signals when generating an interrupt during sequence conversions. The IRQ may be generated at the end of a conversion sequence, or at the end of a series of conversions. The user may select one of four IRQs for conversions, and each may be assigned a different interrupt priority.

Each of the 24 conversions has dedicated results registers, so that the pseudo-DMA engine has dedicated storage for each of the conversion results.

15.2.4 EMUX Control

A dedicated low latency interface controllable by the DTSE or register control allows changing the ADC pre-multiplexer and asserting/de-asserting the S/H circuit in the Configurable Analog Front-End (CAFE), allowing back to back conversions of multiple analog inputs without microcontroller interaction.

For more information on the ADC and DTSE, see the PAC55XX Family User Guide.

15.3 Electrical Characteristics

Table 15-1 ADC and DTSE Electrical Characteristics

(V_P = 12V, V_{SYS} = 5V and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ADC						
f_{ADCCLK}	ADC conversion clock input				40	MHz
$f_{ADCCONV}$	ADC conversion time	Enhanced accuracy mode disabled			16	ADCCLK
		Enhanced accuracy mode enabled			20	ADCCLK
		f_{ADCCLK} = 40MHz; PCx, PDx, PEx, PFx, PGx pins			400	ns
		f_{ADCCLK} = 40MHz; AIO[9:0] pins, VER1 MCU			800	ns
		f_{ADCCLK} = 40MHz; AIO[9:0] pins, VER2 MCU			400	ns
t_{ADCSH}	ADC sample and hold time	f_{ADCCLK} = 40MHz			75	ns
					3	ADCCLK
C_{ADCIC}	ADC input capacitance	ADC MUX input		1		pF
	ADC resolution			12		bits
	ADC effective resolution		10.5			bits
	ADC differential non-linearity (DNL)	F_{ADCCLK} = 25MHz		±0.5		LSB
		F_{ADCCLK} = 40MHz		±0.75		LSB
	ADC integral non-linearity (INL)	F_{ADCCLK} = 25MHz		±0.5		LSB
		F_{ADCCLK} = 40MHz		±0.75		LSB
	ADC offset error[7]			5		LSB
	ADC gain error[7]			0.5		%
REFERENCE VOLTAGE						
V_{REFADC}	ADC reference input voltage	VREF = 2.5V		2.5		V
EMUX CLOCK SPEED						
$f_{EMUXCLK}$	EMUX engine clock input				50	MHz

[7] ADC offset and gain parameters are calculated post-calibration when using the ADCOFF and ADCGAIN calibration parameters from INFO2 FLASH.

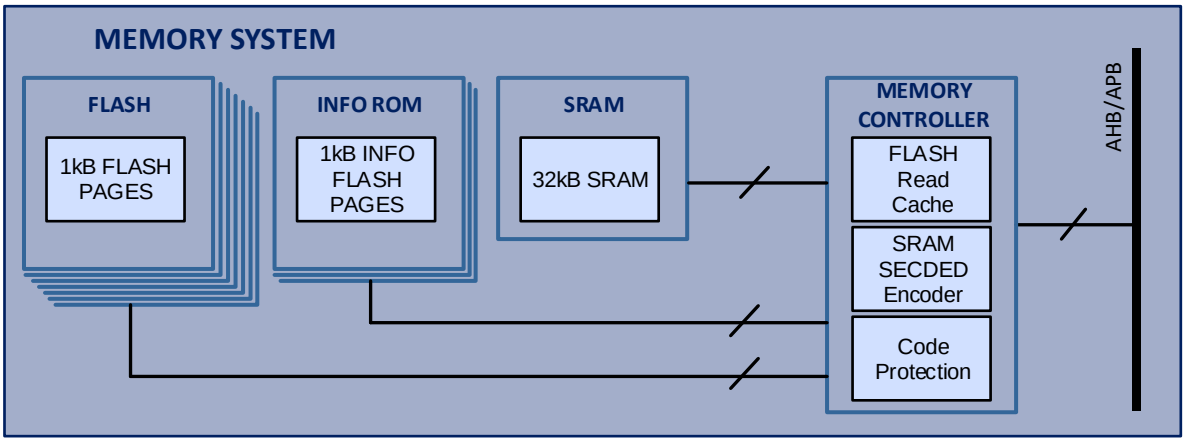
16 MEMORY SYSTEM

16.1 Features

- 128kB Embedded FLASH
  - 30,000 program/erase cycles
  - 10 years data retention
  - FLASH look-ahead buffer for optimizing access
- 1kB INFO-1 Embedded FLASH
- 1kB INFO-2 Embedded FLASH
  - Device ID, Unique ID, trim and manufacturing data
- 1kB INFO-3 Embedded FLASH
  - User data storage, configuration or parameter storage
  - Data or code
- 32kB SRAM
  - 150MHz access for code or data
  - SECDED for read/write operations
- User-configurable code protection

16.2 Memory System Block Diagram

Figure 16-1 Memory System



16.3 Functional Description

The PAC55XX has multiple banks of embedded FLASH memory, SRAM memory as well as peripheral control registers that are program-accessible in a flat memory map.

16.4 Program FLASH

The PAC55XX Memory Controller provides access to 128 1kB pages of main program FLASH for a total of 128kB of FLASH through the system AHB bus. Each page may be individually erased or written while the MCU is executing instructions from SRAM.

The PAC55XX Memory Controller provides a FLASH read buffer that optimizes access from the MCU to the FLASH memory. This look ahead buffer monitors the program execution and fetches instructions from FLASH before they are needed to optimize access to this memory.

16.5 INFO FLASH

The PAC55XX Memory Controller provides access to the INFO-1, INFO-2 and INFO-3 FLASH memories, which are each a single 1kB page for a total of 3kB of memory.

INFO-1 and INFO-2 are read-only memories that contains device-specific information such as the device ID, a unique ID, trimming and calibration data that may be used by programs executing on the PAC55XX.

INFO-3 is available to the user for data or program storage.

16.6 SRAM

The PAC55XX Memory Controller provides access to the 32kB SRAM for non-persistent data storage. The SRAM memory supports word (4B), half-word (2B) and byte addresses.

The PAC55XX Memory Controller can read or write data from RAM at a frequency of up to 150MHz. This memory can also be used for program execution when modifying the contents of FLASH or INFO-3 FLASH.

The PAC55XX Memory Controller also has an SECDED encoder, capable of detecting and correcting single-bit errors, and detecting double-bit errors. The user may read the status of the encoder, to see if a single-bit error has occurred. The user may also enable an interrupt upon detection of single-bit errors. Dual-bit errors can be configured to generate an interrupt in the PAC55XX.[8]

For more information on the PAC55XX Memory Controller, see the PAC55XX Family User Guide.

16.7 Code Protection

The PAC55XX allows user configurable code protection, to secure code from being read from the device.

[8] Note that when writing half-word or single bytes to SRAM, the memory controller must perform a read-modify write to memory to perform the SECDED calculation. These operations will take more than one clock cycle to perform for this reason.

There are four levels of code protection available as shown in the table below.

Table 16-1 Code Protection Level Description

LEVEL	NAME	FEATURES
0	UNLOCKED	• No restrictions
1	RW PROTECTION	• SWD/JTAG enabled • Programmable protection of up to 128 regions of FLASH • User-specified Read or Write protection per region
2	SWD DISABLED	• SWD/JTAG disabled • Programmable protection of up to 128 regions of FLASH • User-specified Read or Write protection per region
3	SWD/JTAG PERMANENTLY DISABLED	• SWD/JTAG disabled • Programmable protection of up to 128 regions of FLASH • User-specified Read or Write protection per region • No recovery

16.8 Electrical Characteristics

Table 16-2 Memory System Electrical Characteristics

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Embedded FLASH						
$t_{READ;FLASH}$	FLASH read time		40			ns
$t_{WRITE;FLASH}$	FLASH write time		30			µs
$t_{PERASE;FLASH}$	FLASH page erase time				2	ms
$t_{MERASE;FLASH}$	FLASH full erase time				10	ms
$N_{PERASE;FLASH}$	FLASH program/erase cycles		30k			cycles
$t_{DR;FLASH}$	FLASH data retention		10			Years
SRAM						
$t_{ACC;SRAM}$	SRAM access time	HCLK = 150MHz; Word (32-bits), aligned	6.67			ns
		HCLK = 150MHz; Half-word (16-bits), byte (8-bits), aligned	6.67			ns

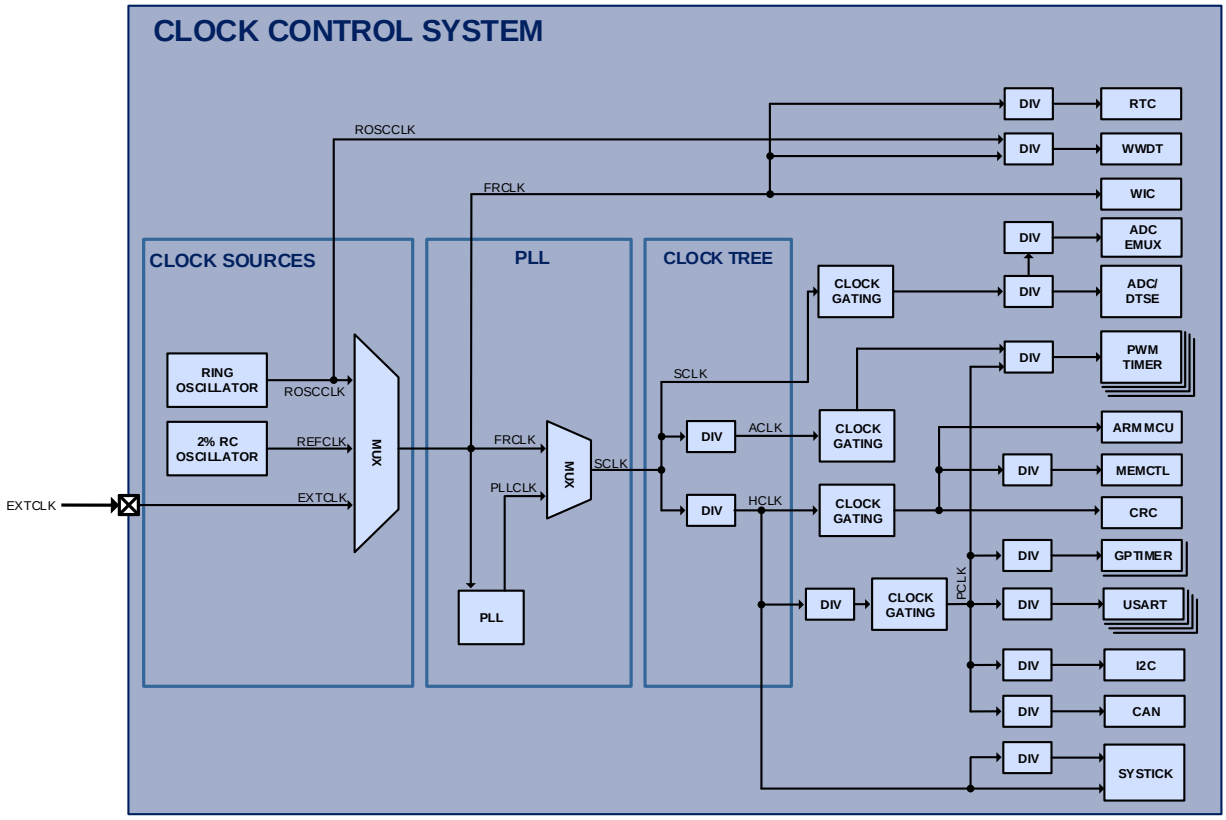
17 SYSTEM AND CLOCK CONTROL

17.1 Features

- 20MHz Ring Oscillator
- High accuracy 1.25% trimmed 4MHz RC oscillator
- External Clock Input for External Clocks up to 20MHz
- PLL with 1MHz to 50MHz input, 62.5MHz to 300MHz output
- Clock dividers for all system clocks
- Clock gating for power conservation during low-power operation

17.2 Block Diagram

Figure 17-1 Clock Control System



17.3 Clock Sources

17.3.1 Ring Oscillator

The Ring Oscillator (ROSC) is an integrated 20MHz clock oscillator that is the default system clock, and is available by default when the PAC55XX comes out of reset. The output of the ROSC is the ***ROSCCLK*** clock. The ***ROSCLK*** may be selected as the ***FRCLK*** clock and may supply the WWDT, for applications that need an independent clock source or need to continue to be clocked when the system is in a low-power mode.

The ROSC may be disabled by the user by a configuration register.

17.3.2 Reference Clock

The Reference Clock (***REFCLK***) is an integrated 1.25% trimmed 4MHz RC clock. This clock is suitable for many applications. This clock may be selected as the ***FRCLK*** and can be used as the input to the PLL and is used to derive the clock for the MMPM.

17.3.3 External Clock Input

The External Clock Input (EXTCLK) is a clock input available through the digital peripheral MUX, and allows the drive the clock system by a 50% duty cycle clock of up to 20MHz. This clock may be selected as FRCLK and can be used as the input the PLL (as long as the accuracy is better than +/- 2%).

17.4 PLL

The PAC55XX contains a Phase Lock Loop (PLL) that can generate very high clock frequencies up to 300MHz for the peripherals and timers in the device. The input to the PLL is the ***FRCLK*** and must be from the ***EXTCLK*** or ***REFCLK*** clock sources

The input to the PLL must be between 1MHz – 50MHz and the output can be configured to be from 62.5MHz to 300MHz. The user can configure the PLL to generate the desired clock output based on a set of configuration registers in the CCS. The output of the PLL is the ***PLLCLK*** clock. The user may configure a MUX to generate the SCLK clock from ***PLLCLK*** or from ***FRCLK***.

In addition to configuring the PLL output frequency, the PLL may be enabled, disabled and bypassed through a set of configuration registers in the CCS.

17.5 Clock Tree

The following are the system clocks available in the clock tree. See the section below to see which clocks are available for each of the digital peripherals in the system.

17.5.1 FRCLK

The free-running clock (***FRCLK***) is generated from one of the four clock sources (***ROSCCLK***, ***EXTCLK*** or ***REFCLK***). This clock may be used by the WWDT and the RTC, for configurations that turn off all other system clocks during low power operation.

The ***FRCLK*** or ***PLLCLK*** is selected via a MUX and the output becomes ***SCLK***.

17.5.2 SCLK

The System Clock (***SCLK***) generates two system clocks: ***ACLK*** and ***HCLK***. Each of these system clocks has their own 3b clock divider and is described below.

17.5.3 PCLK

The Peripheral Clock (***PCLK***) is used by most of the digital peripherals in the PAC55XX. This clock has a 3b clock divider and also has clock gating support, which allows this clock output to be disabled before the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

As shown above, most of the peripherals that use ***PCLK*** also have their own clock dividers so that this clock can be further divided down to meet the application's needs.

17.5.4 ACLK

The Auxiliary Clock (***ACLK***) may be optionally used by the PWM timer block in the PAC55XX in order to generate a very fast clock for PWM output to generate the best possible accuracy and edge generation.

This clock has a 3b clock divider and also has clock gating support, which disables this clock output when the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

As shown above, the ***ACLK*** is an optional input for just the PWM timer block in the PAC55XX.

17.5.5 HCLK

The AHB Clock (***HCLK***) is used by the Arm® Cortex®-M4 MCU and Memory Controller peripheral. This clock has a 3b divider and also has clock gating support, which allows this clock output to be disabled before the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

HCLK supplies PCLK with its clock source.

17.6 Electrical Characteristics

Table 17-1 CCS Electrical Characteristics

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Clock Tree (FRCLK, FCLK, PCLK, ACLK, HCLK)						
f_{FRCLK}	Free-running clock frequency				25	MHz
f_{SCLK}	System clock frequency				300	MHz
f_{PCLK}	Peripheral clock frequency	After divider			150	MHz
f_{ACLK}	Auxiliary clock frequency	After divider			300	MHz
f_{HCLK}	High-speed clock frequency	After divider			150	MHz
Internal Oscillators						
$f_{ROSCCLK}$	Ring oscillator frequency			20		MHz
$f_{TRIM;REFCLK}$	Trimmed RC oscillator frequency	T_A = 25°C	3.96	4	4.05	MHz
		T_A = -40°C to 125°C	3.92	4	4.08	
$f_{JITTER;REFCLK}$	Trimmed RC oscillator clock jitter	T_A = -40°C to 85°C		0.5		%
External Clock Input (EXTCLK)						
f_{EXTCLK}	External Clock Input Frequency				20	MHz
	External Clock Input Duty Cycle		40		60	%
$V_{IH;EXTCLK}$	External Clock Input high-level input voltage		2.1			V
$V_{IL;EXTCLK}$	External Clock Input low-level input voltage				0.825	V
PLL						
$f_{IN;PLL}$	PLL input frequency range		1		50	MHz
$f_{OUT;PLL}$	PLL output frequency range		62.5		300	MHz
$t_{SETTLE;PLL}$	PLL setting time	T_A = 25°C, PLL settled			15	µs
		T_A = 25°C, **PLLLOCK** = 1		200	500	µs
$t_{JITTER;PLL}$	PLL period jitter	RMS		25		ps
		Peak to peak			100	ps
	PLL duty cycle		40	50	60	%

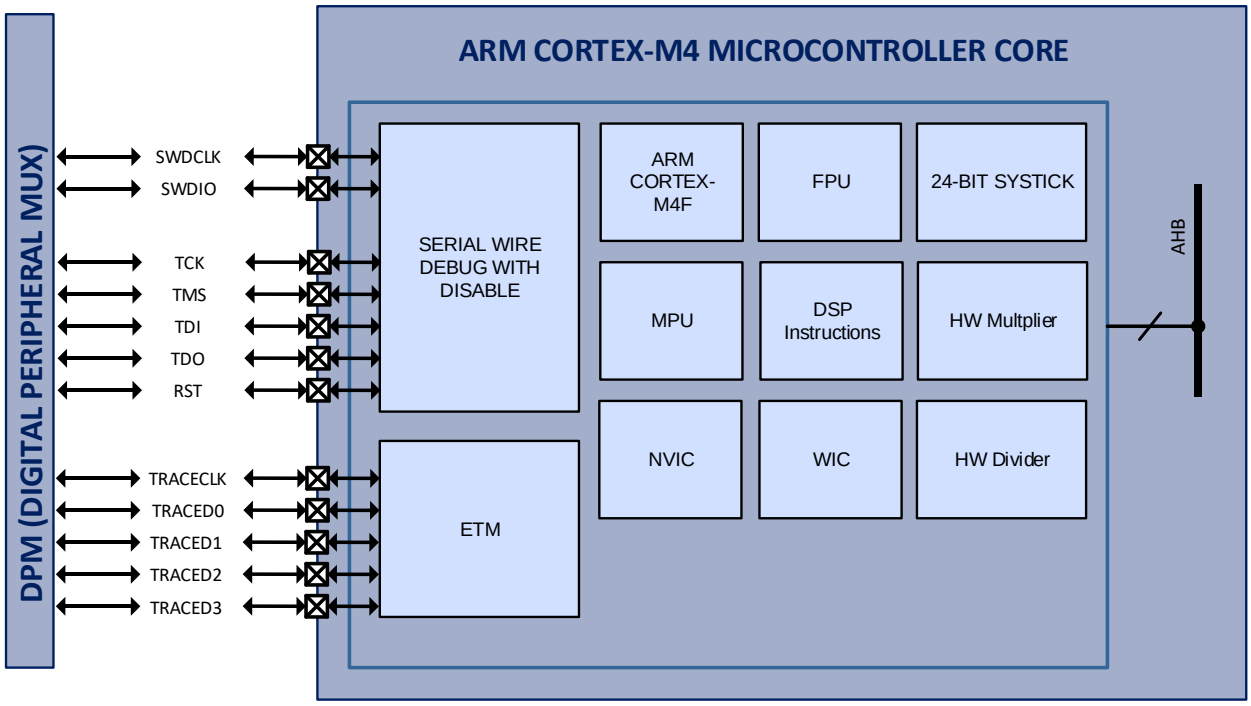
18 ARM® CORTEX®-M4F MCU CORE

18.1 Features

- Arm® Cortex®-M4F core
- SWD or JTAG Debug
- SWD/JTAG code security
- Embedded Trace Module (ETM) for instruction tracing
- Memory Protection Unit (MPU)
- Nested Vectored Interrupt Controller (NVIC) with 29 user interrupts and 8 levels of priority
- Floating Point Unit (FPU)
- Wakeup Interrupt Controller (WIC)
- 24-bit SysTick Count-down Timer
- Hardware Multiply and Divide Instructions

18.2 Block Diagram

Figure 18-1 Arm® Cortex®-M4F Microcontroller Core



18.3 Functional Description

The Arm® Cortex®-M4F microcontroller core is configured for little endian operation and includes hardware support for multiplication and division, DSP instructions as well as an IEEE754 single-precision Floating Point Unit (FPU).

The MCU also contains an 8-region Memory Protection Unit (MPU), as well as a Nested Vector Interrupt Controller (NVIC) that supports 29 user interrupts with 8 levels of priority. There is a 24-bit SysTick count-down timer.

The Arm® Cortex®-M4F supports sleep and deep sleep modes for low power operation. In sleep mode, the Arm® Cortex®-M4F is disabled. In deep sleep mode, the MCU as well as many peripherals are disabled. The Wakeup Interrupt Controller (WIC) can wake up the MCU when in deep sleep mode by using any GPIO interrupt, the Real-Time Clock (RTC) or Windowed Watchdog Timer (WWDT). The PAC55XX also supports clock gating to reduce power during deep sleep operation.

The debugger supports 4 breakpoint and 2 watch-point unit comparators using the SWD or JTAG protocols. The debug serial interfaces may be disabled to prevent memory access to the firmware during customer production.

For more information on the detailed operation of the Microcontroller Core in the PAC55XX, see the PAC55XX Family User Guide.

18.4 Application Typical Current Consumption

The MCU clock configuration and peripheral configuration have a large influence on the amount of load that the power supplies in the PAC55XX will have.

The table below shows a number of popular configurations and what the typical power consumption will be on the VSYS and VCORE power supplies in the PAC55XX.

Table 18-1 PAC55XX Application Typical Current Consumption[9]

CLOCK CONFIGURATION	MCU PERIPHERALS	MCU STATE	I_{VSYS}	I_{VCORE}	I_{VCC33}
CLKREF = 4MHz PLL Disabled ACLK=HCLK=PCLK=SCLK=MCLK = 16MHz ROSCCLK Enabled FRCLK MUX = ROSCCLK	All peripherals disabled	Halted	9.5mA	2.3mA	n/a
CLKREF = 4MHz PLLCLK = 30MHz ACLK=HCLK=PCLK=SCLK= 16MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	All peripherals disabled	Halted	10.5mA	3.5mA	n/a
CLKREF = 4MHz PLLCLK = 150MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	All peripherals disabled	Halted	20mA	13.5mA	n/a
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	All peripherals disabled	Halted	22mA	15mA	n/a
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF ADCCLK = 40MHz	ADC enabled (repeated conversions)	Halted	36mA	16mA	13.5mA
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = PLLCLK	All peripherals disabled	CPU Executes instructions from FLASH	8.5mA	2.2mA	n/a
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	Timer A enabled; TAPWM[7:0] enabled; Fs = 100kHz; 50% duty cycle	Halted	22mA	15mA	n/a

[9] Typical currents are an ambient temperature of 25ºC

18.5 Electrical Characteristics

Table 18-2 MCU and Clock Control System Electrical Characteristics

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{HCLK}	Microcontroller Clock				150	MHz
$I_{Q;VCORE}$	V_{CORE} quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			2	mA
		Hibernate Mode			0	mA
$I_{Q;VSYS}$	V_{SYS} quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			8	mA
		Hibernate Mode			15	µA
$I_{Q;VCCIO}$	VCCIO quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			0.15	mA
		Hibernate Mode			0	mA
$I_{Q;VCC33}$	VCC33 quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			0.4	mA
		Hibernate Mode			0	mA

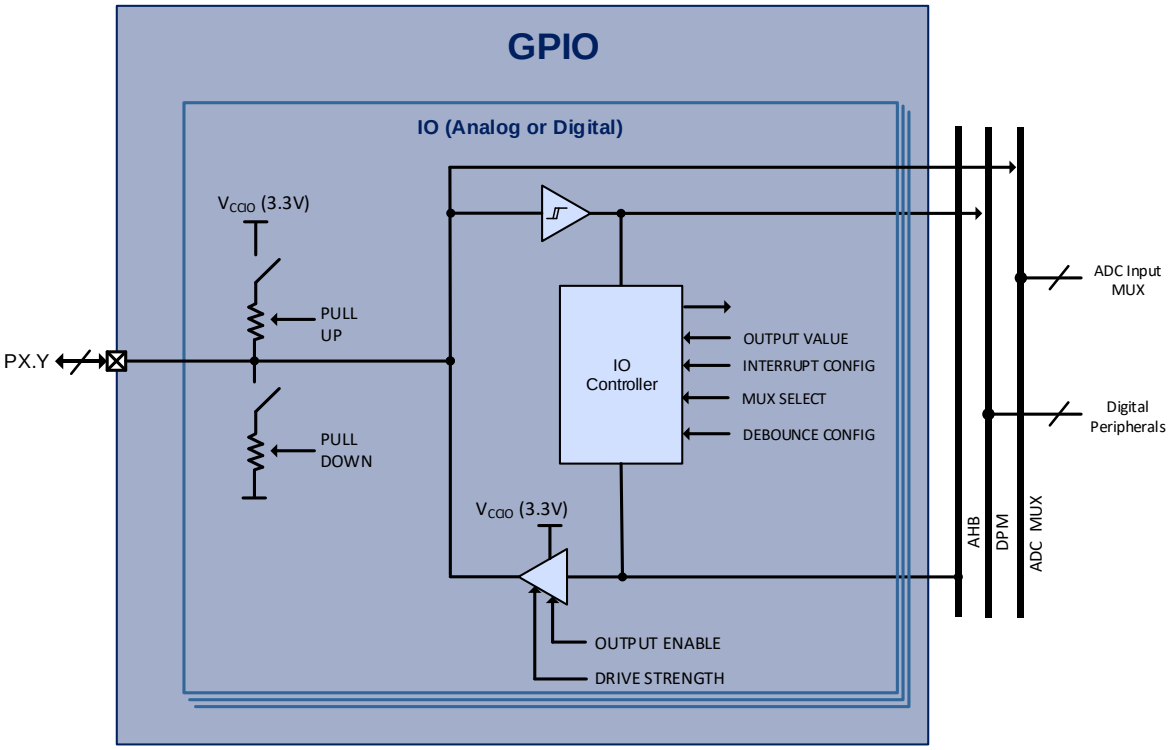
19 IO CONTROLLER

19.1 Features

- 3.3V Input/Output, 4.6V input tolerant
- Push-Pull Output, Open-Drain Output or High-Impedance Input for each IO
- Configurable Pull-up and Pull-down for each IO (60k)
- Configurable Drive Strength for each IO (up to 24mA)
- Analog Input for some IOs
- Edge-sensitive or level-sensitive interrupts
- Rising edge, falling edge or both edge interrupts
- Peripheral MUX allowing up to 8 peripheral selections for each IO
- Configurable De-bouncing Circuit for each IO

19.2 Block Diagram

Figure 19-1 IO Controller Block Diagram



19.3 Functional Description

The PAC55XX IO cells can be used for digital input/output and analog input for the ADC. All IOs are supplied by the V_{CCIO} (3.3V) power supply.

Each IO can be configured for digital push-pull output, open-drain output or high-impedance input. Each IO also has a configurable 60k weak pull-up or weak pull-down that can be enabled.

NOTE: Configuring both pull-up and pull-down at the same time may cause device damage and should be avoided.

Each IO has a configurable de-bouncing filter that can be enabled or disabled, to help filter out noise.

All IO have interrupt capability. Each pin can be configured for either level or edge sensitive interrupts, and can select between rising edge, falling edge and both edges for interrupts. Each pin has a separate interrupt enable and interrupt flag.

Some of the IO on the PAC55XX can be configured as an analog input to the ADC.

19.4 GPIO Current Injection

Under normal operation, there should not be current injected into the GPIOs on the device due to the GPIO voltage below ground or above the GPIO supply (VCCIO). Current will be injected into the GPIO when the GPIO pin voltage is less than -0.3V or when greater than GPIO supply + 0.3V.

In order provide a robust solution when this situation occurs, the PAC52XX family of products allows a small amount of injected current into the GPIO pins, to avoid excessive leakage or device damage.

For information on the GPIO current injection thresholds, see the absolute maximum parameters for this device.

Sustained operation with the GPIO pin voltage greater than the GPIO supply or when the GPIO pin voltage is less than -0.3V may result in reduced lifetime of the device. GPIO current injection should only be a temporary condition.

19.5 Peripheral MUX

The following table shows the available pin MUX options for this device. Note that if the pin is configured for analog input, the peripheral MUX is bypassed.

Table 19-1 PAC5532 Peripheral Pin MUX

PIN	Peripheral MUX Selection								ADC CH
	S0	S1	S2	S3	S4	S5	S6	S7	
PC4	GPIOC4	TBPWM4	TCPWM4	TCIDX	USBMOSI	USCSCLK	CANRXD	I2CSDL	
PC5	GPIOC5	TBPWM5	TCPWM5	TCPHA	USBMISO	USCSS	CANTXD	I2CSDA	
PD2	GPIOD2	TBPWM2	TCPWM2	TDPHB		USCMOSI			ADC2
PD1	GPIOD1	TBPWM1	TCPWM1	TDPHA		USCSS	CANRXD	EMUXC	ADC3
PD0	GPIOD0	TBPWM0	TCPWM0	TDIDX		USCCLK	CANTXD	EMUXD	ADC4
PE0	GPIOE0	TCPWM4	TDPWM0	TAIDX	TBIDX	USCCLK	I2CSCL	EMUXC	
PE1	GPIOE1	TCPWM5	TDPWM1	TAPHA	TBPHA	USCSS	I2CSDA	EMUXD	
PE2	GPIOE2	TCPWM6	TDPWM2	TAPHB	TBPHB	USCMOSI	CANRXD	EXTCLK	
PE3	GPIOE3	TCPWM7	TDPWM3	FRCLK		USCMISO	CANTXD		
PF0	GPIOF0	TCPWM0	TDPWM0	TCK/SWDCL	TBIDX	USBSCLK	TRACED2	TRACECLK	
PF1	GPIOF1	TCPWM1	TDPWM1	TMS/SWDIO	TBPHA	USBSS	TRACED1	TRACED0	
PF2	GPIOF2	TCPWM2	TDPWM2	TDI	TBPHB	USBMOSI	TRACED0	TRACED1	
PF3	GPIOF3	TCPWM3	TDPWM3	TDO	FRCLK	USBMISO	TRACECLK	TRACED2	
PF4	GPIOF4	TCPWM4	TDPWM4		TCIDX	USDSCLK	TRACED3	EMUXC	ADC4
PF5	GPIOF5	TCPWM5	TDPWM5		TCPHA	USDSS		EMUXD	ADC5
PF6	GPIOF6	TCPWM6	TDPWM6		TCPHB	USDMOSI	CANRXD	I2CSCL	ADC6

19.6 Electrical Characteristics

Table 19-2 IO Controller Electrical Characteristics

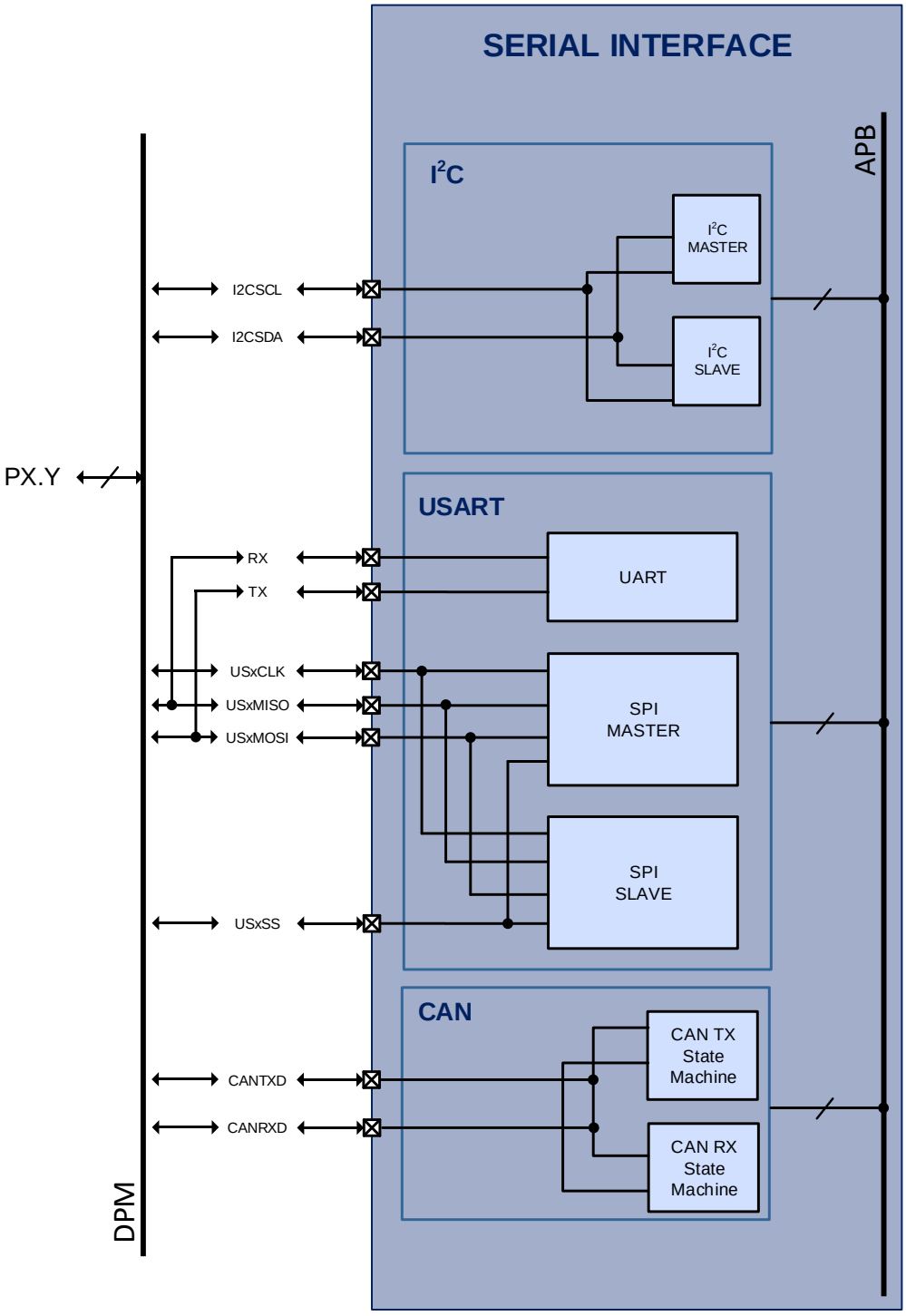
(V_{CCIO} = 3.3V, V_{SYS} = 5V, V_{CORE} = 1.2V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2.1			V
V_{IL}	Low-level input voltage					0.825	V
I_{OL}	Low-level output sink current (Limited by I_{VSYS} and I_{VCCIO})	V_{OL} = 0.4V	DS = 6mA	6			mA
			DS = 8mA	8			
			DS = 11mA	11			
			DS = 14mA	14			
			DS = 17mA	17			
			DS = 20mA	20			
			DS = 22mA	22			
			DS = 25mA	25			
I_{OH}	High-level output source current (Limited by I_{VSYS} and I_{VCCIO})	V_{OH} = 2.4V	DS = 6mA			-6	mA
			DS = 8mA			-8	
			DS = 11mA			-11	
			DS = 14mA			-14	
			DS = 17mA			-17	
			DS = 20mA			-20	
			DS = 22mA			-22	
			DS = 25mA			-25	
I_{IL}	Input leakage current			-2		0.95	µA
R_{PU}	Weak pull-up resistance	When pull-up enabled		45	60	100	kΩ
R_{PD}	Weak pull-down resistance	When pull-down enabled		45	60	115	kΩ
$I_{INJ;GPIO}$	GPIO pin current injection	V_{GPIO} < -0.3V or V_{GPIO} > VCCIO + 0.3V		-15		15	mA
$\Sigma I_{INJ;GPIO}$	Sum of all GPIO pin current injection	V_{GPIO} < -0.3V or V_{GPIO} > VCCIO + 0.3V		-40		40	mA

20 SERIAL INTERFACE

20.1 Block Diagram

Figure 20-1 Serial Interface Block Diagram



20.2 Functional Description

The PAC55XX has three types of serial interfaces: I²C, USART and CAN. The PAC55XX has one I²C controller, one CAN controller and up to 2 USARTs.

20.3 I²C Controller

The PAC55XX contains one I²C controller. This is a configurable APB peripheral and the clock input is PCLK. This peripheral has an input clock divider that can be used to generate various master clock frequencies. The I²C controller can support various modes of operation:

- I²C master operation
  - Standard (100kHz), full-speed (400kHz), fast (1MHz) or high-speed modes (3.4MHz)
  - Single and multi-master
  - Synchronization (multi-master)
  - Arbitration (multi-master)
  - 7-bit or 10-bit slave addressing
- I²C slave operation
  - Standard (100kHz), full-speed (400kHz), fast (1MHz) or high-speed modes (3.4MHz)
  - Clock stretching
  - 7-bit or 10-bit slave addressing

The I²C peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit operations.

20.4 USART

The PAC55XX contains up to 2 Universal Synchronous Receive Transmit (USART) peripherals. Each USART is a configurable APB bus client and input clock is PCLK. These peripherals have a configurable clock divider that can be used to produce various frequencies for the UART or SPI master peripheral.

The number of these peripherals depends on the peripheral MUX configuration. See the IO Controller section on information on how to configure the peripheral MUX with the USART peripheral.

The USART peripheral supports two main modes: SPI mode and UART mode.

20.4.1 USART SPI Mode

- Master or slave mode operation
- 8-bit, 16-bit or 32-bit word transfers
- Configurable clock polarity (active high or active low)
- Configurable data phase (setup/sample or sample/setup)
- Interrupts and status flags for RX and TX operations
- Support for up to 25MHz SPI clock

20.4.2 USART UART Mode

- 8-bit data
- Programmable data bit rate
- Maximum baud rate of 1Mbaud
- RX and TX FIFOs
- Configurable stop bits (1 or 2)
- Configurable parity: even, odd, none
  - Mark/space support for 9-bit addressing protocols
- Interrupt and status flags for RX and TX operations

20.5 CAN

The PAC55XX contains one Controller Area Network (CAN) peripheral. The CAN peripheral is a configurable APB bus client and input clock is PCLK. This peripheral has a configurable clock divider that can be used to produce various frequencies for the CAN peripheral.

- CAN 2.0B support
- 1Mb/s data rate
- 64-byte receive FIFO
- 16-byte transmit buffer
- Standard and extended frame support
- Arbitration
- Overload frame generated on FIFO overflow
- Normal and Listen Only modes supported
- Interrupt and status flags for RX and TX operations

20.6 Dynamic Characteristics

Table 20-1 Serial Interface Dynamic Characteristics

(V_{CCIO} = 3.3V, V_{SYS} = 5V, V_{CORE} = 1.2V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I²C						
f_{I2CCLK}	I²C input clock frequency	Standard mode (100kHz)	2.8			MHz
		Full-speed mode (400kHz)	2.8			MHz
		Fast mode (1MHz)	6.14			MHz
		High-speed mode (3.4MHz)	20.88			MHz
USART (UART mode)						
$f_{UARTCLK}$	USART input clock frequency				f_{PCLK}/16	MHz
$f_{UARTBAUD}$	UART baud rate	$f_{USARTCLK}$ = 7.1825MHz			1	Mbps
USART (SPI mode)						
f_{SPICLK}	USART input clock frequency	Master mode			50	MHz
		Slave mode			50	MHz
$f_{USARTSPICLK}$	USART SPI clock frequency	Master mode			25	MHz
		Slave mode			25	MHz
CAN						
f_{CANCLK}	CAN input clock frequency				50	MHz
f_{CANTX}	CAN transmit clock frequency				1	Mbps
f_{CANRX}	CAN receive clock frequency				1	Mbps

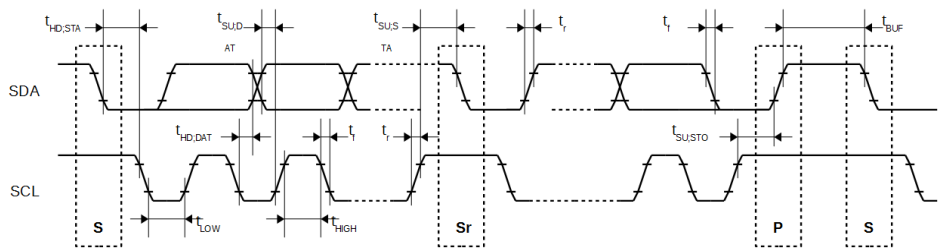
Table 20-2 I²C Dynamic Characteristics

(V_{CCIO} = 3.3V, V_{SYS} = 5V, V_{CORE} = 1.2V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Full-speed mode	0		400	kHz
		Fast mode	0		1	MHz
t_{LOW}	SCL clock low	Standard mode	4.7			µs
		Full-speed mode	1.3			µs
		Fast mode	0.5			µs
t_{HIGH}	SCL clock high	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{HD;STA}$		Standard mode	4.0			µs

	Hold time for a repeated START condition	Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard mode	0		3.45	µs
		Full-speed mode	0		0.9	µs
		Fast mode	0			µs
$t_{SU;DAT}$	Data setup time	Standard mode	250			ns
		Full-speed mode	100			ns
		Fast mode	50			ns
$t_{SU;STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Full-speed mode	1.3			µs
		Fast mode	0.5			µs
t_r	Rise time for SDA and SCL	Standard mode			1000	ns
		Full-speed mode	20		300	ns
		Fast mode			120	ns
t_f	Fall time for SDA and SCL	Standard mode			300	ns
		Full-speed mode			300	ns
		Fast mode			120	ns
C_b	Capacitive load for each bus line	Standard mode, full-speed mode			400	pF
		Fast mode			550	pF

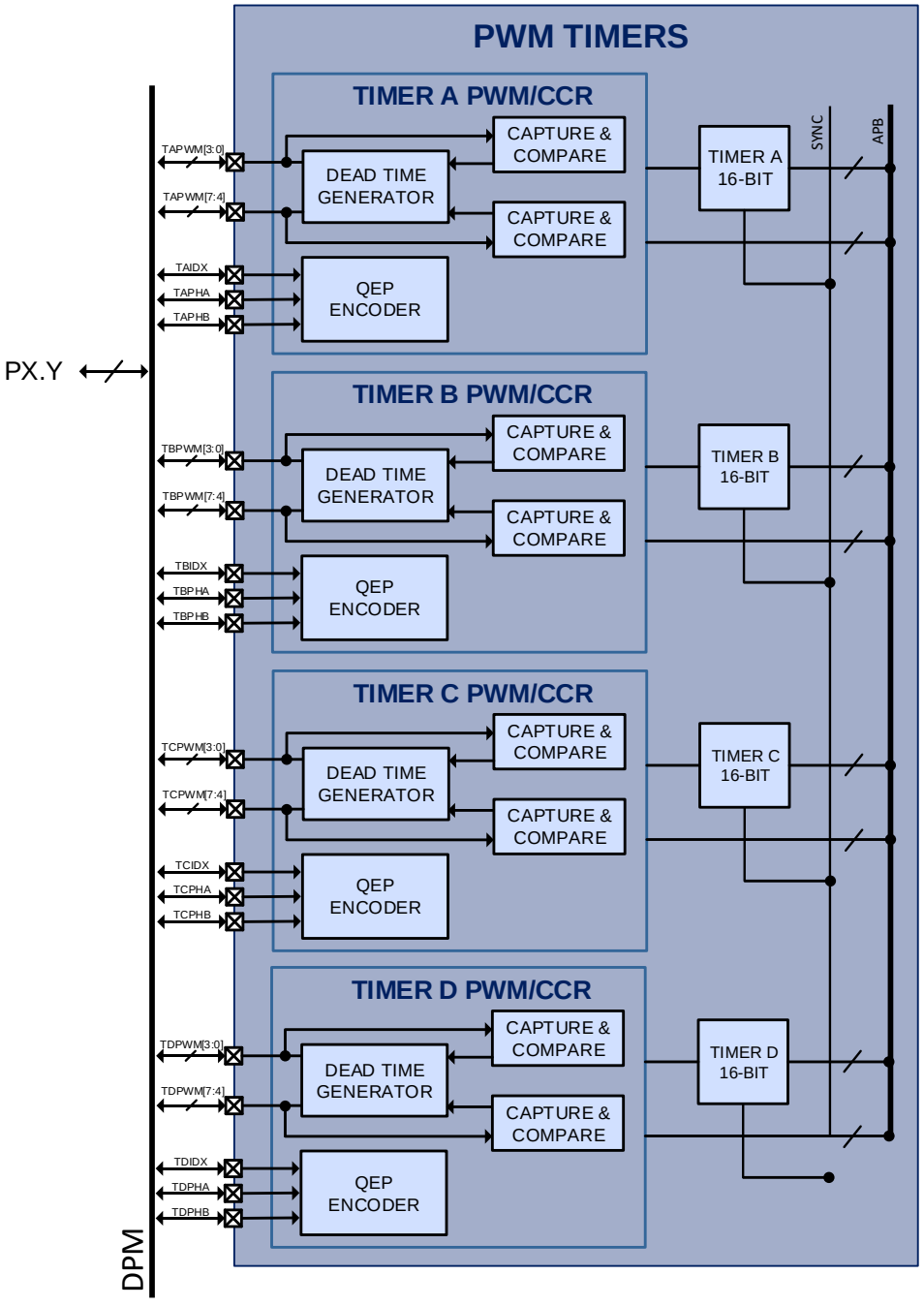
Figure 20-2 I²C Timing Diagram



21 PWM TIMERS

21.1 Block Diagram

Figure 21-1 PWM Timers Block Diagram



21.2 Timer Features

- Configurable input clock source: PCLK or ACLK
- Up to 300MHz input clock
- 3-bit Input clock divider
- Timer counting modes
  - up, up/down and asymmetric
- Timer latch modes
  - Latch when counter = 0
  - Latch when counter = period
  - Latch when CCR value written
  - Latch all CCR values at same time
- Base timer interrupts
- Single shot or auto-reload

21.2.1 CCR/PWM Timer

- PWM output or capture input
- CCR interrupt enable
- CCR interrupt skips
- SW force CCR interrupt
- CCR interrupt type
  - Rising, falling or both
- CCR compare latch modes
  - Latch when counter = 0
  - Latch when counter = period
  - Latch immediate
- CCR capture latch modes
  - Latch on rising edge
  - Latch on falling edge
  - Latch on both rising and falling edges
- Invert CCR output
- CCR phase delay for phase shifted drive topologies
- ADC trigger outputs
  - PWM rising edge or falling edge

21.2.2 Dead-time Generators (DTG)

- DTG enabled
- 12-bit rising edge delay
- 12-bit falling edge delay

21.2.3 QEP Decoder

- QEP encoder enabled
- Direction status
- Configurable Interrupts:
  - Phase A rising edge
  - Phase B rising edge
  - Index event
  - Counter wrap
- 4 different counting modes for best resolution, range and speed performance

22 GENERAL PURPOSE TIMERS

22.1 Block Diagram

Figure 22-1 SOC Bus Watchdog and Wake-up Timer

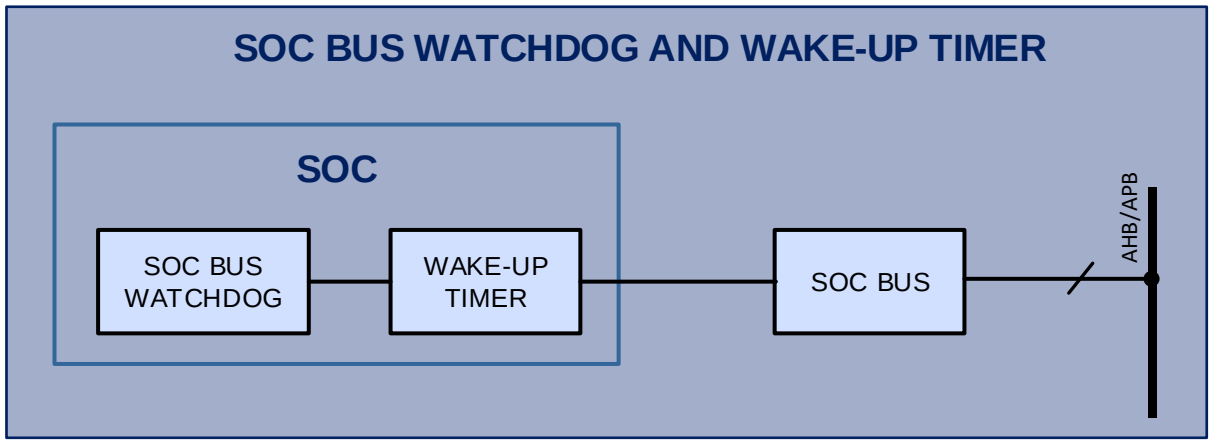
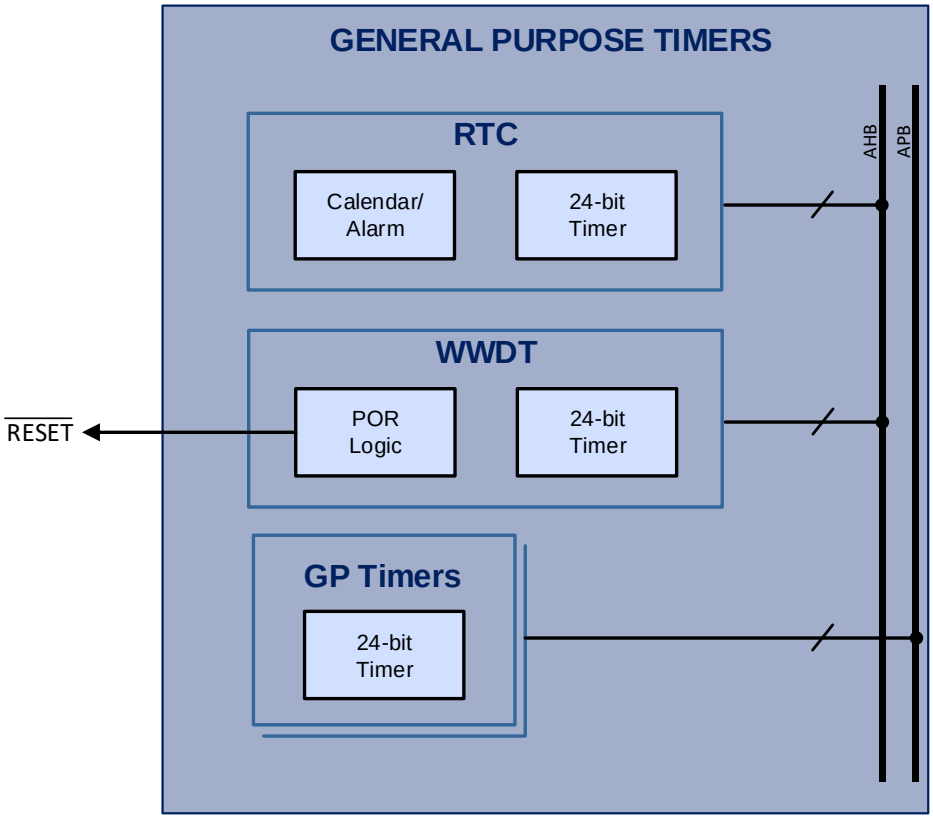


Figure 22-2 General Purpose Timers



22.2 Functional Description

22.2.1 SOC Bus Watchdog Timer

The SOC Bus Watchdog Timer is used to monitor internal SOC Bus communication. It will trigger a device reset if there is no SOC Bus communication to the AFE for 4s or 8s.

22.2.2 Wake-up Timer

The wake-up timer can be used for very low power hibernate and sleep modes to wake up the micro controller periodically. It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4, or 8s.

22.2.3 Real-time Clock with Calendar (RTC)

The 24-bit real-time clock with calendar (RTC) is an AHB bus client and may also be used to measure long time periods and periodic wake up from sleep mode.

The RTC uses FRCLK as its clock source and has a divider that can be configured up to a /65536 input clock divider. In order to count accurately, the input clock divider must be configured to generate a 1MHz clock to the RTC.

The RTC counts the time (seconds, minutes, hours, days) since enabled. It also allows the user to set a calendar date to set an alarm function that can be configured to generate an interrupt to the NVIC when it counts to that value.

22.2.4 Windowed Watchdog Timer (WWDT)

The 24-bit windowed watchdog timer (WWDT) is an AHB bus client and can be used for long time period measurements or periodic wake up from sleep mode. Its primary use is to reset the system via a POR if it is not reset at a certain periodic interval.

The WWDT can be configured to use FRCLK or ROSCCLK as its clock source and has a divider that be configured up to a /65536 input clock divider.

The WWDT can be configured to allow only a small window when it is valid to reset the timer, to maximize application security and catch any stray code operating on the MCU.

The WWDT may be configured to enable an interrupt for the MCU, and the timer can be disabled when unused to save energy for low power operations.

22.2.5 GP Timer (GPT)

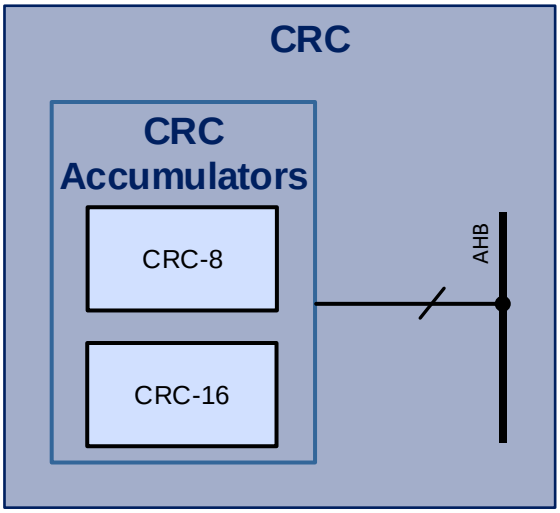
The PAC55XX contains two General Purpose (GP) Timers.

These timers are 24-bit timers and are both APB bus clients. These count-down timers use PCLK as their input clock and have a configurable divider of up to /32768. Each of the GPT can be configured to interrupt the MCU when they count down to 0.

23 CRC

23.1 Block Diagram

Figure 23-1 CRC Block Diagram



23.2 Functional Description

The CRC peripheral can perform CRC calculation on data through registers from the MCU to accelerate the calculation or validation of a CRC for communications protocols or data integrity checks.

The CRC peripheral allows the calculation of both CRC-8 and CRC-16 on data. The CRC peripheral also allows the user to specify a seed value, select the data input to be 8b or 32b and to reflect the final output for firmware efficiency.

The CRC peripheral is an AHB slave and has the following features:

- Polynomial selection via configuration register:
  - CCITT CRC-16 (0x1021)
  - IBM/ANSI CRC-16 (0x8005)
  - Dallas/Maxim CRC-8 (0x31)
- Input data width: 8b, 32b
- Reflect input
- Reflect output
- Specify seed value

24 THERMAL CHARACTERISTICS

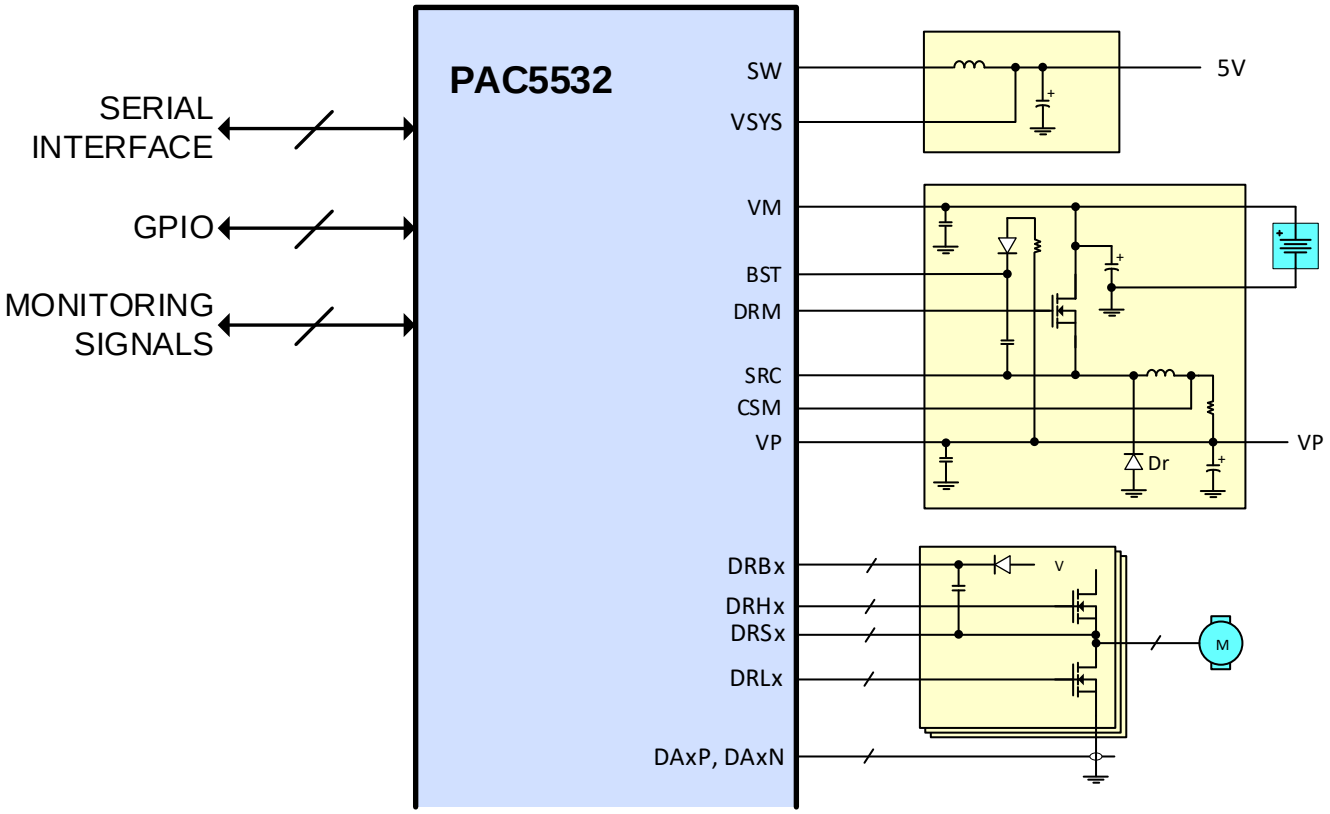
Table 24-1 Thermal Characteristics

PARAMETER	VALUE	UNIT
Operating ambient temperature range	-40 to 125	°C
Operating junction temperature range	-40 to 150	°C
Storage temperature range	-55 to 150	°C
Lead temperature (Soldering, 10 seconds)	300	°C
Junction-to-case thermal resistance (Θ_{JC})	2.897	°C/W
Junction-to-ambient thermal resistance (Θ_{JA})	23.36	°C/W

25 APPLICATION EXAMPLES

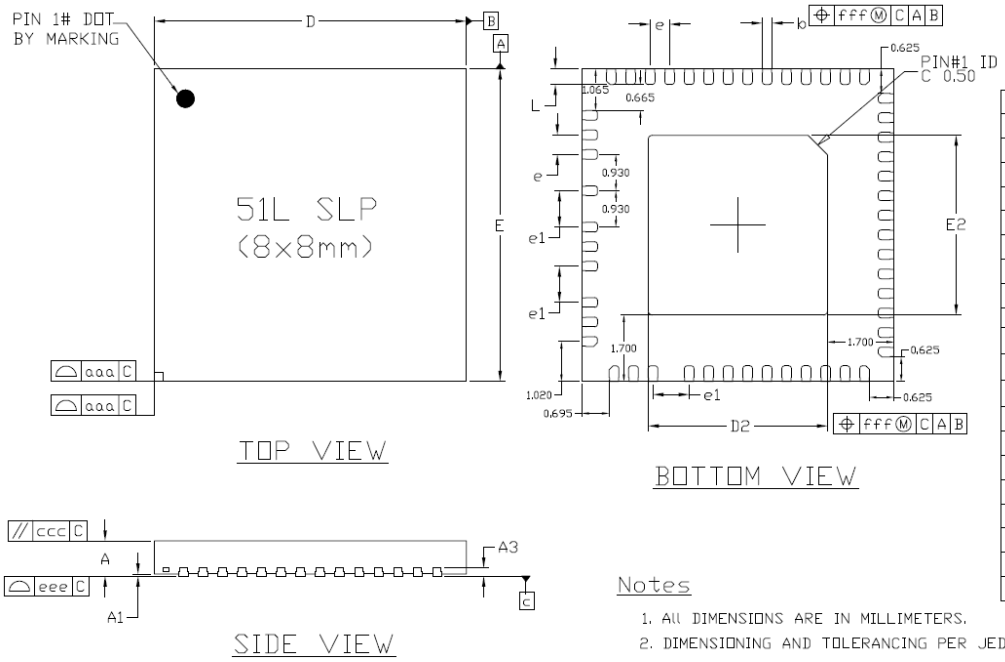
The following simplified diagram shows an example of a single-motor, low-voltage application using the PAC5532 device.

Figure 25-1 3-Phase Motor Using PAC5532 (Simplified Diagram)



26 PACKAGE OUTLINE AND DIMENSIONS

26.1 51L SLP Package Outline and Dimensions



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	---	0.050
A3	0.203 Ref.		
D	7.950	8.000	8.050
E	7.950	8.000	8.050
D2	4.550	4.600	4.650
E2	4.550	4.600	4.650
	---		
b	0.200	0.250	0.300
L	0.350	0.400	0.450
e	0.500 BSC		
e1	0.930 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		