PAC5532EVK1 User's Guide

Power Application Controllers

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OVERVIEW

Active-Semi's PAC5532EVK1 development platform is a complete hardware solution enabling users not only to evaluate the PAC5532 device, but also develop power applications revolving around this powerful and versatile ARM® Cortex®-M4F based microcontroller. The module contains a PAC5532 Power Application Controller® (MCU) and all the necessary circuitry to properly energize the MCU and its internal peripherals once power is applied.

To aid in the application development, the PAC5532EVK1 offers access to each and every one of the PAC5532 device's signals by means of a series of male header connectors.

The PAC5532EVK1 also contains access to an external USB to UART module enabling users to connect the evaluation module to a PC computer through a conventional Virtual Comm Port which can then be used in the communication efforts by taking advantage of the PAC5532's UART interface. Graphical User Interface (GUI) software suites can be employed to externally control particular application features.

Finally, the PAC5532EVK1 module gives access to the PAC5532's SWD and JTAG ports allowing users to both program the application into the device's FLASH memory, as well as debug the application in real time. The provided 4 pin connector is compatible with a decent variety of SWD based debugger/programmer modules, widely available. In parallel, a MIPI20 connector is made available that provides SWD, JTAG and TRACE functionality, greatly expanding the existent debugging capabilities.

Active-Semi's PAC5532EVK1 evaluation kit consists of the following:

- PAC5532EVK1 evaluation module
- PAC5532EVK1 User's Guide
- Schematics, BOM and Layout Drawings

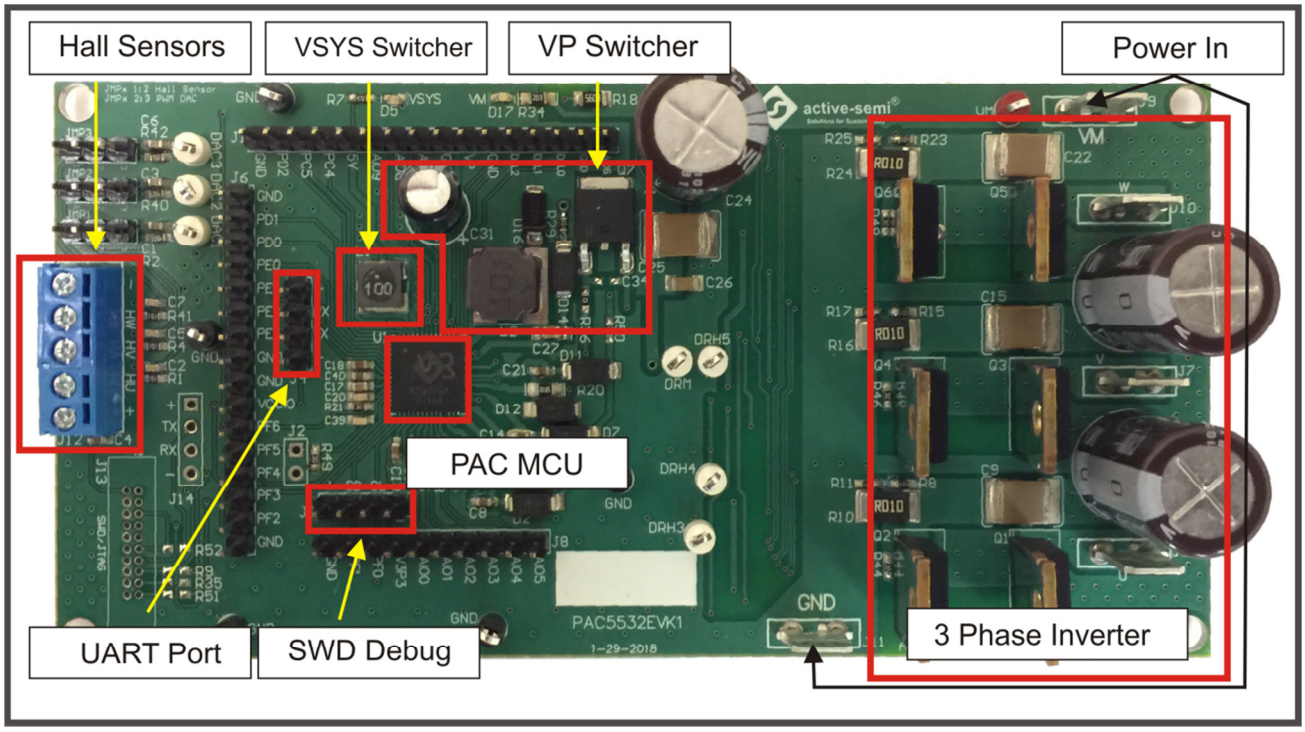


Figure 1: PAC5532EVK1 Block Diagram

Solution Benefits:

- Ideal for high voltage (up to 160V Abs Max) general purpose power applications and controllers
- Single-IC PAC5532 with configurable PWM outputs, ADC inputs, I2C, UART, SPI communication ports and GPIO.
- Gate driving for up to three half H Bridge (tri phase) inverter.
- Schematics, BOM, Layout drawings available

The following sections provide information about the hardware features of Active-Semi's PAC5532EVK1 turnkey solution.

PAC5532EVK1 RESOURCES

Pinout and Signal Connectivity

The following diagram shows the male header pinout for the PAC5532EVK1 evaluation module, as seen from above:

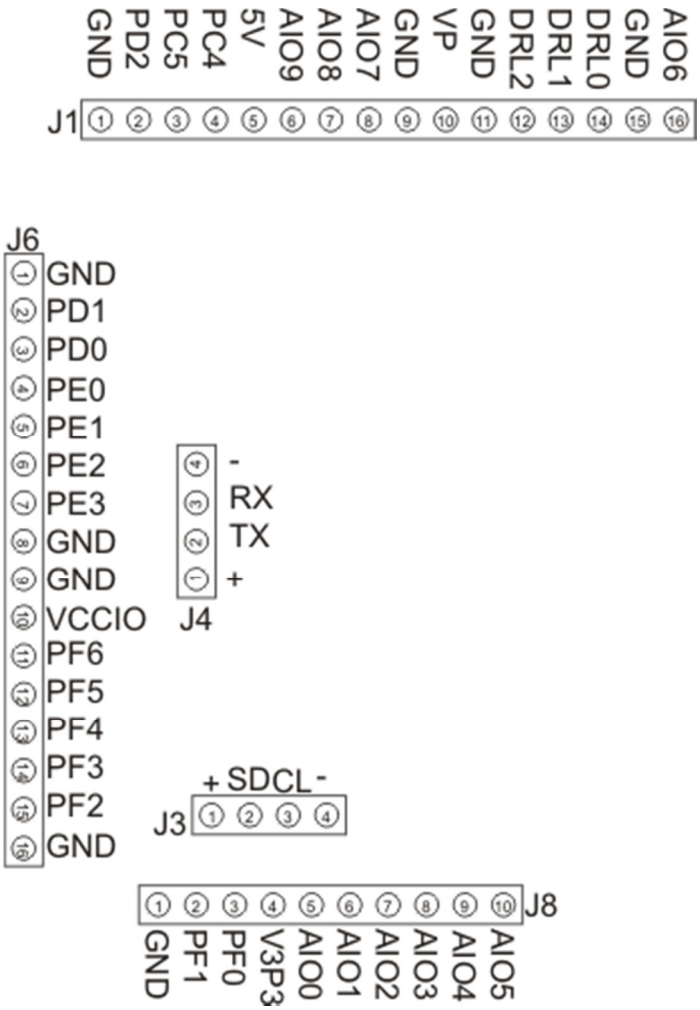


Figure 2 PAC5532EVK1 Headers and Test Stakes Pinout

Power Input

Power to the PAC5532EVK1 evaluation module can be applied to the VIN and GND spade connectors. Said applied power should not exceed 160V (Abs Max).

The PAC5532EVK1 is optimized to operate with voltages ranging from 25V to 120V Nominal (160V Abs Max). When the VIN input voltage goes above 25V, the system exits UVLO protection and all subsystems, including voltage regulators, analog front end and microcontroller, are enabled.

LED's

When an operational voltage is applied, LED D5 will light up. This is the LED which notifies that the VSYS (5V) rail is up and running. VP (12V gate drive), 3.3V (for analog circuitry) and 1.2V (for CPU core) regulators will also be operating at this point in time. The module is now ready for use.

The following table shows the available LEDs and their associated diagnostic function.

LED	Description
D5	VSYS (5V). Lights up when the PAC5532 device is successfully powered up by VIN.
D17	VIN. Lights up when VIN voltage is applied.

SWD Debugging

Connector J3 offers access to the PAC5532 SWD port lines.

J3 Pin	Terminal	Description
1	+	VCCIO (default is 3.3V)
2	SD	SWD Serial Data
3	CL	SWD Serial Clock
4	-	GND (System Ground)

JTAG Debugging

Connector J13 is a standard MIPI20 offering access to the JTAG port as well as single data line TRACE debug.

J13 Pins	Terminal	Description
1	VCC	VCC Power
2	SWDIO/TMS	Serial Wire Debug Data Input Output / JTAG Test Mode Select
3	GND	GND (System GND)
4	SWCLK/TCK	Serial Wire Debug Clock / JTAG Clock
5	GND	GND (System GND)
6	SWO/TDO	Serial Wire Debug Output / JTAG Data Output
7	NC	Not Connected
8	TDI	JTAG Data Input
9	GND	GND (System GND)
10	NC	Not Connected
11	GND	GND (System GND)
12	TRACE CLK	ETM Trace Clock
13	GND	GND (System GND)
14	TRACE DATA 0	ETM Trace Data 0
15	GND	GND (System GND)
16	TRACE DATA 1	ETM Trace Data 1
17	GND	GND (System GND)
18	TRACE DATA 2	ETM Trace Data 2
19	GND	GND (System GND)
20	TRACE DATA 3	ETM Trace Data 3

Serial Communications

Connector J4 offers access to the PAC5532 UART port lines.

J4 Pin	Terminal	Description
1	+	VCCIO (default is 3.3V)
2	TX	MCU Transmit Line (PE3)
3	RX	MCU Receive Line (PE2)
4	-	GND (System Ground)

Alternate Serial Communications

When enabled, connector J14 provides access to a secondary UART port lines.

J14 Pin	Terminal	Description
1	+	VCCIO (default is 3.3V)
2	TX	MCU Transmit Line (PF3 – requires 0 ohm resistor R41 to be populated)
3	RX	MCU Receive Line (PF2)
4	-	GND (System Ground)

Hall Sensor / DAC Interface

Connector J12 offers access to the PAC5532 resources on PORTD utilized for hall sensor based commutation. These resources can be alternatively utilized as PWM DAC outputs for in real time debugging. Jumpers JMP1/2/3 are used to select the preferred function.

NOTE: 2 pin shunts must be placed on the JMP1/2/3 in order for the respective PORTD resources to be made available.

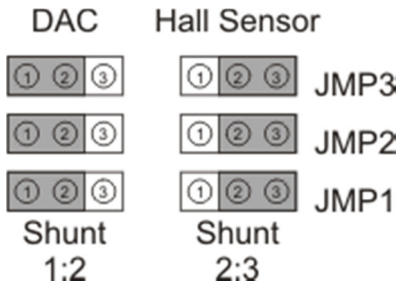


Figure 3 DAC / Hall Sensor Jumper Selection

Jumper JMP1/2/3	Description
1:2	Hall Sensor Functionality
2:3	DAC Functionality

NOTE: J12 functionality is only available when jumpers JMP1/2/3 have been shunted on the Hall Sensor respective position.

J12 Pin	Terminal	Description
1	+	VCCIO (default is 3.3V)
2	Hall Sensor U	PORTD0
3	Hall Sensor V	PORTD1
4	Hall Sensor W	PORTD2
5	GND	GND (System Ground)

NOTE: Test stakes DAC1/2/3 are only available when jumpers JMP1/2/3 have been shunted on the DAC respective position

Test Stake	Description
DAC 1	PORTD0
DAC 2	PORTD1
DAC 3	PORTD2

PAC5532EVK1 SETUP

The setup for the PAC5532EVK1 evaluation module requires up to four simple connections.

1. Connect the VIN power source via spade tab connectors VIN and GND. As VIN power is applied, the LED D17 will light up. Once VIN voltage goes above 25V, the PAC5532's Multi Mode Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D5 lighting up.
2. Connect the 3 Phase BLDC/PMSM motor via spade tab connectors PHASE U, PHASE V and PHASE W.
3. If Serial Communications are desired, connect the USB to UART module 4 pin connection to J4.
4. For debugging/programming, connect a suitable USB SWD module to J3 by using a standard 4 wire cable.

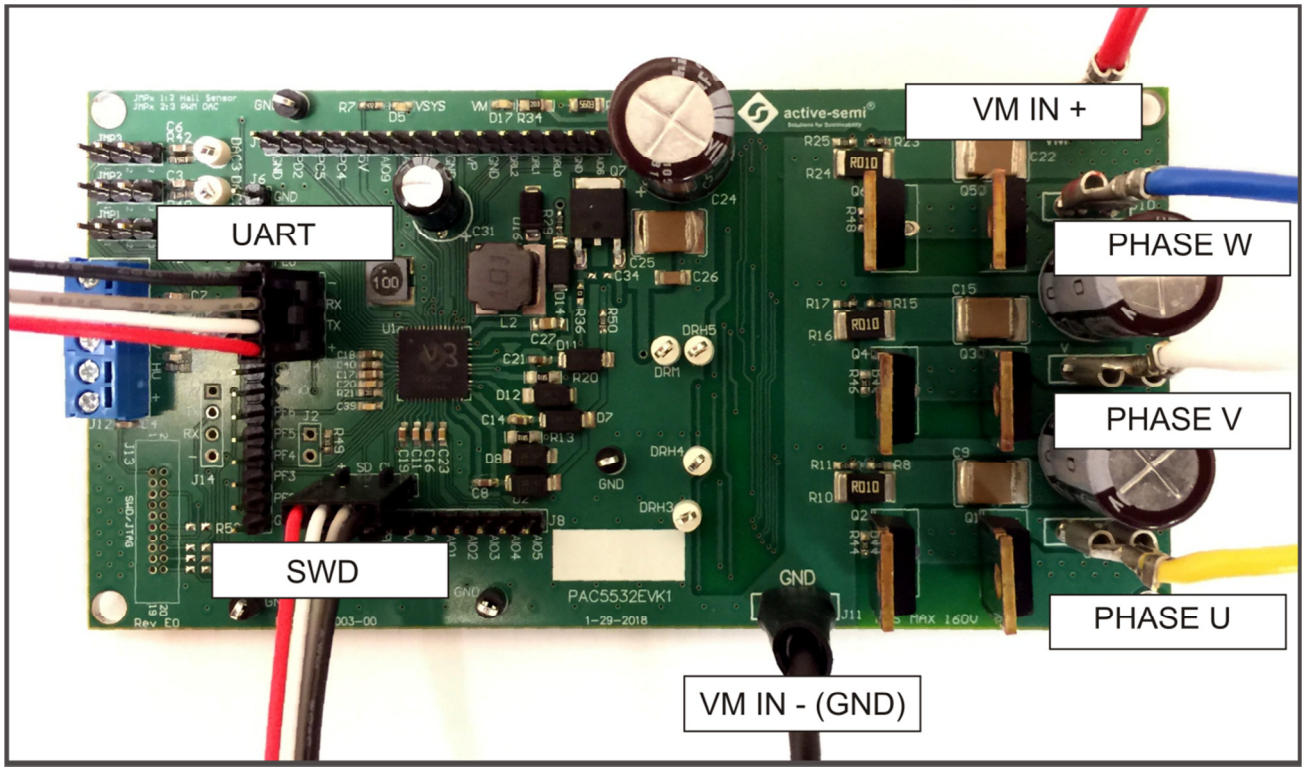


Figure 4: PAC5532EVK1 Evaluation Module Connections

POWER CONSIDERATIONS

Maximum Current and Voltage

The PAC5532EVK1 evaluation module was designed to operate with voltages in the 80V to 120V range. Transients can go to as high as 160V (Abs Max).

The recommended operating current is 10A RMS per phase. Higher currents could be achieved, albeit the user is responsible for applying different techniques to handle the increased thermal dissipation needs. Please see the “Increasing Output Power” section for more information on how to achieve higher current loading.

SENSE Resistors

The SENSE resistors utilized to digitize motor winding current will determine how much current the three phase inverter will be able to handle. The PAC5532EVK1 module ships with 0.01 Ohm 3W SENSE resistors. For higher current handling, a smaller SENSE resistor could be employed.

The equation utilized to compute maximum tri phase inverter leg current is:

$$I_{MAX} = \sqrt{\frac{P_{TOTAL}}{R_{SENSE}}}$$

Users are encouraged to modify SENSE resistor value according to their application. The following table *showcases different resistance values, maximum currents and suggested part numbers.*

Resistance (Ω)	Rated Power (W)	Maximum RMS Current (A)	Part Number
0.01	3	17.3	CRA2512-FZ-R010ELF
0.002	5	50	CSS2H-2512K-2L00F

NOTE: For increased current handling, adding thermal heat sinking to the power FETs must be considered.

Power FETs

The PAC5532EVK1 ships with six IRFB4227PBF TO-220 Power FETs. These power switches are rated at 200V and 130A. RDSON is about 0.020 Ohms. In order to obtain the maximum performance out of these components, some form of heat sinking is required. The evaluation module ships without a heat radiation device. The appendix offers guidelines the measurements users can employ to fabricate their own version of a simple metal heat plate.

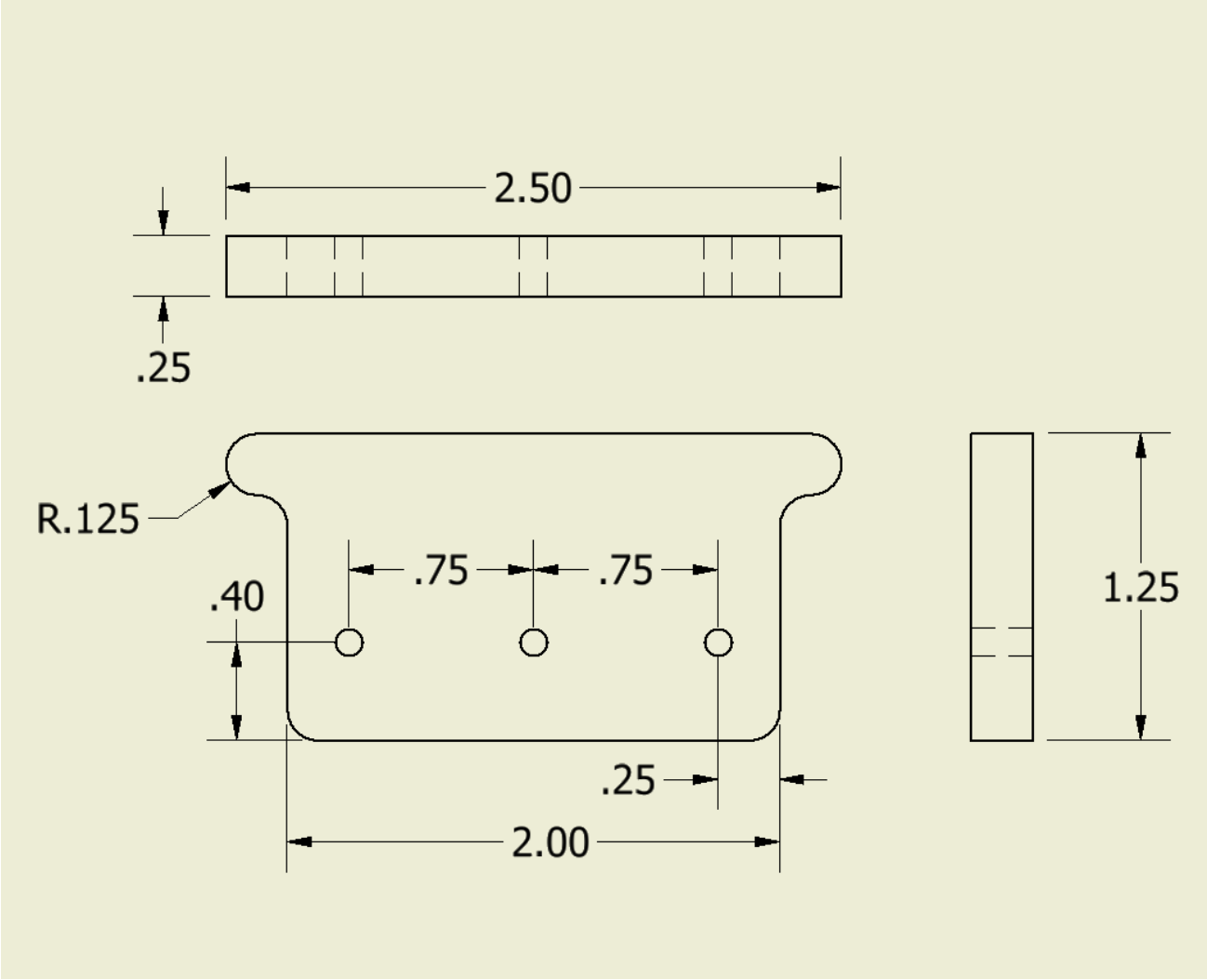
Users are also encouraged to modify the evaluation module by exchanging power switches with other components offering better thermal performance. Power FETs designed with a lower RDSON would tend to require less heat sinking. Traditionally, such FETs would have a lower maximum voltage, but for applications requiring smaller voltages, this may be an acceptable option.

INCREASING OUTPUT POWER (APPENDIX)

In this section we provide different techniques which must be employed when wanting to drive higher then 10A per phase loads. As depicted in previous sections, the user will be responsible for selecting a proper SENSE resistor, suitable power FET, adding heat sinking and in some cases, some extra clamping.

Suggested Heat Sink Profile

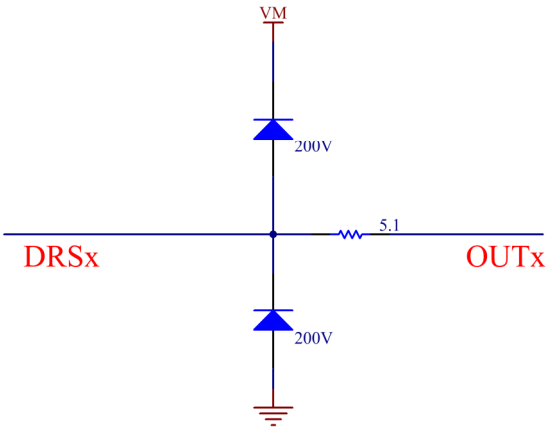
The following drawing offers guidelines for a shape which could be utilized to fabricate a heat radiator. This heat sinking metal plate is intended to be bolted onto the power FETs through the usage of gap pads and insulating washers.



Clamping Mechanisms

When current load increases, destructive voltage transients can be observed. These transients are usually prevalent during dead time, when current must find an asynchronous path (e.g. FET body diodes) to continue its flow. Controlling these transients is of utmost importance to protect both the power switches as well as the PAC5532 pre drive power stage block.

Adding DRS Clamps



The PAC5532EVK1 evaluation module already incorporates a series of clamps put in place to protect the DRSx terminal from negative transients at the phase outputs. However, under high current scenarios, it is plausible to see large positive transients. It is recommended to place a similar diode from DRS to VM in order to clamp the PHASE output to VM.