PAC5556EVK1

Power Application Controllers

PAC5556EVK1 User's Guide

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OVERVIEW

Active-Semi's PAC5556EVK1 development platform is a complete hardware solution enabling users not only to evaluate the PAC5556 device, but also develop power applications revolving around this powerful and versatile ARM® Cortex®-M4F based microcontroller. The module contains a PAC5556 Power Application Controller® (MCU) and all the necessary circuitry to properly energize the MCU and its internal peripherals once power is applied.

To aid in the application development, the PAC5556EVK1 offers access to each and every one of the PAC5556 device's signals by means of a series of male header connectors.

The PAC5556EVK1 also contains access to an external USB to UART module enabling users to connect the evaluation module to a PC computer through a conventional Virtual COM Port which can then be used in the communication efforts by taking advantage of the PAC5556's UART interface. Graphical User Interface (GUI) software suites can be employed to externally control particular application features.

Finally, the PAC5556EVK1 module gives access to the PAC5556's SWD and JTAG ports allowing users to both program the application into the device's FLASH memory, as well as debug the application in real time. The provided 4 pin connector is compatible with a decent variety of SWD based debugger/programmer modules, widely available. In parallel, a MIPI20 connector is made available that provides SWD, JTAG and TRACE functionality, greatly expanding the existent debugging capabilities.

Active-Semi's PAC5556EVK1 evaluation kit consists of the following:

- PAC5556EVK1 evaluation module
- PAC5556EVK1 User's Guide
- Schematics, BOM and Layout Drawings

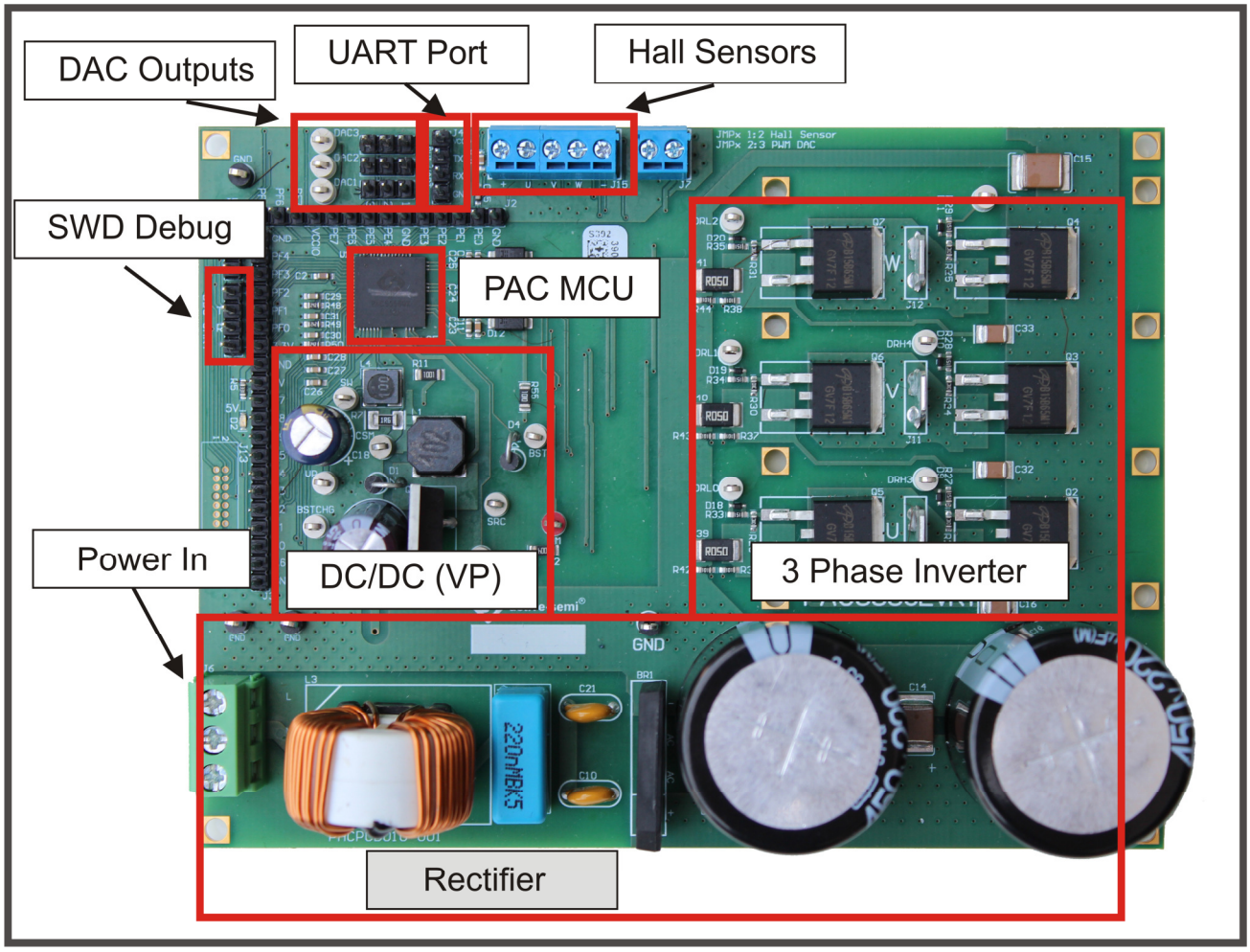

Figure 1: PAC5556EVK1 Block Diagram

Solution Benefits:

- Ideal for High Voltage (110/220 VAC nominal, up to 450VDC Abs Max) general purpose power applications and controllers
- Single-IC PAC5556 with PWM outputs, ADC inputs, I2C, UART, SPI and GPIO.
- Gate driving for up to three half H Bridge (tri phase) inverter.
- Three PWM DAC's for real time debugging.
- Hall Sensor Interface for sensored applications.
- Current and Voltage sensing for sensorless applications.
- Schematics, BOM, Layout drawings available

The following sections provide information about the hardware features of Active-Semi's PAC5556EVK1 turnkey solution.

PAC5556EVK1 RESOURCES

Pinout and Signal Connectivity

The following diagram shows the male header pinout for the PAC5556EVK1 evaluation module, as seen from above:

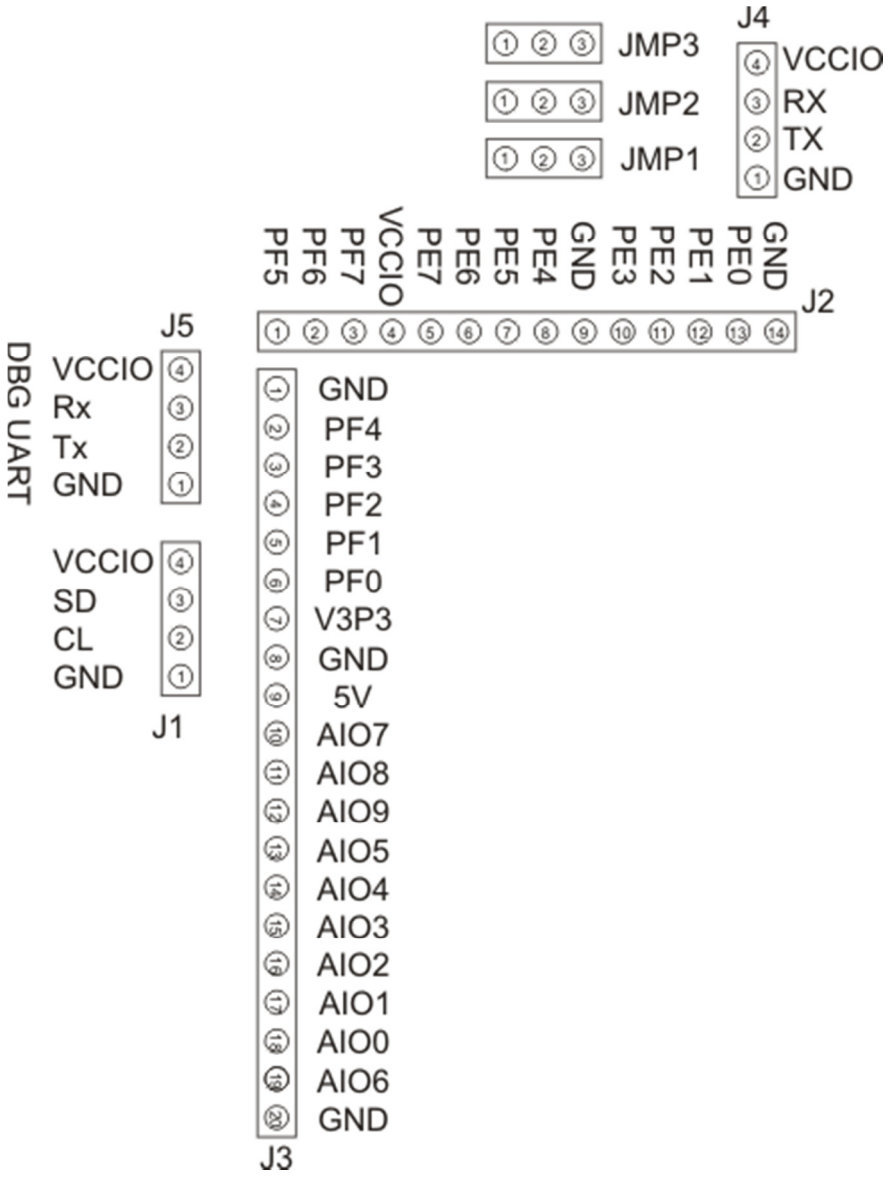

Figure 2 PAC5556EVK1 Headers and Test Stakes Pinout

Power Input

Power to the PAC5556EVK1 evaluation module can be applied to the J6 three position terminal block connector. Power to the PAC5556EVK1 evaluation module should not exceed 240 VAC (450 VDC Abs Max).

The PAC5556EVK1 is optimized to operate with voltages ranging from 110 VAC to 220 VAC Nominal. When the rectified input voltage (VM) goes above around 85 VDC, the system's High Voltage Buck Converter is powered up and the device exits UVLO protection. At this time all subsystems, including internal voltage regulators, analog front end and microcontroller, are enabled.

LED's

When an operational voltage is applied, LED D2 will light up. This is the LED which notifies VSYS (5V) rail is up and running. VP (15V gate drive), 3.3V (for analog circuitry) and 1.2V (for CPU core) regulators will also be operating at this point in time. Module is ready for use.

The following table shows the provided LED and its associated diagnostic function.

LED	Description
D2	VSYS (5V). Light up when the PAC5556 device is successfully powered up by VM.

SWD Debugging

Connector J1 offers access to the PAC5556 SWD port lines.

J1 Pin	Terminal	Description
1	+	VCCIO (3.3V)
2	SD	SWD Serial Data (PF1)
3	CL	SWD Serial Clock (PF0)
4	-	GND (System Ground)

JTAG Debugging

Connector J13 is a standard MIPI20 offering access to the JTAG port as well as single data line TRACE debug.

J13 Pins	Terminal	Description
1	VCC	VCC Power
2	SWDIO/TMS	Serial Wire Debug Data Input Output / JTAG Test Mode Select
3	GND	GND (System GND)
4	SWCLK/TCK	Serial Wire Debug Clock / JTAG Clock
5	GND	GND (System GND)
6	SWO/TDO	Serial Wire Debug Output / JTAG Data Output
7	NC	Not Connected
8	TDI	JTAG Data Input
9	GND	GND (System GND)
10	NC	Not Connected
11	GND	GND (System GND)
12	TRACE CLK	ETM Trace Clock
13	GND	GND (System GND)
14	TRACE DATA 0	ETM Trace Data 0
15	GND	GND (System GND)
16	TRACE DATA 1	ETM Trace Data 1
17	GND	GND (System GND)
18	TRACE DATA 2	ETM Trace Data 2
19	GND	GND (System GND)
20	TRACE DATA 3	ETM Trace Data 3

Serial Communications

Connector J4 offers access to the PAC5556 UART port lines.

J4 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	RX	MCU Receive Line (PE3)
3	TX	MCU Transmit Line (PE2)
4	-	GND (System Ground)

Alternate Serial Communications

When enabled, connector J5 provides access to a secondary UART port lines.

J5 Pin	Terminal	Description
1	+	VCCIO (3.3V)
2	TX	MCU Transmit Line (PF3 – requires 0 ohm resistor R3 to be populated)
3	RX	MCU Receive Line (PF2)
4	-	GND (System Ground)

Hall Sensor / DAC Interface

Terminal Block J15 offers access to the PAC5556 resources on PORTD utilized for hall sensor based commutation. These resources can be alternatively utilized as PWM DAC outputs for in real time debugging. Jumpers JMP1/2/3 are used to select the preferred function.

NOTE: 2 pin shunts must be placed on the JMP1/2/3 in order for the respective PORTD resources to be made available.

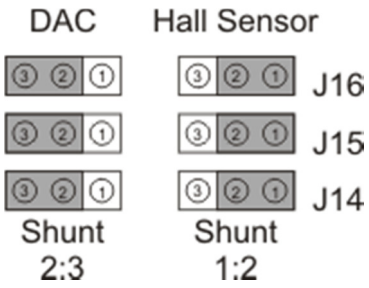

Figure 3 DAC / Hall Sensor Jumper Selection

Jumper JMP1/2/3	Description
1:2	Hall Sensor Functionality
2:3	DAC Functionality

NOTE: J15 functionality is only available when jumpers JMP1/2/3 have been shunted on the Hall Sensor respective position.

J15 Pin	Terminal	Description
1	+	VCCIO (3.3V)
2	Hall Sensor U	PORTE4
3	Hall Sensor V	PORTE5
4	Hall Sensor W	PORTE6
5	GND	GND (System Ground)

NOTE: Test stakes DAC1/2/3 are only available when jumpers JMP1/2/3 have been shunted on the DAC respective position

Test Stake	Description
DAC 1	PORTE4
DAC 2	PORTE5
DAC 3	PORTE6

PAC5556EVK1 SETUP

The setup for the PAC5556EVK1 evaluation module requires up to four simple connections.

1. Connect the 3 Phase BLDC/PMSM motor via space tab connectors PHASE U, PHASE V and PHASE W.
2. If Serial Communications are desired, connect the USB to UART module 4 pin connection to J4.
3. For debugging/programming, connect a suitable USB SWD module to J1 by using a standard 4 wire cable.
4. Connect the line voltage power source via three prong terminal block connector J6. For most systems, only connecting to the Live and Neutral terminals is sufficient.
5. **NOTE**: Due to the high voltage nature of this board, it is highly recommended for all connections to be made prior to applying power. Once rectified input voltage goes above 85VDC, the PAC5556's Multi Mode Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D2 lighting up.

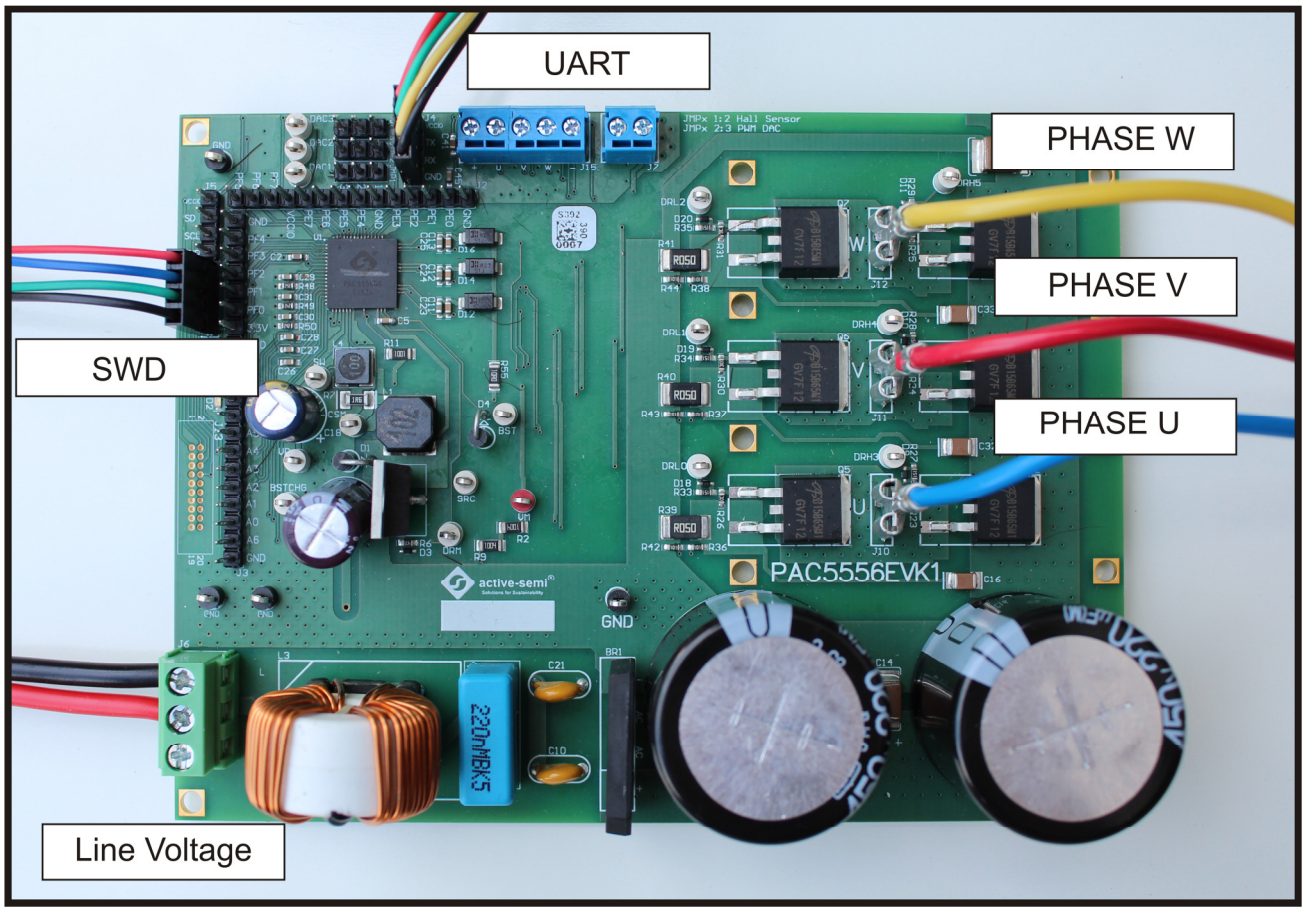

Figure 7: PAC5556EVK1 Evaluation Module Connections