PCA8550

4-bit multiplexed/1-bit latched 5-bit I²C EEPROM DIP switch

Rev. 7 — 8 April 2015 Product data sheet

1. General description

The primary function of the 4-bit 2-to-1 I²C multiplexer is to select either a 4-bit input or data from a non-volatile register and drive this value onto the output pins. One additional non-multiplexed register output is also provided. The non-multiplexed output is latched to prevent output value changes during I²C writes to the non-volatile register. A write protect input is provided to enable/disable the ability to write to the non-volatile register. An “override” input feature forces all outputs to logic 0.

2. Features and benefits

- 4-bit 2-to-1 multiplexer, 1-bit latch DIP switch
- 5-bit internal non-volatile register
- Override input forces all outputs to logic 0
- Internal non-volatile register write/readable via I²C-bus
- Write-protect pin enables/disables I²C writes to register
- 2.5 V multiplexed outputs
- 3.3 V non-multiplexed output (latched)
- 5 V tolerant inputs
- Useful for ‘jumperless’ configuration of PC motherboards
- Designed for use in Pentium Pro/Pentium II systems

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA8550D	PCA8550	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
PCA8550DB	PA8550	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
PCA8550PW	PCA8550	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA8550D	PCA8550D,118	SO16	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T_{amb} = 0 °C to +70 °C
PCA8550DB	PCA8550DB,118	SSOP16	REEL 13" Q1/T1 *STANDARD MARK SMD	2000	T_{amb} = 0 °C to +70 °C
PCA8550PW	PCA8550PW,118	TSSOP16	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T_{amb} = 0 °C to +70 °C

4. Block diagram

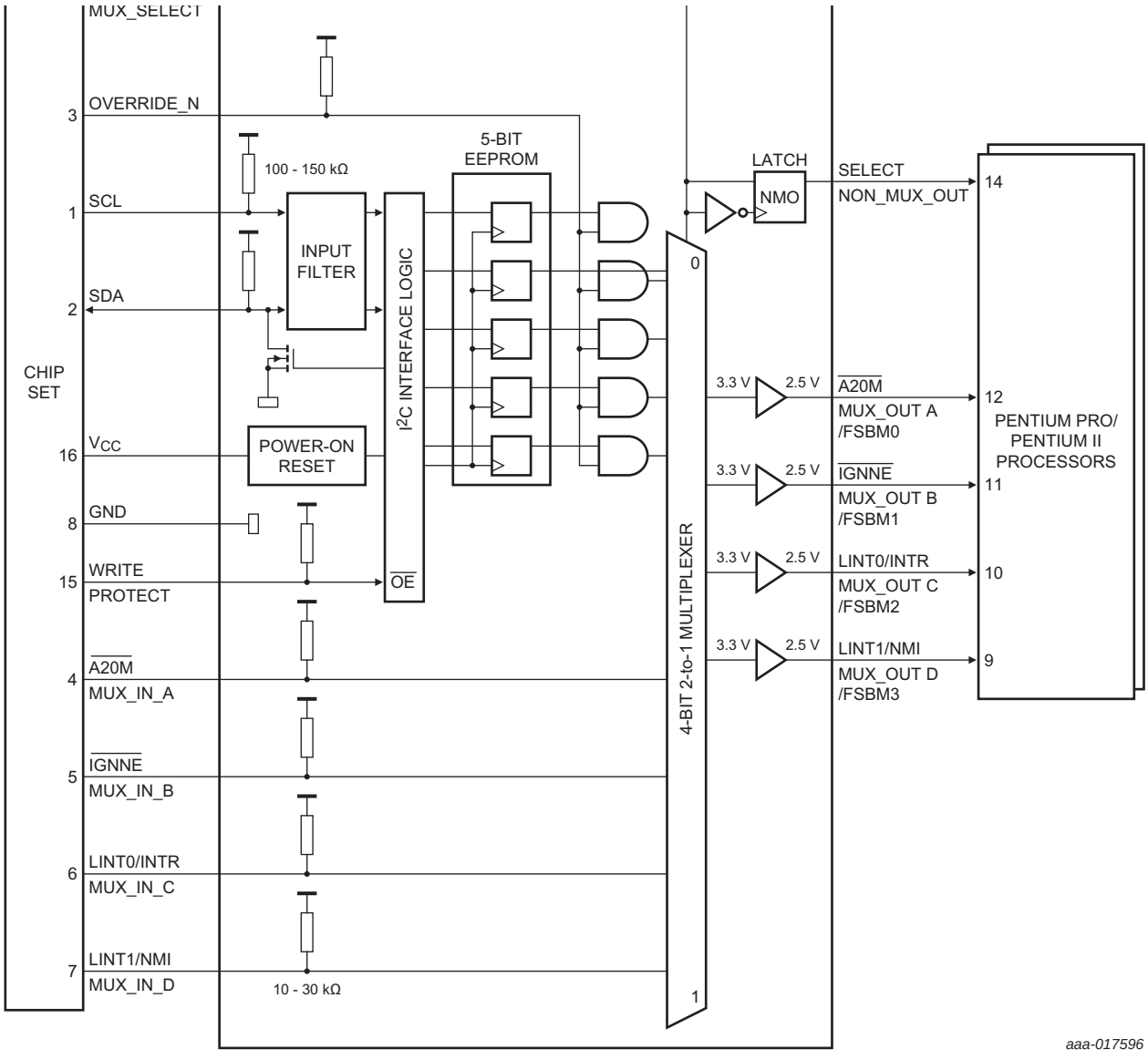


Fig 1. Block diagram

5. Pinning information

5.1 Pin description

Table 3. Pin description

Symbol	Pin	Description
I²C SCL	1	I²C-bus clock
I²C SDA	2	Bi-directional I²C-bus data
OVERRIDE_N	3	Forces all outputs to logic 0
MUX_IN A	4	External inputs to multiplexer
MUX_IN B	5	
MUX_IN C	6	
MUX_IN D	7	
GND	8	Common ground voltage rail
MUX_OUT D	9	2.5 V multiplexed output
MUX_OUT C	10	
MUX_OUT B	11	
MUX_OUT A	12	
MUX_SELECT	13	Selects MUX_IN inputs or register contents for MUX_OUT outputs
NON_MUXED_OUT	14	TTL-level output from non-volatile memory
WP	15	Non-volatile register write-protect
V_{CC}	16	Positive voltage rail

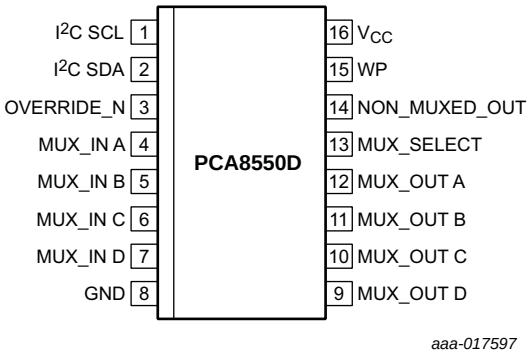


Fig 2. Pin configuration for SO16

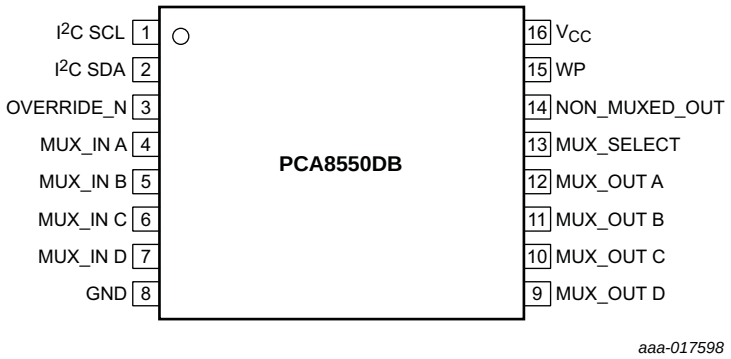


Fig 3. Pin configuration for SSOP16

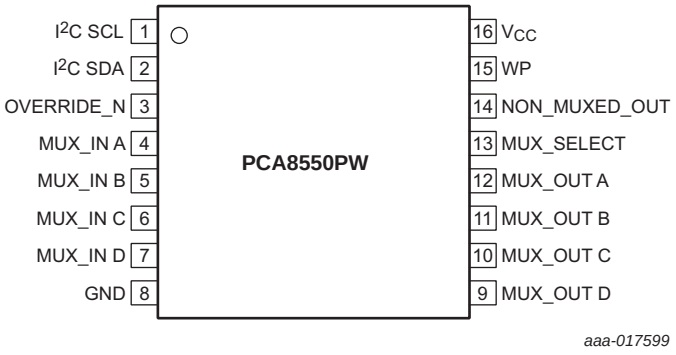


Fig 4. Pin configuration for TSSOP16

6. Functional description

When the MUX_SELECT signal is logic 0, the multiplexer will select the data from the non-volatile register to drive on the MUX_OUT pins. When the MUX_SELECT signal is logic 1, the multiplexer will select the MUX_IN lines to drive on the MUX_OUT pins. The MUX_SELECT signal is also used to latch the NON_MUXED_OUT signal which outputs data from the non-volatile register. The NON_MUXED_OUT signal latch is transparent when MUX_SELECT is in a logic 0 state, and will latch data when MUX_SELECT is in a logic 1 state. When the active-LOW OVERRIDE_N signal is set to logic 0 and the MUX_SELECT signal is at a logic 0, all outputs will be driven to logic 0. This information is summarized in Table 1. The write protect (WP) input is used to control the ability to write the contents of the 5-bit non-volatile register. If the WP signal is logic 0, the I²C-bus will be able to write the contents of the non-volatile register. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile register.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I²C-bus (described in the next section).

The OVERRIDE_N, WP, MUX_IN, and MUX_SELECT signals have internal pull-up resistors. See Section 9 and Section 10 for hysteresis and signal spike suppression figures.

6.1 Function table

Table 4. Function table

OVERRIDE_N	MUX_SELECT	MUX_OUT OUTPUTS	NON_MUXED_OUT OUTPUT
0	0	All 0s	All 0s
0	1	MUX_IN inputs	Latched NON_MUXED_OUT
1	0	From non-volatile register	From non-volatile register
1	1	MUX_IN inputs	From non-volatile register

[1] Latched NON_MUXED_OUT state will be the value present on the NON_MUXED_OUT output at the time of the MUX_SELECT input transitioned from a logic 0 to a logic 1 state.

6.2 I²C-bus interface

Communicating with this device is initiated by sending a valid address on the I²C-bus. The address format (see FIgure 2) is a fixed unique 7-bit value followed by a 1-bit read/write value which determines the direction of the data transfer.

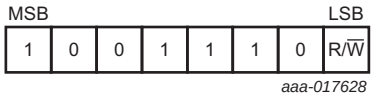


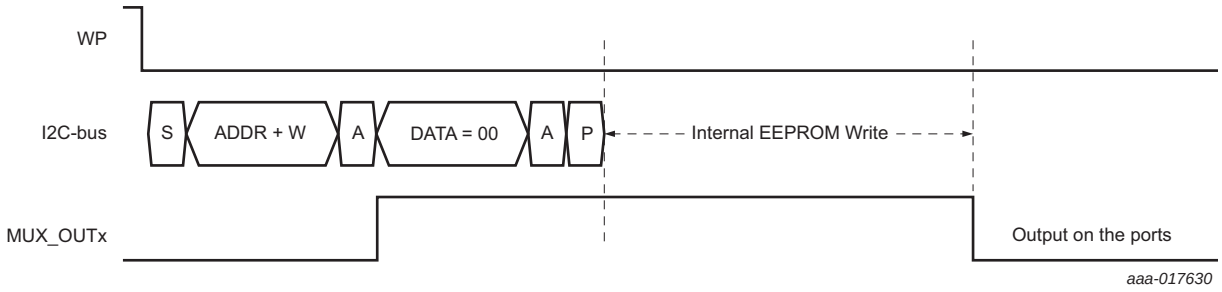
Fig 5. I²C-bus address byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the non-volatile register. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The three high-order bits (see Figure 6) are logic 0. The next bit is data which is non-multiplexed. The low four bits are the data which will be multiplexed. A write with any of the first three bits non-zero will be aborted.

1. To ensure data integrity, the non-volatile register must be internally write protected when V_{CC} to the I²C-bus is powered down or V_{CC} to the component is dropped below normal operating levels.

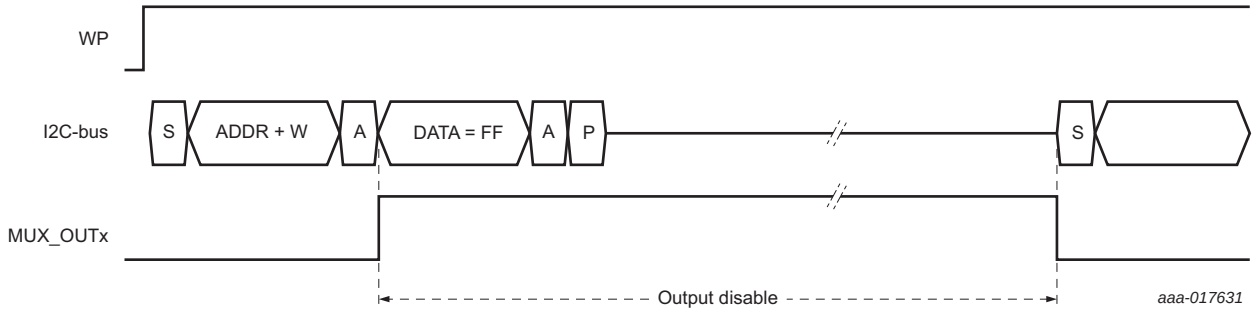
Fig 6. I²C-bus data byte

2. MUX_OUTx will be disabled when the master writes to PCA8550.
   a. With WP enabled, during I²C write cycle the MUX_OUTx will be disabled after the address acknowledge bit and the outputs will be enabled after the internal EEPROM write is completed (Figure 7).
   b. With WP disabled, during I²C write cycle the MUX_OUTx will be disabled after the address acknowledge bit and enabled when there is a START condition on the I²C-bus (Figure 8).



MUX_OUTx output after EEPROM write cycle

Fig 7. Write when WP enabled



Do not write to EEPROM when PW is HIGH, the MUX_OUTx will be disabled until another START condition on the I²C-bus

Fig 8. Write when WP disabled

6.3 Power-on reset

When power is applied to VCC, an internal power-on reset holds the PCA8550 in a reset state until VCC has reached VPOR. At that point, the reset condition is released and the PCA8550 volatile registers and I²C state machine will initialize to their default states.

The MUX_OUT and NON_MUXED_OUT pin values depend on:

- the OVERRIDE_N and MUX_SELECT logic levels
- the previously stored values in the EEPROM register/current MUX_IN pin values as shown in Table 4.

7. Limiting values

Table 5. Limiting values[1] [2]

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+4.6	V
V_I	input voltage	[3]	−1.5	V_{CC} + 1.5	V
V_O	output voltage	[3]	−0.5	V_{CC} + 0.5	V
T_{stg}	storage temperature		−60	+150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[3] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	DC supply voltage		3.0	3.6	V
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	-	2.6	V
V_{IL}	LOW-level input voltage	SCL, SDA; I_{OL} = 3 mA	−0.5	+0.9	V
V_{IH}	HIGH-level input voltage	SCL, SDA; I_{OL} = 3 mA	2.7	4.0	V
V_{OL}	LOW-level output voltage	SCL, SDA; I_{OL} = 3 mA	-	0.4	V
V_{IL}	LOW-level input voltage	OVERRIDE_N, MUX_IN, MUX_SELECT	−0.5	+0.8	V
V_{IH}	HIGH-level input voltage	OVERRIDE_N, MUX_IN, MUX_SELECT	2.0	4.0	V
I_{OL}	LOW-level output current	MUX_OUT NON_MUXED_OUT	-	2.0	mA
I_{OH}	HIGH-level output current	MUX_OUT NON_MUXED_OUT	-	−2.0	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	10	ns/V
T_{amb}	ambient temperature	operating in free air	0	+70	°C

9. Static characteristics

Table 7. Static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input SCL; input/output SDA							
V_{OL}	LOW-level output voltage			0	-	+0.6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		-	-	3	mA
		V_{OL} = 0.6 V		-	-	6	mA
I_{IL}	LOW-level input current	V_{IL} = 0.4 V		–7	-	–32	µA
I_{IH}	HIGH-level input current	V_{IH} = 2.4 V		–1.5	-	–12	µA
V_{hys}	hysteresis voltage			0.19	-	-	V
OVERRIDE_N, WP, MUX_SELECT							
I_{IL}	LOW-level input current		[1]	–86	-	–267	µA
I_{IH}	HIGH-level input current			–20	-	–100	µA
MUX_IN_A, MUX_IN_B, MUX_IN_C, MUX_IN_D							
I_{IL}	LOW-level input current	V_{IL} = 0.4 V		–0.72	-	–2.0	mA
I_{IH}	HIGH-level input current	V_{IH} = 2.4 V		–0.72	-	–2.0	mA
MUX_OUT							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		–0.3	-	+0.4	V
		I_{OL} = 2.0 mA		–0.3	-	+0.7	V
V_{OH}	HIGH-level output voltage	I_{OH} = –100 µA		2.0	-	2.625	V
		I_{OH} = –1.0 mA		1.7	-	2.625	V
NON_MUXED_OUT							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		–0.5	-	+0.4	V
		I_{OL} = 2.0 mA		–0.5	-	+0.7	V
V_{OH}	HIGH-level output voltage	I_{OH} = –100 µA		2.4	-	3.6	V
		I_{OH} = –2.0 mA		2.0	-	3.6	V
I_{CC}	quiescent supply current	V_{CC} = 3.3 V; V_I = 0 V to V_{CC}		-	-	10	mA
		V_I = V_{CC}		-	-	500	µA
C_I	input capacitance			-	-	10	pF
	ESD protection		[2]	2.0			KV
	Input diode clamp voltage			–1.5	-	-	V

[1] V_{hys} is the hysteresis of Schmitt-Trigger inputs

[2] Human body model

10. Dynamic characteristics

Table 8. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{MPD}	Mux input to output propagation delay		-	-	20	ns
t_{SOV}	MUX_SELECT to output valid		-	-	22	ns
t_{OVN}	OVERRIDE_N to NON_MUX output delay		-	-	15	ns
t_{OVM}	OVERRIDE_N to mux output delay		-	-	25	ns
t_r	rise time	output	1.0	-	3	ns/V
t_f	fall time	output	1.0	-	3	ns/V
C_L	load capacitance	test load on outputs	-	-	15	pF

Table 9. I²C-bus dynamic characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		10	400	kHz
t_{HIGH}	HIGH period of the SCL clock		600	-	ns
t_{LOW}	LOW period of the SCL clock		1.3	-	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	50	ns
$t_{SU;DAT}$	data set-up time		100	-	ns
$t_{HD;DAT}$	data hold time		0	-	ns
t_r	rise time of both SDA and SCL signals	10 pF to 400 pF bus	20	300	ns
t_f	fall time of both SDA and SCL signals	10 pF to 400 pF bus	20	300	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		600	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		600	-	ns
$t_{SU;STO}$	set-up time for STOP condition		600	-	ns
C_b	capacitive load for each bus line		-	400	pF
$T_{cy(W)}$	write cycle time[1]		TYPICAL = 15		ms

[1] WRITE CYCLE time can only be measured indirectly during write cycle. The device will not acknowledge its I²C address.

11. Non-volatile storage specifications

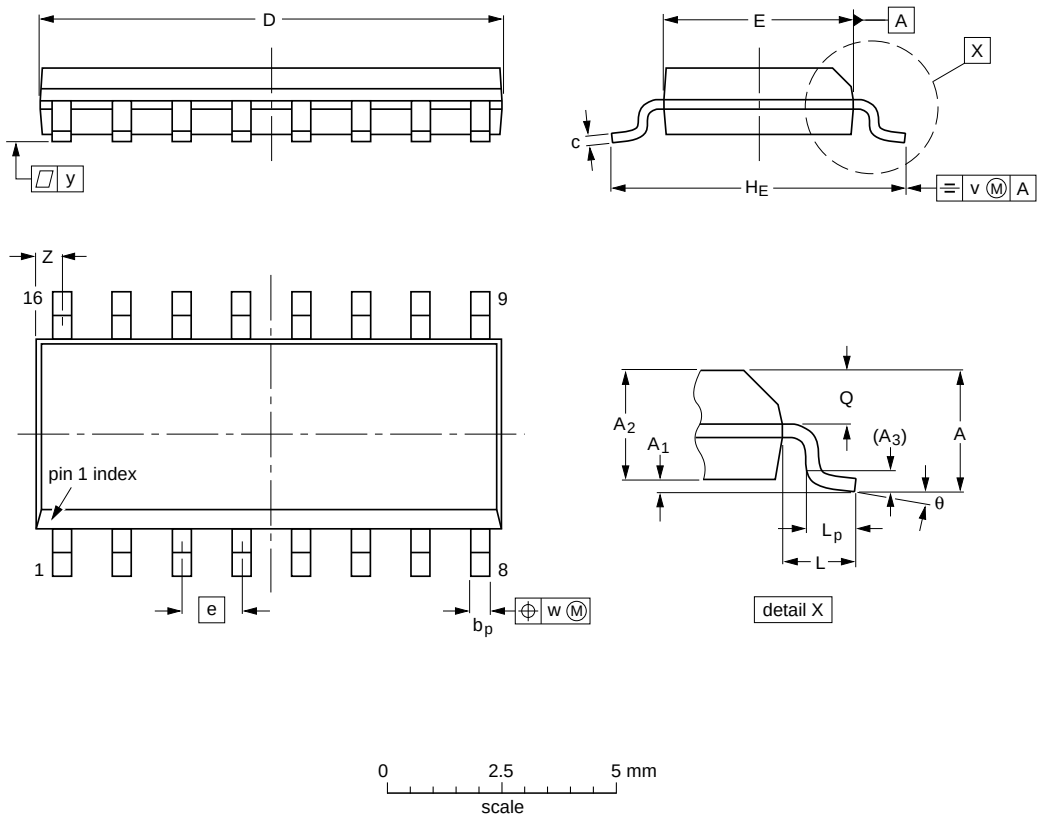
Table 10. Non-volatile storage specifications

Parameter	Specification
memory cell data retention	10 years (minimum)
number of memory cell write cycles	100,000 cycles (minimum)

Application note *AN250, "I²C DIP Switch"* provides additional information on memory cell data retention and the minimum number of write cycles.

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

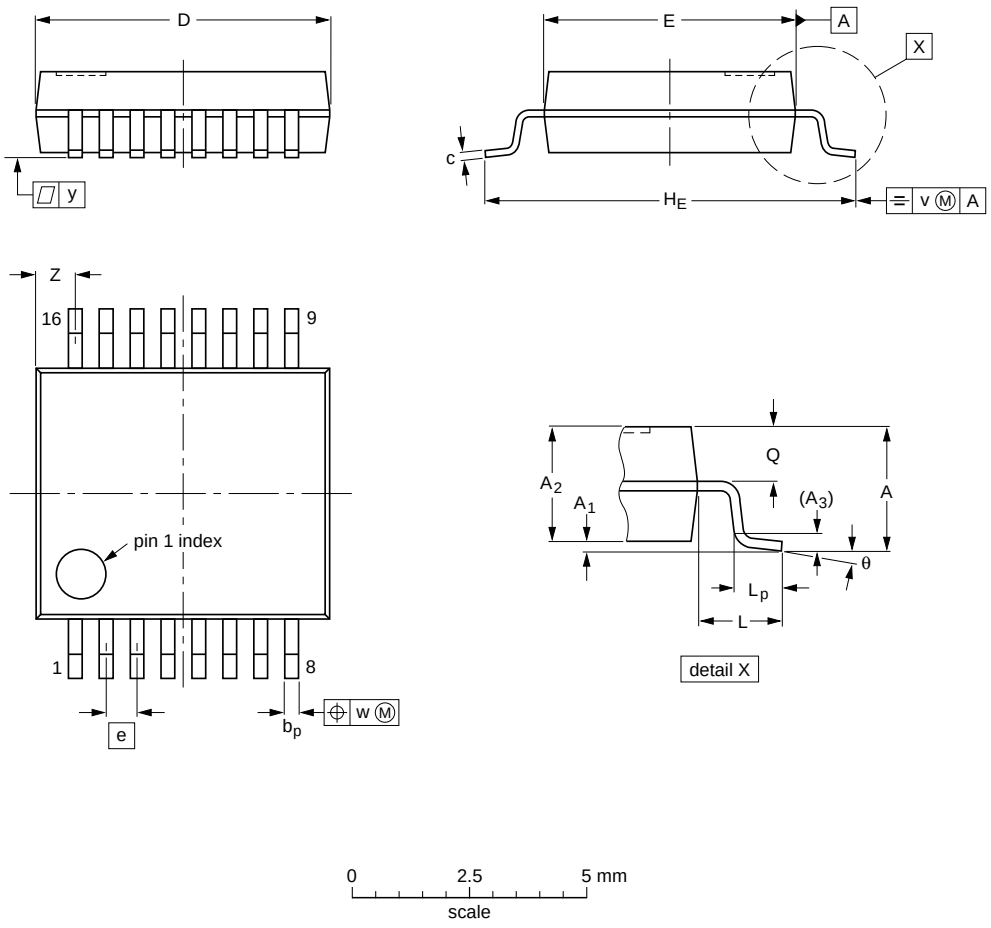
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

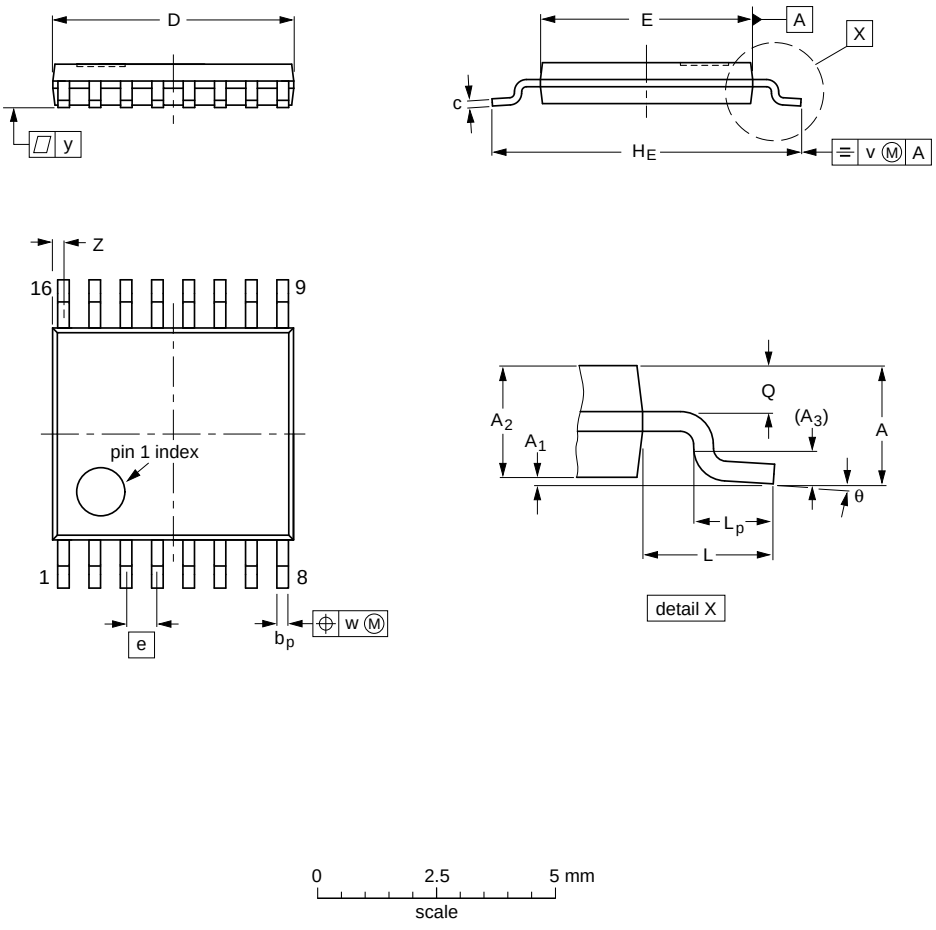
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT403-1 (TSSOP16)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020D)

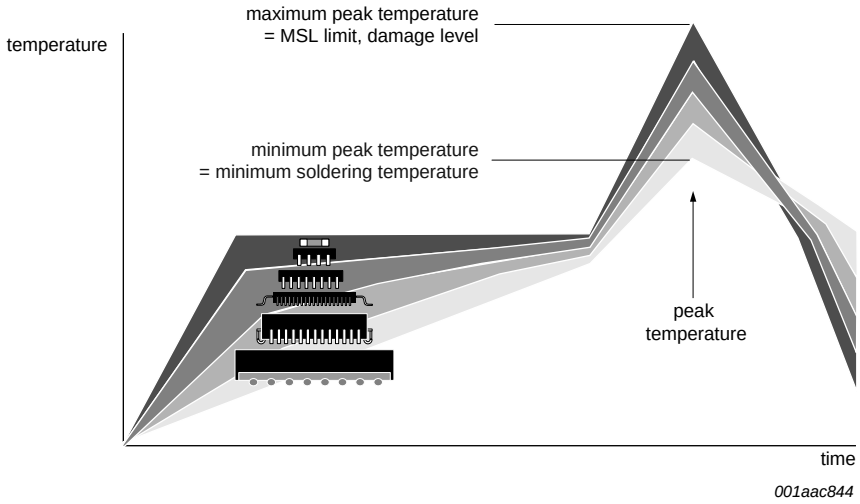
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 12.



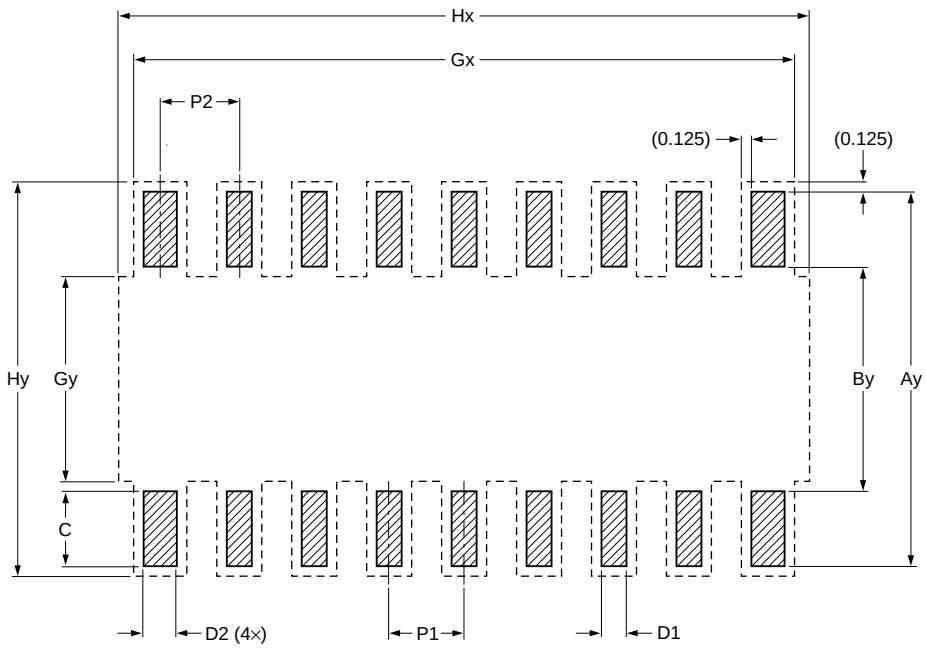
MSL: Moisture Sensitivity Level

Fig 12. Temperature profiles for large and small components

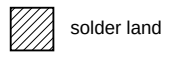
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Soldering: PCB footprints

Footprint information for reflow soldering of SO16 package **SOT109-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

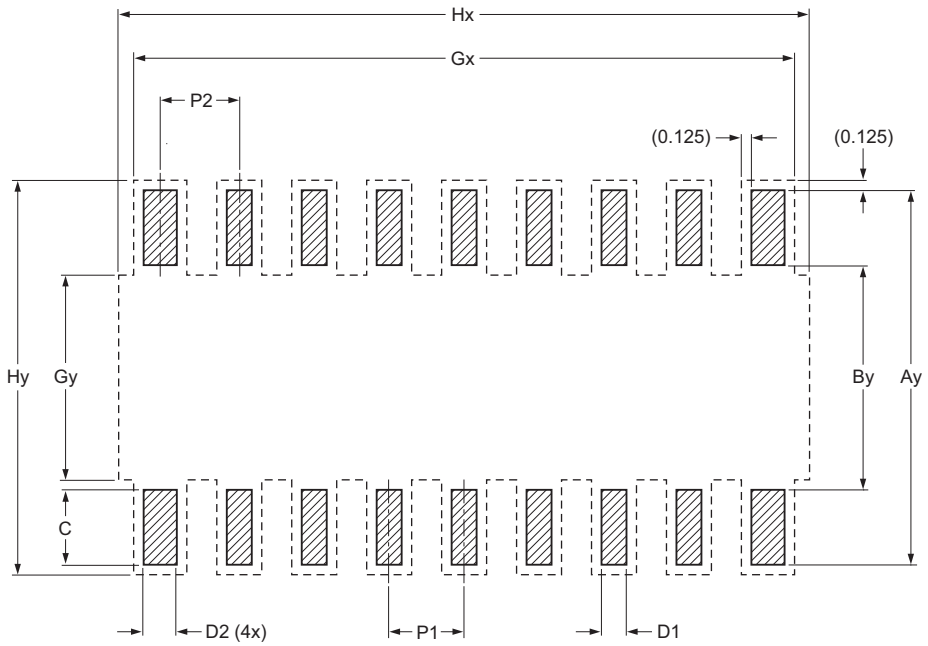


DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
1.270	1.320	7.400	3.900	1.750	0.700	0.800	10.040	5.200	11.900	7.650

Fig 13. PCB footprint for SOT109-1 (SO16); reflow soldering

Footprint information for reflow soldering of SSOP16 package **SOT338-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

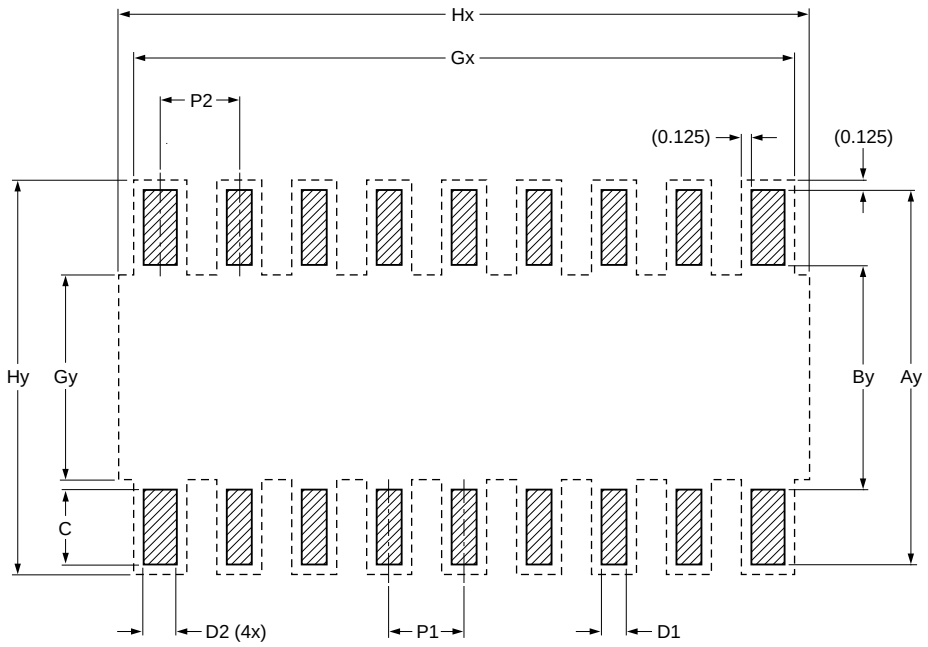
P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.65	0.75	8.6	5.4	1.6	0.4	0.6	5.6	6.1	7.0	8.85

Issue date ~~09-02-22~~ 15-03-26

sot338-1_fr

Fig 14. PCB footprint for SOT338-1 (TSSOP16); reflow soldering

Footprint information for reflow soldering of TSSOP16 package **SOT403-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1_fr

Fig 15. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA8550 v.7	20150408	Product data sheet	-	PCA8550 v.6
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Updated Section 6.2.			
PCA8550 v.6	20030627	Product data sheet	-	PCA8550 v.5
PCA8550 v.5	20010112	Product data sheet	-	PCA8550 v.4

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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