



PCA8574; PCA8574A

Remote 8-bit I/O expander for I²C-bus with interrupt

Rev. 3 — 3 June 2013

Product data sheet

1. General description

The PCA8574/74A provides general-purpose remote I/O expansion via the two-wire bidirectional I²C-bus (serial clock (SCL), serial data (SDA)).

The devices consist of eight quasi-bidirectional ports, 400 kHz I²C-bus interface, three hardware address inputs and interrupt output operating between 2.3 V and 5.5 V. The quasi-bidirectional port can be independently assigned as an input to monitor interrupt status or keypads, or as an output to activate indicator devices such as LEDs. The system master can read from the input port or write to the output port through a single register.

The low current consumption of 4.5 μ A (typical, static) is great for mobile applications and the latched output ports have 25 mA high current sink drive capability for directly driving LEDs.

The PCA8574 and PCA8574A are identical, except for the different fixed portion of the slave address. The three hardware address pins allow eight of each device to be on the same I²C-bus, so there can be up to 16 of these I/O expanders PCA8574/74A together on the same I²C-bus, supporting up to 128 I/Os (for example, 128 LEDs).

The active LOW open-drain interrupt output ($\overline{\text{INT}}$) can be connected to the interrupt logic of the microcontroller and is activated when any input state differs from its corresponding input port register state. It is used to indicate to the microcontroller that an input state has changed and the device needs to be interrogated without the microcontroller continuously polling the input register via the I²C-bus.

The internal Power-On Reset (POR) initializes the I/Os as inputs with a weak internal pull-up 100 μ A current source.

2. Features and benefits

- I²C-bus to parallel port expander
- 400 kHz I²C-bus interface (Fast-mode I²C-bus)
- Operating supply voltage 2.3 V to 5.5 V with 5.5 V tolerant I/Os held to V_{DD} with 100 μ A current source
- 8-bit remote I/O pins that default to inputs at power-up
- Latched outputs with 25 mA sink capability for directly driving LEDs
- Total package sink capability of 200 mA
- Active LOW open-drain interrupt output
- Eight programmable slave addresses using three address pins
- Low standby current (4.5 μ A typical)
- -40 °C to +85 °C operation



- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA
- Packages offered: SO16, TSSOP16, SSOP20

3. Applications

- LED signs and displays
- Servers
- Key pads
- Industrial control
- Medical equipment
- PLCs
- Cellular telephones
- Mobile devices
- Gaming machines
- Instrumentation and test measurement

4. Ordering information

Table 1. Ordering information

| Type number | Topside mark | Package | | |
|---------------------------|--------------|---------|--|----------|
| | | Name | Description | Version |
| PCA8574D ^[1] | PCA8574D | SO16 | plastic small outline package; 16 leads; body width 7.5 mm | SOT162-1 |
| PCA8574AD ^[2] | PCA8574AD | | | |
| PCA8574PW | PCA8574 | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| PCA8574APW | PA8574A | | | |
| PCA8574TS ^[3] | PCA8574 | SSOP20 | plastic shrink small outline package; 20 leads; body width 4.4 mm | SOT266-1 |
| PCA8574ATS ^[4] | PA8574A | | | |

[1] PCA8574D drop-in replacement for PCF8574T/3.

[2] PCA8574AD drop-in replacement for PCF8574AT/3.

[3] PCA8574TS drop-in replacement for PCF8574TS/3.

[4] PCA8574ATS drop-in replacement for PCF8574ATS/3.

4.1 Ordering options

Table 2. Ordering options

| Type number | Orderable part number | Package | Packing method | Minimum order quantity | Temperature range |
|-------------|-----------------------|---------|---|------------------------|-------------------------------------|
| PCA8574D | PCA8574D,512 | SO16 | Standard marking * tube dry pack | 1920 | T _{amb} = -40 °C to +85 °C |
| | PCA8574D,518 | SO16 | Reel 13" Q1/T1 *standard mark SMD dry pack | 1000 | T _{amb} = -40 °C to +85 °C |
| PCA8574AD | PCA8574AD,512 | SO16 | Standard marking * tube dry pack | 1920 | T _{amb} = -40 °C to +85 °C |
| | PCA8574AD,518 | SO16 | Reel 13" Q1/T1 *standard mark SMD dry pack | 1000 | T _{amb} = -40 °C to +85 °C |
| PCA8574PW | PCA8574PW,112 | TSSOP16 | Standard marking * IC's tube - DSC bulk pack | 2400 | T _{amb} = -40 °C to +85 °C |
| | PCA8574PW,118 | TSSOP16 | Reel 13" Q1/T1 *standard mark SMD | 2500 | T _{amb} = -40 °C to +85 °C |
| PCA8574APW | PCA8574APW,112 | TSSOP16 | Standard marking * IC's tube - DSC bulk pack | 2400 | T _{amb} = -40 °C to +85 °C |
| | PCA8574APW,118 | TSSOP16 | Reel 13" Q1/T1 *standard mark SMD | 2500 | T _{amb} = -40 °C to +85 °C |
| PCA8574TS | PCA8574TS,112 | SSOP20 | Standard marking * IC's tube - DSC bulk pack | 1350 | T _{amb} = -40 °C to +85 °C |
| | PCA8574TS,118 | SSOP20 | Reel 13" Q1/T1 *standard mark SMD | 2500 | T _{amb} = -40 °C to +85 °C |
| PCA8574ATS | PCA8574ATS,112 | SSOP20 | Standard marking * IC's tube - DSC bulk pack | 1350 | T _{amb} = -40 °C to +85 °C |
| | PCA8574ATS,118 | SSOP20 | Reel 13" Q1/T1 *standard mark SMD | 2500 | T _{amb} = -40 °C to +85 °C |

5. Block diagram

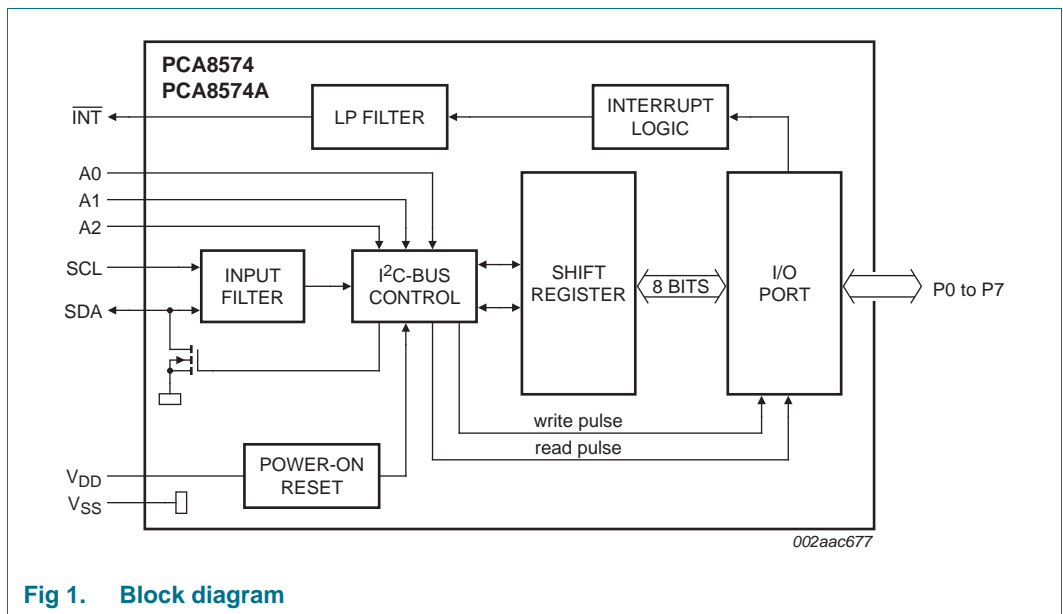


Fig 1. Block diagram

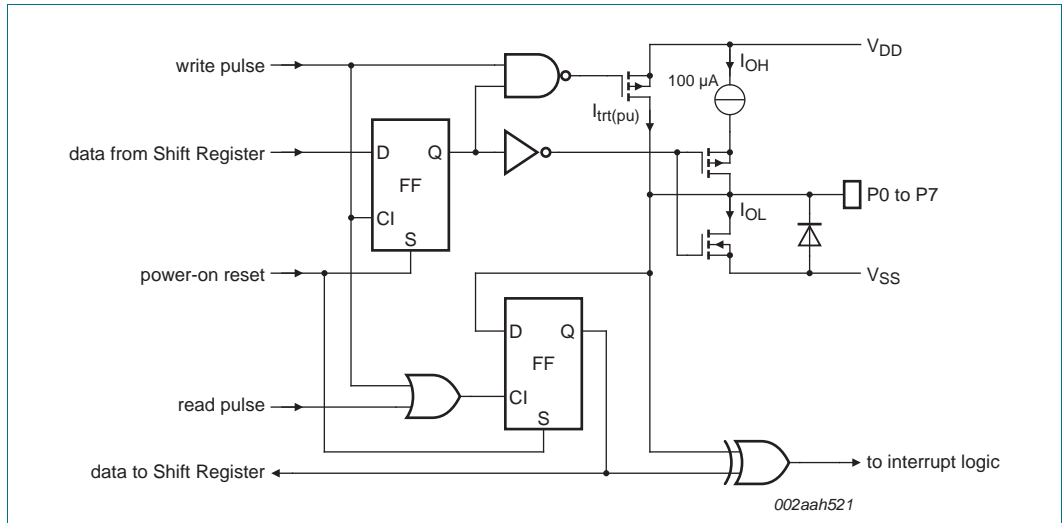
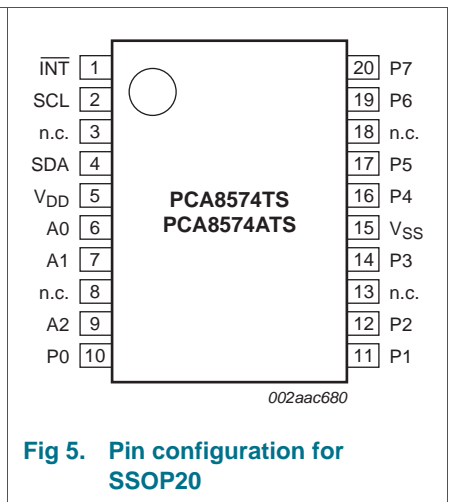
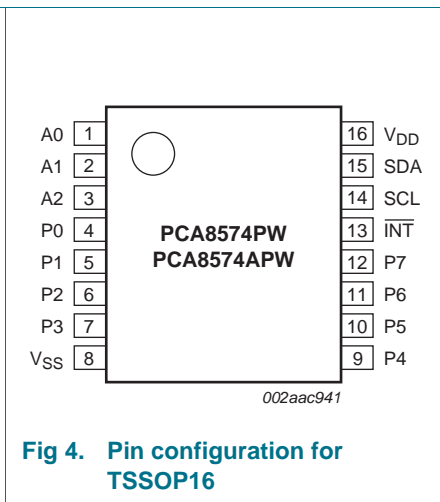
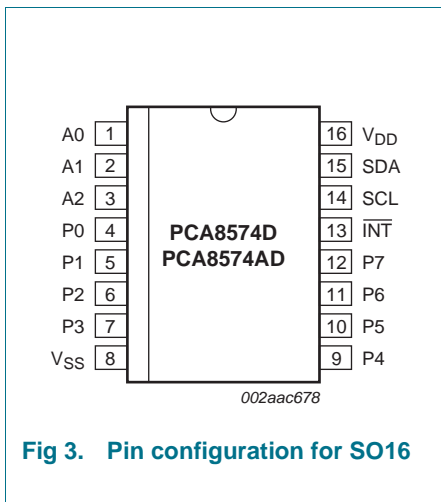


Fig 2. Simplified schematic diagram of P0 to P7

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

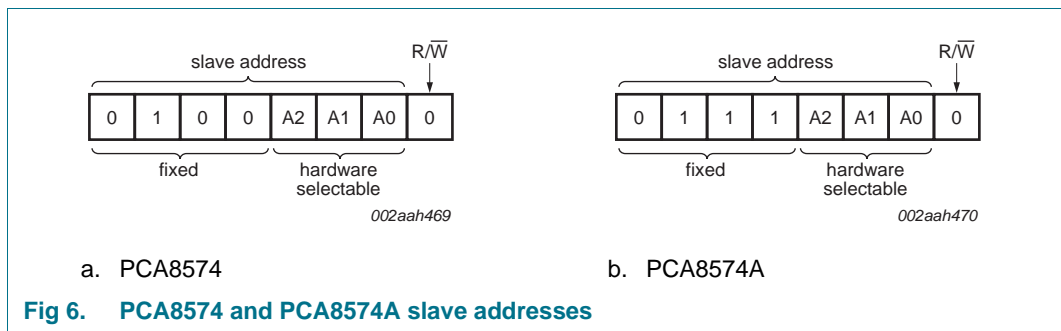
| Symbol | Pin | | Description |
|-------------------------|-------------|--------------|-------------------------------|
| | DIP16, SO16 | SSOP20 | |
| A0 | 1 | 6 | address input 0 |
| A1 | 2 | 7 | address input 1 |
| A2 | 3 | 9 | address input 2 |
| P0 | 4 | 10 | quasi-bidirectional I/O 0 |
| P1 | 5 | 11 | quasi-bidirectional I/O 1 |
| P2 | 6 | 12 | quasi-bidirectional I/O 2 |
| P3 | 7 | 14 | quasi-bidirectional I/O 3 |
| V _{SS} | 8 | 15 | supply ground |
| P4 | 9 | 16 | quasi-bidirectional I/O 4 |
| P5 | 10 | 17 | quasi-bidirectional I/O 5 |
| P6 | 11 | 19 | quasi-bidirectional I/O 6 |
| P7 | 12 | 20 | quasi-bidirectional I/O 7 |
| $\overline{\text{INT}}$ | 13 | 1 | interrupt output (active LOW) |
| SCL | 14 | 2 | serial clock line |
| SDA | 15 | 4 | serial data line |
| V _{DD} | 16 | 5 | supply voltage |
| n.c. | - | 3, 8, 13, 18 | not connected |

7. Functional description

Refer to [Figure 1 “Block diagram”](#).

7.1 Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address format of the PCA8574/74A is shown in [Figure 6](#). Slave address pins A2, A1 and A0 are held HIGH or LOW to choose one of eight slave addresses. To conserve power, no internal pull-up resistors are incorporated on pins A2, A1, or A0 so they must be externally held HIGH or LOW. The address pins (A2, A1, A0) can connect to V_{DD} or V_{SS} directly or through resistors.



The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation (write operation is shown in [Figure 6](#)).

7.1.1 Address maps

The PCA8574 and PCA8574A are functionally the same, but have a different fixed portion (A6 to A3) of the slave address. This allows eight of the PCA8574 and eight of the PCA8574A to be on the same I²C-bus without address conflict.

Table 4. PCA8574 address map

| Pin connectivity | | | Address of PCA8574 | | | | | | | | Address byte value | | 7-bit hexadecimal address without R/W |
|------------------|-----------------|-----------------|--------------------|----|----|----|----|----|----|-----|--------------------|------|---------------------------------------|
| A2 | A1 | A0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Write | Read | |
| V _{SS} | V _{SS} | V _{SS} | 0 | 1 | 0 | 0 | 0 | 0 | 0 | - | 40h | 41h | 20h |
| V _{SS} | V _{SS} | V _{DD} | 0 | 1 | 0 | 0 | 0 | 0 | 1 | - | 42h | 43h | 21h |
| V _{SS} | V _{DD} | V _{SS} | 0 | 1 | 0 | 0 | 0 | 1 | 0 | - | 44h | 45h | 22h |
| V _{SS} | V _{DD} | V _{DD} | 0 | 1 | 0 | 0 | 0 | 1 | 1 | - | 46h | 47h | 23h |
| V _{DD} | V _{SS} | V _{SS} | 0 | 1 | 0 | 0 | 1 | 0 | 0 | - | 48h | 49h | 24h |
| V _{DD} | V _{SS} | V _{DD} | 0 | 1 | 0 | 0 | 1 | 0 | 1 | - | 4Ah | 4Bh | 25h |
| V _{DD} | V _{DD} | V _{SS} | 0 | 1 | 0 | 0 | 1 | 1 | 0 | - | 4Ch | 4Dh | 26h |
| V _{DD} | V _{DD} | V _{DD} | 0 | 1 | 0 | 0 | 1 | 1 | 1 | - | 4Eh | 4Fh | 27h |

Table 5. PCA8574A address map

| Pin connectivity | | | Address of PCA8574A | | | | | | | | Address byte value | | 7-bit hexadecimal address without R/W |
|------------------|-----------------|-----------------|---------------------|----|----|----|----|----|----|-----|--------------------|------|---------------------------------------|
| A2 | A1 | A0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Write | Read | |
| V _{SS} | V _{SS} | V _{SS} | 0 | 1 | 1 | 1 | 0 | 0 | 0 | - | 70h | 71h | 38h |
| V _{SS} | V _{SS} | V _{DD} | 0 | 1 | 1 | 1 | 0 | 0 | 1 | - | 72h | 73h | 39h |
| V _{SS} | V _{DD} | V _{SS} | 0 | 1 | 1 | 1 | 0 | 1 | 0 | - | 74h | 75h | 3Ah |
| V _{SS} | V _{DD} | V _{DD} | 0 | 1 | 1 | 1 | 0 | 1 | 1 | - | 76h | 77h | 3Bh |
| V _{DD} | V _{SS} | V _{SS} | 0 | 1 | 1 | 1 | 1 | 0 | 0 | - | 78h | 79h | 3Ch |
| V _{DD} | V _{SS} | V _{DD} | 0 | 1 | 1 | 1 | 1 | 0 | 1 | - | 7Ah | 7Bh | 3Dh |
| V _{DD} | V _{DD} | V _{SS} | 0 | 1 | 1 | 1 | 1 | 1 | 0 | - | 7Ch | 7Dh | 3Eh |
| V _{DD} | V _{DD} | V _{DD} | 0 | 1 | 1 | 1 | 1 | 1 | 1 | - | 7Eh | 7Fh | 3Fh |

8. I/O programming

8.1 Quasi-bidirectional I/Os

A quasi-bidirectional I/O is an input or output port without using a direction control register. Whenever the master reads the register, the value returned to master depends on the actual voltage or status of the pin. At power-on, all the ports are HIGH with a weak 100 μ A internal pull-up to V_{DD} , but can be driven LOW by an internal transistor, or an external signal. The I/O ports are entirely independent of each other, but each I/O octal is controlled by the same read or write data byte.

Advantages of the quasi-bidirectional I/O over totem pole I/O include:

- Better for driving LEDs since the p-channel (transistor to V_{DD}) is small, which saves die size and therefore cost. LED drive only requires an internal transistor to ground, while the LED is connected to V_{DD} through a current-limiting resistor. Totem pole I/O have both n-channel and p-channel transistors, which allow solid HIGH and LOW output levels without a pull-up resistor — good for logic levels.
- Simpler architecture — only a single register and the I/O can be both input and output at the same time. Totem pole I/O have a direction register that specifies the port pin direction and it is always in that configuration unless the direction is explicitly changed.
- Does not require a command byte. The simplicity of one register (no need for the pointer register or, technically, the command byte) is an advantage in some embedded systems where every byte counts because of memory or bandwidth limitations.

There is only one register to control four possibilities of the port pin: Input HIGH, input LOW, output HIGH, or output LOW.

Input HIGH: The master needs to write 1 to the register to set the port as an input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin up to V_{DD} or drives logic 1, then the master will read the value of 1.

Input LOW: The master needs to write 1 to the register to set the port to input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin down to V_{SS} or drives logic 0, which sinks the weak 100 μ A current source, then the master will read the value of 0.

Output HIGH: The master writes 1 to the register. There is an additional 'accelerator' or strong pull-up current when the master sets the port HIGH. The additional strong pull-up is only active during the HIGH time of the acknowledge clock cycle. This accelerator current helps the port's 100 μ A current source make a faster rising edge into a heavily loaded output, but only at the start of the acknowledge clock cycle to avoid bus contention if an external signal is pulling the port LOW to V_{SS} /driving the port with logic 0 at the same time. After the half clock cycle there is only the 100 μ A current source to hold the port HIGH.

Output LOW: The master writes 0 to the register. There is a strong current sink transistor that holds the port pin LOW. A large current may flow into the port, which could potentially damage the part if the master writes a 0 to the register and an external source is pulling the port HIGH at the same time.

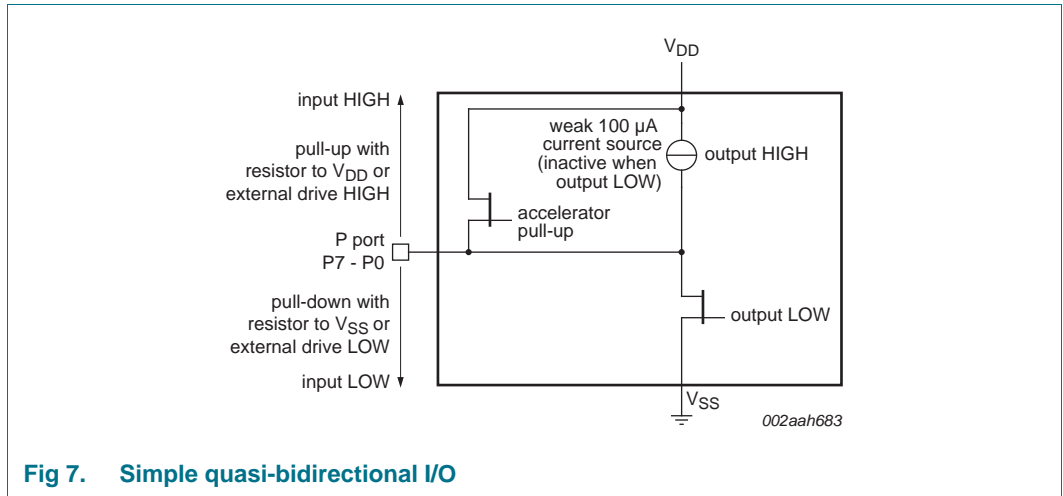


Fig 7. Simple quasi-bidirectional I/O

8.2 Writing to the port (Output mode)

The master (microcontroller) sends the START condition and slave address setting the last bit of the address byte to logic 0 for the write mode. The PCA8574/74A acknowledges and the master then sends the data byte for P7 to P0 to the port register. As the clock line goes HIGH, the 8-bit data is presented on the port lines after it has been acknowledged by the PCA8574/74A. If a LOW is written, the strong pull-down turns on and stays on. If a HIGH is written, the strong pull-up turns on for 1/2 of the clock cycle, then the line is held HIGH by the weak current source. The master can then send a STOP or ReSTART condition or continue sending data. The number of data bytes that can be sent successively is not limited and the previous data is overwritten every time a data byte has been sent and acknowledged.

Ensure a logic 1 is written for any port that is being used as an input to ensure the strong external pull-down is turned off.

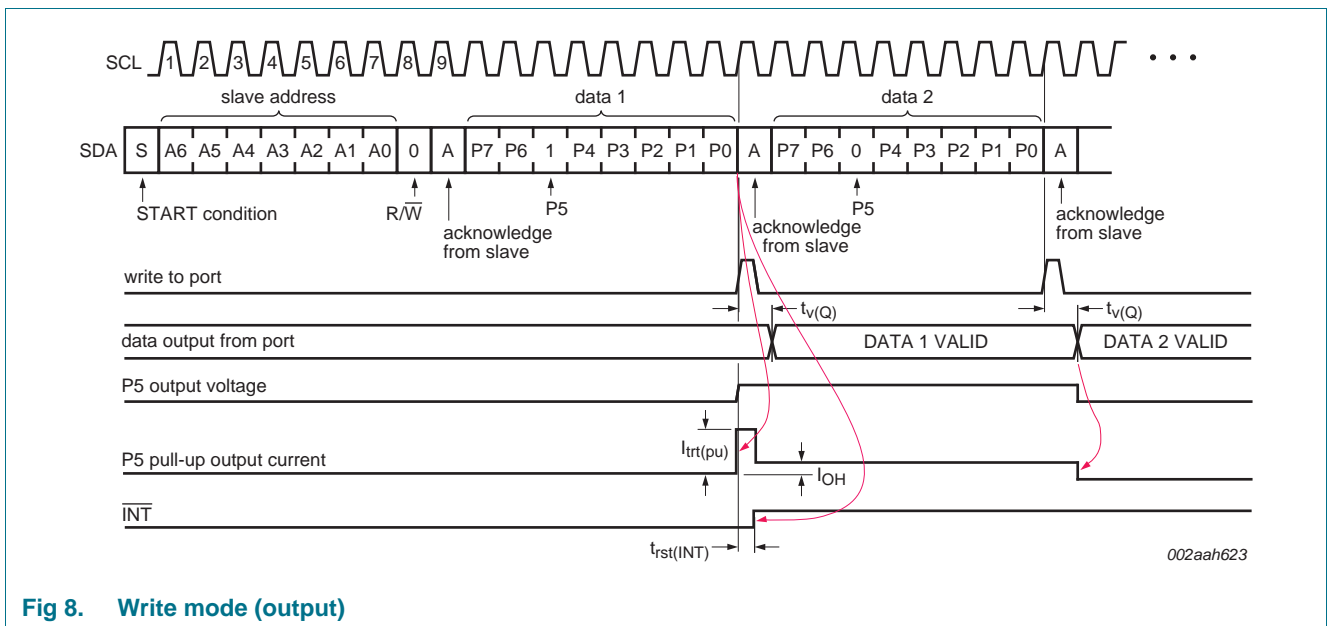


Fig 8. Write mode (output)

Simple code WRITE mode:

<S> <slave address + write> **<ACK>** <data out> **<ACK>** <data out> **<ACK>** ...
 <data out> **<ACK>** <P>

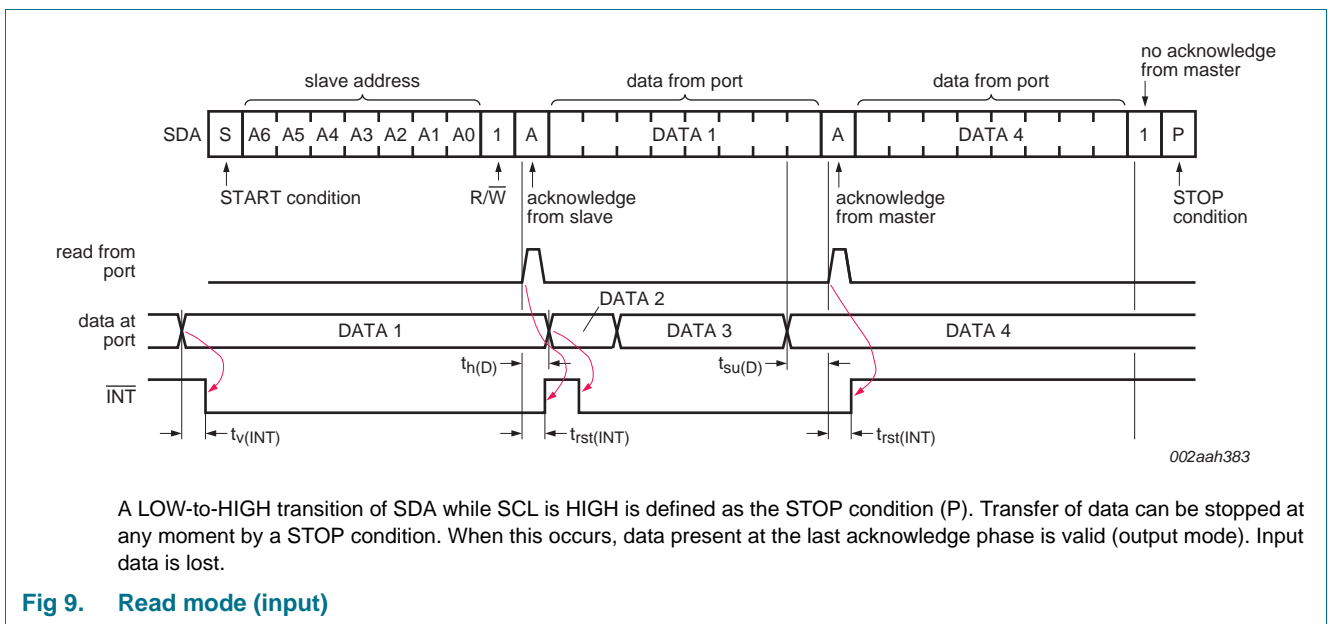
Remark: Bold type = generated by slave device.

8.3 Reading from a port (Input mode)

The port must have been previously written to logic 1, which is the condition after power-on reset. To enter the Read mode the master (microcontroller) addresses the slave device and sets the last bit of the address byte to logic 1 (address byte read). The slave will acknowledge and then send the data byte to the master. The master will NACK and then send the STOP condition or ACK and read the input register again.

The read of any pin being used as an output will indicate HIGH or LOW depending on the actual state of the input pin.

If the data on the input port changes faster than the master can read, this data may be lost. The DATA 2 and DATA 3 are lost because these data did not meet the setup time and hold time (see [Figure 9](#)).



Simple code for Read mode:

<S> <slave address + read> **<ACK>** **<data in>** **<ACK>** ... **<data in>** **<ACK>** **<data in>**
 <NACK> <P>

Remark: Bold type = generated by slave device.

8.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA8574; PCA8574A in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA8574; PCA8574A registers and I²C-bus/SMBus state machine will initialize to their default states of all I/Os to inputs with weak current source to V_{DD}. Thereafter V_{DD} must be lowered below V_{POR} and back up to the operation voltage for power-on reset cycle.

8.5 Interrupt output ($\overline{\text{INT}}$)

The PCA8574/74A provides an open-drain output ($\overline{\text{INT}}$) which can be fed to a corresponding input of the microcontroller (see [Figure 10](#)). As soon as a port input is changed, the $\overline{\text{INT}}$ will be active (LOW) and notify the microcontroller.

An interrupt is generated at any rising or falling edge of the port inputs. After time t_{v(Q)}, the signal $\overline{\text{INT}}$ is valid.

The interrupt will reset to HIGH when data on the port is changed to the original setting or data is read or written by the master.

In the Write mode, the interrupt may be reset (HIGH) on the rising edge of the acknowledge bit of the data byte and also on the rising edge of the write to port pulse. The interrupt will always be reset (HIGH) on the falling edge of the write to port pulse (see [Figure 8](#)).

The interrupt is reset (HIGH) in the Read mode on the rising edge of the acknowledge of slave address byte and on the rising edge of the read from port pulse (see [Figure 9](#)).

During the interrupt reset, any I/O change close to the read or write pulse may not generate an interrupt, or the interrupt will have a very short pulse. After the interrupt is reset, any change in I/Os will be detected and transmitted as an $\overline{\text{INT}}$.

At power-on reset all ports are in Input mode and the initial state of the ports is HIGH, therefore, for any port pin that is pulled LOW or driven LOW by external source, the interrupt output will be active (output LOW).

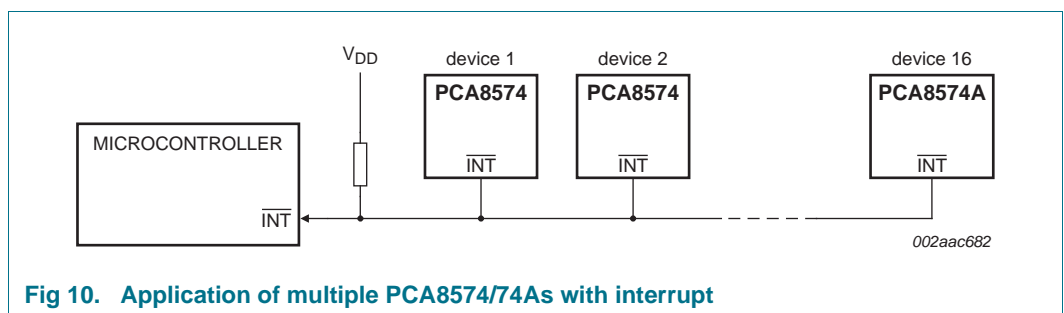


Fig 10. Application of multiple PCA8574/74As with interrupt

9. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-wire communication between different ICs or modules. The two wires are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 11](#)).



Fig 11. Bit transfer

9.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 12](#)).



Fig 12. Definition of START and STOP conditions

9.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 13](#)).

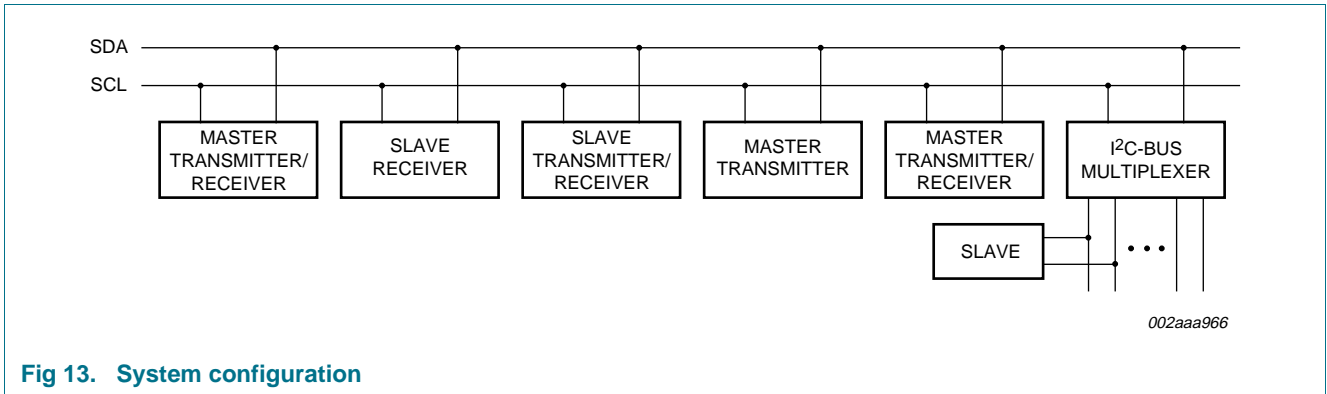


Fig 13. System configuration

9.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit (see Figure 14). The acknowledge bit is an active LOW level (generated by the receiving device) that indicates to the transmitter that the data transfer was successful.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that wants to issue an acknowledge bit has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge bit related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.



Fig 14. Acknowledgement on the I²C-bus

10. Application design-in information

10.1 Bidirectional I/O expander applications

In the 8-bit I/O expander application shown in [Figure 15](#), P0 and P1 are inputs, and P2 to P7 are outputs. When used in this configuration, during a write, **the input (P0 and P1) must be written as HIGH so the external devices fully control the input ports.** The desired HIGH or LOW logic levels may be written to the ports used as outputs (P2 to P7). If 10 μ A internal output HIGH is not enough current source, the port needs external pull-up resistor. During a read, the logic levels of the external devices driving the input ports (P0 and P1) and the previous written logic level to the output ports (P2 to P7) will be read.

The GPIO also has an interrupt line ($\overline{\text{INT}}$) that can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O informs the microprocessor that there has been a change of data on its ports without having to communicate via the I²C-bus.

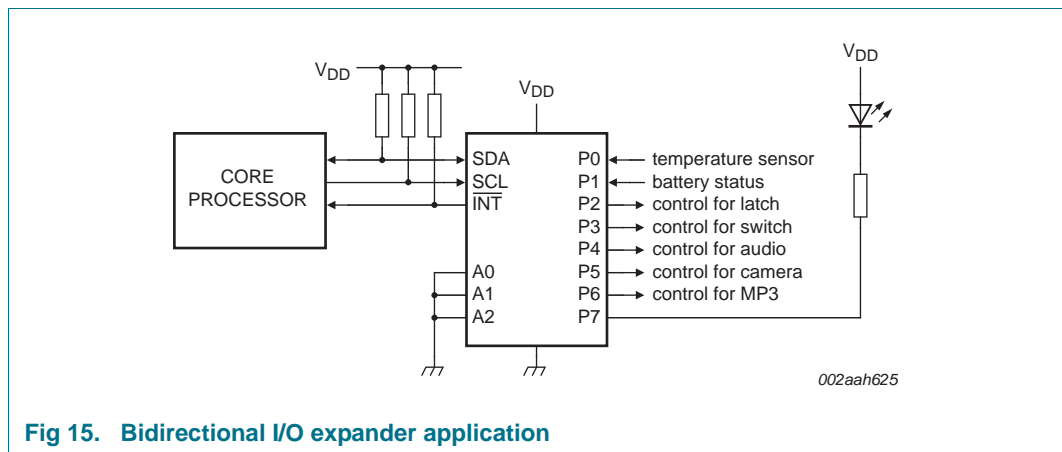


Fig 15. Bidirectional I/O expander application

10.2 How to read and write to I/O expander (example)

In the application example of PCA8574 shown in [Figure 15](#), the microcontroller wants to control the P3 switch ON and the P7 LED ON when the temperature sensor P0 changes.

1. When the system power on:

Core Processor needs to issue an initial command to set P0 and P1 as inputs and P[7:2] as outputs with value 1010 00 (LED off, MP3 off, camera on, audio off, switch off and latch off).

2. Operation:

When the temperature changes above the threshold, the temperature sensor signal will toggle from HIGH to LOW. The $\overline{\text{INT}}$ will be activated and notifies the 'core processor' that there have been changes on the input pins. Read the input register. If P0 = 0 (temperature sensor has changed), then turn on LED and turn on switch.

3. Software code:

```
//System Power on
// write to PCA8574 with data 1010 0011b to set P[7:2] outputs and P[1:0] inputs
<S> <0100 0000> <ACK> <1010 0011> <ACK> <P> //Initial setting for PCA8574
```

```

while (INT == 1); //Monitor the interrupt pin. If INT = 1 do nothing
//When INT = 0 then read input ports
<S> <slave address read> <ACK> <1010 0010> <NACK> <P> //Read PCA8574 data
If (P0 == 0) //Temperature sensor activated
{
    // write to PCA8574 with data 0010 1011b to turn on LED (P7), on Switch (P3)
    and keep P[1:0] as input ports.
    <S> <0100 0000> <ACK> <0010 1011> <ACK> <P> // Write to PCA8574
}
    
```

10.3 High current-drive load applications

The GPIO has a minimum guaranteed sinking current of 25 mA per bit at 4.5 V. In applications requiring additional drive, two port pins may be connected together to sink up to 50 mA current. Both bits must then always be turned on or off together. Up to 8 pins can be connected together to drive 200 mA, which is the device recommended total limit. Each pin needs its own limiting resistor as shown in [Figure 16](#) to prevent damage to the device should all ports not be turned on at the same time.

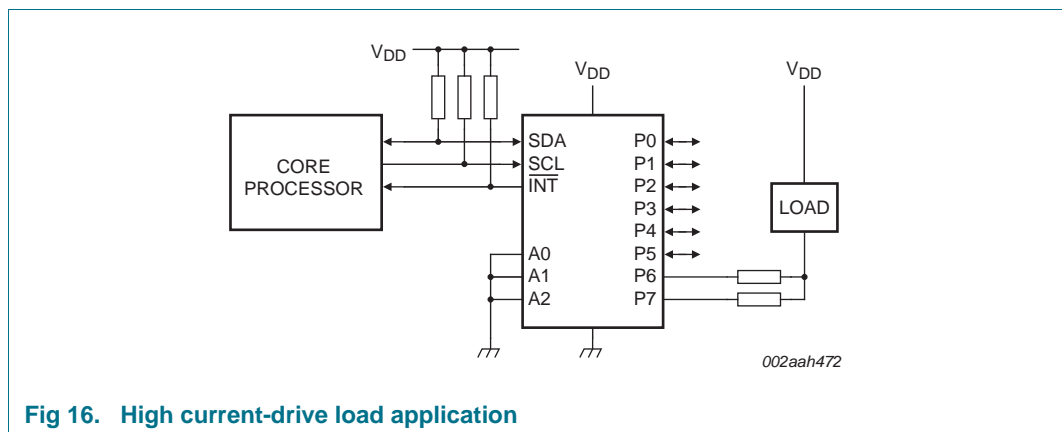


Fig 16. High current-drive load application

10.4 Migration path

NXP offers newer, more capable drop-in replacements for the PCF8574/74A in newer space-saving packages.

Table 6. Migration path

| Type number | I ² C-bus frequency | Voltage range | Number of addresses per device | Interrupt | Reset | Total package sink current |
|-------------|--------------------------------|----------------|--------------------------------|-----------|-------|----------------------------|
| PCF8574/74A | 100 kHz | 2.5 V to 6 V | 8 | yes | no | 80 mA |
| PCA8574/74A | 400 kHz | 2.3 V to 5.5 V | 8 | yes | no | 200 mA |
| PCA9674/74A | 1 MHz Fm+ | 2.3 V to 5.5 V | 64 | yes | no | 200 mA |
| PCA9670 | 1 MHz Fm+ | 2.3 V to 5.5 V | 64 | no | yes | 200 mA |
| PCA9672 | 1 MHz Fm+ | 2.3 V to 5.5 V | 16 | yes | yes | 200 mA |

PCA9670 replaces the interrupt output of the PCA9674 with a hardware reset input to retain the maximum number of addresses. The PCA9672 replaces address A2 of the PCA9674 with a hardware reset input to retain the interrupt, but limit the number of addresses.

11. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|------------------------------|------------|-----------------------|------|------|
| V _{DD} | supply voltage | | -0.5 | +6 | V |
| I _{DD} | supply current | | - | ±100 | mA |
| I _{SS} | ground supply current | | - | ±400 | mA |
| V _I | input voltage | | V _{SS} - 0.5 | 5.5 | V |
| I _I | input current | | - | ±20 | mA |
| I _O | output current | [1] | - | ±50 | mA |
| P _{tot} | total power dissipation | | - | 400 | mW |
| P/out | power dissipation per output | | - | 100 | mW |
| T _{j(max)} | maximum junction temperature | | - | 125 | °C |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| T _{amb} | ambient temperature | operating | -40 | +85 | °C |

[1] Total package (maximum) output current is 400 mA.

12. Thermal characteristics

Table 8. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|----------------------|---|-----------------|-----|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | SO16 package | 115 | °C/W |
| | | TSSOP16 package | 160 | °C/W |
| | | SSOP20 package | 136 | °C/W |

13. Static characteristics

Table 9. Static characteristics
 $V_{DD} = 2.3\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--|-----------------------------------|---|--------------|------|---------------|---------------|-------------|
| Supplies | | | | | | | |
| V_{DD} | supply voltage | | 2.3 | - | 5.5 | V | |
| I_{DD} | supply current | Operating mode; no load; $V_I = V_{DD}$ or V_{SS} ; $f_{SCL} = 400\text{ kHz}$; A0, A1, A2 = static H or L | - | 200 | 500 | μA | |
| I_{stb} | standby current | Standby mode; no load; $V_I = V_{DD}$ or V_{SS} ; $f_{SCL} = 0\text{ kHz}$ | - | 4.5 | 10 | μA | |
| V_{POR} | power-on reset voltage | | [1] | - | 1.8 | 2.0 | V |
| Input SCL; input/output SDA | | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.5 | - | +0.3 V_{DD} | V | |
| V_{IH} | HIGH-level input voltage | | 0.7 V_{DD} | - | 5.5 | V | |
| I_{OL} | LOW-level output current | $V_{OL} = 0.4\text{ V}$; $V_{DD} = 2.3\text{ V}$ | 20 | 35 | - | mA | |
| | | $V_{OL} = 0.4\text{ V}$; $V_{DD} = 3.0\text{ V}$ | 25 | 44 | - | mA | |
| | | $V_{OL} = 0.4\text{ V}$; $V_{DD} = 4.5\text{ V}$ | 30 | 57 | - | mA | |
| I_L | leakage current | $V_I = V_{DD}$ or V_{SS} | -1 | - | +1 | μA | |
| C_i | input capacitance | $V_I = V_{SS}$ | - | 5 | 10 | pF | |
| I/Os; P0 to P7 | | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.5 | - | +0.3 V_{DD} | V | |
| V_{IH} | HIGH-level input voltage | | 0.7 V_{DD} | - | 5.5 | V | |
| I_{OL} | LOW-level output current | $V_{OL} = 0.5\text{ V}$; $V_{DD} = 2.3\text{ V}$ | [2] | 12 | 26 | - | mA |
| | | $V_{OL} = 0.5\text{ V}$; $V_{DD} = 3.0\text{ V}$ | [2] | 17 | 33 | - | mA |
| | | $V_{OL} = 0.5\text{ V}$; $V_{DD} = 4.5\text{ V}$ | [2] | 25 | 40 | - | mA |
| $I_{OL(tot)}$ | total LOW-level output current | $V_{OL} = 0.5\text{ V}$; $V_{DD} = 4.5\text{ V}$ | [2] | - | - | 200 | mA |
| I_{OH} | HIGH-level output current | $V_{OH} = V_{SS}$ | -30 | -138 | -300 | μA | |
| $I_{trt(pu)}$ | transient boosted pull-up current | $V_{OH} = V_{SS}$; see Figure 8 | -0.5 | -1.0 | - | mA | |
| C_i | input capacitance | | [3] | - | 2.1 | 10 | pF |
| C_o | output capacitance | | [3] | - | 2.1 | 10 | pF |
| Interrupt INT (see Figure 8 and Figure 9) | | | | | | | |
| I_{OL} | LOW-level output current | $V_{OL} = 0.4\text{ V}$ | 3.0 | - | - | mA | |
| C_o | output capacitance | | - | 3 | 5 | pF | |
| Inputs A0, A1, A2 | | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.5 | - | +0.3 V_{DD} | V | |
| V_{IH} | HIGH-level input voltage | | 0.7 V_{DD} | - | 5.5 | V | |
| I_{LI} | input leakage current | | -1 | - | +1 | μA | |
| C_i | input capacitance | | - | 3.5 | 5 | pF | |

[1] The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all I/Os to logic 1 (with current source to V_{DD}).

[2] Each bit must be limited to a maximum of 25 mA and the total package limited to 200 mA due to internal busing limits.

[3] The value is not tested, but verified on sampling basis.

14. Dynamic characteristics

Table 10. Dynamic characteristics

$V_{DD} = 2.3\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; unless otherwise specified. Limits are for Fast-mode I²C-bus.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|------------|-----------------------------------|-----|-----|------|
| f _{SCL} | SCL clock frequency | | 0 | - | 400 | kHz |
| t _{BUF} | bus free time between a STOP and START condition | | 1.3 | - | - | μs |
| t _{HD;STA} | hold time (repeated) START condition | | 0.6 | - | - | μs |
| t _{SU;STA} | set-up time for a repeated START condition | | 0.6 | - | - | μs |
| t _{SU;STO} | set-up time for STOP condition | | 0.6 | - | - | μs |
| t _{HD;DAT} | data hold time | | 0 | - | - | ns |
| t _{VD;ACK} | data valid acknowledge time | | [1] 0.1 | - | 0.9 | μs |
| t _{VD;DAT} | data valid time | | [2] 50 | - | - | ns |
| t _{SU;DAT} | data set-up time | | 100 | - | - | ns |
| t _{LOW} | LOW period of the SCL clock | | 1.3 | - | - | μs |
| t _{HIGH} | HIGH period of the SCL clock | | 0.6 | - | - | μs |
| t _f | fall time of both SDA and SCL signals | | [3][4] 20 + 0.1C _b [5] | - | 300 | ns |
| t _r | rise time of both SDA and SCL signals | | 20 + 0.1C _b [5] | - | 300 | ns |
| t _{SP} | pulse width of spikes that must be suppressed by the input filter | | [6] - | - | 50 | ns |

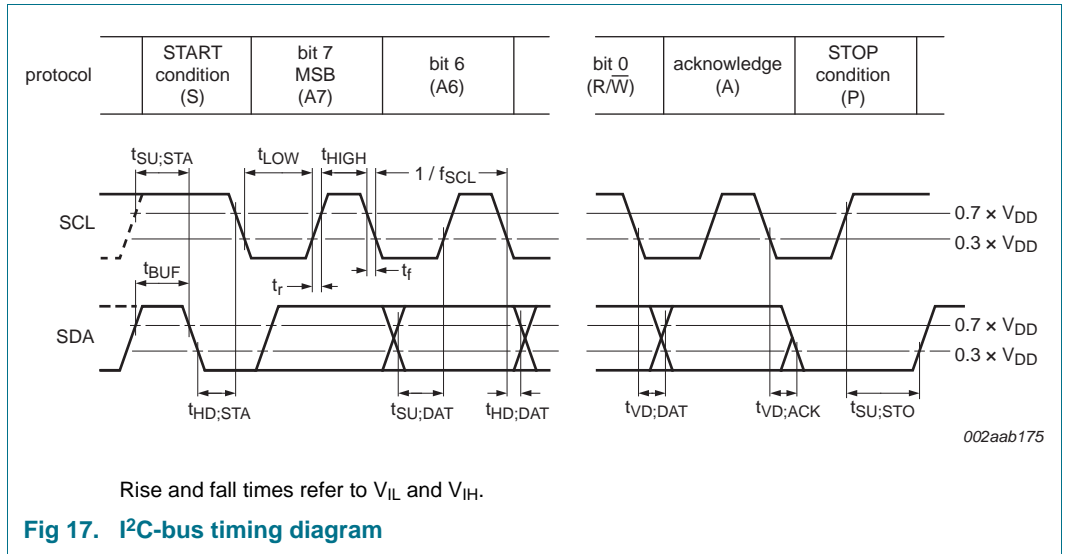
Port timing; C_L ≤ 100 pF (see Figure 8 and Figure 9)

| | | | | | | |
|--------------------|------------------------|--|---|---|---|----|
| t _{v(Q)} | data output valid time | | - | - | 4 | μs |
| t _{su(D)} | data input set-up time | | 0 | - | - | μs |
| t _{h(D)} | data input hold time | | 4 | - | - | μs |

Interrupt timing; C_L ≤ 100 pF (see Figure 8 and Figure 9)

| | | | | | | |
|-----------------------|---|--------------------------------------|---|---|---|----|
| t _{v(INT)} | valid time on pin $\overline{\text{INT}}$ | from port to $\overline{\text{INT}}$ | - | - | 4 | μs |
| t _{rst(INT)} | reset time on pin $\overline{\text{INT}}$ | from SCL to $\overline{\text{INT}}$ | - | - | 4 | μs |

- [1] t_{VD;ACK} = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
- [2] t_{VD;DAT} = minimum time for SDA data out to be valid following SCL LOW.
- [3] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.
- [4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
- [5] C_b = total capacitance of one bus line in pF.
- [6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.



15. Package outline

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1

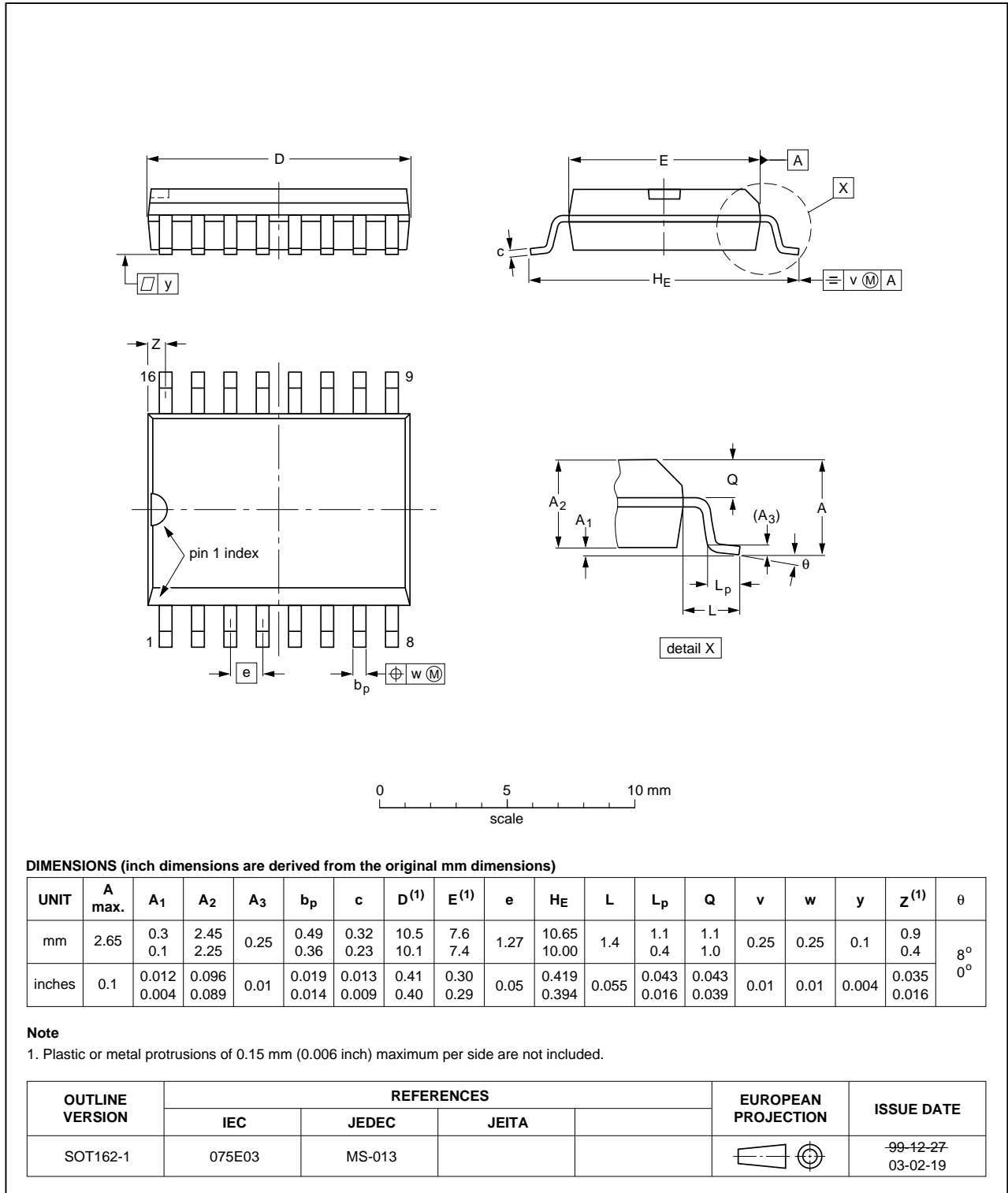


Fig 18. Package outline SOT162-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

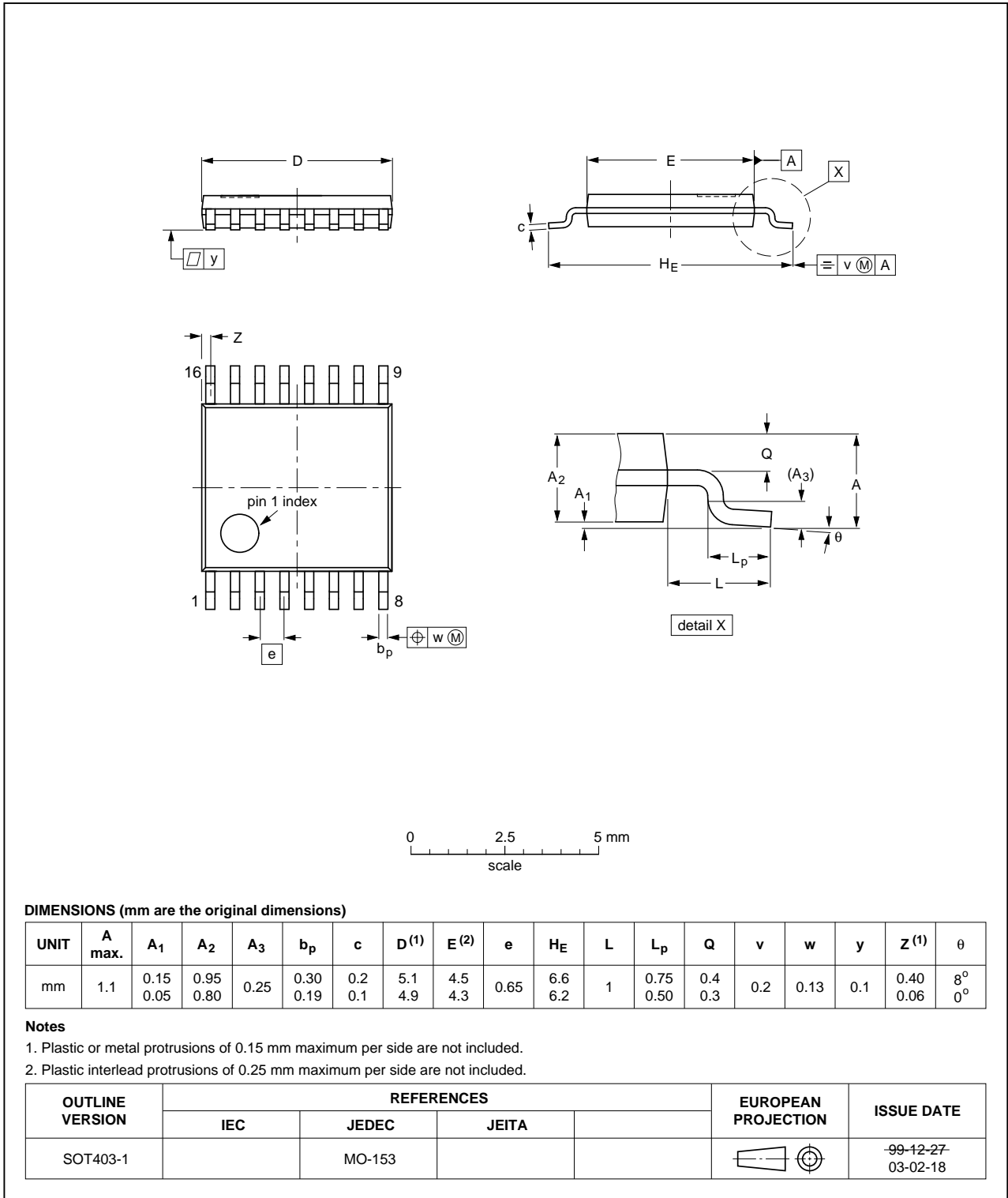


Fig 19. Package outline SOT403-1 (TSSOP16)

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1

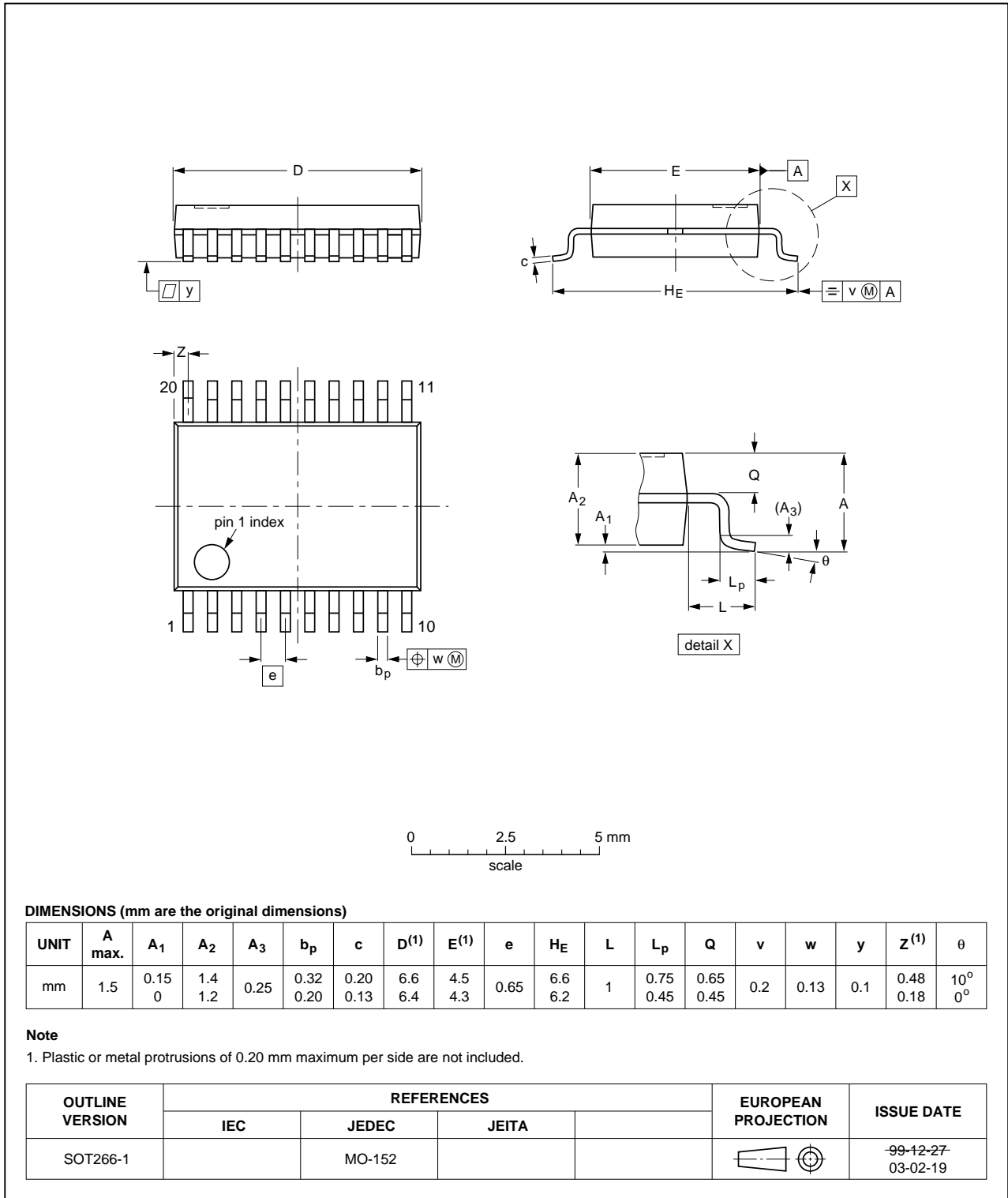


Fig 20. Package outline SOT266-1 (SSOP20)

16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 21](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 11](#) and [12](#)

Table 11. SnPb eutectic process (from J-STD-020D)

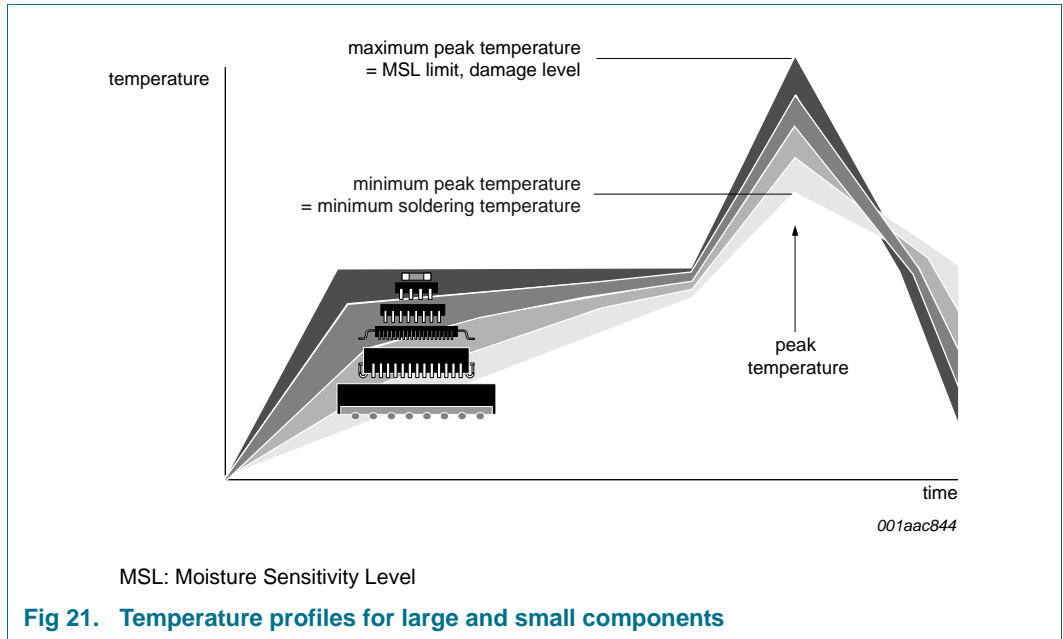
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 12. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 21](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

18. Soldering: PCB footprints

Footprint information for reflow soldering of SO16 package

SOT162-1

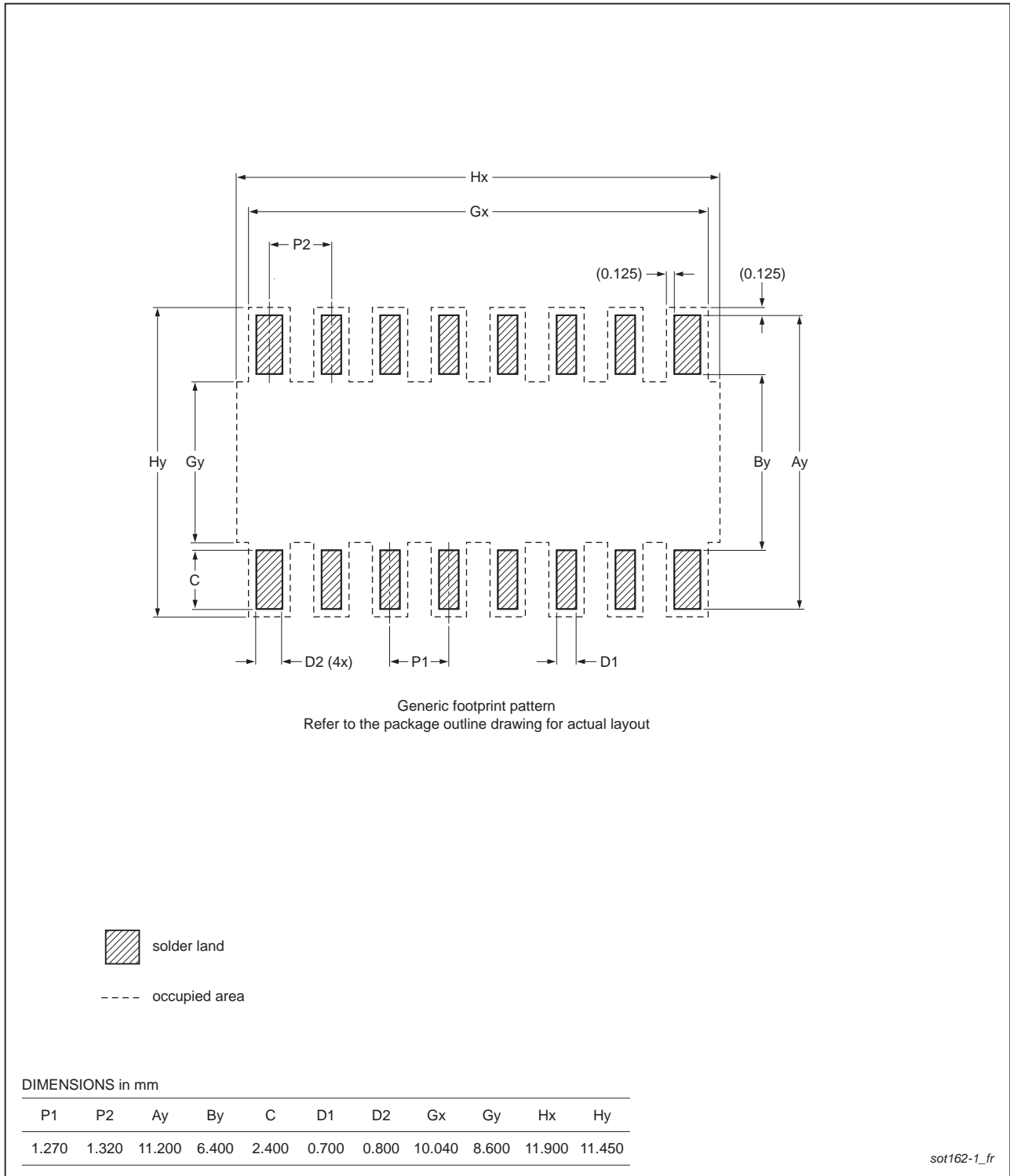


Fig 22. PCB footprint for SOT162-1 (SO16); reflow soldering

Footprint information for reflow soldering of TSSOP16 package

SOT403-1

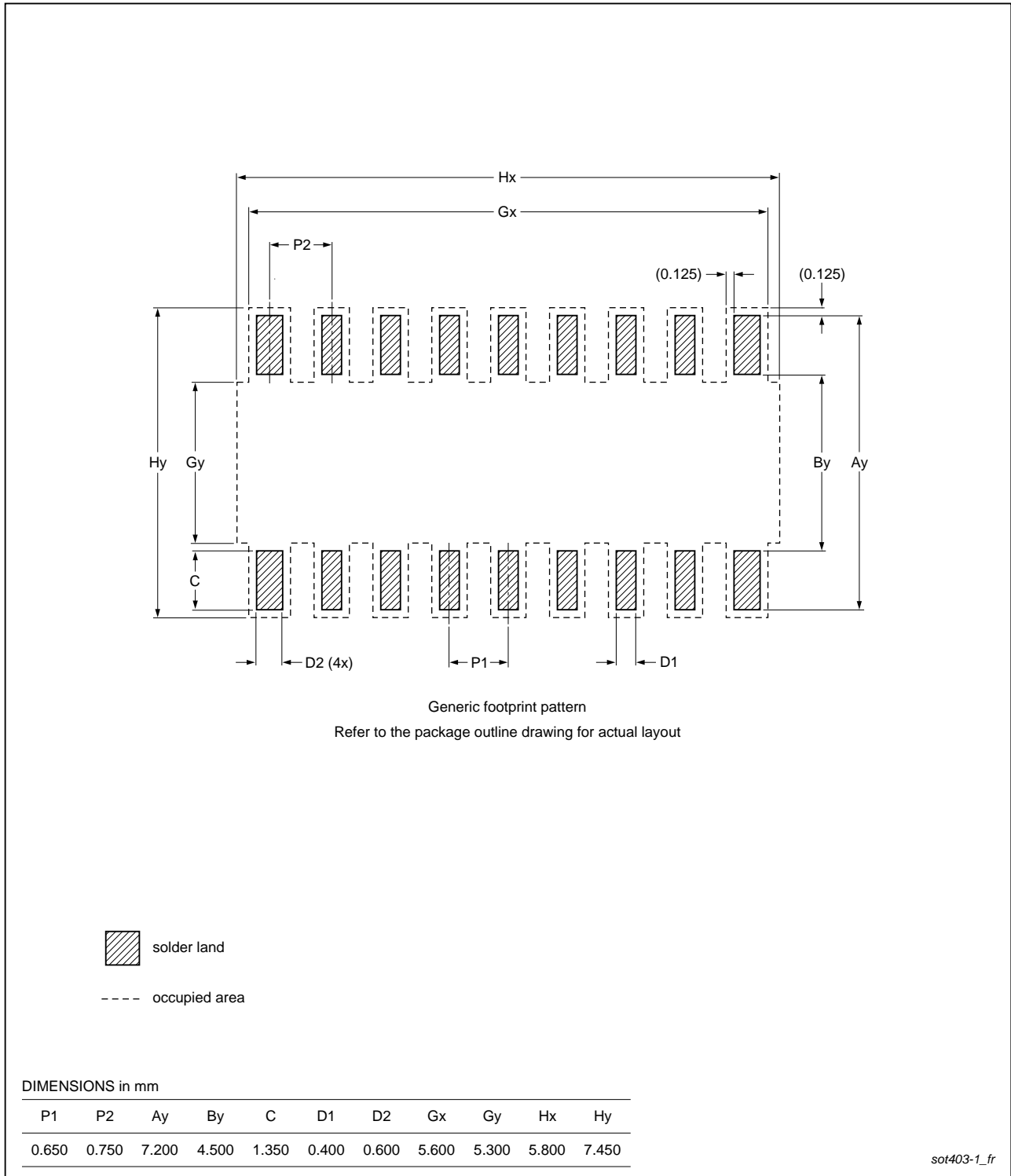


Fig 23. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

Footprint information for reflow soldering of SSOP20 package

SOT266-1



Fig 24. PCB footprint for SOT266-1 (SSOP20); reflow soldering

19. Abbreviations

Table 13. Abbreviations

| Acronym | Description |
|----------------------|---|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| FF | Flip-Flop |
| GPIO | General Purpose Input/Output |
| HBM | Human Body Model |
| I/O | Input/Output |
| I ² C-bus | Inter-Integrated Circuit bus |
| IC | Integrated Circuit |
| LED | Light Emitting Diode |
| LP | Low-Pass |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| PLC | Programmable Logic Controller |
| POR | Power-On Reset |
| SMBus | System Management Bus |

20. Revision history

Table 14. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------------|--------------|--------------------|---------------|----------------------|
| PCA8574_PCA8574A v.3 | 20130603 | Product data sheet | - | PCA8574_PCA8574A v.2 |

Modifications:

- [Section 1 “General description”](#) re-written
- [Section 2 “Features and benefits”](#)
 - added (new) first bullet item
 - appended “(Fast-mode I²C-bus)” to second bullet item
 - added (new) third bullet item
 - (new) fifth bullet item changed from “50 mA sink capability” to “25 mA sink capability”
 - deleted (old) eighth bullet item, “Readable device ID (manufacturer, device type, and revision)”
 - 12th bullet item: deleted phrase “200 V MM per JESD22-A115”
 - 14th bullet item: deleted “DIP16”
- [Table 1 “Ordering information”](#):
 - deleted discontinued DIP16 package option (PCA8574N, PCA8574AN)
 - Topside mark for PCA8574ATS corrected from “PCA8574A” to “PA8574A”
 - added [Table note \[1\]](#), [Table note \[2\]](#), [Table note \[3\]](#) and [Table note \[4\]](#)
- Added (new) [Table 2 “Ordering options”](#)
- [Figure 1 “Block diagram”](#) modified: switched positions of blocks “INTERRUPT LOGIC” and “LP FILTER”
- [Figure 2 “Simplified schematic diagram of P0 to P7”](#) modified: removed diode between “V_{DD}” and “P0 to P7” signal lines

Table 14. Revision history ...continued

| Document ID | Release date | Data sheet status | Change notice | Supersedes | |
|----------------------------|--|--------------------|---------------|----------------------|--|
| Modifications: (continued) | <ul style="list-style-type: none"> • Section 6.1 “Pinning”: <ul style="list-style-type: none"> – deleted (old) Figure 3, “Pin configuration for DIP16” – pin names changed from “AD0, AD1, AD2” to “A0, A1, A2”, respectively • Section 6.2 “Pin description”: (old) Table 3, “Pin description for SO16, TSSOP16” and (old) Table 4, “Pin description for SSOP20” are merged in (new) Table 3 “Pin description” • Section 7.1 “Device address” re-written • Section 7.1.1 “Address maps” re-written • Section 8.1 “Quasi-bidirectional I/Os” re-written • Section 8.2 “Writing to the port (Output mode)” re-written • Figure 8 “Write mode (output)”: timing measurement symbol corrected from “$t_{d(rst)}$” to “$t_{rst(INT)}$” • Section 8.3 “Reading from a port (Input mode)” re-written • Figure 9 “Read mode (input)”: <ul style="list-style-type: none"> – timing measurement symbol corrected from “$t_{v(D)}$” to “$t_{v(INT)}$” – timing measurement symbol corrected from “$t_{d(rst)}$” to “$t_{rst(INT)}$” • Section 8.4 “Power-on reset”: second and third sentences re-written • Figure 9 “Read mode (input)” modified: corrected label from “data into port” to “data at port” • Section 8.5 “Interrupt output (INT)”, fourth, fifth and sixth paragraphs re-written; added new seventh paragraph • Figure 10 “Application of multiple PCA8574/74As with interrupt” updated (changed from “device 8, PCA8574” to “device 16, PCA8574A”) • Added (new) Section 10.2 “How to read and write to I/O expander (example)” • Section 10.3 “High current-drive load applications”: <ul style="list-style-type: none"> – 1st sentence changed from “maximum sinking current of 25 mA per bit” to “minimum guaranteed sinking current of 25 mA per bit at 4.5 V” – 4th sentence changed from “device total limit” to “device recommended total limit” • Figure 16 “High current-drive load application” modified: added resistor on P6 and P7 signal lines • Added (new) Section 10.4 “Migration path” • Table 7 “Limiting values”: added $T_{j(max)}$ limits • Added Section 12 “Thermal characteristics” • Table 9 “Static characteristics”, sub-section “I/Os; P0 to P7”: added V_{IL} and V_{IH} characteristics • Table 10 “Dynamic characteristics”, sub-section “Interrupt timing”: <ul style="list-style-type: none"> – symbol/parameter corrected from “$t_{v(D)}$, data input valid time” to “$t_{v(INT)}$, valid time on pin \overline{INT}” – symbol/parameter corrected from “$t_{d(rst)}$, reset delay time” to “$t_{rst(INT)}$, reset time on pin \overline{INT}” • Figure 17 “I²C-bus timing diagram” updated: added $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$ reference lines • Deleted (old) Figure 18, “Package outline SOT38-1 (DIP16)” • Updated soldering information • Added Section 18 “Soldering: PCB footprints” | | | | |
| PCA8574_PCA8574A v.2 | 20070514 | Product data sheet | - | PCA8574_PCA8574A v.1 | |
| PCA8574_PCA8574A v.1 | 20070117 | Product data sheet | - | - | |

21. Legal information

21.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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