



# PCA9527

3-channel bidirectional bus extender for HDMI, I<sup>2</sup>C-bus and SMBus

Rev. 1.1 — 20 August 2021

Product data sheet

## 1 General description

The PCA9527 is a 3-channel bidirectional open-drain bus buffer for Display Data Control (DDC) clock, data and Consumer Electronic Control (CEC) for HDMI application. The device has two power supply pins to allow voltage level shift from 2.7 V to 5 V, and a rise time accelerator on port A of each DDC clock and data for driving longer cable (up to 18 meters or 1400 pF reliably without violating the bus rise time). The 5 V tolerant CEC channel is internally connected to  $V_{CC(B)}$  and has no rise time accelerator. The CEC channel can be used as an interrupt or reset.

While retaining all the operating modes and features of the I<sup>2</sup>C-bus system during the level shift, it also permits extension of the I<sup>2</sup>C-bus by providing bidirectional buffering for data (SDA), clock (SCL), and CEC. Using the PCA9527 enables the system designer to isolate bus capacitance to meet HDMI DDC version 1.3 distance specification. The SDAx and SCLx pins are overvoltage tolerant and are high-impedance when the PCA9527 is unpowered. The port B drivers (SDAB, SCLB, CECB) with static level offset behave much like the drivers on the PCA9515 device, while the SDAA and SCLA drivers integrate the rise time accelerator, sink more current and eliminate the static offset voltage. The CECA driver has the same current and static offset voltage features as the SDAA and SCLA, but it does not have the rise time accelerator and is powered and referenced to  $V_{CC(B)}$ . This results in a LOW on the port B translating into a nearly 0 V LOW on port A, providing zero offset. The static level offset design of the port B I/O drivers prevent them from being connected to another device that has rise time accelerator including the PCA9507 (port B), PCA9510, PCA9511, PCA9512, PCA9513, PCA9514, PCA9515, PCA9516A, PCA9517 (port B), or PCA9518A. Port A of two or more PCA9527s can be connected together, however, to allow a star topography with port A on the common bus, and port A can be connected directly to any other buffer with static or dynamic offset voltage. Multiple PCA9527s can be connected in series, port A to port B, with no build-up in offset voltage with only time of flight delays to consider. Rise time accelerators on the SDAA and SCLA pins are turned on when input threshold is above  $0.3V_{CC(A)}$ . The PCA9527 SDA and SCL drivers are not enabled unless  $V_{CC(A)}$  and  $V_{CC(B)}$  are above 2.7 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle. The output pull-down on the port B internal buffer LOW is set for approximately 0.5 V, while the input threshold of the internal buffer is set about 70 mV lower (0.43 V). When the port B I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring.

## 2 Features

- 3-channel, bidirectional buffer isolates capacitance allowing 1400 pF on port A and 400 pF on port B
- Exceeds 18 meters (above the maximum distance for HDMI DDC)
- Rise time accelerator and normal I/O on port A (no accelerator for CEC)



- Static level offset on port B
- Voltage level translation from 2.7 V to 5.5 V
- CEC is 5 V tolerant, powered by V<sub>CC(B)</sub>
- Upgrade replacement over PCA9507 and PCA9517A for cable application
- I<sup>2</sup>C-bus, SMBus and DDC-bus compatible
- Active HIGH buffer enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I<sup>2</sup>C-bus devices and multiple controllers
- Powered-off high-impedance I<sup>2</sup>C-bus pins
- Port A operating supply voltage range of 2.7 V to 5.5 V
- Port B operating supply voltage range of 2.7 V to 3.6 V
- 5 V tolerant I<sup>2</sup>C-bus and enable pins
- 0 Hz to 400 kHz clock frequency (the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater)
- ESD protection exceeds 8000 V HBM per JESD22-A114, 500 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Package offered: TSSOP10

### 3 Ordering information

Table 1. Ordering information

| Type number | Topside mark | Package                |  | Version  |
|-------------|--------------|------------------------|--|----------|
|             |              | Name                   | Description  |          |
| PCA9527DP   | 9527         | TSSOP10 <sup>[1]</sup> | plastic thin shrink small outline package; 10 leads; body width 3 mm | SOT552-1 |

[1] Also known as MSOP10.

Standard packing quantities and other packaging data are available at [www.nxp.com/packages/](http://www.nxp.com/packages/).

#### 3.1 Ordering options

Table 2. Ordering options

| Type number | Orderable part number         | Package | Packing method   | Minimum order quantity | Temperature                         |
|-------------|-------------------------------|---------|--|------------------------|-------------------------------------|
| PCA9527DP   | PCA9527DP, 118 <sup>[1]</sup> | TSSOP10 | REEL 13" Q1/T1<br>*STANDARD MARK SMD                       | 2500                   | T <sub>amb</sub> = -40 °C to +85 °C |
|             | PCA9527DPZ                    | TSSOP10 | REEL 13" Q1/T1<br>*STANDARD MARK SMD<br>SSB <sup>[2]</sup> | 2500                   | T <sub>amb</sub> = -40 °C to +85 °C |

[1] Discontinued in 202104010DN - drop in replacement is PCA9527DPZ - this is documented in PCN202104008A.

[2] This packing method uses a Static Shielding Bag (SSB) solution. Material should be kept in the sealed bag between uses.

## 4 Functional diagram

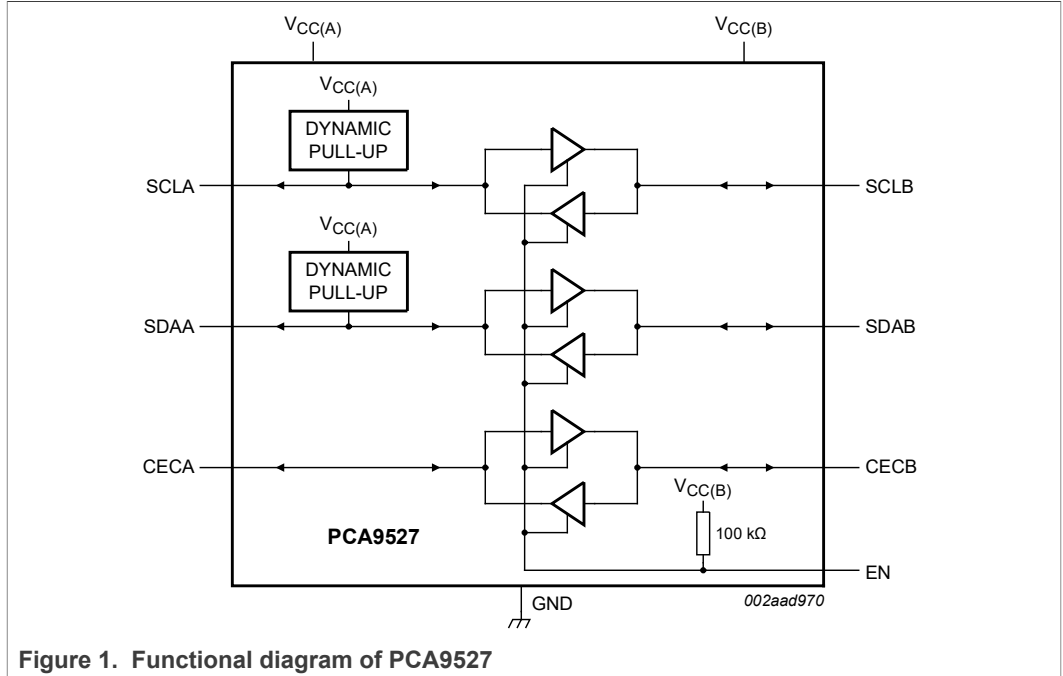


Figure 1. Functional diagram of PCA9527

## 5 Pinning information

### 5.1 Pinning

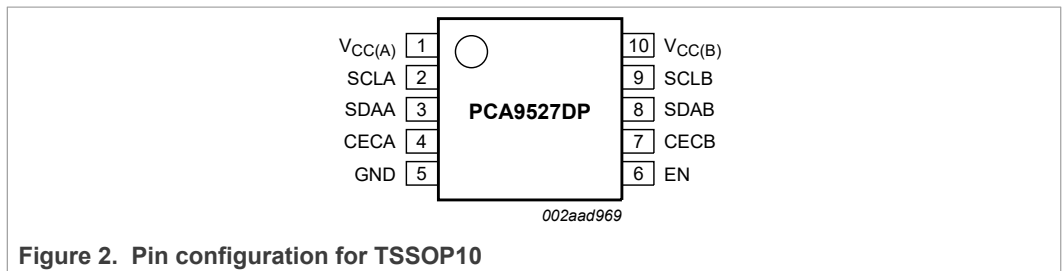


Figure 2. Pin configuration for TSSOP10

### 5.2 Pin description

Table 3. Pin description

| Symbol             | Pin | Description  |
|--------------------|-----|--|
| V <sub>CC(A)</sub> | 1   | port A supply voltage (2.7 V to 5.5 V)   |
| SCLA               | 2   | serial clock port A bus with rise time accelerator for DDC line or cable, 5 V tolerant |
| SDAA               | 3   | serial data port A bus with rise time accelerator for DDC line or cable, 5 V tolerant  |
| CECA               | 4   | serial data with normal I/O powered by V <sub>CC(B)</sub> , 5 V tolerant               |
| GND                | 5   | supply ground (0 V)  |

Table 3. Pin description...continued

| Symbol             | Pin | Description  |
|--------------------|-----|--|
| EN                 | 6   | active HIGH buffer enable input  |
| CECB               | 7   | serial data with static level offset, powered by V <sub>CC(B)</sub> , 5 V tolerant |
| SDAB               | 8   | serial data port B bus with static level offset, 5 V tolerant                      |
| SCLB               | 9   | serial clock port B bus with static level offset, 5 V tolerant                     |
| V <sub>CC(B)</sub> | 10  | port B supply voltage (2.7 V to 3.6 V)   |

## 6 Functional description

Refer to [Figure 1](#).

The PCA9527 consists of 3 channels of bidirectional open-drain I/Os specifically designed to support up-translation/down-translation between low voltages (as low as 2.7 V) and a 3.3 V or 5 V I<sup>2</sup>C-bus and SMBus. The device contains a rise time accelerator, specifically on port A of the SCLA and SDAA that enables the device to drive a long cable or a heavier capacitive load for DDC, I<sup>2</sup>C-bus and SMBus applications. With dual supply rails, the device translates from voltage ranges 2.7 V to 5.5 V down to a voltage as low as 2.7 V without degradation of system performance. Unlike the SDAA and SCLA, the CECA is powered by the V<sub>CC(B)</sub> and does not have a rise time accelerator, but is similar in that its port A has normal I/O and port B static level offset. All I/Os are overvoltage tolerant to 5.5 V even when the device is un-powered (V<sub>CC(B)</sub> and/or V<sub>CC(A)</sub> = 0 V).

The PCA9527 includes a power-up circuit that keeps the SDA and SCL output drivers turned off until V<sub>CC(A)</sub> and V<sub>CC(B)</sub> rise above 2.7 V. The CECA output drivers are turned OFF until V<sub>CC(B)</sub> rises above 2.7 V. V<sub>CC(A)</sub> and V<sub>CC(B)</sub> can be applied in any sequence at power-up.

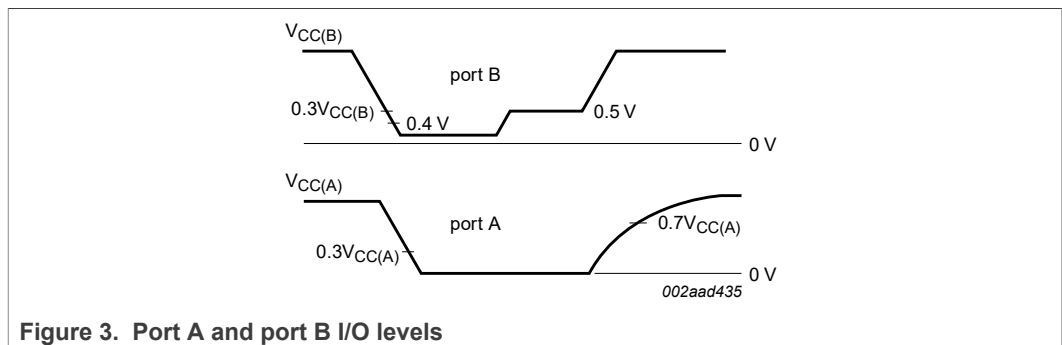


Figure 3. Port A and port B I/O levels

When port B falls first and goes below 0.3V<sub>CC(B)</sub> the port A driver is turned on and port A pulls down to 0 V. As port A falls below 0.3V<sub>CC(A)</sub> the port B pulls down to about 0.5 V. The external port B driver must drive the port B to a LOW that is ≤ 0.4 V or else it is not possible to know who is driving the port A LOW. The PCA9527 direction control assumes that port A is controlling the part unless port B falls below 0.4 V. When the port B voltage is ≤ 0.4 V the port A driver of the PCA9527 is on and holds port A down to nearly 0 V. As the port B voltage rises because the external driver turns off, the port B voltage rises up to ~0.5 V because port A is LOW; once port B rises to ~0.5 V the port A pull-down driver turns off. Then port A rises with a rise time determined by the RC of port A when it crosses the port A threshold ~0.3V<sub>CC(A)</sub> the port B driver is turned off and the rising edge accelerator is turned on, which causes a faster rising edge until it reaches the turn-off

point for the rising edge accelerator  $\sim 0.7V_{CC(A)}$ . Then it continues to rise at the slower rate determined by the RC of port A. When the port B driver turns off, port B rises with the RC of port B.

$V_{CC(A)}$  powers the  $0.3V_{CC(A)}$  reference for SCLA and SDAA as well as the port A power good detect circuit.  $V_{CC(B)}$  powers the rest of the chip including the port B I/Os, the CEC I/Os, and the support functions. [Figure 3](#) illustrates the threshold and I/O levels for port A and port B.

### 6.1 Enable

The EN pin is active HIGH with an internal  $\sim 100\text{ k}\Omega$  pull-up to  $V_{CC(B)}$  and allows the user to select when the buffer is active. The enable pin puts the PCA9527 in a power-down state when it is disabled, so that there is a recovery delay and a lower power-down power. This can be used to isolate the line when the HDMI DDC transmitter or receiver is not ready, or from a badly behaved target on power-up until after the system power-up reset. It should never change state during an I<sup>2</sup>C-bus operation, because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I<sup>2</sup>C-bus parts being enabled. The enable pin should only change state when the global bus and the buffer port are in an idle state, to prevent system failures.

### 6.2 Rise time accelerators

PCA9527 has rise time accelerators on port A of SCL and SDA only; the CECA pin does not have a rise time accelerator. During port A positive bus transitions a current source is switched on to quickly slew the SDAA and SCLA lines HIGH once the input level of  $0.3V_{CC(A)}$  is exceeded for the PCA9527 and turns off as the  $0.7V_{CC(A)}$  voltage is approached.

### 6.3 Resistor pull-up value selection

#### 6.3.1 Port A (SDAA and SCLA)

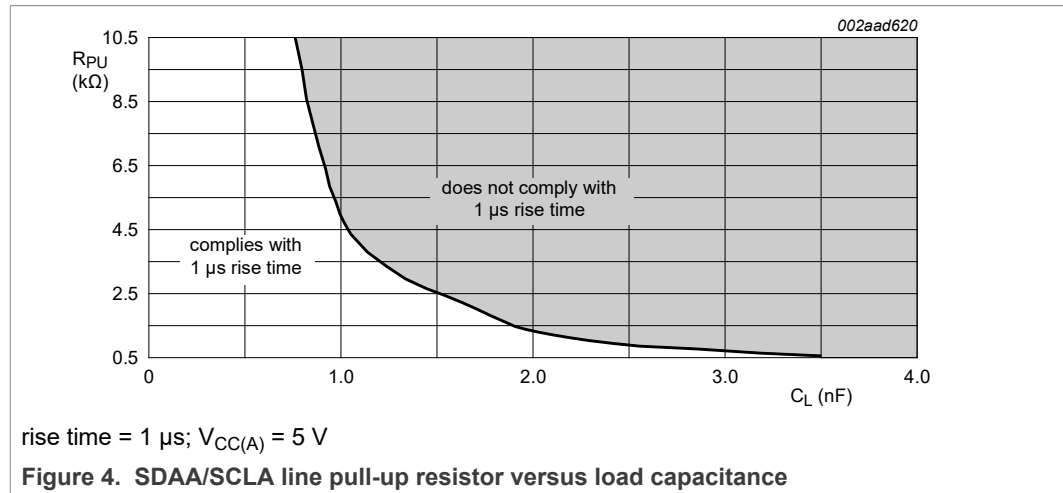
SDAA and SCLA are open-drain I/O that have rise time accelerators and strong pull-down. When the inputs transition above  $0.3V_{CC(A)}$ , the rise time accelerator activates and boosts the pull-up current during rising edge to meet the I<sup>2</sup>C-bus rise time specification when the device drives a long cable or heavier capacitance load. The strong pull-down enables the output to drive to nearly zero voltage for logic LOW. The selection for pull-up resistors are defined in the HDMI DDC specification shown in [Table 4](#). For HDMI transmitter applications like digital video player, recorder, or set-top box, the pull-up resistor is in the range of  $1.5\text{ k}\Omega$  to  $2\text{ k}\Omega$ . For HDMI receiver applications like in LCD TV or video card, the pull-up resistor is  $47\text{ k}\Omega$  on the SCLA line, and there is no pull-up on the SDAA line. Please refer to [Table 4](#), [Figure 6](#) and [Figure 7](#) for more details. [Figure 4](#) shows the port A pull-up resistor values (in  $\text{k}\Omega$ ) versus capacitance load (in  $\text{nF}$ ) for  $5\text{ V}$  supply voltage complied with  $1\text{ }\mu\text{s}$  rise time per I<sup>2</sup>C-bus Standard-mode specification. The graph contrasts a shaded and unshaded region. Any resistor value chosen within the unshaded region would comply with  $1\text{ }\mu\text{s}$  rise time, while any value chosen in the shaded region would not.

**Table 4. HDMI DDC pull-up resistors specification**

| Pin  | Where                   | Minimum              | Maximum              |
|------|-------------------------|----------------------|----------------------|
| SDAA | at the source (DVD/STB) | $1.5\text{ k}\Omega$ | $2.0\text{ k}\Omega$ |

Table 4. HDMI DDC pull-up resistors specification...continued

| Pin  | Where                   | Minimum      | Maximum |
|------|-------------------------|--------------|---------|
|      | at the sink (LCD TV)    | -            | -       |
| SCLA | at the source (DVD/STB) | 1.5 kΩ       | 2.0 kΩ  |
|      | at the sink (LCD TV)    | 47 kΩ ± 10 % |         |



### 6.3.2 Port A (CECA)

CECA does not have a rise time accelerator, but has a standard open-drain I/O. In addition to incurring no offset voltage, it has edge rate control and a lower capacitance than those of standard discrete MOSFET, and isolates the input/output capacitance. It is designed for a lower speed channel for consumer electronic control (less than 10 kHz) or general purpose interrupt or reset over long cable.

CECA does not have internal pull-up. The pull-up resistor is calculated using standard I<sup>2</sup>C-bus pull-up resistor formula, as shown in [Section 6.3.3CECB](#)".

### 6.3.3 Port B (SDAB, SCLB, CECB)

SDAB and SCLB are standard I<sup>2</sup>C-bus with static level offset that has no rise time accelerator. The static level offset produces an output LOW of 0.5 V (typical) at 6 mA. As with the standard I<sup>2</sup>C-bus system, pull-up resistors are required to provide the logic HIGH levels. The size of these pull-up resistors depends on the system requirement, and should meet the current sinking capability of the device that drives the buffer, as well as that of the buffer. The minimum and maximum pull-up resistors are determined and the pull-up resistor's value is chosen to be within the minimum and maximum range.

Using [Equation 1](#), calculate the minimum pull-up resistor value:

$$R_{PU(min)} = \frac{V_{pu(max)} - 0.4V}{I_{OL(max)}} \quad (1)$$

Where:

R<sub>PU(min)</sub> is the minimum pull-up resistor value for the open-drain SCLB and SDAB.

$V_{PU(max)}$  is the maximum supply rail of the pull-up resistor and should not exceed 5.5 V.

0.4 V is the maximum  $V_{OL}$  of the device that drives the buffer on logic LOW.

$I_{OL(max)}$  at  $V_{OL} = 0.4$  V is the maximum sink current of the device that drives the buffer on logic LOW.

The maximum pull-up resistor should also be sized such that the RC time constant meets the standard I<sup>2</sup>C-bus rise time, which is 1 μs for Standard-mode (100 kHz) or 300 ns for Fast-mode (400 kHz). DDC bus complies with the I<sup>2</sup>C-bus Standard-mode and operates below 100 kHz, and maximum rise time is 1 μs using a simplified RC equation.

Using Equation 2, calculate the maximum pull-up resistor value:

$$R_{PU(max)} \times C_{L(max)} = 1.2 \times t_r \quad (2)$$

Where:

$R_{PU(max)}$  is the maximum allowable pull-up resistor on the SCLB and SDAB in order to meet the I<sup>2</sup>C-bus rise time specification.

$C_{L(max)}$  is the maximum allowable capacitance load (include the capacitance of driver, the line, and the buffer) in order to meet the rise time specification.

$t_r$  is the rise time specified as 1 μs (for bus speed 100 kHz or lower) and 300 ns (for bus speed 400 kHz or lower).

The chosen pull-up resistor  $R_{PU}$  is:  $R_{PU(min)} \leq R_{PU} \leq R_{PU(max)}$ .

## 7 Application design-in information

A typical application is shown in Figure 5. In this example, the system controller is running on a 3.3 V I<sup>2</sup>C-bus while the target is connected to a 5 V bus. Both buses run at 400 kHz. Controller devices can be placed on either bus. HDMI DDC applications for DVD/R and LCD TV are shown in Figure 6 and Figure 7, respectively. In these applications the HDMI transmitter or receiver is 3.3 V, while the DDC line is 5 V, PCA9527 behaves like a voltage level shifter, a buffer and long cable bus extender to ensure signal integrity for accessing the EDID on the DDC line.

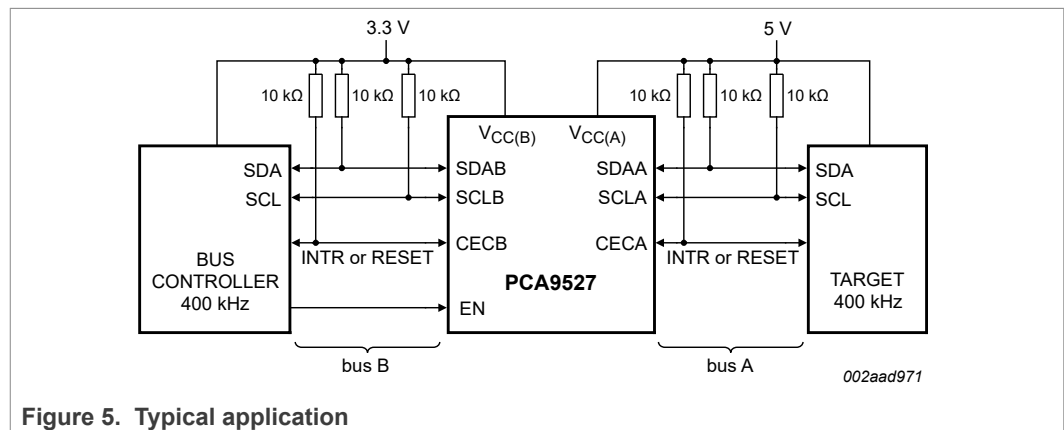


Figure 5. Typical application

3-channel bidirectional bus extender for HDMI, I<sup>2</sup>C-bus and SMBus

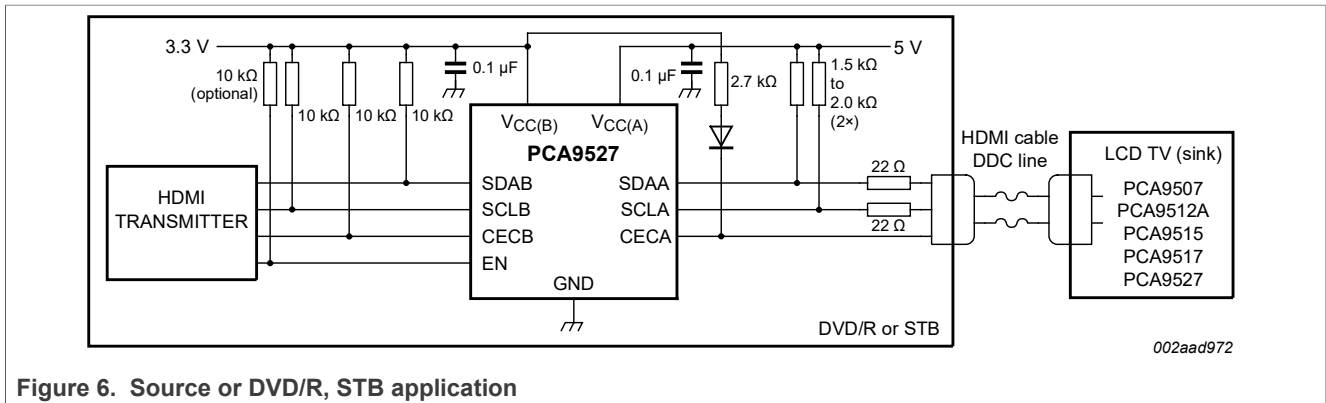


Figure 6. Source or DVD/R, STB application

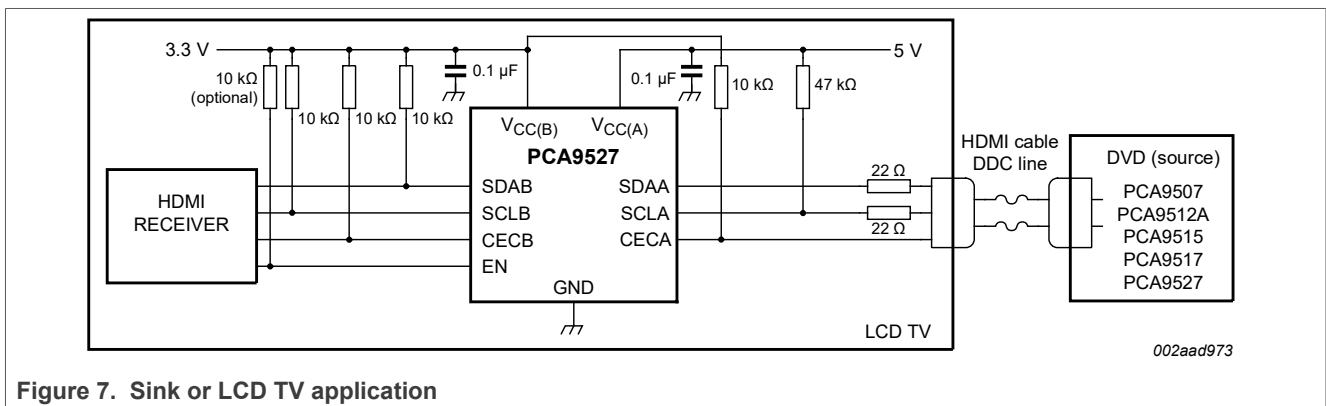


Figure 7. Sink or LCD TV application

According to [Figure 5](#), when port A of the PCA9527 is pulled LOW by a driver on the I<sup>2</sup>C-bus, a comparator detects the falling edge when it goes below 0.3V<sub>CC(A)</sub> and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PCA9527 falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground. In order to illustrate what would be seen in a typical application, refer to [Figure 11](#) and [Figure 12](#).

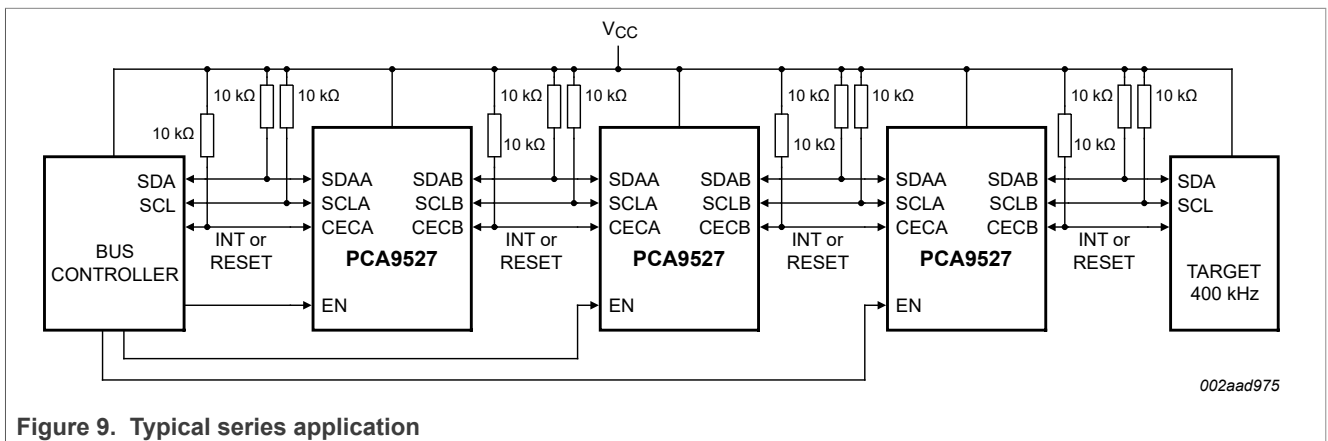
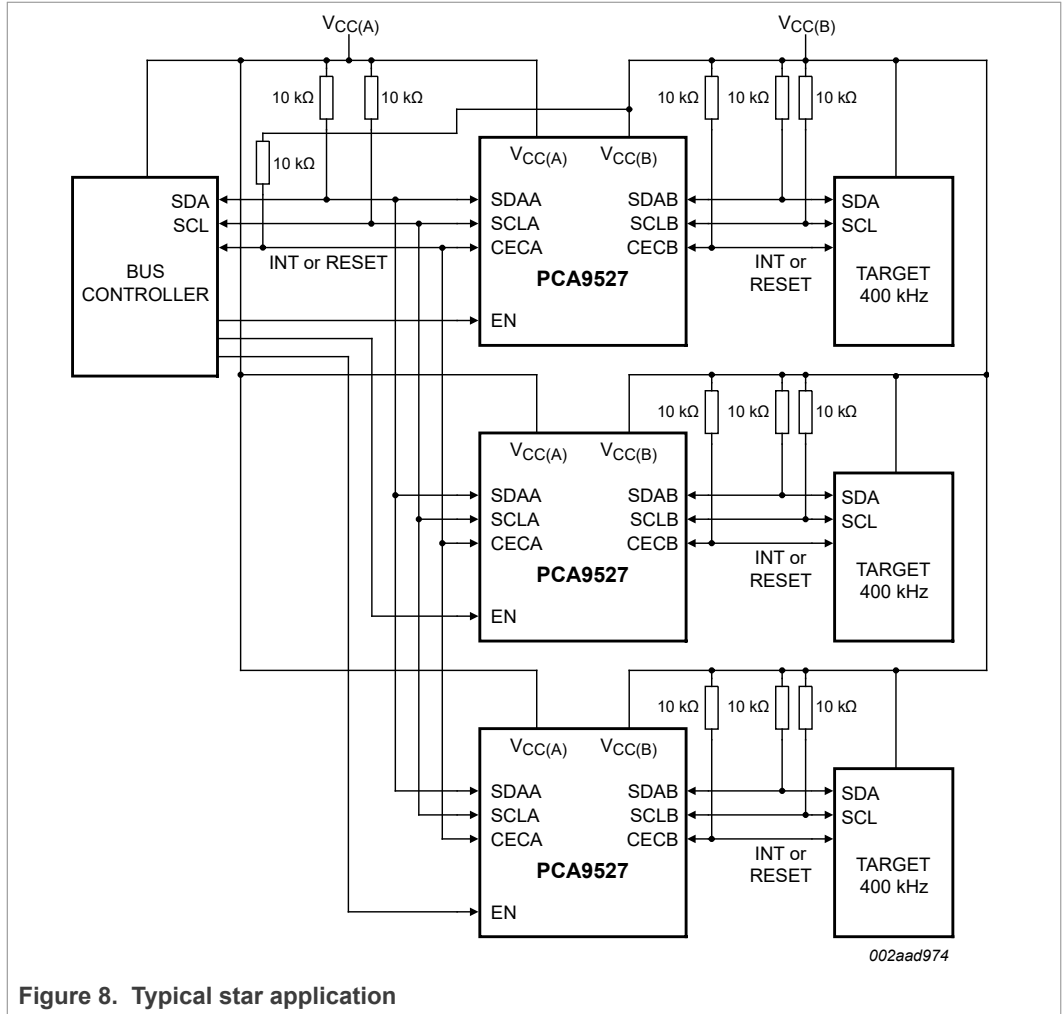
If the bus controller in [Figure 5](#) were to write to the target through the PCA9527, waveforms shown in [Figure 11](#) would be observed on the A bus. This looks like a normal I<sup>2</sup>C-bus transmission except that the HIGH level may be as low as 2.7 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

The controller drives the B bus to ground or lets it float to V<sub>CC(B)</sub> as it sends data to the target at the falling edge of the 8<sup>th</sup> clock, controller releases SDAB on the B bus and target pulls SDAA on the A bus to ground, causing the PCA9527 to pull SDAB on the B bus to 0.5 V. At the falling edge of the 9<sup>th</sup> clock, the controller again drives the B bus and target releases the A bus.

Multiple PCA9527 port A sides can be connected in a star configuration ([Figure 8](#)), allowing all nodes to communicate with each other.

Multiple PCA9527s can be connected in series ([Figure 9](#)) as long as port A is connected to port B. I<sup>2</sup>C-bus target devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.





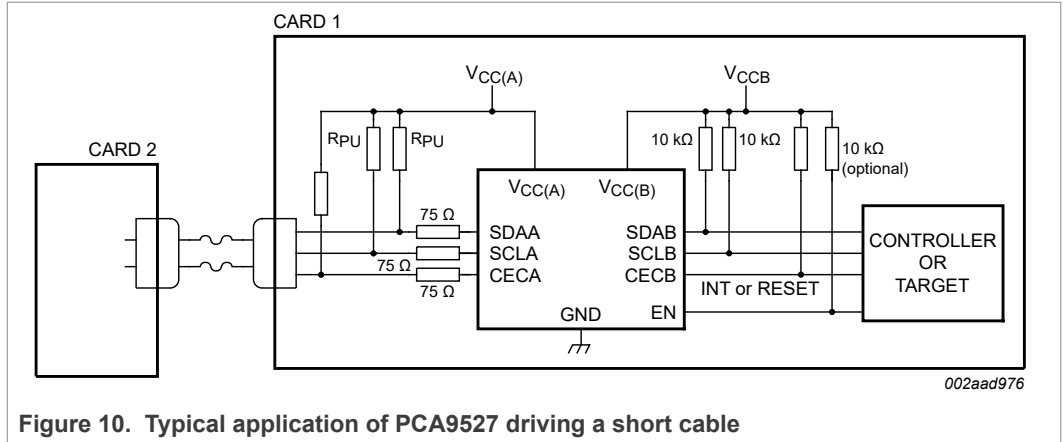


Figure 10. Typical application of PCA9527 driving a short cable

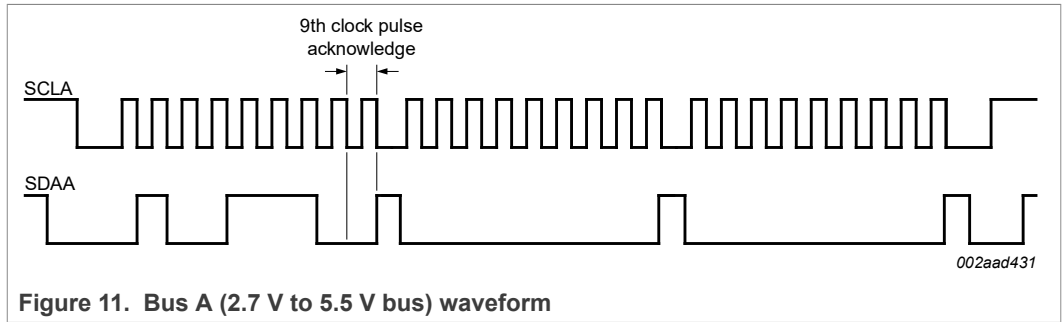


Figure 11. Bus A (2.7 V to 5.5 V bus) waveform

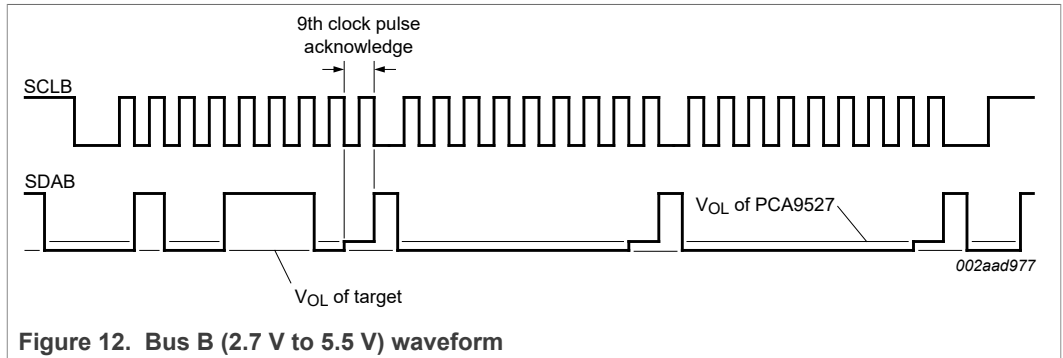


Figure 12. Bus B (2.7 V to 5.5 V) waveform

## 8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol             | Parameter                      | Conditions         | Min  | Max | Unit |
|--------------------|--------------------------------|--------------------|------|-----|------|
| V <sub>CC(B)</sub> | supply voltage port B          |                    | -0.5 | +7  | V    |
| V <sub>CC(A)</sub> | supply voltage port A          |                    | -0.5 | +7  | V    |
| V <sub>I/O</sub>   | voltage on an input/output pin | port B; port A; EN | -0.5 | +7  | V    |
| I <sub>I/O</sub>   | input/output current           | port A; port B     | -    | 50  | mA   |

Table 5. Limiting values...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol           | Parameter               | Conditions            | Min | Max  | Unit |
|------------------|-------------------------|-----------------------|-----|------|------|
| I <sub>SS</sub>  | ground supply current   |                       | -   | 100  | mA   |
| P <sub>tot</sub> | total power dissipation |                       | -   | 100  | mW   |
| T <sub>stg</sub> | storage temperature     |                       | -55 | +125 | °C   |
| T <sub>amb</sub> | ambient temperature     | operating in free air | -40 | +85  | °C   |
| T <sub>j</sub>   | junction temperature    |                       | -   | +125 | °C   |

## 9 Static characteristics

Table 6. Static characteristics

V<sub>CC</sub> = 2.7 V to 5.5 V; GND = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified.

| Symbol                                      | Parameter                          | Conditions  | Min                   | Typ | Max                    | Unit |
|---|------------------------------------|---|-----------------------|-----|------------------------|------|
| <b>Supplies</b>                             |                                    |   |                       |     |                        |      |
| V <sub>CC(B)</sub>                          | supply voltage port B              |   | 2.7                   | -   | 3.6                    | V    |
| V <sub>CC(A)</sub>                          | supply voltage port A              |   | <sup>[1]</sup> 2.7    | -   | 5.5                    | V    |
| I <sub>stb</sub>                            | standby current                    | inputs ≥ V <sub>CC</sub> or GND on pin V <sub>CC(A)</sub> ;<br>EN = 0 V   | -                     | 40  | 60                     | μA   |
| I <sub>CCH(A)</sub>                         | port A HIGH-level supply current   |   | -                     | 0.5 | 0.8                    | mA   |
| I <sub>CCL(A)</sub>                         | port A LOW-level supply current    | A port channels LOW; V <sub>CC(B)</sub> = 3.6 V;<br>V <sub>CC(A)</sub> = 5.5 V; B port open                                     | -                     | 1.1 | 1.7                    | mA   |
| I <sub>stb</sub>                            | standby current                    | inputs ≥ V <sub>CC</sub> or GND on pin V <sub>CC(B)</sub> ;<br>EN = 0 V   | -                     | 40  | 60                     | μA   |
| I <sub>CCH(B)</sub>                         | port B HIGH-level supply current   | all inputs HIGH; V <sub>CC(B)</sub> = 3.6 V;<br>SDAA = SCLA = V <sub>CC(A)</sub> ; SDAB,<br>SCLB, CECn, EN = V <sub>CC(B)</sub> |                       |     |                        |      |
|   |                                    | V <sub>CC(A)</sub> = 5 V  | -                     | 0.8 | 1.2                    | mA   |
|   |                                    | V <sub>CC(A)</sub> = 0 V  | -                     | 0.5 | 0.7                    | mA   |
| I <sub>CCL(B)</sub>                         | port B LOW-level supply current    | B port channels LOW; V <sub>CC(B)</sub> = 3.6 V;<br>A port open   |                       |     |                        |      |
|   |                                    | V <sub>CC(A)</sub> = 5 V  | -                     | 1.4 | 2.2                    | mA   |
|   |                                    | V <sub>CC(A)</sub> = 0 V  | -                     | 0.7 | 1.1                    | mA   |
| I <sub>CC(B)c</sub>                         | contention port B supply current   | V <sub>CC(B)</sub> = 3.6 V; SDAB = SCLB =<br>0.2 V  | -                     | 1.4 | 2.2                    | mA   |
| <b>Input and output SDAB, SCLB and CECB</b> |                                    |   |                       |     |                        |      |
| V <sub>IH</sub>                             | HIGH-level input voltage           |   | 0.7V <sub>CC(B)</sub> | -   | 5.5                    | V    |
| V <sub>IL</sub>                             | LOW-level input voltage            |   | <sup>[2]</sup> -0.5   | -   | +0.3V <sub>CC(B)</sub> | V    |
| V <sub>ILc</sub>                            | contention LOW-level input voltage |   | -0.5                  | 0.4 | -                      | V    |
| V <sub>IK</sub>                             | input clamping voltage             | I <sub>I</sub> = -18 mA   | -                     | -   | -1.2                   | V    |
| I <sub>LI</sub>                             | input leakage current              | V <sub>I</sub> = 5.5 V  | -                     | -   | ±1                     | μA   |

**Table 6. Static characteristics...continued**

$V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                             | Parameter  | Conditions  | Min                 | Typ  | Max             | Unit          |
|------------------------------------|--|---|---------------------|------|-----------------|---------------|
| $I_{IL}$                           | LOW-level input current  | $V_I = 0.2\text{ V}$  | -                   | -    | 10              | $\mu\text{A}$ |
| $V_{OL}$                           | LOW-level output voltage   | $I_{OL} = 100\text{ }\mu\text{A or }6\text{ mA}$                                      | 0.47                | 0.52 | 0.6             | V             |
| $V_{OL}-V_{ILc}$                   | difference between LOW-level output and LOW-level input voltage contention | guaranteed by design  | -                   | -    | 70              | mV            |
| $C_{io}$                           | input/output capacitance   | $V_I = 3\text{ V or }0\text{ V}$ ; $V_{CC} = 3.3\text{ V}$                            | -                   | 6    | 8               | pF            |
|                                    |  | $V_I = 3\text{ V or }0\text{ V}$ ; $V_{CC} = 0\text{ V}$                              | -                   | 6    | 8               | pF            |
| <b>Input and output SDAA, SCLA</b> |  |   |                     |      |                 |               |
| $V_{IH}$                           | HIGH-level input voltage   |   | $0.7V_{CC(A)}$      | -    | 5.5             | V             |
| $V_{IL}$                           | LOW-level input voltage  |   | <sup>[3]</sup> -0.5 | -    | $+0.3V_{CC(A)}$ | V             |
| $V_{IK}$                           | input clamping voltage   | $I_I = -18\text{ mA}$   | -                   | -    | -1.2            | V             |
| $I_{LI}$                           | input leakage current  | $V_{CC} = V_I = 5.5\text{ V}$   | -                   | -    | $\pm 1$         | $\mu\text{A}$ |
| $I_{IL}$                           | LOW-level input current  | $V_I = 0.2\text{ V}$  | -                   | -    | 10              | $\mu\text{A}$ |
| $V_{OL}$                           | LOW-level output voltage   | $I_{OL} = 6\text{ mA}$  | -                   | 0.1  | 0.2             | V             |
| $C_{io}$                           | input/output capacitance   | $V_I = 3\text{ V or }0\text{ V}$ ; $V_{CC} = 3.3\text{ V}$                            | -                   | 6    | 8               | pF            |
|                                    |  | $V_I = 3\text{ V or }0\text{ V}$ ; $V_{CC} = 0\text{ V}$                              | -                   | 6    | 8               | pF            |
| $I_{trt(pu)}$                      | transient boosted pull-up current  | SCLA, SDAA only; $V_{CC(A)} = 4.5\text{ V}$ ; slew rate = $1.25\text{ V}/\mu\text{s}$ | -                   | 6    | -               | mA            |
| <b>Input and output CECA</b>       |  |   |                     |      |                 |               |
| $V_{IH}$                           | HIGH-level input voltage   |   | $0.7V_{CC(B)}$      | -    | 5.5             | V             |
| $V_{IL}$                           | LOW-level input voltage  |   | <sup>[3]</sup> -0.5 | -    | $+0.3V_{CC(B)}$ | V             |
| $V_{IK}$                           | input clamping voltage   | $I_I = -18\text{ mA}$   | -                   | -    | -1.2            | V             |
| $I_{LI}$                           | input leakage current  | $V_{CC} = V_I = 5.5\text{ V}$   | -                   | -    | $\pm 1$         | $\mu\text{A}$ |
| $I_{IL}$                           | LOW-level input current  | $V_I = 0.2\text{ V}$  | -                   | -    | 10              | $\mu\text{A}$ |
| $V_{OL}$                           | LOW-level output voltage   | $I_{OL} = 6\text{ mA}$  | -                   | 0.1  | 0.2             | V             |
| $C_{io}$                           | input/output capacitance   | $V_I = 3\text{ V or }0\text{ V}$ ; $V_{CC} = 3.3\text{ V}$                            | -                   | 6    | 8               | pF            |
|                                    |  | $V_I = 3\text{ V or }0\text{ V}$ ; $V_{CC} = 0\text{ V}$                              | -                   | 6    | 8               | pF            |
| <b>Enable</b>                      |  |   |                     |      |                 |               |
| $V_{IL}$                           | LOW-level input voltage  |   | -0.5                | -    | $+0.3V_{CC(B)}$ | V             |
| $V_{IH}$                           | HIGH-level input voltage   |   | $0.7V_{CC(B)}$      | -    | 5.5             | V             |
| $I_{IL(EN)}$                       | LOW-level input current on pin EN  | $V_I = 0.2\text{ V}$ , EN pin only; $V_{CC} = 3.6\text{ V}$                           | -                   | -10  | -30             | $\mu\text{A}$ |
| $I_{LI}$                           | input leakage current  | $V_I = V_{CC}$  | -1                  | -    | +1              | $\mu\text{A}$ |
| $C_i$                              | input capacitance  | $V_I = 3.0\text{ V or }0\text{ V}$  | -                   | 2    | 5               | pF            |

[1] LOW-level supply voltage.

[2]  $V_{IL}$  specification is for the first LOW level seen by the SDAB/SCLB/CECB lines.  $V_{ILc}$  is for the second and subsequent LOW levels seen by the SDAB/SCLB/CECB lines to retain a valid LOW level the static level must be less than  $V_{ILc}$ .

[3]  $V_{IL}$  for port A with envelope noise must be below  $0.3V_{CC(A)}$  for stable performance.

## 10 Dynamic characteristics

Table 7. Dynamic characteristics

$V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.<sup>[1][2]</sup>

| Symbol                   | Parameter                               | Conditions  | Min                | Typ <sup>[3]</sup> | Max | Unit |
|--------------------------|---|---|--------------------|--------------------|-----|------|
| t <sub>PLH</sub>         | LOW to HIGH propagation delay           | port B to port A; <a href="#">Figure 15</a>   | <sup>[4]</sup> 70  | 115                | 350 | ns   |
| t <sub>PHL</sub>         | HIGH to LOW propagation delay           | port B to port A; <a href="#">Figure 13</a>   | 40                 | 75                 | 180 | ns   |
| t <sub>TLH</sub>         | LOW to HIGH output transition time      | port A; <a href="#">Figure 13</a>   | 20                 | 155                | 280 | ns   |
| t <sub>THL</sub>         | HIGH to LOW output transition time      | port A; <a href="#">Figure 13</a>   | 20                 | 60                 | 100 | ns   |
| t <sub>PLH</sub>         | LOW to HIGH propagation delay           | port A to port B; <a href="#">Figure 14</a>   | <sup>[5]</sup> 125 | 175                | 310 | ns   |
| t <sub>PHL</sub>         | HIGH to LOW propagation delay           | port A to port B; <a href="#">Figure 14</a>   | <sup>[5]</sup> 130 | 220                | 330 | ns   |
| t <sub>TLH</sub>         | LOW to HIGH output transition time      | port B; <a href="#">Figure 14</a>   | 80                 | 130                | 260 | ns   |
| t <sub>THL</sub>         | HIGH to LOW output transition time      | port B; <a href="#">Figure 14</a>   | 20                 | 45                 | 100 | ns   |
| t <sub>PLH</sub>         | LOW to HIGH propagation delay           | CECA; <a href="#">Figure 16</a>   | 40                 | 110                | 250 | ns   |
| t <sub>PHL</sub>         | HIGH to LOW propagation delay           | CECA; <a href="#">Figure 16</a>   | 40                 | 80                 | 180 | ns   |
| t <sub>TLH</sub>         | LOW to HIGH output transition time      | CECA; <a href="#">Figure 16</a>   | 80                 | 150                | 260 | ns   |
| t <sub>THL</sub>         | HIGH to LOW output transition time      | CECA; <a href="#">Figure 16</a>   | 20                 | 60                 | 100 | ns   |
| t <sub>su</sub>          | set-up time                             | EN HIGH before START condition  | <sup>[6]</sup> 200 | -                  | -   | μs   |
| t <sub>h</sub>           | hold time                               | EN HIGH after STOP condition  | <sup>[6]</sup> 200 | -                  | -   | ns   |
| t <sub>rec(pd-act)</sub> | recovery time from power-down to active | V <sub>CC(A)</sub> power-down to active; EN HIGH and V <sub>CC(B)</sub> on; V <sub>CC(A)</sub> ramping up | <sup>[7]</sup> 200 | -                  | -   | μs   |
|                          |   | V <sub>CC(B)</sub> power-down to active; EN HIGH and V <sub>CC(A)</sub> on; V <sub>CC(B)</sub> ramping up | <sup>[8]</sup> 200 | -                  | -   | μs   |

- [1] Times are specified with loads of 1.35 kΩ pull-up resistance and 57 pF load capacitance on port B, and 450 Ω pull-up resistance and 57 pF load capacitance on port A. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.
- [2] Pull-up voltages are V<sub>CC(A)</sub> on port A and V<sub>CC(B)</sub> on port B.
- [3] Typical values were measured with V<sub>CC(A)</sub> = 3.3 V at T<sub>amb</sub> = 25 °C, unless otherwise noted.
- [4] The t<sub>PLH</sub> delay data from port B to port A is measured at 0.5 V on port B to 0.3V<sub>CC(A)</sub> on port A.
- [5] The proportional delay data from port A to port B is measured at 0.3V<sub>CC(A)</sub> on port A to 0.3V<sub>CC(B)</sub> on port B.
- [6] The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.
- [7] If the V<sub>CC(A)</sub> ramp up is fast, then the t<sub>rec(pd-act)</sub> time must be allowed before the inputs are switched. If the supply ramp up is slow, the channels may be connected even before the final supply voltage is reached.
- [8] If the V<sub>CC(B)</sub> ramp up is fast, then the t<sub>rec(pd-act)</sub> time must be allowed before the inputs are switched. If the supply ramp up is slow, the channels may be connected even before the final supply voltage is reached.

10.1 AC waveforms

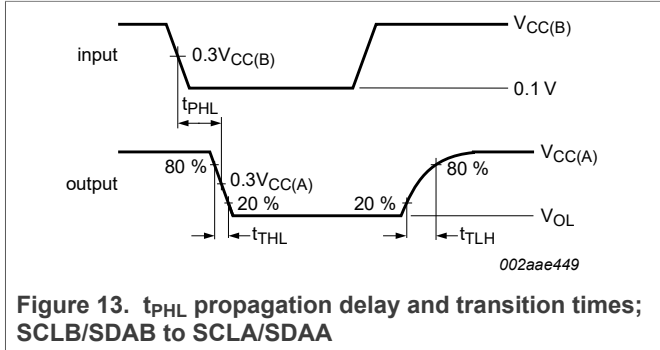


Figure 13.  $t_{PHL}$  propagation delay and transition times; SCLB/SDAB to SCLA/SDAA

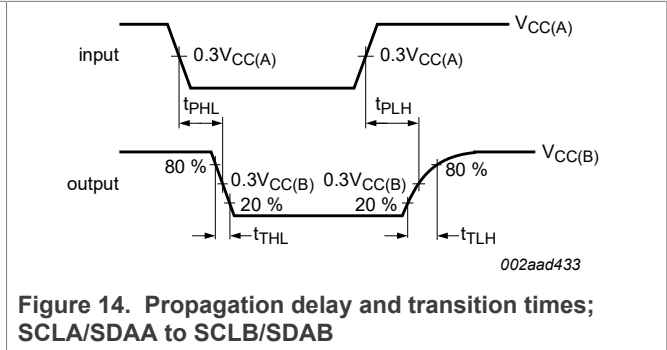
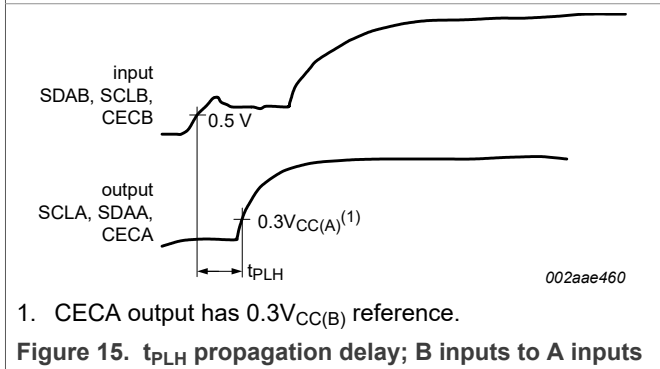


Figure 14. Propagation delay and transition times; SCLA/SDAA to SCLB/SDAB



1. CECA output has  $0.3V_{CC(B)}$  reference.  
Figure 15.  $t_{PLH}$  propagation delay; B inputs to A inputs

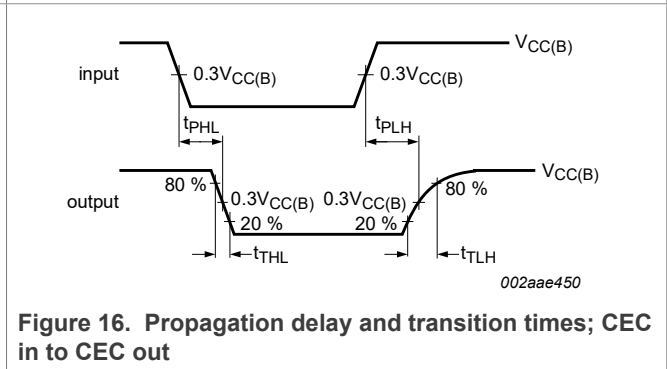
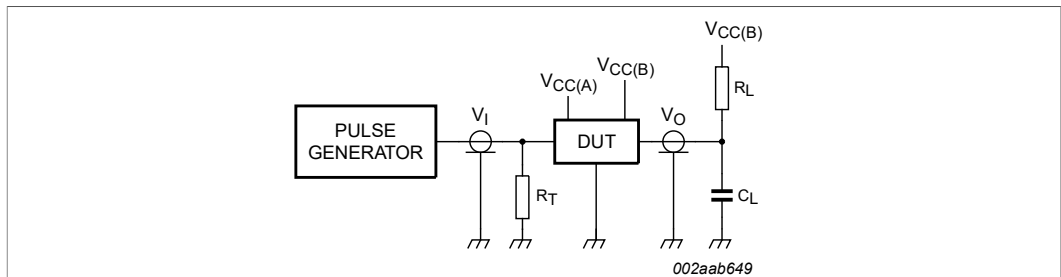


Figure 16. Propagation delay and transition times; CEC in to CEC out

11 Test information



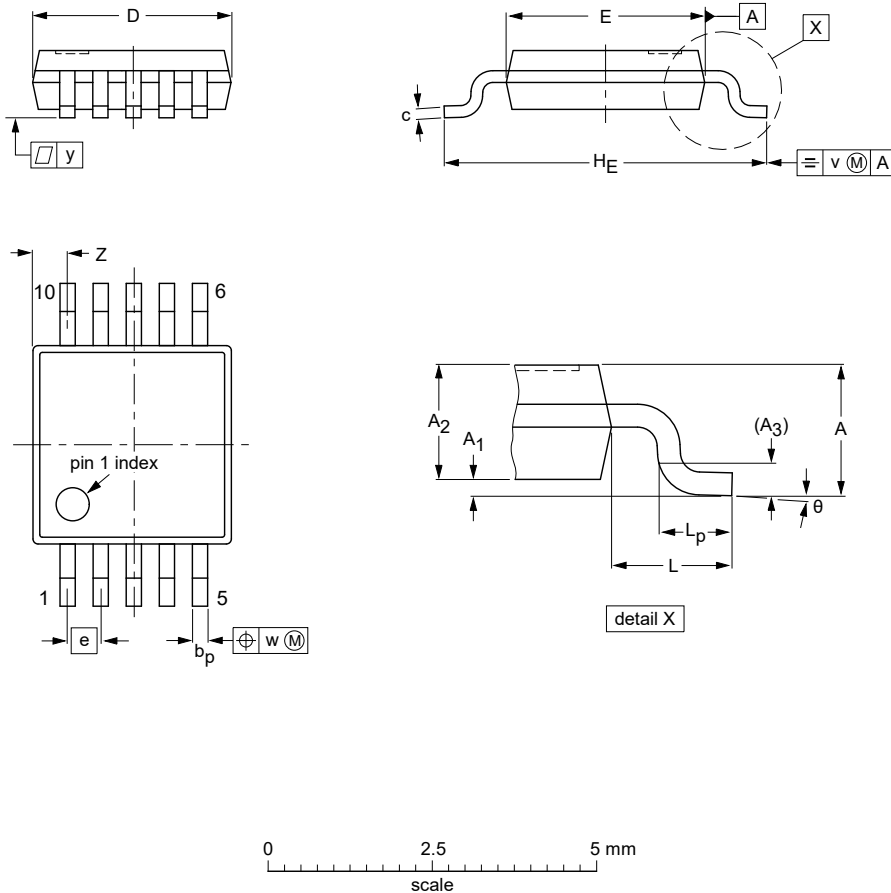
$R_L$  = load resistor; 1.35 k $\Omega$  on port B (2.7 V to 5 V) and 1.5 k $\Omega$  on port A (5.0 V).  
 $C_L$  = load capacitance includes jig and probe capacitance; 57 pF.  
 $R_T$  = termination resistance should be equal to  $Z_o$  of pulse generators.

Figure 17. Test circuit for open-drain outputs

12 Package outline

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm

SOT552-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(2)</sup> | e   | H <sub>E</sub> | L    | L <sub>p</sub> | v   | w   | y   | Z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|------|----------------|-----|-----|-----|------------------|----------|
| mm   | 1.1    | 0.15<br>0.05   | 0.95<br>0.80   | 0.25           | 0.30<br>0.15   | 0.23<br>0.15 | 3.1<br>2.9       | 3.1<br>2.9       | 0.5 | 5.0<br>4.8     | 0.95 | 0.7<br>0.4     | 0.1 | 0.1 | 0.1 | 0.67<br>0.34     | 6°<br>0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |       |       | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|-------|-------|---------------------|----------------------|
|                 | IEC        | JEDEC | JEITA |                     |                      |
| SOT552-1        |            |       |       |                     | 99-07-29<br>03-02-18 |

Figure 18. Package outline SOT552-1 (TSSOP10)

## 13 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 13.4 Reflow soldering

Key characteristics in reflow soldering are:



- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 19](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 8](#) and [Table 9](#)

**Table 8. SnPb eutectic process (from J-STD-020D)**

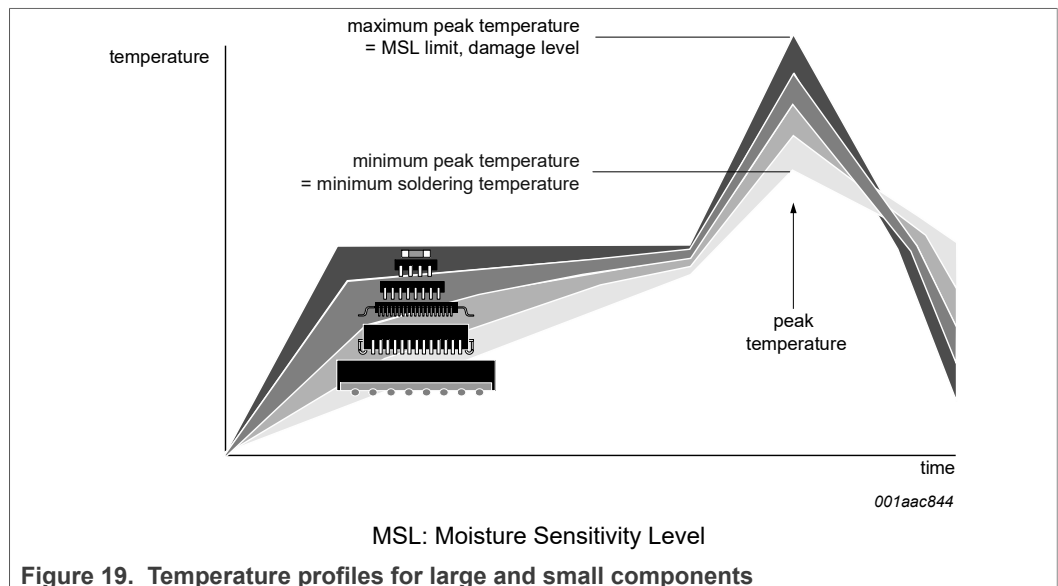
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 9. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 19](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 14 Abbreviations

Table 10. Abbreviations

| Acronym              | Description                                       |
|----------------------|---|
| CDM                  | Charged-Device Model                              |
| CEC                  | Consumer Electronic Control                       |
| CMOS                 | Complementary Metal-Oxide Semiconductor           |
| DDC                  | Display Data Channel                              |
| DVD                  | Digital Video Disc                                |
| DUT                  | Device Under Test                                 |
| EDID                 | Extended Display Identification Data              |
| ESD                  | ElectroStatic Discharge                           |
| HBM                  | Human Body Model                                  |
| HDMI                 | High-Definition Multimedia Interface              |
| I <sup>2</sup> C-bus | Inter Integrated Circuit bus                      |
| I/O                  | Input/Output                                      |
| LCD                  | Liquid Crystal Display                            |
| MM                   | Machine Model                                     |
| MOSFET               | Metal-Oxide Semiconductor Field-Effect Transistor |
| RC                   | Resistor-Capacitor network                        |
| SMBus                | System Management Bus                             |
| STB                  | Set-Top Box                                       |

## 15 Revision history

Table 11. Revision history

| Document ID    | Release date | Data sheet status   | Change notice | Supersedes |
|----------------|--------------|---|---------------|------------|
| PCA9527 v. 1.1 | 20210820     | Product data sheet  | PCN202104008A | PCA9527_1  |
|                |              | <ul style="list-style-type: none"> <li>• These global changes:               <ul style="list-style-type: none"> <li>– "Master" or "master" revised to "Controller" or "controller" to conform with NXP inclusive language guidelines.</li> <li>– "Slave" or "slave" revised to "Target" or "target" to conform with NXP inclusive language guidelines.</li> </ul> </li> <li>• Added section 3.1 Ordering Options with Table 2. Ordering Options.</li> </ul> |               |            |
| PCA9527_1      | 20090629     | Product data sheet  | -             | -          |

## 16 Legal information

### 16.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 16.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

## 16.4 Licenses

### Purchase of NXP ICs with HDMI technology

Use of an NXP IC with HDMI technology in equipment that complies with the HDMI standard requires a license from HDMI Licensing LLC, 1060 E. Arques Avenue Suite 100, Sunnyvale CA 94085, USA, e-mail: [admin@hdmi.org](mailto:admin@hdmi.org).

## 16.5 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP B.V.

**NXP** — wordmark and logo are trademarks of NXP B.V.

## Tables

|         |  |    |          |   |    |
|---------|--|----|----------|---|----|
| Tab. 1. | Ordering information .....                     | 2  | Tab. 7.  | Dynamic characteristics .....                 | 13 |
| Tab. 2. | Ordering options .....                         | 2  | Tab. 8.  | SnPb eutectic process (from J-STD-020D) ..... | 17 |
| Tab. 3. | Pin description .....                          | 3  | Tab. 9.  | Lead-free process (from J-STD-020D) .....     | 17 |
| Tab. 4. | HDMI DDC pull-up resistors specification ..... | 5  | Tab. 10. | Abbreviations .....                           | 18 |
| Tab. 5. | Limiting values .....                          | 10 | Tab. 11. | Revision history .....                        | 19 |
| Tab. 6. | Static characteristics .....                   | 11 |          |   |    |

## Figures

|          |   |    |          |   |    |
|----------|---|----|----------|---|----|
| Fig. 1.  | Functional diagram of PCA9527 .....                           | 3  | Fig. 12. | Bus B (2.7 V to 5.5 V) waveform .....                                     | 10 |
| Fig. 2.  | Pin configuration for TSSOP10 .....                           | 3  | Fig. 13. | tPHL propagation delay and transition times; SCLB/SDAB to SCLA/SDAA ..... | 14 |
| Fig. 3.  | Port A and port B I/O levels .....                            | 4  | Fig. 14. | Propagation delay and transition times; SCLA/SDAA to SCLB/SDAB .....      | 14 |
| Fig. 4.  | SDAA/SCLA line pull-up resistor versus load capacitance ..... | 6  | Fig. 15. | tPLH propagation delay; B inputs to A inputs .....                        | 14 |
| Fig. 5.  | Typical application .....                                     | 7  | Fig. 16. | Propagation delay and transition times; CEC in to CEC out .....           | 14 |
| Fig. 6.  | Source or DVD/R, STB application .....                        | 8  | Fig. 17. | Test circuit for open-drain outputs .....                                 | 14 |
| Fig. 7.  | Sink or LCD TV application .....                              | 8  | Fig. 18. | Package outline SOT552-1 (TSSOP10) .....                                  | 15 |
| Fig. 8.  | Typical star application .....                                | 9  | Fig. 19. | Temperature profiles for large and small components .....                 | 18 |
| Fig. 9.  | Typical series application .....                              | 9  |          |   |    |
| Fig. 10. | Typical application of PCA9527 driving a short cable .....    | 10 |          |   |    |
| Fig. 11. | Bus A (2.7 V to 5.5 V bus) waveform .....                     | 10 |          |   |    |