# PCF8562

## Universal LCD driver for low multiplex rates

Rev. 8 — 27 September 2021 Product data sheet

## 1 General description

The PCF8562 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 32 segments. The PCF8562 is compatible with most microcontrollers and communicates via the two-line bidirectional $I^2C$-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

## 2 Features and benefits

- AEC-Q100 compliant (PCF8562TT/S400/2) for automotive applications
- Single chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, ½, or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 32 segment drives:
  - Up to sixteen 7-segment numeric characters
  - Up to eight 14-segment alphanumeric characters
  - Any graphics of up to 128 elements
- 32 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
  - From 2.5 V for low-threshold LCDs
  - Up to 6.5 V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz $I^2C$-bus interface
- No external components required
- Manufactured in silicon gate CMOS process

1 The definition of the abbreviations and acronyms used in this data sheet can be found in Section 17.

# 3 Ordering information

**Table 1. Ordering information**

| Type number | Topside mark | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| PCF8562TT/2[1] | PCF8562TT | TSSOP48 | plastic thin shrink small outline package, 48 leads; body width 6.1 mm | SOT362-1 |
| PCF8562TT/S400/2[2] | PCF8562TT/S400 | TSSOP48 | plastic thin shrink small outline package, 48 leads; body width 6.1 mm | SOT362-1 |

[1] Not to be used for new designs. Replacement part is PCF85162T/1 for industrial applications.
[2] Not to be used for new designs. Replacement part is PCF85162T/Q900/1 for automotive applications.

## 3.1 Ordering options

**Table 2. Ordering options**

| Type number | Orderable part number | Package | Packing method[1] | Minimum order quantity | Temperature |
|---|---|---|---|---|---|
| PCF8562TT/2 | PCF8562TT/2,118[2] | TSSOP48 | reel 13 inch q1 non dry pack | 2000 | $T_{amb}$ = -40 °C to +85 °C |
| | PCF8562TT/2,518 | TSSOP48 | reel 13 inch q1 dry pack | 2000 | $T_{amb}$ = -40 °C to +85 °C |
| PCF8562TT/S400/2 | PCF8562TT/S400/2,1[3] | TSSOP48 | reel 13 inch q1 non dry pack | 2000 | $T_{amb}$ = -40 °C to +85 °C |
| | PCF8562TT/S400/2,5 | TSSOP48 | reel 13 inch q1 dry pack | 2000 | $T_{amb}$ = -40 °C to +85 °C |

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.
[2] Discontinuation Notice 202107021DN - drop in replacement is PCF8562TT/2,518 - this is documented in PCN202102010F01.
[3] Discontinuation Notice 202107021DN - drop in replacement is PCF8562TT/S400/2,5 - this is documented in PCN202102010F01.

# 4 Block diagram

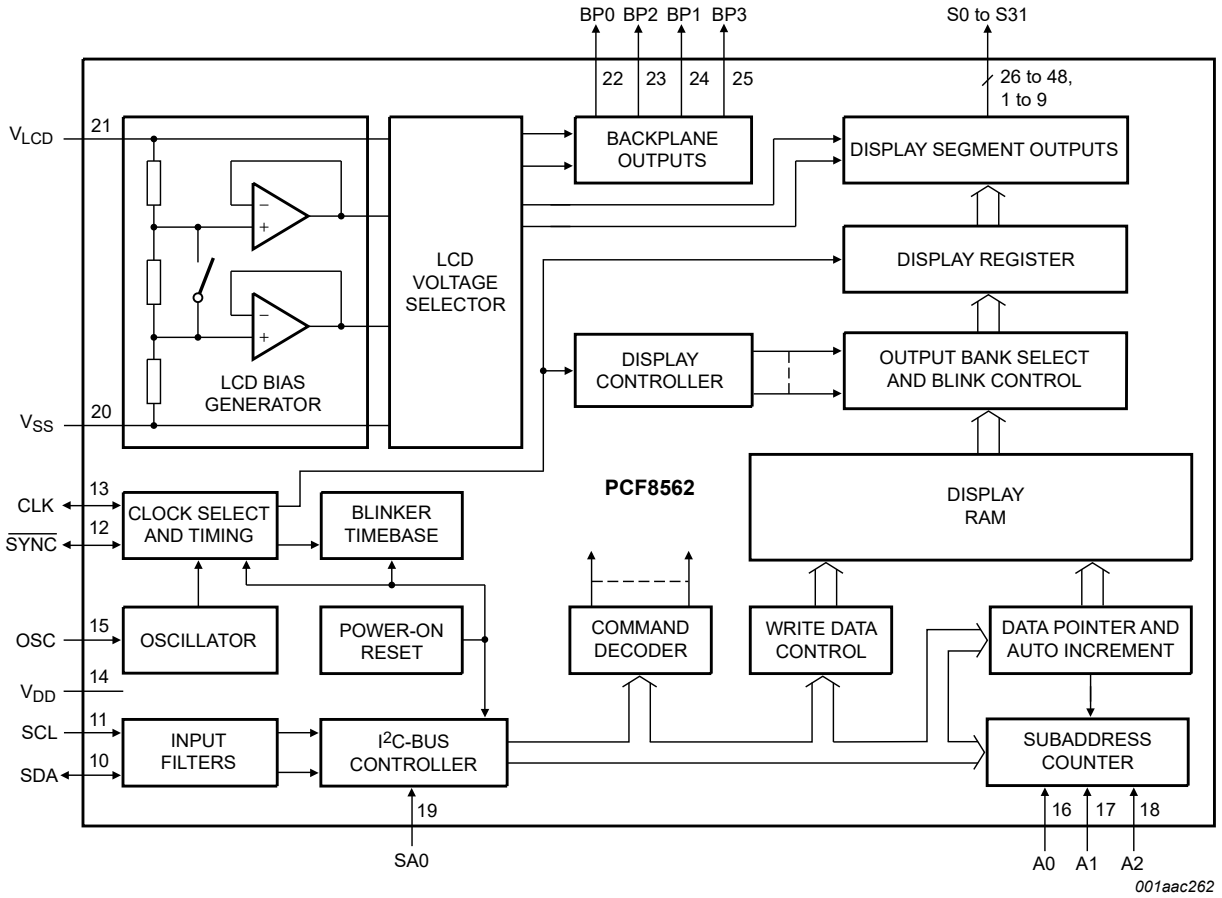
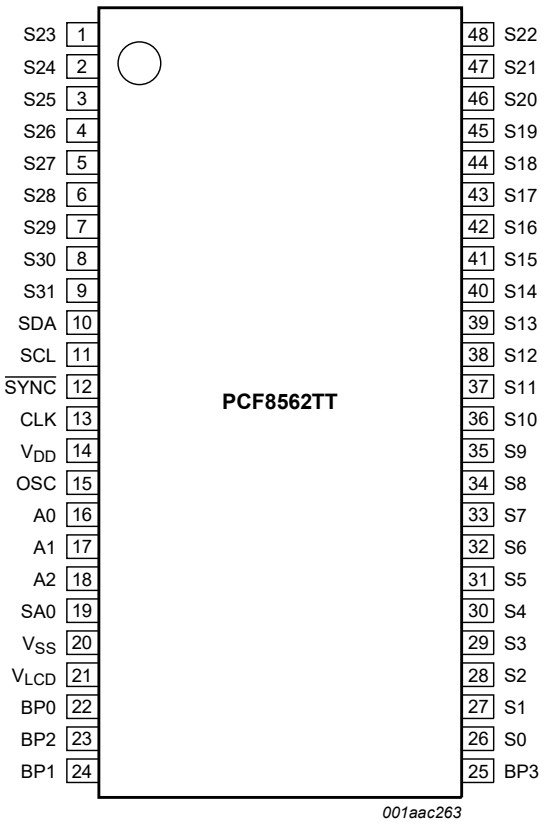



**Figure 1. Block diagram of PCF8562**

# 5 Pinning information

## 5.1 Pinning




Top view. For mechanical details, see Figure 22.

**Figure 2. Pinning diagram for TSSOP48 (PCF8562TT)**

## 5.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| SDA | 10 | input/output | $I^2C$-bus serial data line |
| SCL | 11 | input | $I^2C$-bus serial clock |
| $\overline{SYNC}$ | 12 | input/output | cascade synchronization |
| CLK | 13 | input/output | clock line |
| $V_{DD}$ | 14 | supply | supply voltage |
| OSC | 15 | input | internal oscillator enable |
| A0 to A2 | 16 to 18 | input | subaddress inputs |
| SA0 | 19 | input | $I^2C$-bus address input |
| $V_{SS}$ | 20 | supply | ground supply voltage |
| $V_{LCD}$ | 21 | supply | LCD supply voltage |

**Table 3. Pin description**...*continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| BP0 to BP3 | 22 to 25 | output | LCD backplane outputs |
| S0 to S22,<br>S23 to S31 | 26 to 48,<br>1 to 9 | output | LCD segment outputs |

# 6 Functional description

The PCF8562 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 3). It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 32 segments.

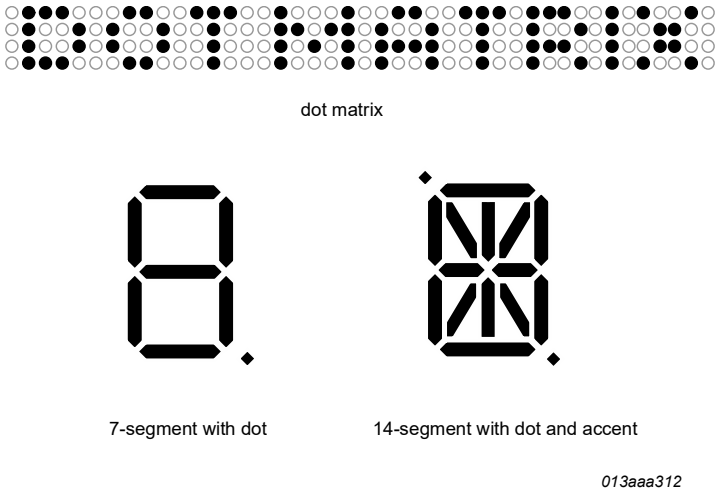
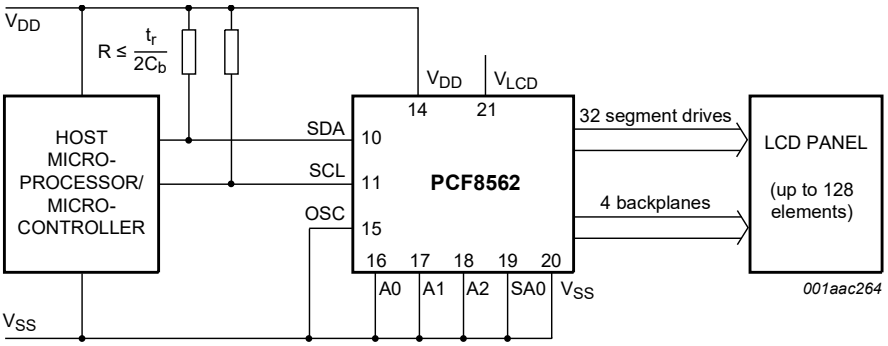



**Figure 3. Example of displays suitable for PCF8562**

The possible display configurations of the PCF8562 depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 4. All of these configurations can be implemented in the typical system shown in Figure 4.

**Table 4. Selection of possible display configurations**

| Number of Backplanes | Icons | Digits/Characters | | Dot matrix/ Elements |
|---|---|---|---|---|
| | | 7-segment | 14-segment | |
| 4 | 128 | 16 | 8 | 128 dots (4 × 32) |
| 3 | 96 | 12 | 6 | 96 dots (3 × 32) |
| 2 | 64 | 8 | 4 | 64 dots (2 × 32) |
| 1 | 32 | 4 | 2 | 32 dots (1 × 32) |




The resistance of the power lines must be kept to a minimum.

**Figure 4. Typical system configuration**

The host microcontroller maintains the 2-line I$^2$C-bus communication channel with the PCF8562. The internal oscillator is enabled by connecting pin OSC to pin $V_{SS}$. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies ($V_{DD}$, $V_{SS}$, and $V_{LCD}$) and the LCD panel chosen for the application.

## 6.1 Power-On Reset (POR)

At power-on the PCF8562 resets to the following starting conditions:

- All backplane and segment outputs are set to $V_{LCD}$
- The selected drive mode is: 1:4 multiplex with $^1/_3$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I$^2$C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- Display is disabled

**Remark:** Do not transfer data on the I$^2$C-bus for at least 1 ms after a power-on to allow the reset action to complete.

## 6.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider consisting of three impedances connected in series between $V_{LCD}$ and $V_{SS}$. The center impedance is bypassed by switch if the $^1/_2$ bias voltage level for the 1:2 multiplex drive mode configuration is selected. The LCD voltage can be temperature compensated externally, using the supply to pin $V_{LCD}$.

## 6.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{LCD}$ and the resulting discrimination ratios (D) are given in Table 5.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

**Table 5. Biasing characteristics**

| LCD drive mode | Number of: | | LCD bias configuration | $\frac{V_{off(RMS)}}{V_{LCD}}$ | $\frac{V_{on(RMS)}}{V_{LCD}}$ | $D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$ |
|---|---|---|---|---|---|---|
| | Backplanes | Levels | | | | |
| static | 1 | 2 | static | 0 | 1 | ∞ |
| 1:2 multiplex | 2 | 3 | ½ | 0.354 | 0.791 | 2.236 |
| 1:2 multiplex | 2 | 4 | ⅓ | 0.333 | 0.745 | 2.236 |
| 1:3 multiplex | 3 | 4 | ⅓ | 0.333 | 0.638 | 1.915 |
| 1:4 multiplex | 4 | 4 | ⅓ | 0.333 | 0.577 | 1.732 |

A practical value for $V_{LCD}$ is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias
a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = \frac{V_{LCD}}{\sqrt{\frac{a^2+2a+n}{n\times(1+a)^2}}} \quad (1)$$

where the values for n are

n = 1 for static drive mode
n = 2 for 1:2 multiplex drive mode
n = 3 for 1:3 multiplex drive mode
n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = \frac{V_{LCD}}{\sqrt{\frac{a^2-2a+n}{n\times(1+a)^2}}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2+2a+n}{a^2-2a+n}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage $V_{LCD}$ as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4\times\sqrt{3})}{3}\right] = 2.309V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when $^1/_3$ bias is used.

It should be noted that $V_{LCD}$ is sometimes referred as the LCD operating voltage.

### 6.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 5. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the $V_{LCD}$ voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

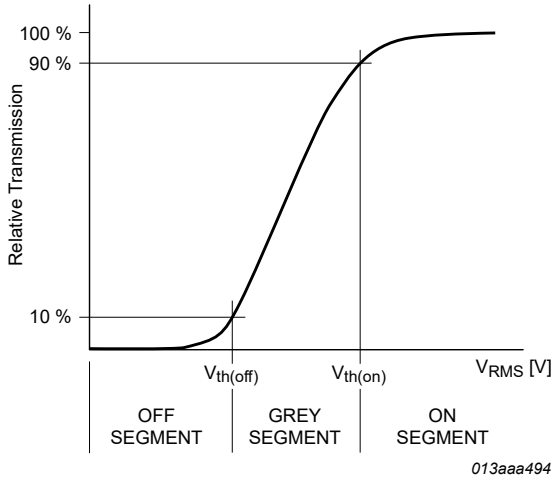
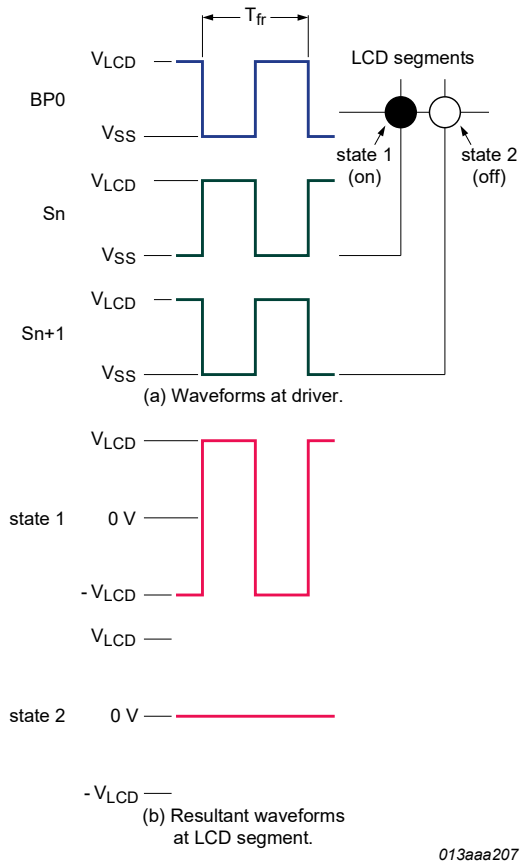



**Figure 5. Electro-optical characteristic: relative transmission curve of the liquid**

## 6.4 LCD drive mode waveforms

### 6.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment (Sn) drive waveforms for this mode are shown in Figure 6.

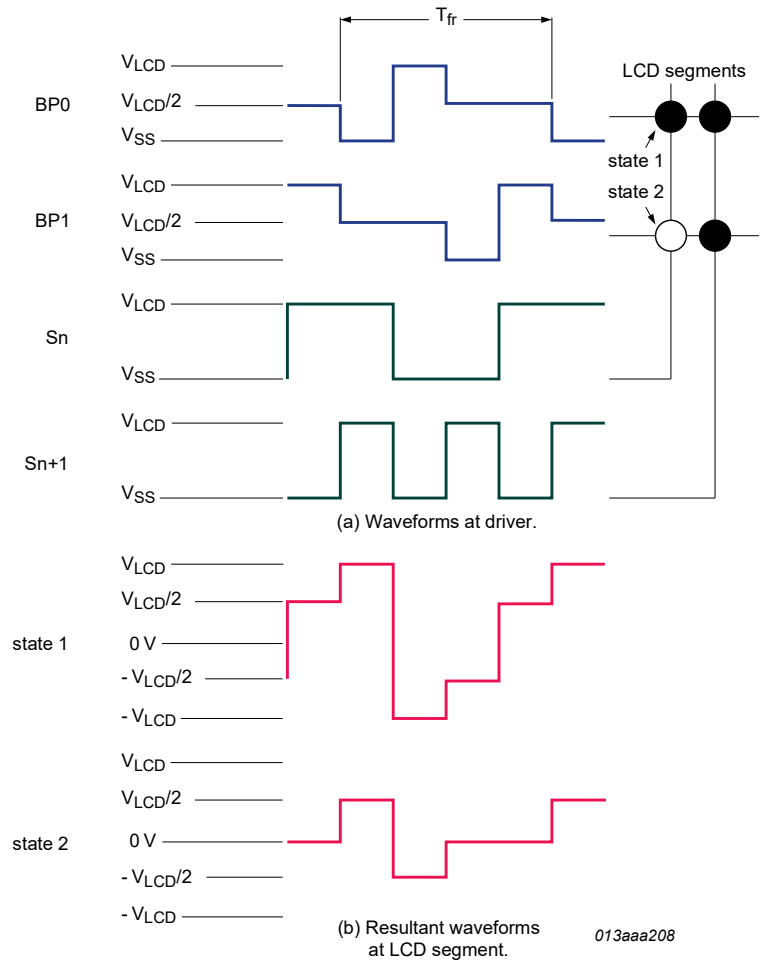



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.
$V_{on(RMS)} = V_{LCD}$.
$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t)$.
$V_{off(RMS)} = 0$ V.

**Figure 6. Static drive mode waveforms**

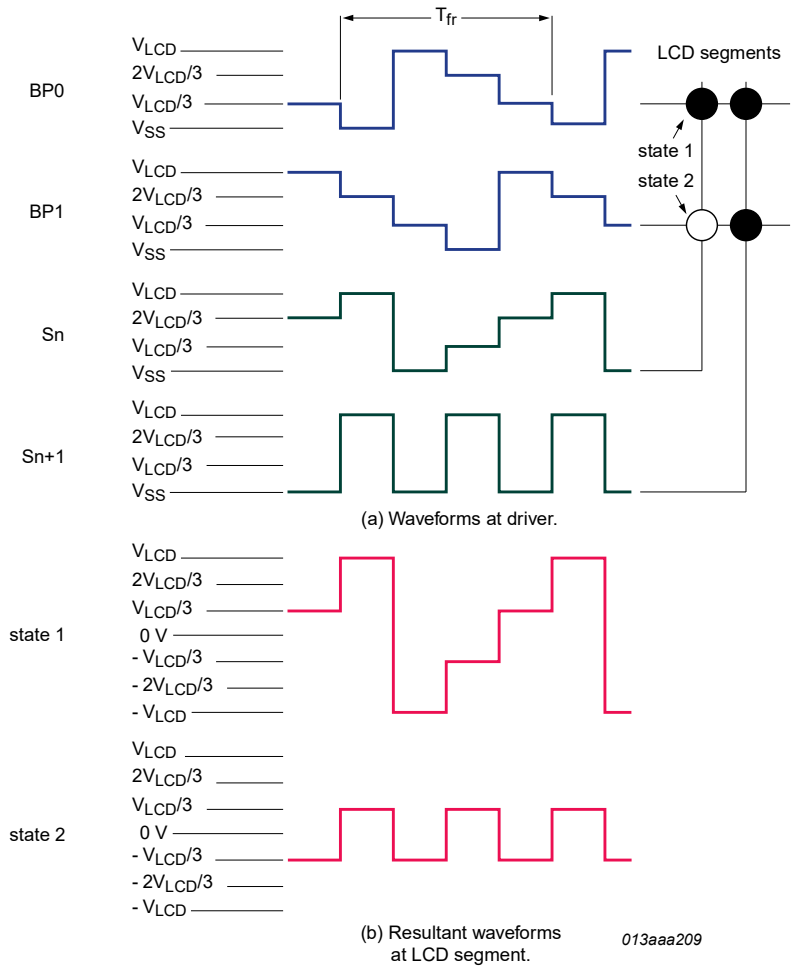
### 6.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8562 allows the use of $^1/_2$ bias or $^1/_3$ bias in this mode as shown in Figure 7 and Figure 8.




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.
$V_{on(RMS)} = 0.791V_{LCD}$.
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.
$V_{off(RMS)} = 0.354V_{LCD}$.

**Figure 7. Waveforms for the 1:2 multiplex drive mode with $^1/_2$ bias**

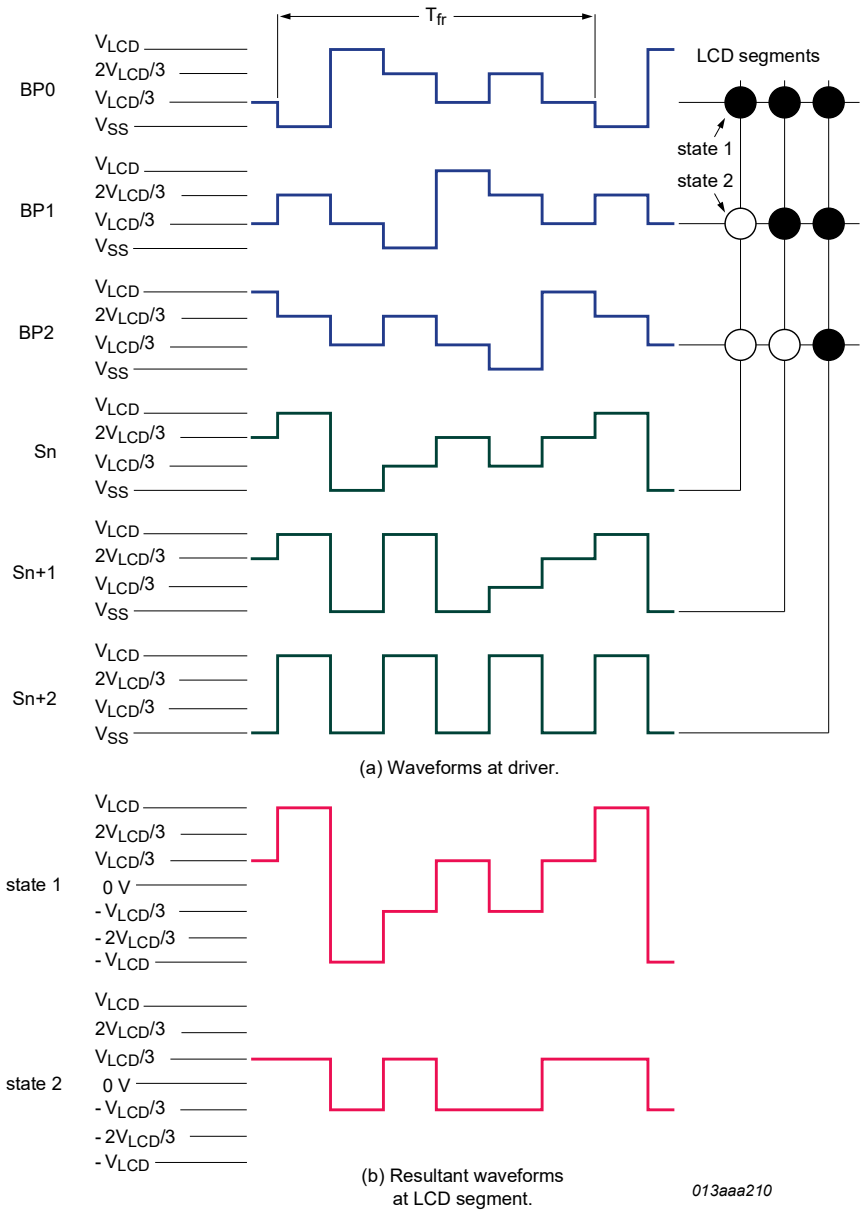



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.
$V_{on(RMS)} = 0.745V_{LCD}$.
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.
$V_{off(RMS)} = 0.333V_{LCD}$.

**Figure 8. Waveforms for the 1:2 multiplex drive mode with $^1/_3$ bias**

### 6.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 9.

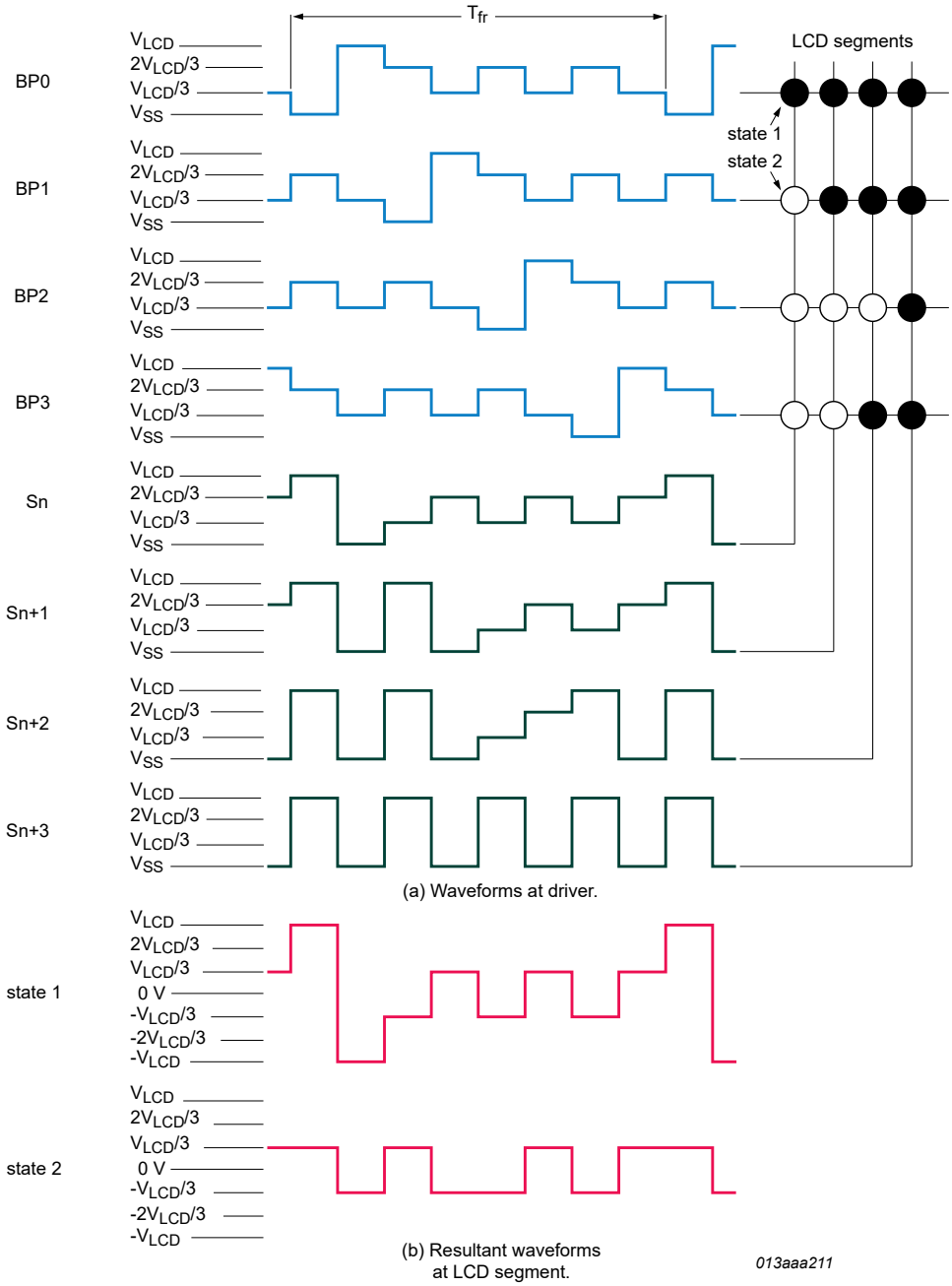



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.
$V_{on(RMS)} = 0.638V_{LCD}$.
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.
$V_{off(RMS)} = 0.333V_{LCD}$.

**Figure 9. Waveforms for the 1:3 multiplex drive mode with $^1/_3$ bias**

### 6.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 10.




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

**Figure 10. Waveforms for the 1:4 multiplex drive mode with $^1/_3$ bias**

## 6.5 Oscillator

### 6.5.1 Internal clock

The internal logic of the PCF8562 and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin $V_{SS}$.

### 6.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to $V_{DD}$.

The LCD frame signal frequency is determined by the clock frequency ($f_{clk}$).

**Remark:** A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

## 6.6 Timing

The PCF8562 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock: $f_{fr} = \frac{f_{clk}}{24}$.

## 6.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

## 6.8 Segment outputs

The LCD drive section includes 32 segment outputs S0 to S31 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display latch. When less than 32 segment outputs are required, the unused segment outputs should be left open-circuit.

## 6.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In the 1:2 multiplex drive mode, BP0 and BP2, respectively, BP1 and BP3 carry the same signals and may also be paired to increase the drive capabilities.
- In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

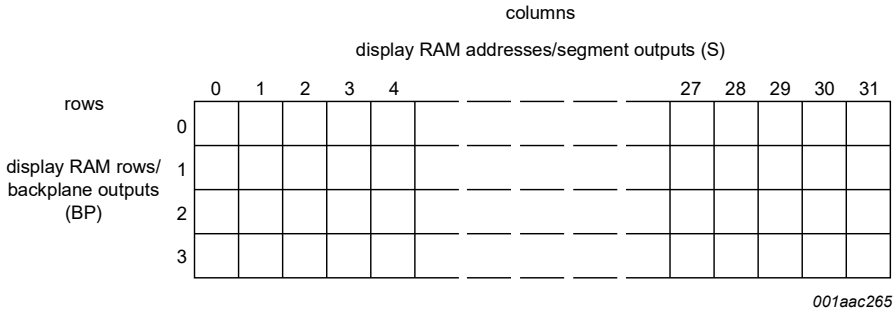
## 6.10 Display RAM

The display RAM is a static 32 × 4-bit RAM which stores LCD data. There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

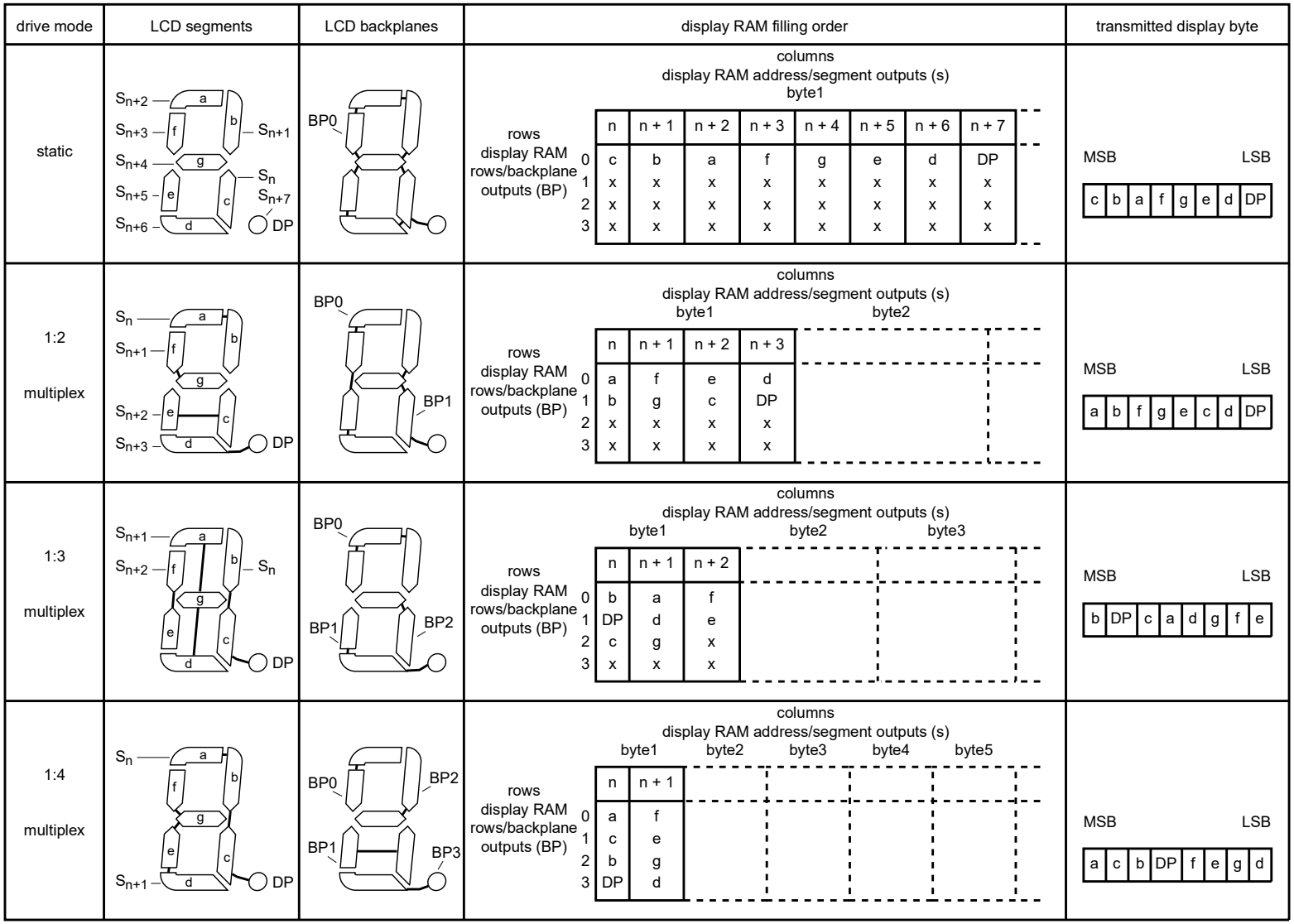
The display RAM bit map Figure 11 shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 31 which correspond with the segment outputs S0 to S31. In multiplexed LCD applications the segment data of the first, second, third, and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.




The display RAM bit map shows the direct relationship between the display RAM addresses and the segment outputs and between the bits in a RAM word and the backplane outputs.

**Figure 11. Display RAM bit map**

When display data is transmitted to the PCF8562, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and depending on the current multiplex drive mode the bits are stored singularly, in pairs, triples or quadruples. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 12; the RAM filling organization depicted applies equally to other LCD types.




x = data bit unchanged.

**Figure 12. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the $I^2C$-bus**

The following applies to Figure 12:

- In static drive mode the eight transmitted data bits are placed in row 0 as one byte.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as two successive 4-bit RAM words.
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 6.10.3).
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words.

### 6.10.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 12). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 12.

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an $I^2C$-bus data access is terminated early then the state of the data pointer is unknown. The data pointer should be re-written prior to further RAM accesses.

### 6.10.2 Subaddress counter

The storage of display data is determined by the content of the subaddress counter. Storage is allowed to take place only when the content of the subaddress counter matches with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 13). If the content of the subaddress counter and the hardware subaddress do not match then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The hardware subaddress must not be changed while the device is being accessed on the $I^2C$-bus interface.

### 6.10.3 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 6 (see Figure 12 as well).

**Table 6. Standard RAM filling in 1:3 multiplex drive mode**

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are not connected** to any elements on the display.*

| Display RAM bits (rows)/ backplane outputs (BPn) | Display RAM addresses (columns)/segment outputs (Sn) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : |
| **0** | a7 | a4 | a1 | b7 | b4 | b1 | c7 | c4 | c1 | d7 | : |
| **1** | a6 | a3 | a0 | b6 | b3 | b0 | c6 | c3 | c0 | d6 | : |
| **2** | a5 | a2 | - | b5 | b2 | - | c5 | c2 | - | d5 | : |
| **3** | - | - | - | - | - | - | - | - | - | - | : |

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 7.

**Table 7. Entire RAM filling by rewriting in 1:3 multiplex drive mode**

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are connected** to elements on the display.*

| Display RAM bits (rows)/ backplane outputs (BPn) | Display RAM addresses (columns)/segment outputs (Sn) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : |
| **0** | a7 | a4 | a1/b7 | b4 | b1/c7 | c4 | c1/d7 | d4 | d1/e7 | e4 | : |
| **1** | a6 | a3 | a0/b6 | b3 | b0/c6 | c3 | c0/d6 | d3 | d0/e6 | e3 | : |
| **2** | a5 | a2 | b5 | b2 | c5 | c2 | d5 | d2 | e5 | e2 | : |
| **3** | - | - | - | - | - | - | - | - | - | - | : |

In the case described in Table 7 the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8 etc. have to be connected to elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written.
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6.
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6.

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some elements remain unused or can be used, but it has to be considered in the module layout process as well as in the driver software design.

### 6.10.4 Output bank selector

The output bank selector (see Table 14) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the content of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The PCF8562 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the content of row 2 to be selected for display instead of the content of row 0. In the 1:2 multiplex mode, the content of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

### 6.10.5 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration.

The bank-select command (see Table 14) can be used to load display data in row 2 in static drive mode or in rows 2 and 3 in 1:2 mode. The input bank selector functions are independent of the output bank selector.

## 6.11 Blinking

The display blinking capabilities of the PCF8562 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 15). The blink frequencies are fractions of the clock frequency. The ratio between the clock and blink frequencies depends on the blink mode selected (see Table 8).

An additional feature is for an arbitrary selection of LCD elements to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternative RAM bank is available, groups of LCD elements can blink by selectively changing the display RAM data at fixed time intervals.

**Table 8. Blinking frequencies[1]**

| Blink mode | Normal operating mode ratio | Nominal blink frequency |
|---|---|---|
| off | - | blinking off |
| 1 | $\frac{f_{clk}}{768}$ | 2 Hz |
| 2 | $\frac{f_{clk}}{1536}$ | 1 Hz |
| 3 | $\frac{f_{clk}}{3072}$ | 0.5 Hz |

[1] Blink modes 1, 2, and 3 and the nominal blink frequencies 0.5 Hz, 1 Hz, and 2 Hz correspond to an oscillator frequency ($f_{clk}$) of 1 536 Hz (see Section 11).

The entire display can blink at a frequency other than the nominal blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 11).

## 6.12 Command decoder

The command decoder identifies command bytes that arrive on the $I^2C$-bus. The commands available to the PCF8562 are defined in Table 9.

**Table 9. Definition of PCF8562 commands**

| Command | Operation code | | | | | | | | Reference |
|---|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| mode-set | C | 1 | 0 | -[1] | E | B | M[1:0] | | Table 11 |
| load-data-pointer | C | 0 | 0 | P[4:0] | | | | | Table 12 |
| device-select | C | 1 | 1 | 0 | 0 | A[2:0] | | | Table 13 |
| bank-select | C | 1 | 1 | 1 | 1 | 0 | I | O | Table 14 |
| blink-select | C | 1 | 1 | 1 | 0 | AB | BF[1:0] | | Table 15 |

[1] Not used.

All available commands carry a continuation bit C in their most significant bit position as shown in Figure 18. When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data (see Table 10).

**Table 10. C bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | C | | **continue bit** |
| | | 0 | last control byte in the transfer; next byte will be regarded as display data |
| | | 1 | control bytes continue; next byte will be a command too |

**Table 11. Mode-set command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | C | 0, 1 | see Table 10 |
| 6, 5 | - | 10 | fixed value |
| 4 | - | - | unused |
| 3 | E | | **display status** |
| | | 0 | disabled (blank)[1] |
| | | 1 | enabled |
| 2 | B | | **LCD bias configuration**[2] |
| | | 0 | 1/3 bias |
| | | 1 | 1/2 bias |
| 1 to 0 | M[1:0] | | **LCD drive mode selection** |
| | | 01 | static; BP0 |
| | | 10 | 1:2 multiplex; BP0, BP1 |
| | | 11 | 1:3 multiplex; BP0, BP1, BP2 |
| | | 00 | 1:4 multiplex; BP0, BP1, BP2, BP3 |

[1] The possibility to disable the display allows implementation of blinking under external control.
[2] Not applicable for static drive mode.

**Table 12. Load-data-pointer command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | C | 0, 1 | see Table 10 |
| 6, 5 | - | 00 | fixed value |
| 4 to 0 | P[4:0] | 00000 to 11111 | 5 bit binary value, 0 to 31; transferred to the data pointer to define one of 32 display RAM addresses |

**Table 13. Device-select command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | C | 0, 1 | see Table 10 |
| 6 to 3 | - | 1100 | fixed value |
| 2 to 0 | A[2:0] | 000 to 111 | 3 bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses |

**Table 14. Bank-select command bit description**

| Bit | Symbol | Value | Description | |
|---|---|---|---|---|
| | | | Static | 1:2 multiplex[1] |
| 7 | C | 0, 1 | see Table 10 | |
| 6 to 2 | - | 11110 | fixed value | |
| 1 | I | | **input bank selection**; storage of arriving display data | |
| | | 0 | RAM bit 0 | RAM bits 0 and 1 |
| | | 1 | RAM bit 2 | RAM bits 2 and 3 |
| 0 | O | | **output bank selection**; retrieval of LCD display data | |
| | | 0 | RAM bit 0 | RAM bits 0 and 1 |
| | | 1 | RAM bit 2 | RAM bits 2 and 3 |

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

**Table 15. Blink-select command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | C | 0, 1 | see Table 10 |
| 6 to 3 | - | 1110 | fixed value |
| 2 | AB | | **blink mode selection** |
| | | 0 | normal blinking[1] |
| | | 1 | alternate RAM bank blinking[2] |
| 1 to 0 | BF[1:0] | | **blink frequency selection** |
| | | 00 | off |
| | | 01 | 1 |

**Table 15. Blink-select command bit description**...*continued*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| | | 10 | 2 |
| | | 11 | 3 |

[1] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.
[2] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

### 6.13 Display controller

The display controller executes the commands identified by the command decoder. It contains the device's status registers and coordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.

## 7 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta Line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 13).

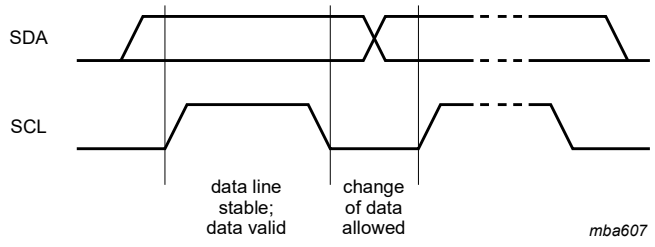



**Figure 13. Bit transfer**

### 7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 14).

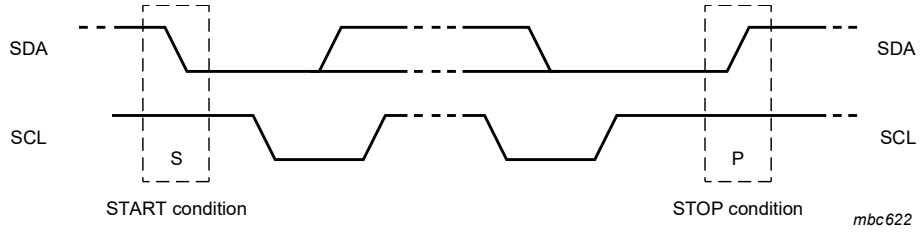



**Figure 14. Definition of START and STOP conditions**

## 7.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the controller and the devices which are controlled by the controller are the targets (see Figure 15).

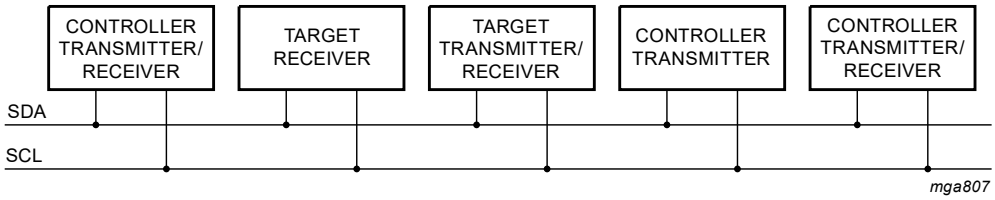



**Figure 15. System configuration**

## 7.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A target receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A controller receiver must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.

Acknowledgement on the $I^2C$-bus is illustrated in Figure 16.

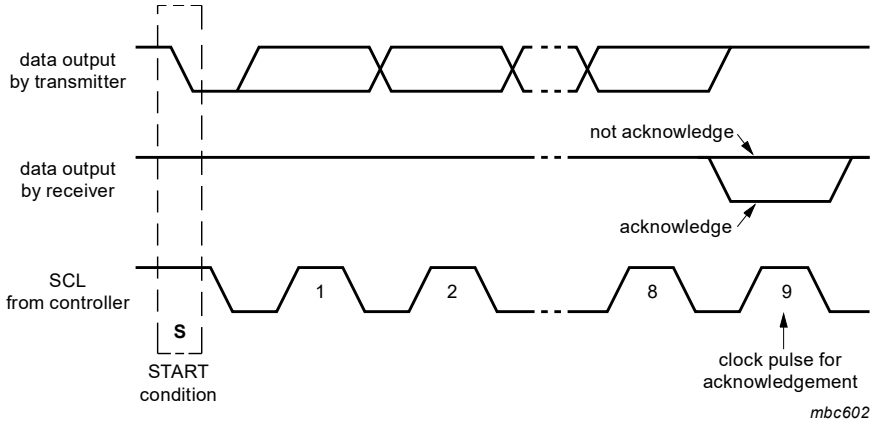



**Figure 16. Acknowledgement of the I²C-bus**

## 7.5 I²C-bus controller

The PCF8562 acts as an I²C-bus target receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus controller receiver. The only data output from the PCF8562 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus target address, on the transferred command data and on the hardware subaddress.

## 7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

## 7.7 I²C-bus protocol

Two I²C-bus target addresses (0111 000 and 0111 001) are reserved for the PCF8562. The least significant bit of the target address that a PCF8562 will respond to is defined by the level tied to its SA0 input. The PCF8562 is a write-only device and will not respond to a read access.

The I²C-bus protocol is shown in Figure 17. The sequence is initiated with a START condition (S) from the I²C-bus controller which is followed by one of two possible PCF8562 target addresses available. All PCF8562s whose SA0 inputs correspond to bit 0 of the target address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCF8562s whose SA0 inputs are set to the alternative level.

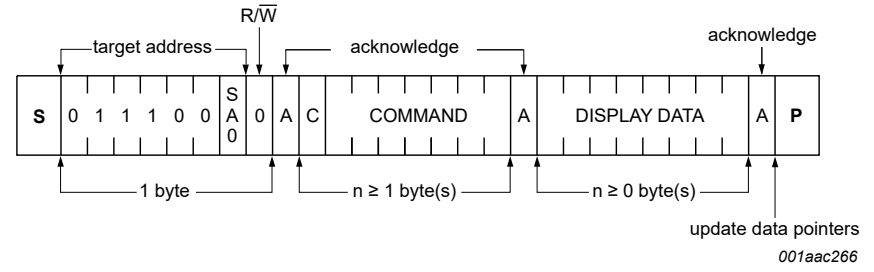



**Figure 17. I²C-bus protocol**

After an acknowledgement, one or more command bytes follow, that define the status of each addressed PCF8562.

The last command byte sent is identified by resetting its most significant bit, continuation bit C, (see Figure 18). The command bytes are also acknowledged by all addressed PCF8562s on the bus.

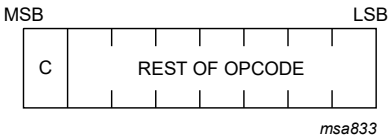



**Figure 18. Format of command byte**

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated.

An acknowledgement, after each byte, is asserted only by the PCF8562s that are addressed via address lines A0, A1 and A2. After the last display byte, the $I^2C$-bus controller asserts a STOP condition (P). Alternately a START may be asserted to restart an $I^2C$-bus access.

# 8 Internal circuitry

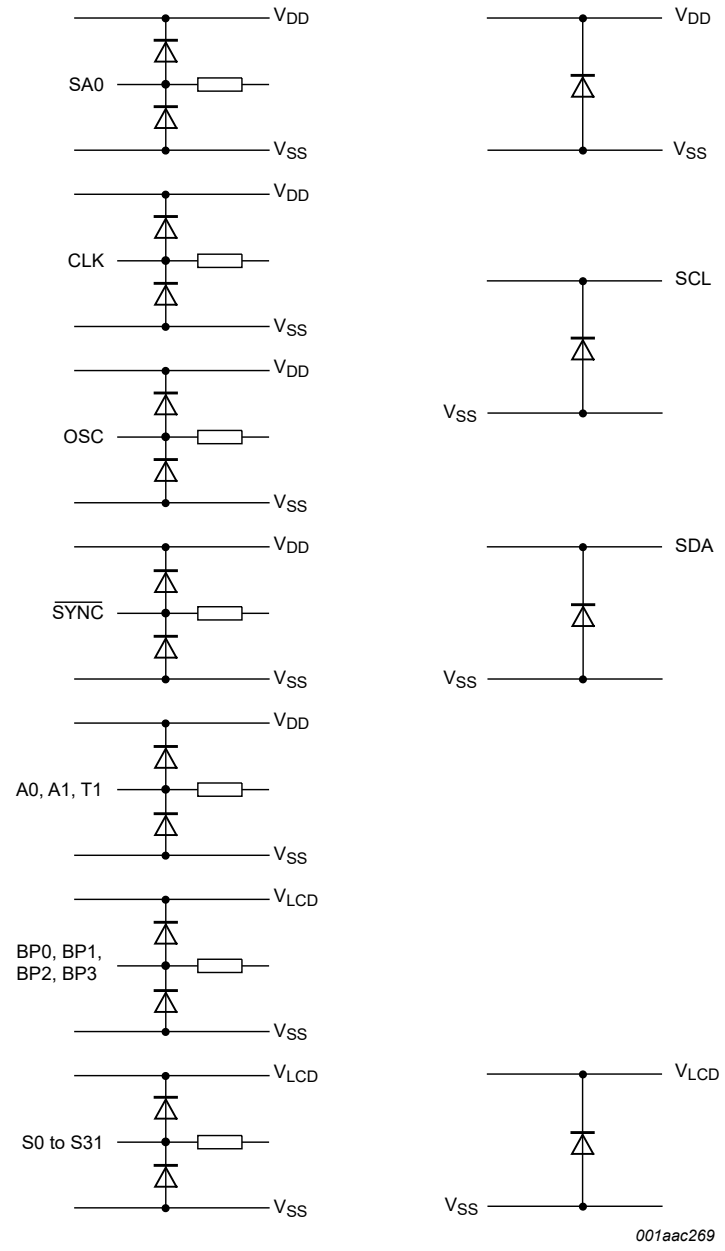



**Figure 19. Device protection circuits**

# 9 Limiting values

**CAUTION**

Static voltages across the liquid crystal display can build up when the LCD supply voltage ($V_{LCD}$) is on while the IC supply voltage ($V_{DD}$) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, $V_{LCD}$ and $V_{DD}$ must be applied or removed together.

**Table 16. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | -0.5 | +6.5 | V |
| $V_{LCD}$ | LCD supply voltage | | | -0.5 | +7.5 | V |
| $V_I$ | input voltage | on each of the pins CLK, SDA, SCL, $\overline{SYNC}$, SA0, OSC, A0 to A2 | | -0.5 | +6.5 | V |
| $V_O$ | output voltage | on each of the pins S0 to S31, BP0 to BP3 | | -0.5 | +7.5 | V |
| $I_I$ | input current | | | -10 | +10 | mA |
| $I_O$ | output current | | | -10 | +10 | mA |
| $I_{DD}$ | supply current | | | -50 | +50 | mA |
| $I_{DD(LCD)}$ | LCD supply current | | | -50 | +50 | mA |
| $I_{SS}$ | ground supply current | | | -50 | +50 | mA |
| $P_{tot}$ | total power dissipation | | | - | 400 | mW |
| $P_o$ | output power | | | - | 100 | mW |
| $V_{esd}$ | electrostatic discharge voltage | HBM | [1] | - | ±5 000 | V |
| | | MM | [2] | - | ±200 | V |
| | | CDM | [3] | - | ±1 500 | V |
| $I_{lu}$ | latch-up current | | [4] | - | 300 | mA |
| $T_{stg}$ | storage temperature | | [5] | -65 | +150 | °C |
| $T_{amb}$ | ambient temperature | operating device | | -40 | +85 | °C |

[1] Pass level; Human Body Model (HBM), according to [1].
[2] Pass level; Machine Model (MM), according to [2].
[3] Pass level; Charged-Device Model (CDM), according to [3].
[4] Pass level; latch-up testing according to [4] at maximum ambient temperature ($T_{amb(max)}$).
[5] According to the NXP store and transport requirements (see [5]) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

# 10 Static characteristics

**Table 17. Static characteristics**

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 6.5 V; $T_{amb}$ = -40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $V_{DD}$ | supply voltage | | | 1.8 | - | 5.5 | V |
| $V_{LCD}$ | LCD supply voltage | | [1] | 2.5 | - | 6.5 | V |
| $I_{DD}$ | supply current | $f_{clk(ext)}$ = 1 536 Hz | [2] | - | 3.5 | 7 | µA |
| $I_{DD(LCD)}$ | LCD supply current | $f_{clk(ext)}$ = 1 536 Hz | [2] | - | 23 | 32 | µA |
| **Logic**[3] | | | | | | | |
| $V_{P(POR)}$ | power-on reset supply voltage | | | 1.0 | 1.3 | 1.6 | V |

**Table 17. Static characteristics**...*continued*

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 6.5 V; $T_{amb}$ = -40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | LOW-level input voltage | on pins CLK, $\overline{SYNC}$, OSC, A0 to A2, SA0, SCL, SDA | | $V_{SS}$ | - | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | on pins CLK, $\overline{SYNC}$, OSC, A0 to A2, SA0, SCL, SDA | [4][5] | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $I_{OL}$ | LOW-level output current | output sink current; $V_{OL}$ = 0.4 V; $V_{DD}$ = 5 V | | | | | |
| | | on pins CLK and $\overline{SYNC}$ | | 1 | - | - | mA |
| | | on pin SDA | | 3 | - | - | mA |
| $I_{OH(CLK)}$ | HIGH-level output current on pin CLK | output source current; $V_{OH}$ = 4.6 V; $V_{DD}$ = 5 V | | 1 | - | - | mA |
| $I_L$ | leakage current | $V_I = V_{DD}$ or $V_{SS}$; on pins CLK, SCL, SDA, A0 to A2 and SA0 | | -1 | - | +1 | µA |
| $I_{L(OSC)}$ | leakage current on pin OSC | $V_I = V_{DD}$ | | -1 | - | +1 | µA |
| $C_I$ | input capacitance | | [6] | - | - | 7 | pF |
| **LCD outputs** | | | | | | | |
| $\Delta V_O$ | output voltage variation | on pins BP0 to BP3 and S0 to S31 | | -100 | - | +100 | mV |
| $R_O$ | output resistance | $V_{LCD}$ = 5 V | [7] | | | | |
| | | on pins BP0 to BP3 | | - | 1.5 | - | kΩ |
| | | on pins S0 to S31 | | - | 6.0 | - | kΩ |

[1] $V_{LCD} > 3$ V for $\frac{1}{3}$ bias.
[2] LCD outputs are open-circuit; inputs at $V_{SS}$ or $V_{DD}$; external clock with 50 % duty factor; $I^2C$-bus inactive.
[3] The $I^2C$-bus interface of PCF8562 is 5 V tolerant.
[4] When tested, $I^2C$ pins SCL and SDA have no diode to $V_{DD}$ and may be driven to the $V_I$ limiting values given in Table 16 (see Figure 19 as well).
[5] Propagation delay of driver between clock (CLK) and LCD driving signals.
[6] Periodically sampled, not 100 % tested.
[7] Outputs measured one at a time.

# 11 Dynamic characteristics

**Table 18. Dynamic characteristics**

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 6.5 V; $T_{amb}$ = -40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Clock** | | | | | | | |
| $f_{clk(int)}$ | internal clock frequency | | [1] | 1 440 | 1 850 | 2 640 | Hz |
| $f_{clk(ext)}$ | external clock frequency | | | 960 | - | 2 640 | Hz |
| $t_{clk(H)}$ | HIGH-level clock time | | | 60 | - | - | µs |
| $t_{clk(L)}$ | LOW-level clock time | | | 60 | - | - | µs |

**Table 18. Dynamic characteristics**...*continued*

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 6.5 V; $T_{amb}$ = -40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Synchronization** | | | | | | | |
| $t_{PD(SYNC\_N)}$ | $\overline{SYNC}$ propagation delay | | | - | 30 | - | ns |
| $t_{SYNC\_NL}$ | $\overline{SYNC}$ LOW time | | | 1 | - | - | µs |
| $t_{PD(drv)}$ | driver propagation delay | $V_{LCD}$ = 5 V | [2] | - | - | 30 | µs |
| **$I^2C$-bus**[3] | | | | | | | |
| Pin SCL | | | | | | | |
| $f_{SCL}$ | SCL clock frequency | | | - | - | 400 | kHz |
| $t_{LOW}$ | LOW period of the SCL clock | | | 1.3 | - | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | | 0.6 | - | - | µs |
| Pin SDA | | | | | | | |
| $t_{SU;DAT}$ | data set-up time | | | 100 | - | - | ns |
| $t_{HD;DAT}$ | data hold time | | | 0 | - | - | ns |
| Pins SCL and SDA | | | | | | | |
| $t_{BUF}$ | bus free time between a STOP and START condition | | | 1.3 | - | - | µs |
| $t_{SU;STO}$ | set-up time for STOP condition | | | 0.6 | - | - | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition | | | 0.6 | - | - | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | | 0.6 | - | - | µs |
| $t_r$ | rise time of both SDA and SCL signals | $f_{SCL}$ = 400 kHz | | - | - | 0.3 | µs |
| | | $f_{SCL}$ < 125 kHz | | - | - | 1.0 | µs |
| $t_f$ | fall time of both SDA and SCL signals | | | - | - | 0.3 | µs |
| $C_b$ | capacitive load for each bus line | | | - | - | 400 | pF |
| $t_{w(spike)}$ | spike pulse width | on the $I^2C$-bus | | - | - | 50 | ns |

[1] Typical output duty factor: 50 % measured at the CLK output pin.
[2] Not tested in production.
[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$.

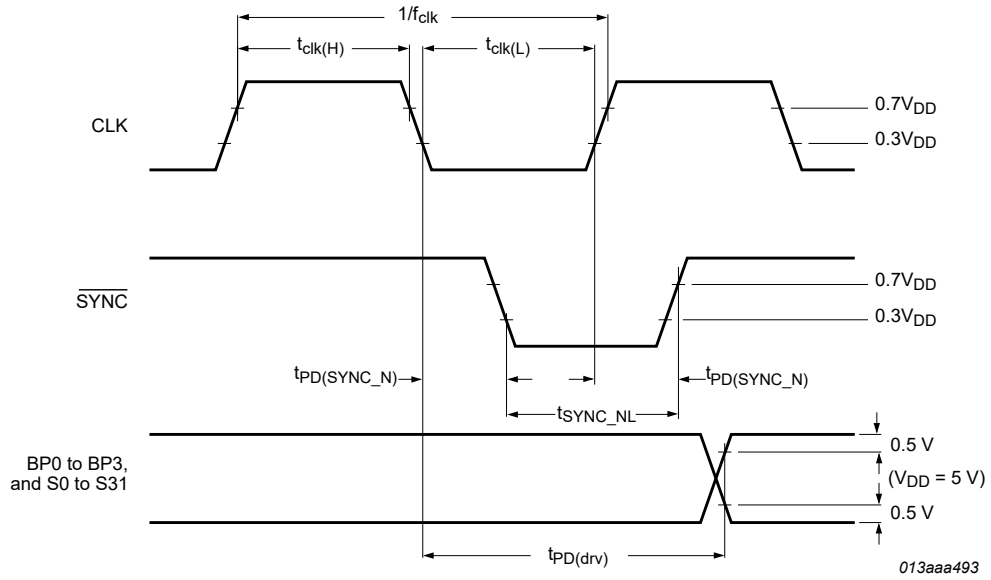



**Figure 20. Driver timing waveforms**

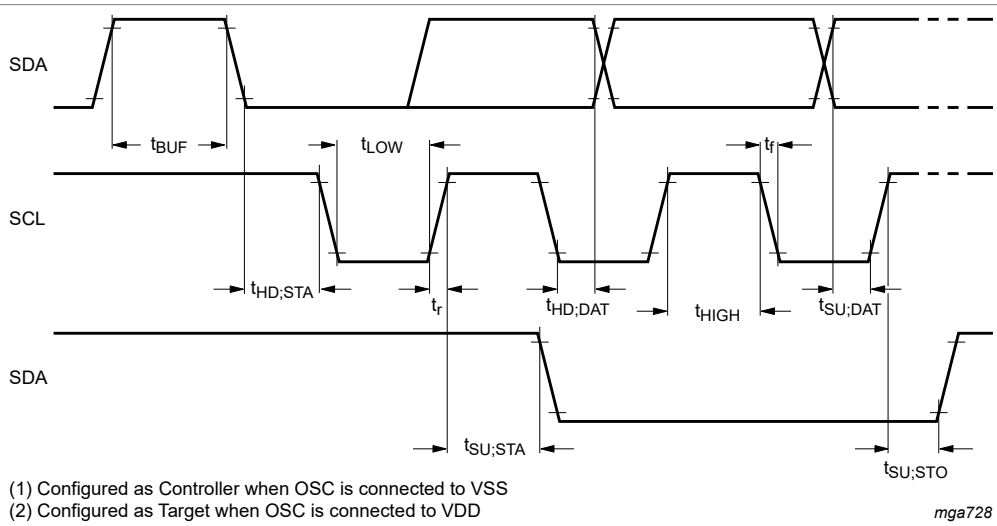



**Figure 21. I²C-bus timing waveforms**

# 12 Application information

## 12.1 Multiple chip operation

For large display configurations or for more segments (> 128 elements) to drive please refer to the PCF8576D device.

The contact resistance between the $\overline{\text{SYNC}}$ input/output on each cascaded device must be controlled. If the resistance is too high, the device will not be able to synchronize properly; this is particularly applicable to chip-on-glass applications. The maximum $\overline{\text{SYNC}}$ contact resistance allowed for the number of devices in cascade is given in Table 19.

Table 19. $\overline{\text{SYNC}}$ contact resistance

| Number of devices | Maximum contact resistance |
|---|---|
| 2 | 6 000 Ω |
| 3 to 5 | 2 200 Ω |
| 6 to 10 | 1 200 Ω |
| 10 to 16 | 700 Ω |

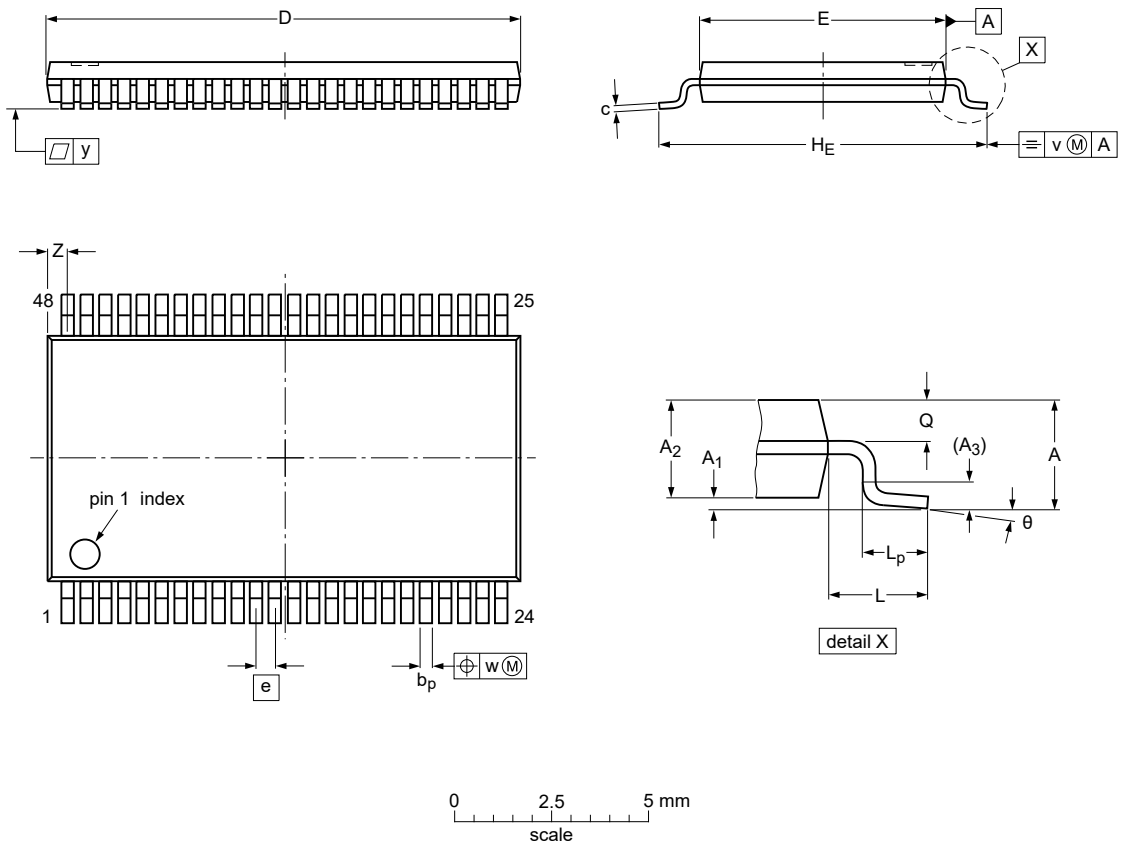
# 13 Test information

## 13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

## 14 Package outline

**TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm** **SOT362-1**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.2 | 0.15 | 1.05 | 0.25 | 0.28 | 0.2 | 12.6 | 6.2 | 0.5 | 8.3 | 1 | 0.8 | 0.50 | 0.25 | 0.08 | 0.1 | 0.8 | 8° |
| | nom | | | | | | | | | | | | | | | | | | |
| | min | | 0.05 | 0.85 | | 0.17 | 0.1 | 12.4 | 6.0 | | 7.9 | | 0.4 | 0.35 | | | | 0.4 | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

*sot362-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT362-1 | | MO-153 | | | | ~~03-02-19~~ 13-08-05 |

**Figure 22. Package outline SOT362-1 (TSSOP48)**

# 15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

# 16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 23) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 20 and Table 21

**Table 20. SnPb eutectic process (from J-STD-020D)**

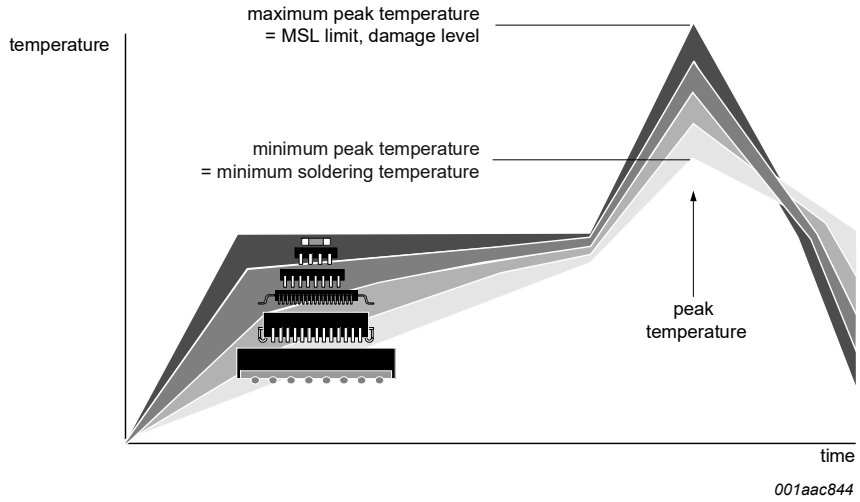
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume (mm³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 21. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume (mm³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 23.




MSL: Moisture Sensitivity Level

**Figure 23. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

# 17 Abbreviations

**Table 22. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| CDM | Charged-Device Model |
| HBM | Human Body Model |
| ITO | Indium Tin Oxide |
| LCD | Liquid Crystal Display |
| LSB | Least Significant Bit |
| MM | Machine Model |
| MSB | Most Significant Bit |
| MSL | Moisture Sensitivity Level |
| PCB | Printed Circuit Board |
| RAM | Random Access Memory |
| RMS | Root Mean Square |
| SCL | Serial Clock Line |
| SDA | Serial Data line |
| SMD | Surface Mount Device |

## 18 References

[1] JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[2] JESD22-A115 Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[3] JESD22-C101 Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[4] JESD78 IC Latch-Up Test

[5] NX3-00092 NXP store and transport requirements

# 19 Revision history

**Table 23. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCF8562 v.8 | 20210927 | Product data sheet | PCN202102010F01 | PCF8562 v.7 |
| Modifications: | • Updated Section 3, Ordering information. See Change notice column.<br>• Removed Marking section (formerly Section 4).<br>• Global: The terms "master" and "slave" changed to "controller" and "target" to comply with NXP inclusive language policy. | | | |
| PCF8562 v.7 | 20150721 | Product data sheet | - | PCF8562 v.6 |
| Modifications: | • Table 17: Replaced values (LCD) supply | | | |
| PCF8562 v.6 | 20110616 | Product data sheet | - | PCF8562 v.5 |
| Modifications: | • Added design-in and replacement part information<br>• Added Section 7.10.3 | | | |
| PCF8562 v.5 | 20100519 | Product data sheet | - | PCF8562 v.4 |
| PCF8562 v.4 | 20090318 | Product data sheet | - | PCF8562 v.3 |
| PCF8562 v.3 | 20081202 | Product data sheet | - | PCF8562 v.2 |
| PCF8562 v.2 | 20070122 | Product data sheet | - | PCF8562 v,1 |
| PCF8562 v.1 | 20050801 | Product data sheet | - | - |

# 20 Legal information

## 20.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## Tables



## Figures