PCF8576E

Universal LCD driver for low multiplex rates

Rev. 1 — 22 January 2013 Product data sheet

1. General description

The PCF8576E is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments. It can be easily cascaded for larger LCD applications. The PCF8576E is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

2. Features and benefits

- Single chip LCD controller and driver
- Selectable backplane drive configuration: static or 2, 3, 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives:
  - Up to 20 7-segment numeric characters
  - Up to 10 14-segment alphanumeric characters
  - Any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
  - From 2.5 V for low-threshold LCDs
  - Up to 6.5 V for high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I^2C-bus interface
- May be cascaded for large LCD applications (up to 2560 elements possible)
- No external components required
- Compatible with chip-on-glass and chip-on-board technology
- Manufactured in silicon gate CMOS process

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 17.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8576EUG	bare die	59 bumps	PCF8576EUG

3.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF8576EUG/2DA/1	935299982026	PCF8576EUG/2DA/1KP	1	chips in tray

4. Marking

Table 3. Marking codes

Product type number	Marking code
PCF8576EUG/2DA/1	PC8576E-1

5. Block diagram

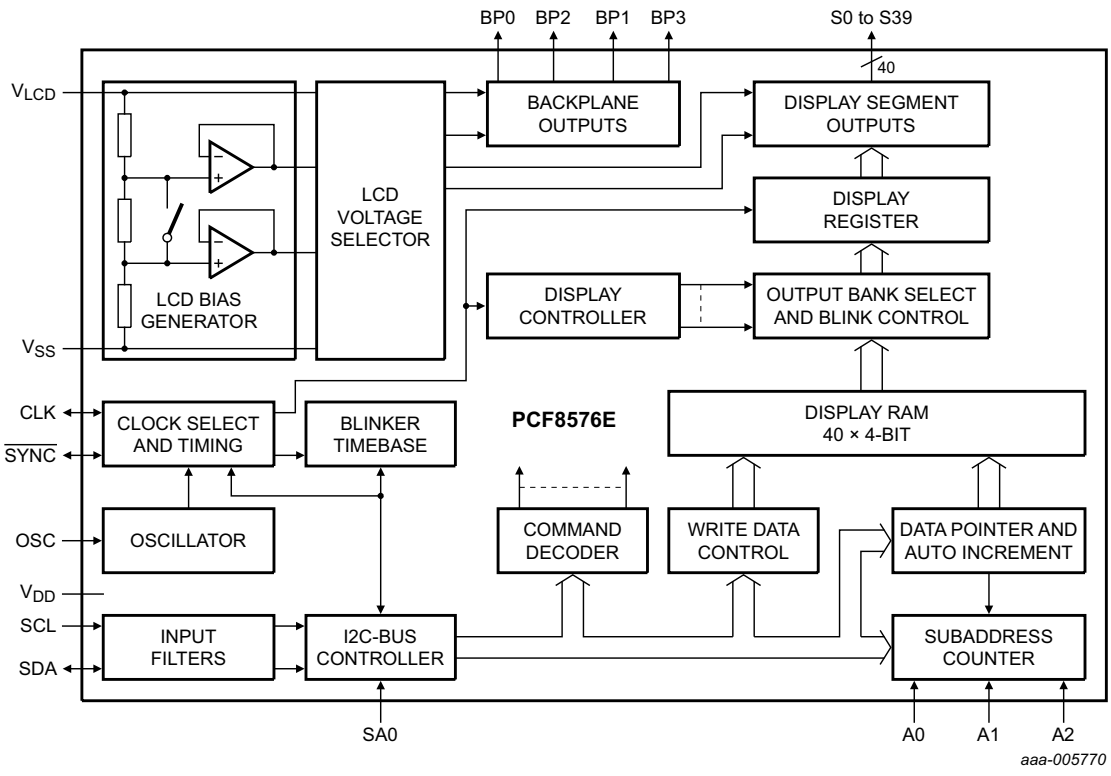
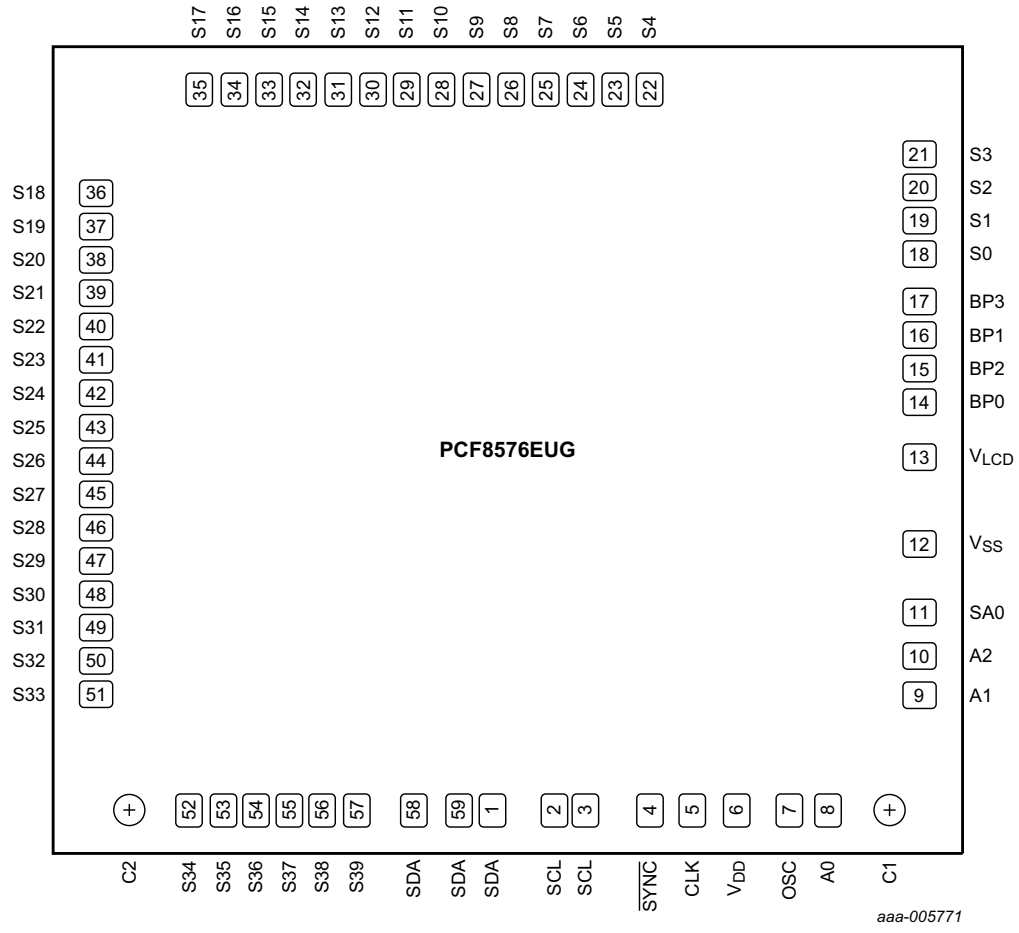


Fig 1. Block diagram of PCF8576E

6. Pinning information

6.1 Pinning



Viewed from active side. C1 and C2 are alignment marks. For mechanical details, see Figure 24.

Fig 2. Pinning diagram for PCF8576EUG (bare die)

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
SDA	1, 58, 59	I^2C-bus serial data input and output
SCL	2, 3	I^2C-bus serial clock input
CLK	5	external clock input or output
V_{DD}	6	supply voltage
$\overline{SYNC}$	4	cascade synchronization input or output
OSC	7	internal oscillator enable input
A0 to A2	8 to 10	subaddress inputs
SA0	11	I^2C-bus address input; bit 0
V_{SS}	12[1]	ground supply voltage
V_{LCD}	13	LCD supply voltage
BP0, BP2, BP1, BP3	14 to 17	LCD backplane outputs
S0 to S39	18 to 57	LCD segment outputs
n.c.	-	not connected

[1] The substrate (rear side of the die) is connected to V_{SS} and should be electrically isolated.

7. Functional description

7.1 Commands of PCF8576E

The commands available to the PCF8576E are defined in Table 5.

Table 5. Definition of PCF8576E commands

Command	Operation code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
mode-set	C	1	0	-[1]	E	B	M[1:0]		Table 7
load-data-pointer	C	0	P[5:0]						Table 8
device-select	C	1	1	0	0	A[2:0]			Table 9
bank-select	C	1	1	1	1	0	I	O	Table 10
blink-select	C	1	1	1	0	AB	BF[1:0]		Table 11

[1] Not used.

All available commands carry a continuation bit C in their most significant bit position as shown in Figure 18. When this bit is set logic 1, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is set logic 0, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data (see Table 6).

Table 6. C bit description

Bit	Symbol	Value	Description
7	C		**continue bit**
		0	last control byte in the transfer; next byte will be regarded as display data
		1	control bytes continue; next byte will be a command too

Table 7. Mode-set command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6, 5	-	10	fixed value
4	-	-	unused
3	E		**display status**[1]
		0	disabled (blank)[2]
		1	enabled
2	B		**LCD bias configuration**[3]
		0	$\frac{1}{3}$ bias
		1	$\frac{1}{2}$ bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] The display is disabled by setting all backplane and segment outputs to V_{LCD}.

[3] Not applicable for static drive mode.

Table 8. Load-data-pointer command bit description

See Section 7.11.1.

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6	-	0	fixed value
5 to 0	P[5:0]	000000 to 100111	6 bit binary value, 0 to 39; transferred to the data pointer to define one of forty display RAM addresses

Table 9. Device-select command bit description

See Section 7.11.2.

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6 to 3	-	1100	fixed value
2 to 0	A[2:0]	000 to 111	3 bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses

Table 10. Bank-select command bit description

See Section 7.11.5 and Section 7.11.6.

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
7	C	0, 1	see Table 6	
6 to 2	-	11110	fixed value	
1	I		**input bank selection**; storage of arriving display data	
		0	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3
0	O		**output bank selection**; retrieval of LCD display data	
		0	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

Table 11. Blink-select command bit description

See Section 7.12.

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6 to 3	-	1110	fixed value
2	AB		**blink mode selection**
		0	normal blinking[1]
		1	alternate RAM bank blinking[2]
1 to 0	BF[1:0]		**blink frequency selection**
		00	off
		01	1
		10	2
		11	3

[1] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[2] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

7.1.1 Initialization

At power-on the status of the I^2C-bus and the registers of the PCF8576E is undefined. Therefore the PCF8576E should be initialized as quickly as possible after power-on to ensure a proper bus communication and to avoid display artifacts. The following instructions should be accomplished for initialization:

- I^2C-bus (see Section 8) initialization (only necessary if no communication with another I^2C device on the bus has already taken place)
  - generating a START condition
  - sending 0h and ignoring the acknowledge
  - generating a STOP condition
- Mode-set command (see Table 7), setting
  - bit E = 0
  - bit B to the required LCD bias configuration

  - bits M[1:0] to the required LCD drive mode
- Load-data-pointer command (see Table 8), setting
  - bits P[5:0] to 0h (or any other required address)
- Device-select command (see Table 9), setting
  - bits A[2:0] to the required hardware subaddress (for example, 0h)
- Bank-select command (see Table 10), setting
  - bit I to 0
  - bit O to 0
- Blink-select command (see Table 11), setting
  - bit AB to 0 or 1
  - bits BF[1:0] to 00 (or to a desired blinking mode)
- writing meaningful information (for example, a logo) into the display RAM

After the initialization, the display can be switched on by setting bit E = 1 with the mode-set command.

7.2 Possible display configurations

The possible display configurations of the PCF8576E depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 12. All of these configurations can be implemented in the typical system shown in Figure 4.

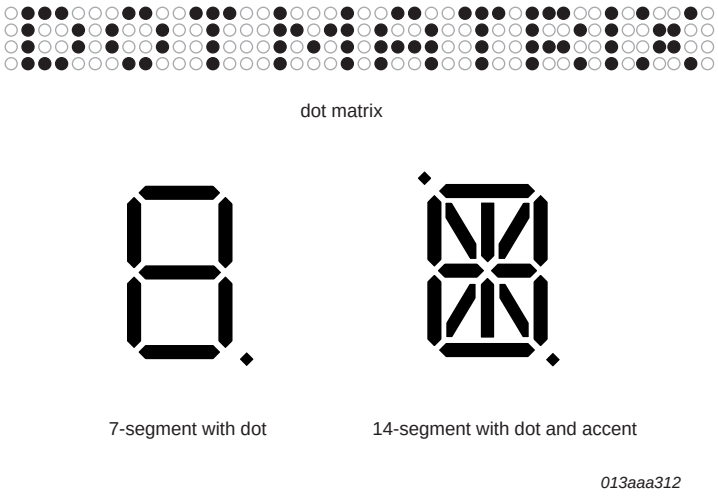


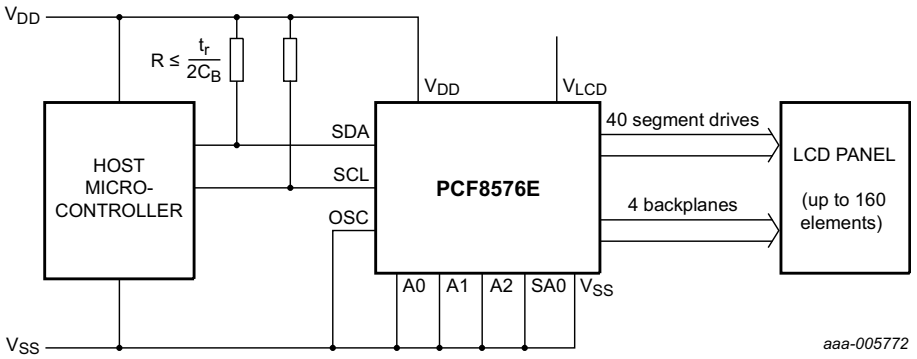
Fig 3. Example of displays suitable for PCF8576E

Table 12. Selection of possible display configurations

Number of Backplanes	Icons	Digits/Characters		Dot matrix/ Elements
		7-segment[1]	14-segment[2]	
4	160	20	10	160 (4 × 40)
3	120	15	7	120 (3 × 40)
2	80	10	5	80 (2 × 40)
1	40	5	2	40 (1 × 40)

[1] 7 segment display has 8 elements including the decimal point.

[2] 14 segment display has 16 elements including decimal point and accent dot.



The resistance of the power lines must be kept to a minimum.

For chip-on-glass applications, due to the Indium Tin Oxide (ITO) track resistance, each supply line must be routed separately between the chip and the connector.

Fig 4. Typical system configuration

The host microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8576E. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.

7.3 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between pins V_{LCD} and V_{SS}. The center impedance is bypassed by switch if the $\frac{1}{2}$ bias voltage level for the 1:2 multiplex drive mode configuration is selected. The LCD voltage can be temperature compensated externally using the supply to pin V_{LCD}.

7.4 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 13.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 13. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (1)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1+a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

7.4.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 5. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

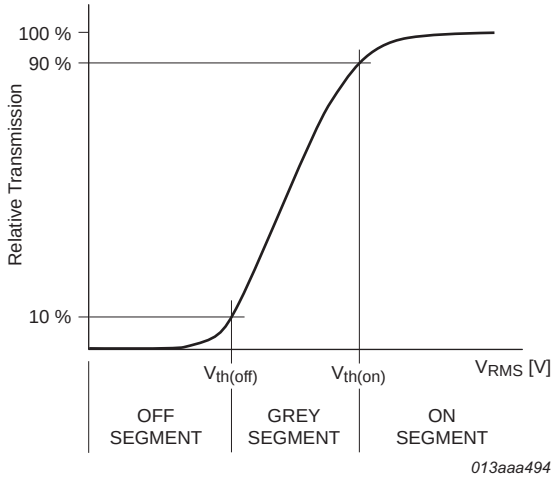
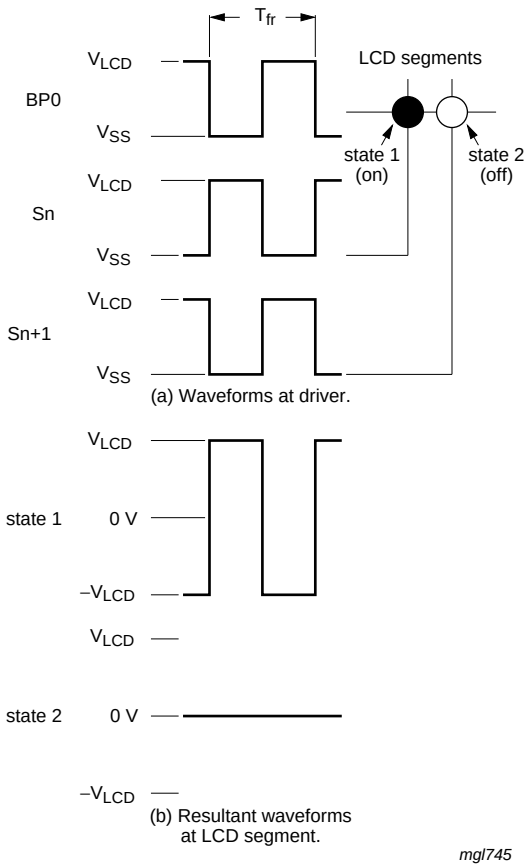


Fig 5. Electro-optical characteristic: relative transmission curve of the liquid

7.5 LCD drive mode waveforms

7.5.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment drive (S_n) waveforms for this mode are shown in Figure 6.



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = V_{LCD}$.

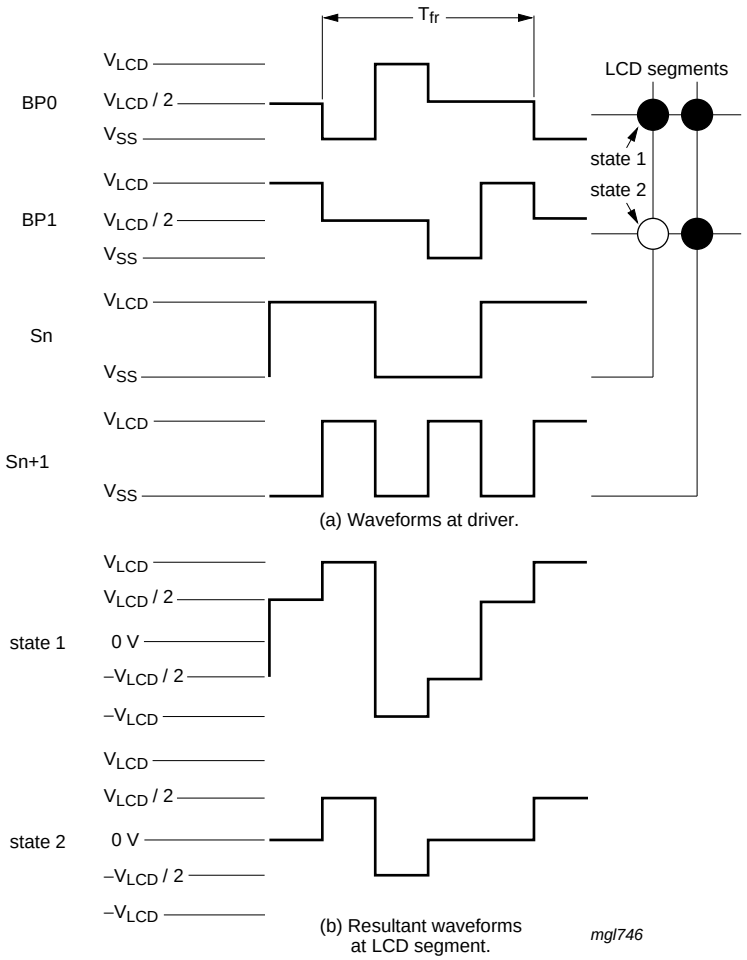
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

(4) $V_{off(RMS)} = 0$ V.

Fig 6. Static drive mode waveforms

7.5.2 1:2 Multiplex drive mode

The 1:2 multiplex drive mode is used when two backplanes are provided in the LCD. This mode allows fractional LCD bias voltages of ½ bias or ⅓ bias as shown in Figure 7 and Figure 8.



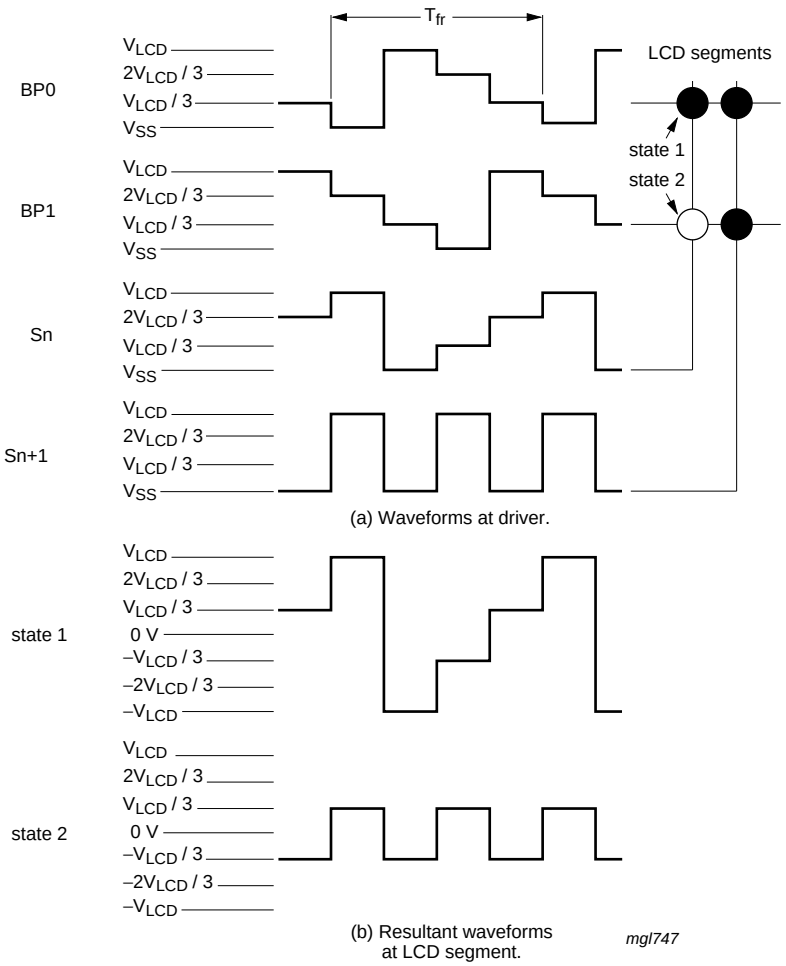
(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.791V_{LCD}$.

(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.354V_{LCD}$.

Fig 7. Waveforms for the 1:2 multiplex drive mode with ½ bias



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.745V_{LCD}$.

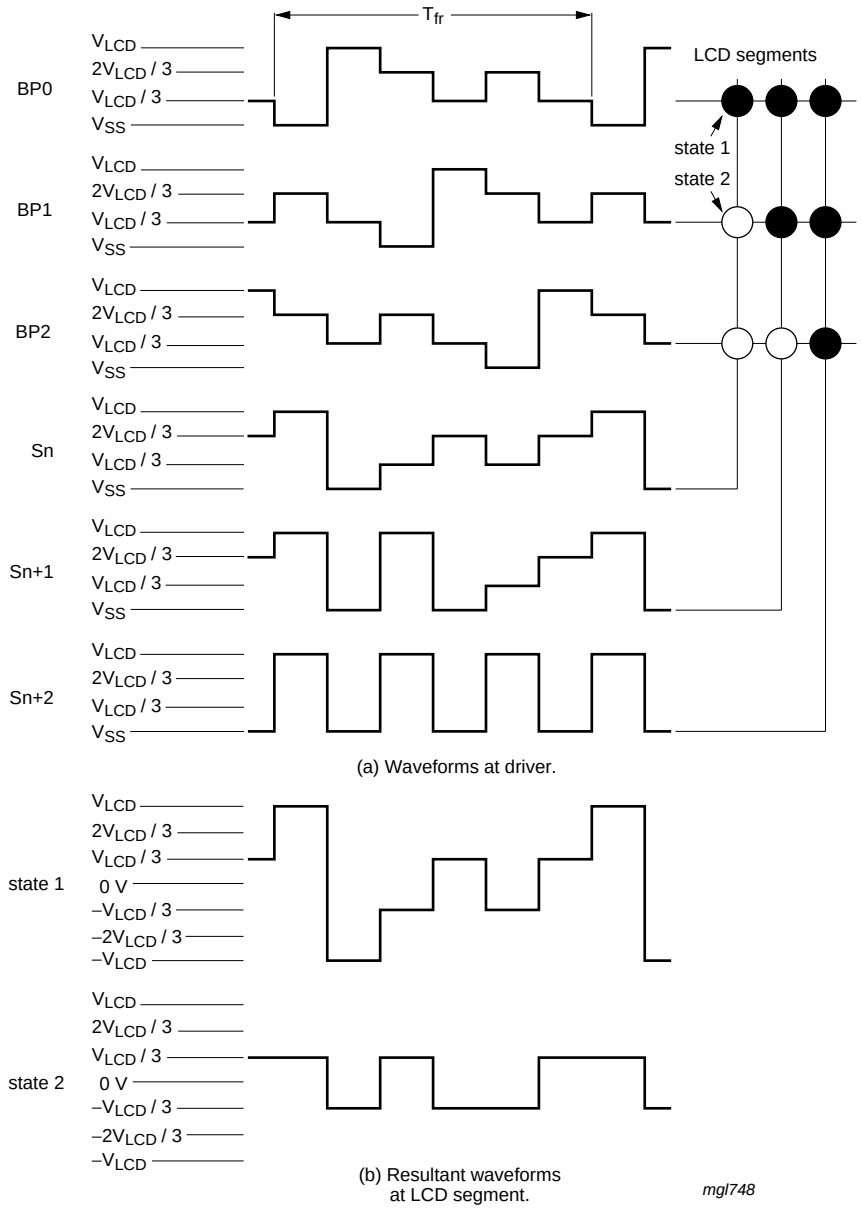
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 8. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

7.5.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies (see Figure 9).



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.638V_{LCD}$.

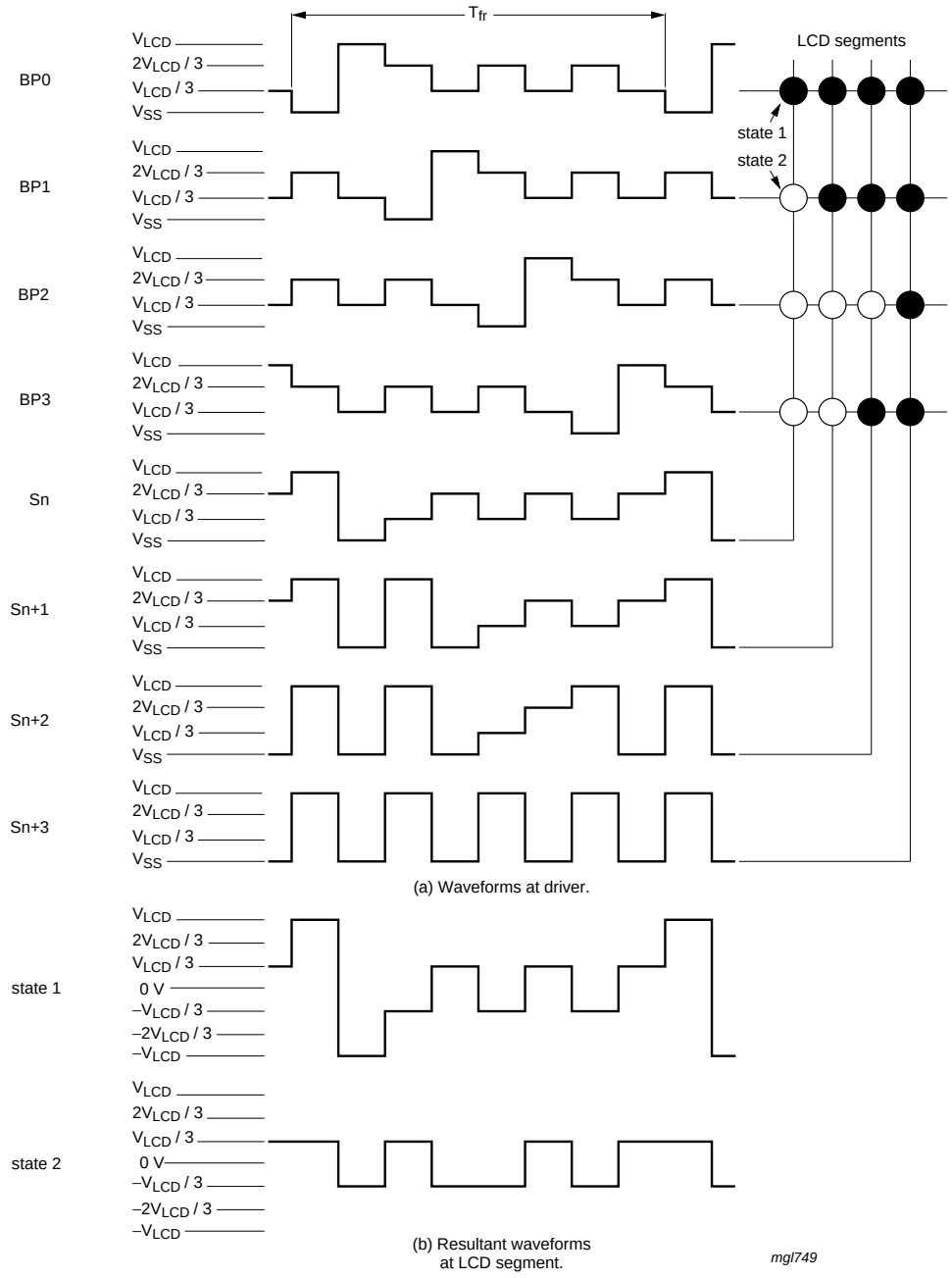
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

7.5.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies (see Figure 10).



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.577V_{LCD}$.

(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 10. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

7.6 Oscillator

7.6.1 Internal clock

The internal logic of the PCF8576E and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several PCF8576Es in the system that are connected in cascade.

7.6.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}. The LCD frame signal frequency is determined by the clock frequency (f_{clk}).

Remark: A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.7 Timing

The PCF8576E timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCF8576E in the system is maintained by the synchronization signal at pin $\overline{SYNC}$. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock: $f_{fr} = \frac{f_{clk}}{24}$.

7.8 Display register

The display latch holds the display data while the corresponding multiplex signals are generated.

7.9 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display latch. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7.10 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode, BP0 and BP2, respectively, BP1 and BP3 all carry the same signals and may also be paired to increase the drive capabilities.
- In static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.11 Display RAM

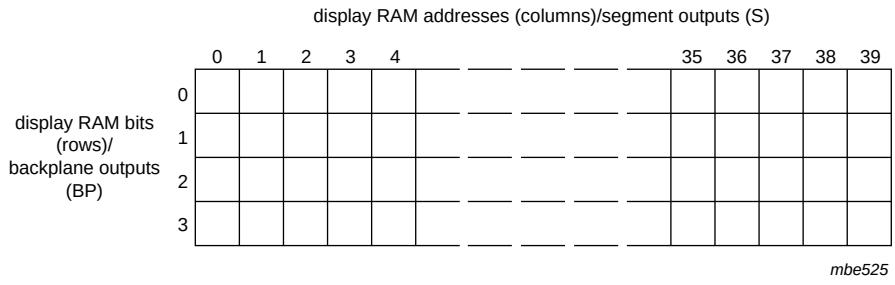
The display RAM is a static 40 × 4-bit RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

The display RAM bit map, Figure 11, shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.



The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs; and between the bits in a RAM row and the backplane outputs.

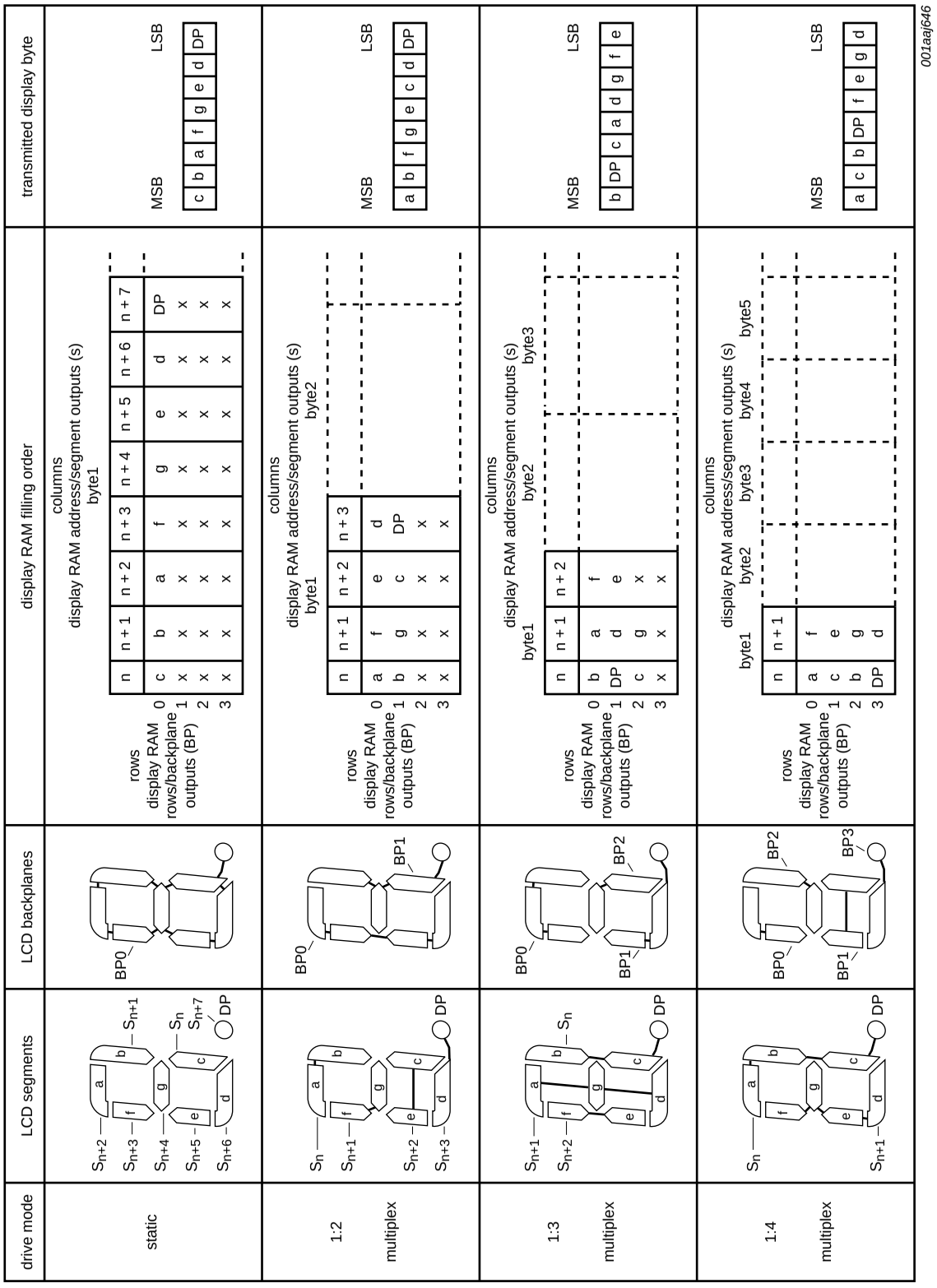
Fig 11. Display RAM bit map

When display data is transmitted to the PCF8576E, the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and depending on the current multiplex drive mode the bits are stored singularly,

in pairs, triples, or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in Figure 12; the RAM filling organization depicted applies equally to other LCD types.

The following applies to Figure 12:

- In static drive mode the eight transmitted data bits are placed into row 0 as one byte.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as two successive 4-bit RAM words.
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 7.11.3).
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words.



x = data bit unchanged.

Fig 12. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus

7.11.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 8). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 12. After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I^2C-bus data access terminates early then the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.

7.11.2 Subaddress counter

The storage of display data is determined by the contents of the subaddress counter. Storage is allowed only when the content of the subaddress counter match with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 9). If the content of the subaddress counter and the hardware subaddress do not match then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576E occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

The hardware subaddress must not be changed while the device is being accessed on the I^2C-bus interface.

7.11.3 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 14 (see Figure 12 as well).

Table 14. Standard RAM filling in 1:3 multiplex drive mode

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are not connected** to any elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**:**
0	a7	a4	a1	b7	b4	b1	c7	c4	c1	d7	:
1	a6	a3	a0	b6	b3	b0	c6	c3	c0	d6	:
2	a5	a2	-	b5	b2	-	c5	c2	-	d5	:
3	-	-	-	-	-	-	-	-	-	-	:

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 15.

Table 15. Entire RAM filling by rewriting in 1:3 multiplex drive mode

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are connected** to elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**:**
0	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	e4	:
1	a6	a3	a0/b6	b3	b0/c6	c3	c0/d6	d3	d0/e6	e3	:
2	a5	a2	b5	b2	c5	c2	d5	d2	e5	e2	:
3	-	-	-	-	-	-	-	-	-	-	:

In the case described in Table 15 the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8 etc. have to be connected to elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written.
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6.
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6.

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some elements remain unused or can be used, but it has to be considered in the module layout process as well as in the driver software design.

7.11.4 Writing over the RAM address boundary

In all multiplex drive modes, depending on the setting of the data pointer, it is possible to fill the RAM over the RAM address boundary. If the PCF8576E is part of a cascade the additional bits fall into the next device that also generates the acknowledge signal. If the PCF8576E is a single device or the last device in a cascade the additional bits will be discarded and no acknowledge signal will be generated.

7.11.5 Output bank selector

The output bank selector (see Table 10) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the selected LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The PCF8576E includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex

mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.11.6 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command (see Table 10). The input bank selector functions independently to the output bank selector.

7.12 Blinking

The display blinking capabilities of the PCF8576E are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 11). The blink frequencies are derived from the clock frequency. The ratio between the clock and blink frequencies depends on the blink mode selected (see Table 11).

An additional feature is for an arbitrary selection of LCD elements to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternative RAM bank is available, groups of LCD elements can blink by selectively changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 7).

Table 16. Blinking frequencies

Blink mode	Normal operating mode ratio	Nominal blink frequency[1]
off	-	blinking off
1	$\frac{f_{clk}}{768}$	2 Hz
2	$\frac{f_{clk}}{1536}$	1 Hz
3	$\frac{f_{clk}}{3072}$	0.5 Hz

[1] Blink modes 1, 2 and 3 and the nominal blink frequencies 0.5 Hz, 1 Hz and 2 Hz correspond to an oscillator frequency (f_{clk}) of 1536 Hz (see Section 12).

7.13 Display controller

The display controller executes the commands identified by the command decoder. It contains the device's status registers and coordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.

8. Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 13).

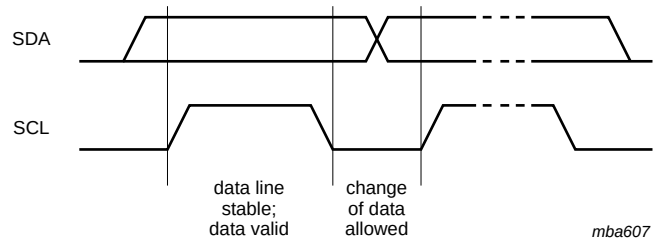


Fig 13. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P.

The START and STOP conditions are illustrated in Figure 14.

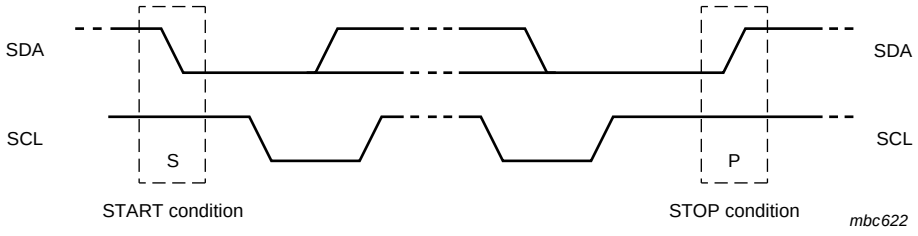


Fig 14. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 15.

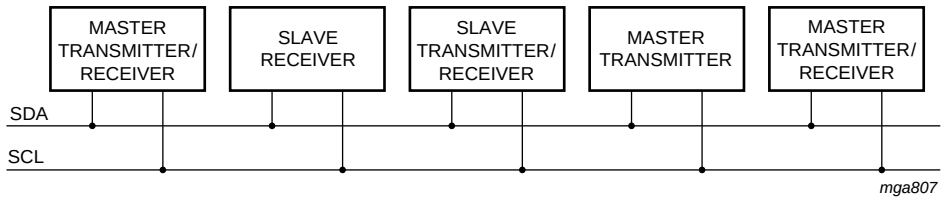


Fig 15. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is illustrated in Figure 16.

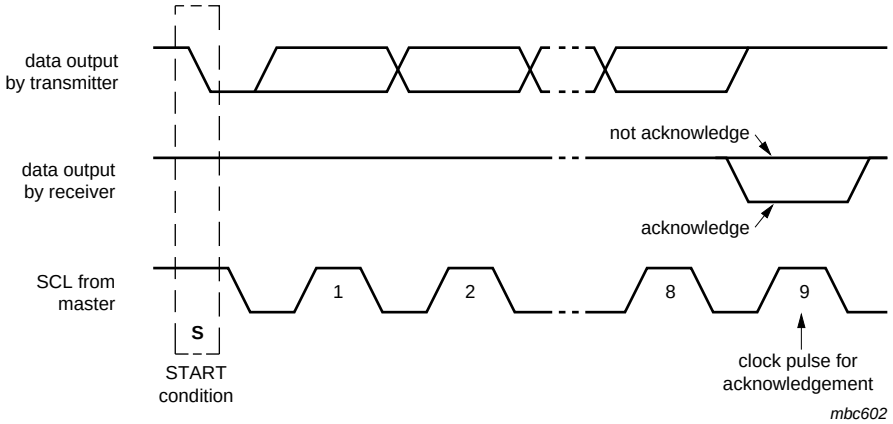


Fig 16. Acknowledgement of the I^2C-bus

8.4 I²C-bus controller

The PCF8576E acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8576E are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1, and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1, and A2 are tied to V_{SS} or V_{DD} using a binary coding scheme, so that no two devices with a common I²C-bus slave address have the same hardware subaddress.

8.5 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

8.6 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are used to address the PCF8576E. The entire I²C-bus slave address byte is shown in Table 17.

Table 17. I²C slave address byte

Bit	Slave address							
	7	6	5	4	3	2	1	0
	MSB							LSB
	0	1	1	1	0	0	SA0	R/$\overline{W}$

The PCF8576E is a write-only device and will not respond to a read access, therefore bit 0 should always be logic 0. Bit 1 of the slave address byte that a PCF8576E will respond to, is defined by the level tied to its SA0 input (V_{SS} for logic 0 and V_{DD} for logic 1).

Having two reserved slave addresses allows the following on the same I²C-bus:

- Up to 16 PCF8576E for very large LCD applications
- The use of two types of LCD multiplex drive

The I²C-bus protocol is shown in Figure 17. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of two possible PCF8576E slave addresses available. All PCF8576Es whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCF8576Es whose SA0 inputs are set to the alternative level.

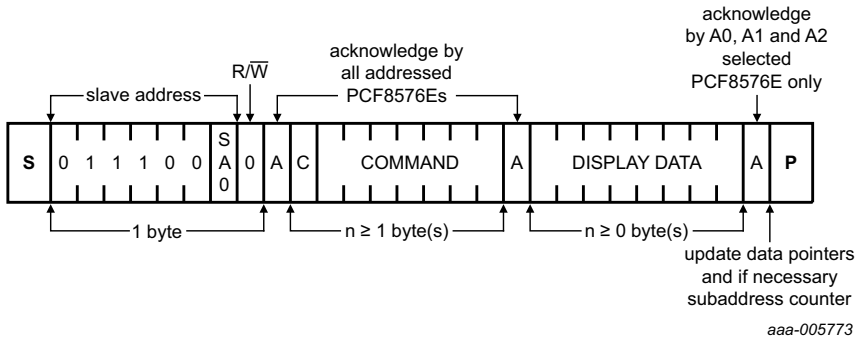


Fig 17. I²C-bus protocol

After an acknowledgement, one or more command bytes follow, that define the status of each addressed PCF8576E.

The last command byte sent is identified by resetting its most significant bit, continuation bit C, (see Figure 18). The command bytes are also acknowledged by all addressed PCF8576E on the bus.

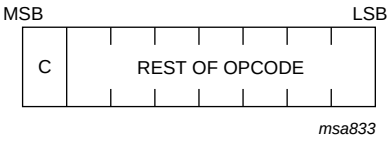


Fig 18. Format of command byte

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data directed to the intended PCF8576E device.

An acknowledgement after each byte is asserted only by the PCF8576Es that are addressed via address lines A0, A1, and A2. After the last display byte, the I²C-bus master asserts a STOP condition (P). Alternately a START may be asserted to restart an I²C-bus access.

9. Internal circuitry

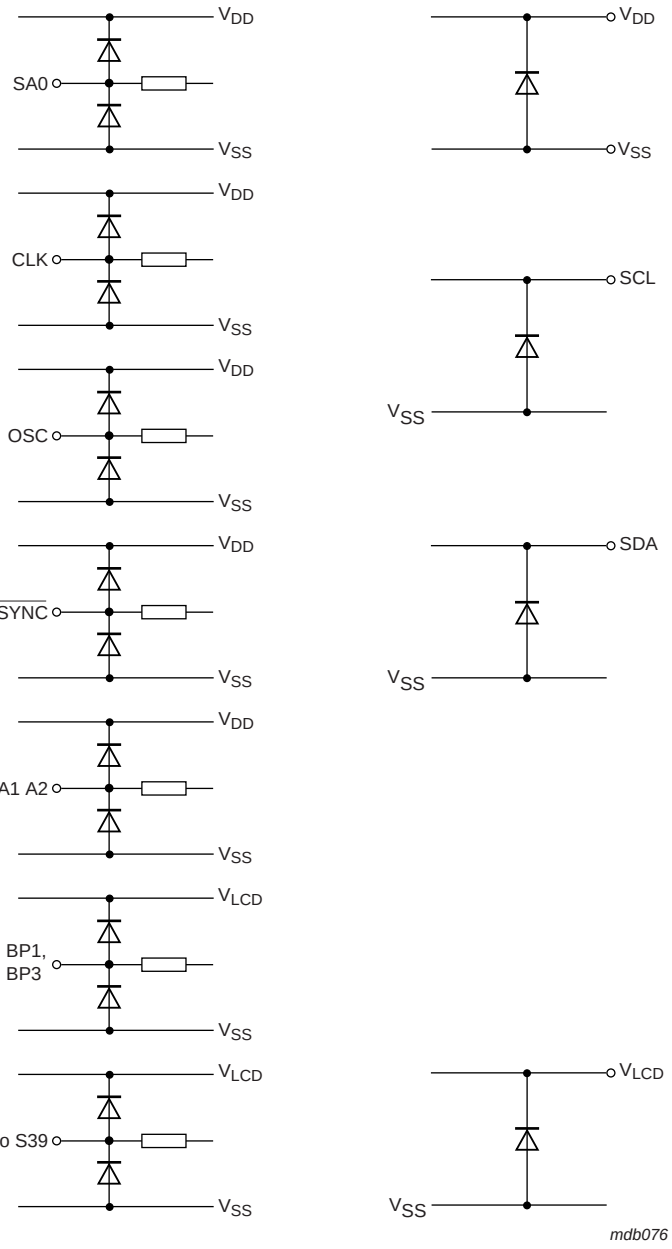


Fig 19. Device protection circuits

10. Limiting values

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+6.5	V
V_{LCD}	LCD supply voltage			−0.5	+7.5	V
V_I	input voltage	on each of the pins CLK, SDA, SCL, $\overline{SYNC}$, SA0, OSC, A0 to A2		−0.5	+6.5	V
V_O	output voltage	on each of the pins S0 to S39, BP0 to BP3		−0.5	+7.5	V
I_I	input current			−10	+10	mA
I_O	output current			−10	+10	mA
I_{DD}	supply current			−50	+50	mA
$I_{DD(LCD)}$	LCD supply current			−50	+50	mA
I_{SS}	ground supply current			−50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P_o	output power			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±5000	V
I_{lu}	latch-up current		[2]	-	200	mA
T_{stg}	storage temperature		[3]	−65	+150	°C
T_{amb}	ambient temperature	operating device		−40	+85	°C

[1] Pass level; Human Body Model (HBM) according to Ref. 8 “JESD22-A114”.

[2] Pass level; latch-up testing according to Ref. 9 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[3] According to the store and transport requirements (see Ref. 12 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

11. Static characteristics

Table 19. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage		[1]	2.5	-	6.5	V
I_{DD}	supply current	$f_{clk(ext)}$ = 1536 Hz	[2]	-	6	20	μA
		V_{DD} = 3.0 V; T_{amb} = 25 °C		-	2.7	-	μA
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)}$ = 1536 Hz	[2]	-	18	30	μA
		$V_{DD(LCD)}$ = 3.0 V; T_{amb} = 25 °C		-	17.5	-	μA
Logic[3]							
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2, SA0, SCL, SDA		V_{SS}	-	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2, SA0, SCL, SDA	[4][5]	0.7V_{DD}	-	V_{DD}	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 5 V					
		on pins CLK and $\overline{SYNC}$		1	-	-	mA
		on pin SDA		3	-	-	mA
$I_{OH(CLK)}$	HIGH-level output current on pin CLK	output source current; V_{OH} = 4.6 V; V_{DD} = 5 V		1	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}; on pins CLK, SCL, SDA, A0 to A2 and SA0		−1	-	+1	μA
$I_{L(OSC)}$	leakage current on pin OSC	V_I = V_{DD}		−1	-	+1	μA
C_I	input capacitance		[6]	-	-	7	pF
LCD outputs							
ΔV_O	output voltage variation	on pins BP0 to BP3 and S0 to S39		−100	-	+100	mV
R_O	output resistance	V_{LCD} = 5 V	[7]				
		on pins BP0 to BP3		-	1.5	-	kΩ
		on pins S0 to S39		-	6.0	-	kΩ

[1] V_{LCD} > 3 V for ⅓ bias.

[2] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I^2C-bus inactive.

[3] The I^2C-bus interface of PCF8576E is 5 V tolerant.

[4] When tested, I^2C pins SCL and SDA have no diode to V_{DD} and may be driven to the V_I limiting values given in Table 18.

[5] Propagation delay of driver between clock (CLK) and LCD driving signals.

[6] Periodically sampled, not 100 % tested.

[7] Outputs measured one at a time.

12. Dynamic characteristics

Table 20. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
$f_{clk(int)}$	internal clock frequency		[1]	1440	1850	2640	Hz
$f_{clk(ext)}$	external clock frequency			960	-	2640	Hz
$t_{clk(H)}$	HIGH-level clock time			60	-	-	µs
$t_{clk(L)}$	LOW-level clock time			60	-	-	µs
Synchronization							
$t_{PD(SYNC\_N)}$	$\overline{SYNC}$ propagation delay			-	30	-	ns
t_{SYNC_NL}	$\overline{SYNC}$ LOW time			1	-	-	µs
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V	[2]	-	-	30	µs
I²C-bus[3]							
Pin SCL							
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
Pin SDA							
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
Pins SCL and SDA							
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals	f_{SCL} = 400 kHz		-	-	0.3	µs
		f_{SCL} < 125 kHz		-	-	1.0	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{w(spike)}$	spike pulse width	on the I²C-bus		-	-	50	ns

[1] Typical output duty factor: 50 % measured at the CLK output pin.

[2] Not tested in production.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

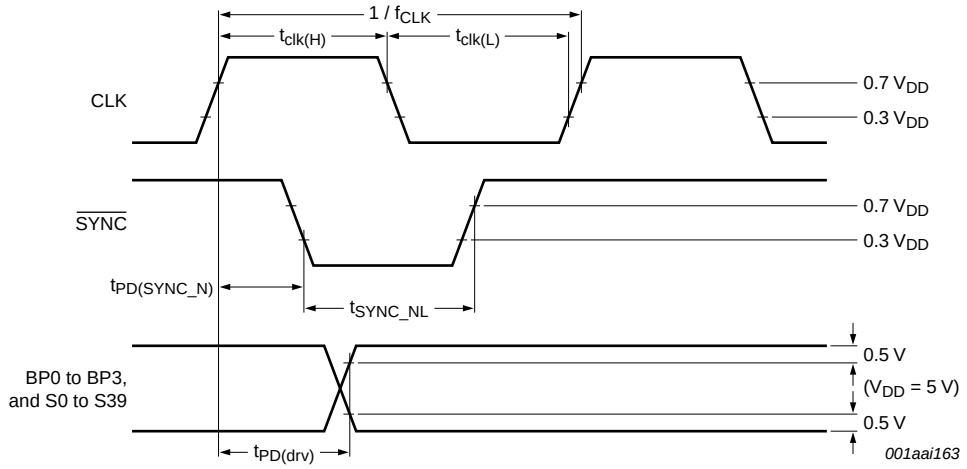


Fig 20. Driver timing waveforms

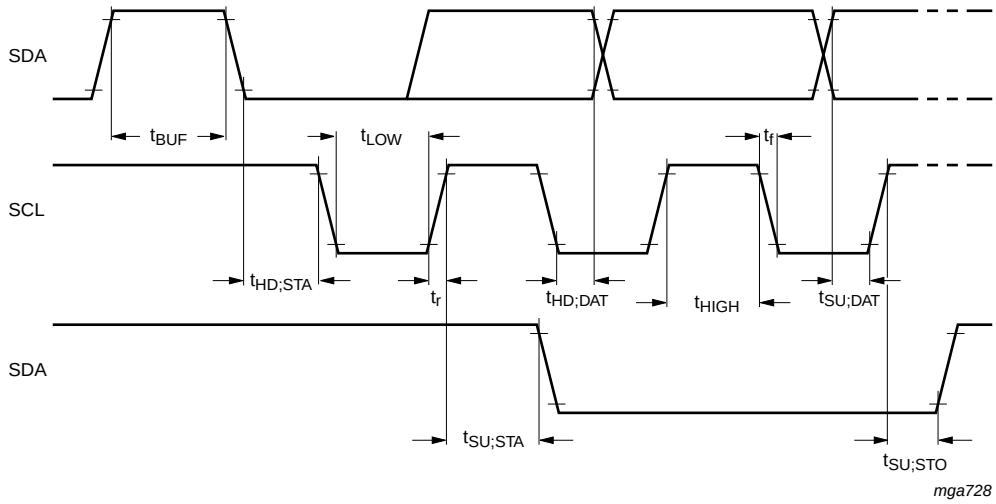


Fig 21. I²C-bus timing waveforms

13. Application information

13.1 Cascaded operation

In large display configurations, up to 16 PCF8576Es can be differentiated on the same I^2C-bus by using the 3-bit hardware subaddresses (A0, A1 and A2) and the programmable I^2C-bus slave address (SA0).

Table 21. Addressing cascaded PCF8576E

Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

PCF8576Es connected in cascade are synchronized to allow the backplane signals from only one device in the cascade to be shared. This arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other cascaded PCF8576Es contribute additional segment outputs but their backplane outputs are left open-circuit (see Figure 22).

All PCF8576Es connected in cascade are correctly synchronized by the $\overline{\text{SYNC}}$ signal. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is lost accidentally, for example, by noise in adverse electrical environments, or if the LCD multiplex drive mode is changed in an application using several cascaded PCF8576Es, as the drive mode cannot be changed on all of the cascaded devices simultaneously. $\overline{\text{SYNC}}$ can be either an input or an output signal; a $\overline{\text{SYNC}}$ output is implemented as an open-drain driver with an internal pull-up resistor. The PCF8576E asserts $\overline{\text{SYNC}}$ at the start of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. If cascade synchronization is lost, it is restored by the first PCF8576E to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for each LCD drive mode is shown in Figure 23.

The contact resistance between the $\overline{SYNC}$ on each cascaded device must be controlled. If the resistance is too high, the device is not able to synchronize properly; this is particularly applicable to chip-on-glass applications. The maximum $\overline{SYNC}$ contact resistance allowed for the number of devices in cascade is given in Table 22.

Table 22. $\overline{SYNC}$ contact resistance

Number of devices	Maximum contact resistance
2	6 kΩ
3 to 5	2.2 kΩ
6 to 10	1.2 kΩ
10 to 16	700 Ω

The PCF8576E can be cascaded with the PCF8562. This allows optimal drive selection for a given number of pixels to display. Figure 20 and Figure 21 show the timing of the synchronization signals.

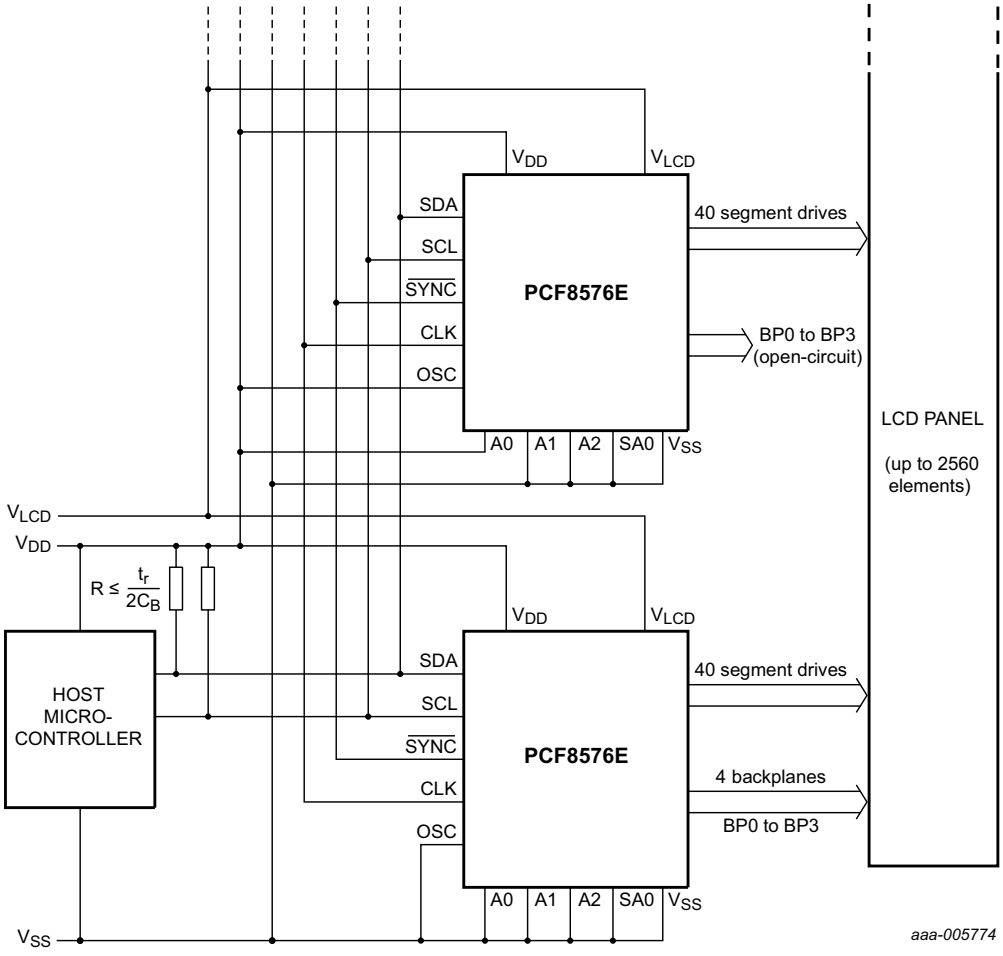


Fig 22. Cascaded PCF8576E configuration

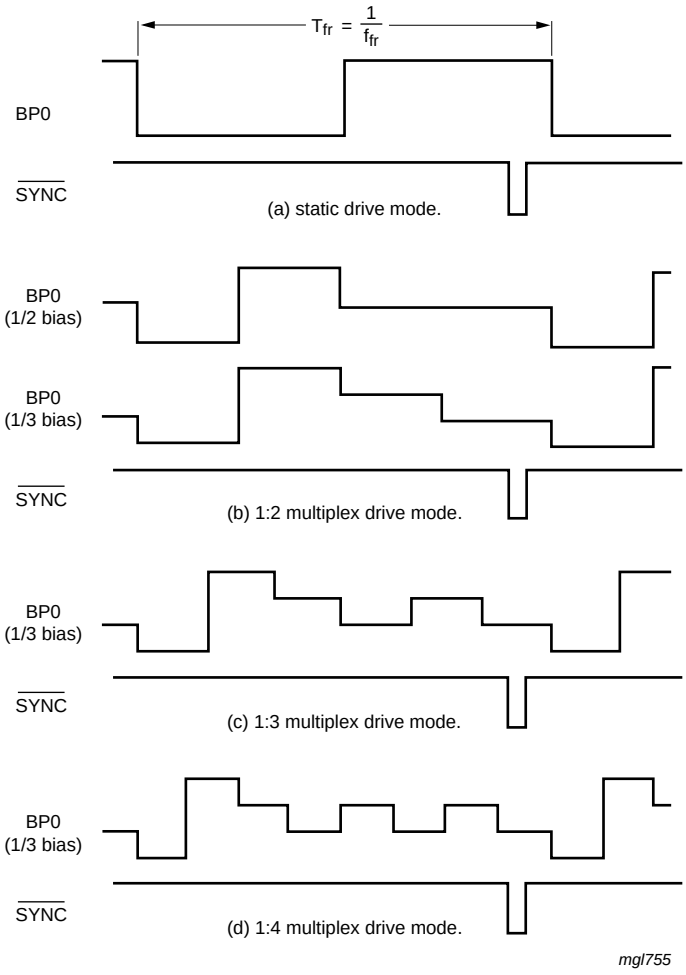
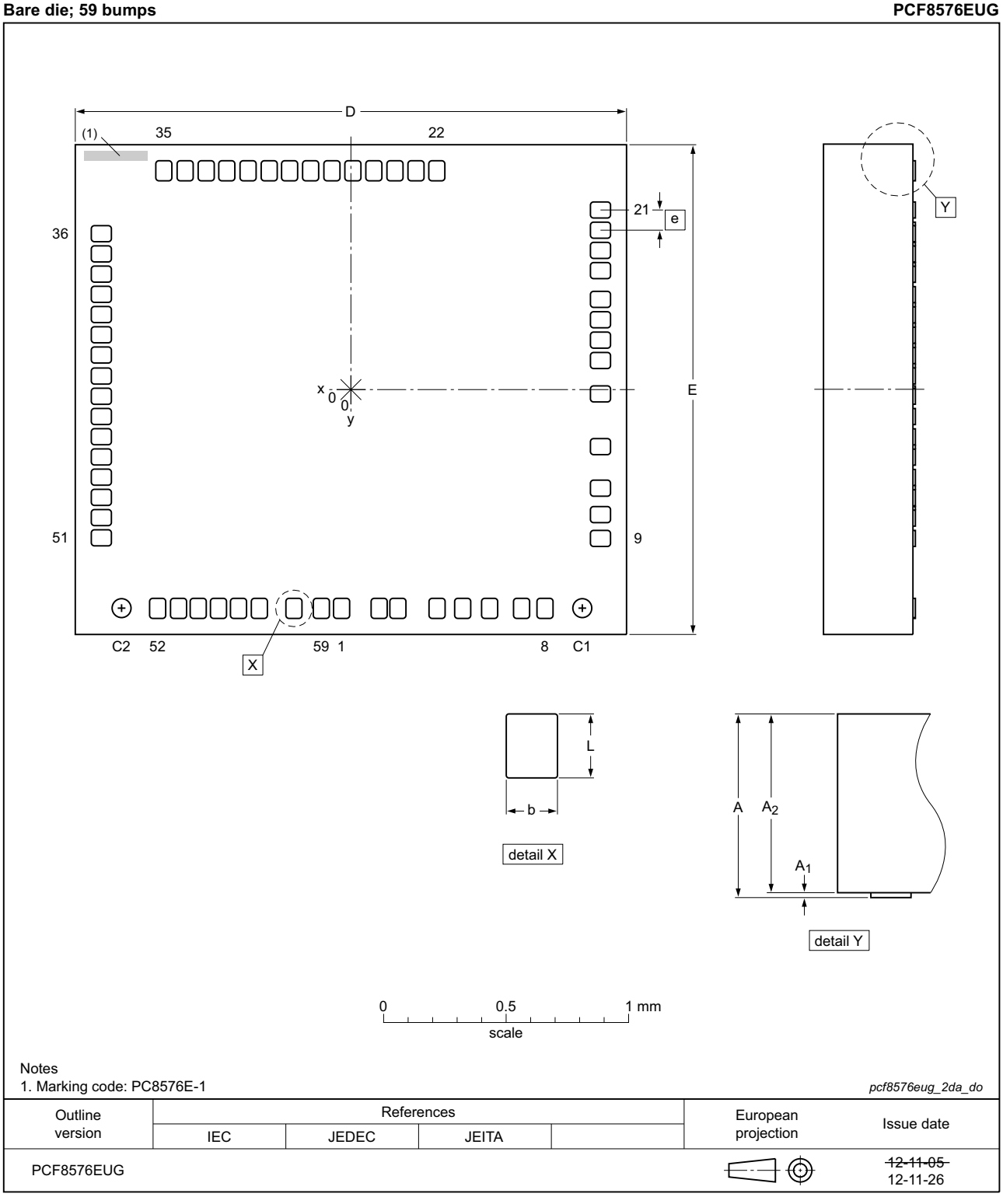


Fig 23. Synchronization of the cascade for the various PCF8576E drive modes

14. Bare die outline

Bare die; 59 bumps **PCF8576EUG**



Notes
1. Marking code: PC8576E-1

pcf8576eug_2da_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8576EUG						~~12-11-05~~ 12-11-26

Fig 24. Bare die outline PCF8576EUG (for dimensions see Table 23)

Table 23. Dimensions of PCF8576EUG

Original dimensions are in mm.

Unit (mm)	A	A_1	A_2	b	D	E	e[1]	L
max	-	0.012	-	-	-	-	-	-
nom	0.40	0.015	0.381	0.052	2.2	2.0	-	0.077
min	-	0.018	-	-	-	-	0.072	-

[1] Dimension not drawn to scale.

Table 24. Bump location for PCF8576EUG

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 2, and Figure 24).

Symbol	Pad	X (µm)	Y (µm)	Description
SDA	1	−34.38	−876.6	I^2C-bus serial data input/output
SCL	2	109.53	−876.6	I^2C-bus serial clock input
SCL	3	181.53	−876.6	
$\overline{SYNC}$	4	365.58	−876.6	cascade synchronization input/output
CLK	5	469.08	−876.6	external clock input/output
V_{DD}	6	577.08	−876.6	supply voltage
OSC	7	740.88	−876.6	internal oscillator enable input
A0	8	835.83	−876.6	subaddress inputs
A1	9	1005.48	−630.9	
A2	10	1005.48	−513.9	
SA0	11	1005.48	−396.9	I^2C-bus address input; bit 0
V_{SS}	12	1005.48	−221.4	ground supply voltage
V_{LCD}	13	1005.48	10.71	LCD supply voltage
BP0	14	1005.48	156.51	LCD backplane outputs
BP2	15	1005.48	232.74	
BP1	16	1005.48	308.97	
BP3	17	1005.48	385.2	
S0	18	1005.48	493.2	LCD segment outputs
S1	19	1005.48	565.2	
S2	20	1005.48	637.2	
S3	21	1005.48	709.2	

Table 24. Bump location for PCF8576EUG *…continued*

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 2, and Figure 24).

Symbol	Pad	X (μm)	Y (μm)	Description
S4	22	347.22	876.6	LCD segment outputs
S5	23	263.97	876.6	
S6	24	180.72	876.6	
S7	25	97.47	876.6	
S8	26	14.22	876.6	
S9	27	−69.03	876.6	
S10	28	−152.28	876.6	
S11	29	−235.53	876.6	
S12	30	−318.78	876.6	
S13	31	−402.03	876.6	
S14	32	−485.28	876.6	
S15	33	−568.53	876.6	
S16	34	−651.78	876.6	
S17	35	−735.03	876.6	
S18	36	−1005.5	625.59	
S19	37	−1005.5	541.62	
S20	38	−1005.5	458.19	
S21	39	−1005.5	374.76	
S22	40	−1005.5	291.33	
S23	41	−1005.5	207.9	
S24	42	−1005.5	124.47	
S25	43	−1005.5	41.04	
S26	44	−1005.5	−42.39	
S27	45	−1005.5	−125.8	
S28	46	−1005.5	−209.3	
S29	47	−1005.5	−292.7	
S30	48	−1005.5	−376.1	
S31	49	−1005.5	−459.5	
S32	50	−1005.5	−543	
S33	51	−1005.5	−625.6	
S34	52	−735.03	−876.6	
S35	53	−663.03	−876.6	
S36	54	−591.03	−876.6	
S37	55	−519.03	−876.6	
S38	56	−447.03	−876.6	
S39	57	−375.03	−876.6	
SDA	58	−196.38	−876.6	I^2C-bus serial data input/output
SDA	59	−106.38	−876.6	

Table 25. Alignment marks

All x/y coordinates represent the position of the center of each alignment mark with respect to the center (x/y = 0) of the chip (see Figure 2, and Figure 24).

Symbol	Location		Dimension
	X (μm)	Y (μm)	Diameter (μm)
C1	930.42	−870.3	72
C2	−829.98	−870.3	72

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

16. Packing information

16.1 Tray information

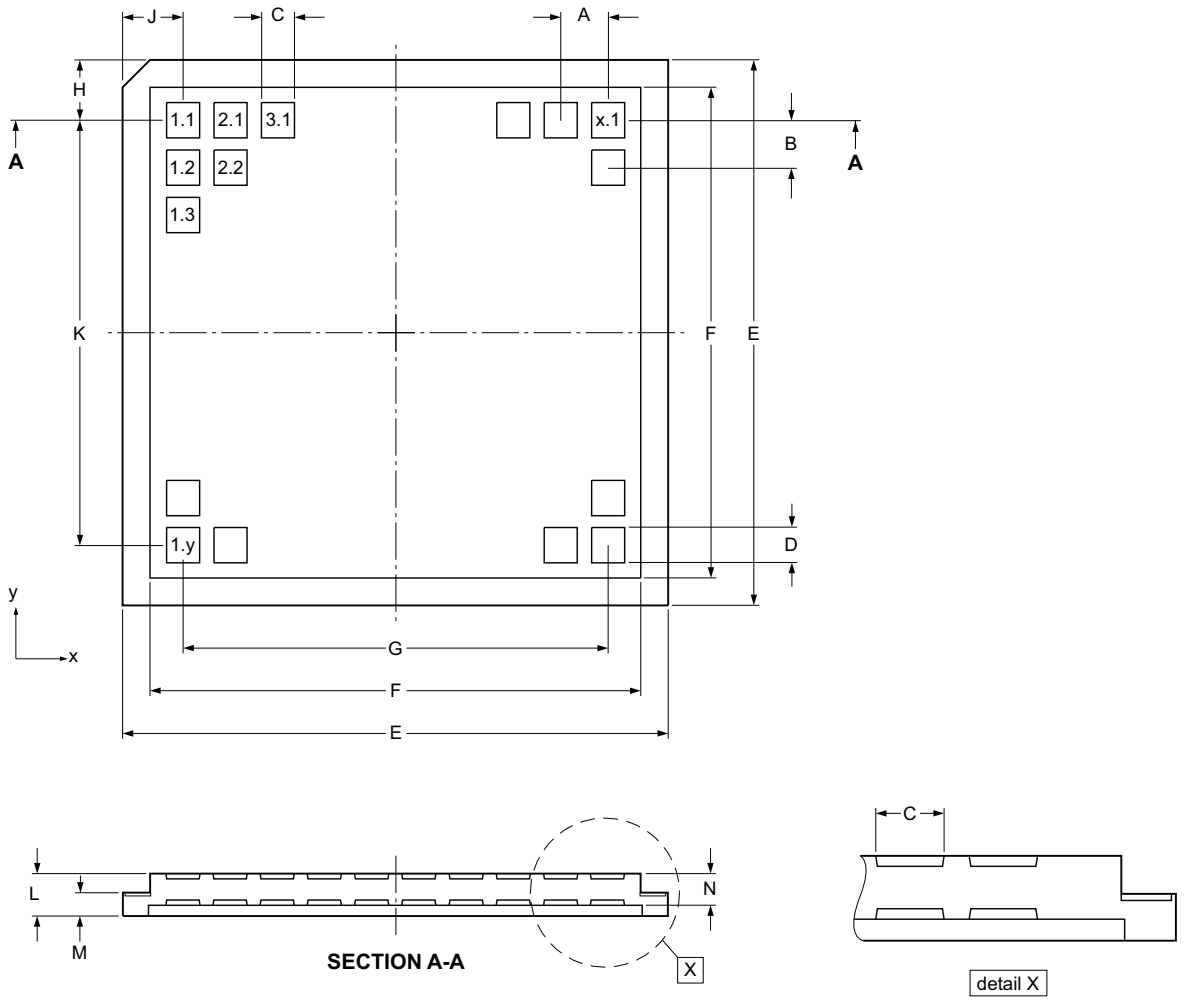


Fig 25. Tray details

Table 26. Description of tray details

Tray details are shown in Figure 25.

Tray details													
Dimensions													
A	B	C	D	E	F	G	H	J	K	L	M	N	Unit
3.6	3.6	2.36	2.11	50.8	45.72	39.6	5.6	5.6	39.6	3.96	2.18	2.49	mm
Number of pockets													
x direction							y direction						
12							12						

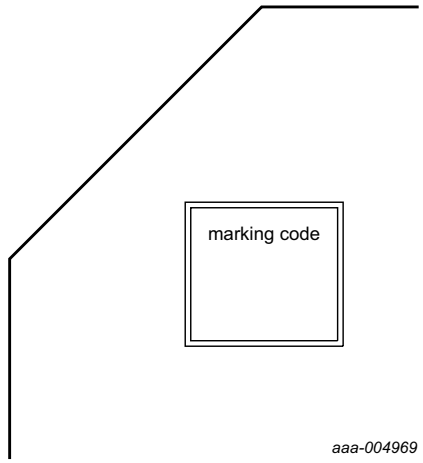


Fig 26. Tray alignment

17. Abbreviations

Table 27. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
HBM	Human Body Model
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed Circuit Board
RAM	Random Access Memory
RMS	Root Mean Square
SCL	Serial CLock line
SDA	Serial DAta line
SMD	Surface Mount Device

18. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10365 —** Surface mount reflow soldering description

[3] **AN10706 —** Handling bare die

[4] **AN10853 —** ESD and EMC sensitivity of IC

[5] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[6] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[7] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[8] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[9] **JESD78 —** IC Latch-Up Test

[10] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[11] **UM10204 —** I^2C-bus specification and user manual

[12] **UM10569 —** Store and transport requirements

19. Revision history

Table 28. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8576E v.1	20130122	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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22. Tables

23. Figures