PD69108/F

8 PORTS PSE POE MANAGER

DATASHEET

DESCRIPTION

Microsemi's PD69108 Power over Ethernet (PoE) Manager integrates power, analog and state of the art logic into a single 48 pin, plastic QFN package. The device is used in Ethernet switches and Midspans, enabling network devices to share power and data over the same cable.

The PD69108 device is an 8 ports, mixed-signal, high-voltage PoE driver. It enables detection of IEEE802.3at-2009 compliant Type 1 and Type 2 PDs (Powered Devices), ensuring safe power feeding and disconnection of ports with full digital control and a minimum of external components.

The PD69108 executes all real time functions as specified in the IEEE802.3af-2003 ("AF") and IEEE802.3at-2009 High Power ("AT") standards, including load detection and "AF" and "AT" classification. In addition, the PD69108 features Multiple Classification Attempts (MCA) port status monitoring, and provides system level activities such as power management and MIB support for system management.

The PoE device is designed to detect and disable disconnected ports utilizing DC disconnection methods, as specified in the IEEE 802.3af-2003 and IEEE802.3at-2009 standards.

The unit provides PD protection such as over-load, under-load, over-voltage and short-circuiting. It supports supply voltages ranging from 44 to 57 VDC with no need for additional power supply sources. The chip includes built-in internal thermal protection.

Optionally, the PD69108 can detect legacy/pre-standard PD devices.

The PD69108 is a low power device using an internal MOSFET and an external 0.36 Ω sense resistor.

KEY FEATURES

- IEEE802.3af-2003 compliant
- IEEE802.3at-2009 compliant, including two-event classification
- Supports pre-standard PD detection
- Supports Cisco devices detection
- Single DC voltage input (44 to 57 VDC)
- Input voltage out of range protection
- Wide temperature range: -10°C to +85°C
- PD69108F version covering -40°C to +85°C
- Over-temperature protection
- Low power dissipation (0.36 Ω sense resistor and 0.3Ω MOSFET Rdson)
- Includes Reset command pin
- 4 x direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- Configurable AT/AF modes
- Configurable standard and legacy detection mode
- Power soft start mechanism
- On-chip thermal protection
- Voltage monitoring/protection
- Built in 3.3 VDC and 5 VDC regulators
- Internal power on reset
- RoHS compliant
- Emergency power management supporting four configurable power bank I/Os
- Can be cascaded to up to 12 PoE devices (96 ports)

IMPORTANT: For the most current data, consult MICROSEMI's website: http://www.microsemi.com

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PACKAGE ORDER INFO		THERMAL DATA
T_A (°C)	Plastic 48 pin QFN 8 mm x 8 mm	TYPICAL THERMAL RESISTANCE-JUNCTION TO AMBIENT 25° C/W
	RoHS compliant / Pb-free/MSL1	TYPICAL THERMAL RESISTANCE-JUNCTION TO CASE 4° C/W
-10 to +85	**PD69108ILQ**	**Junction Temperature Calculation**: $T_J = T_A + (P_D \times \theta_{JA})$. The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.
-40 to +85	**PD69108FILQ**	
Note: Available in Tape and Reel. Append the letters "TR" to the part number.		

POWER DISSIPATION

Rsense Power Dissipation: 0.36 Ω x $Iport^2$
Rds_ON Power Dissipation: 0.3Ω x $Iport^2$

- Pport_AF = 15.4 W ==> PRsense = 28.2mW
  PRds_ON = 23.4mW
- Pport_AT = 30 W ==> PRsense = 107 mW
  PRds_ON = 88.5mW

** Calculated for Supply input Voltage of 55V

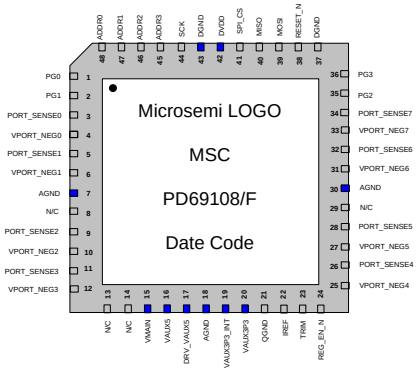
INTERNAL 3.3V VOLTAGE REGULATOR IS USED	EXTERNAL 3.3V VOLTAGE REGULATOR IS USED
PD69108 self power dissipation: 1.1 W	PD69108 self power dissipation: 0.5 W
PD69108 8 ports AF Application Power dissipation = 1.1 W + [8 x (28.2 mW + 23.4mW)] = 1.51W	PD69108 AF 8 ports Application Power dissipation = 0.5 W + [8 x (28.2mW + 23.4mW)] = 0.91W
PD69108 8 ports AT Application Power dissipation = 1.1 W + [8 x (107 mW + 88.5mW)] = 2.66W	PD69108 8 ports AT Application Power dissipation = 0.5 W + [8 x (107 mW + 88.5mW)] = 2.06W

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (V_{MAIN})	-0.3 to 74 VDC
Port_Neg[0..7] Pins	-0.3 to 74 VDC
Port_Sense[0..7] Pins	-0.3 to 3.6 VDC
QGND, GND Pins	-0.3 to 0.3 VDC
All Other Pins	-0.3 to 3.6 VDC
PD69108 Operating Ambient Temperature Range	-10° to +85° C
PD69108F Operating Ambient Temperature Range	-40° to +85° C
Maximum Operating Junction Temperature	+150° C
ESD Protection at all I/O Pins	± 2 KV HBM
Storage Temperature Range	-65° to +150° C

Notes:
Exceeding these ratings can cause damage to the device. All voltages are with respect to ground. Currents are marked positive when flowing into specified terminals and marked negative when flowing out of a specified terminal.

PACKAGE PIN OUT



(Top View)

RoHS / Pb-free 100% Matte Tin Finish

ROHS AND SOLDER REFLOW INFORMATION

RoHS 6/6
Pb-free 100% Matte Tin Finish
Package Peak Temperature for Solder Reflow 260°C (+0°C, -5°C)
(40 seconds maximum exposure)

Notes:
Exceeding these ratings can cause damage to the device.

IPC/JEDEC J-STD-020C July 2004

Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

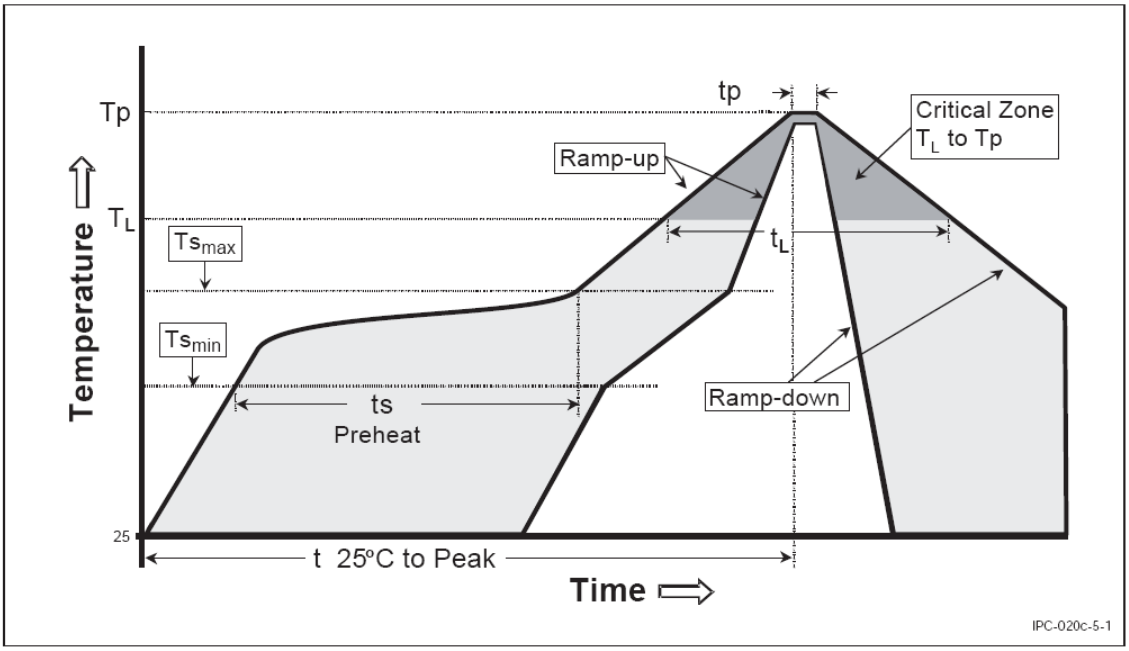


Figure 5-1 Classification Reflow Profile

Table 4-2 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 +0 °C *	260 +0 °C *	260 +0 °C *
1.6 mm - 2.5 mm	260 +0 °C *	250 +0 °C *	245 +0 °C *
≥2.5 mm	250 +0 °C *	245 +0 °C *	245 +0 °C *

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0 °C. For example 260 °C+0°C) at the rated MSL level.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply to the operating ambient temperature.

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	PD69108 POE MANAGER			UNITS
			MIN	TYP	MAX	
POWER SUPPLY						
Input Voltage	V_{MAIN}	Supports Full IEEE802.3 functionality	44	55	57	V
Power Supply Current @ Operating Mode		V_{MAIN} = 55 VDC			20	mA
5V Output Voltage	V_{AUX5}		4.5	5	5.5	V_{DC}
3.3V Output Voltage	V_{AUX3P3}		2.97	3.3	3.63	V_{DC}
3.3V Output Current		Without external NPN			5	mA
		With external NPN transistor on VAUX5			30	mA
3.3V Input Voltage	V_{AUX3P3}	REG_EN_N pin = 3.3V (internal reg. is disabled) VAUX3P3_INT=5V	3	3.3	3.6	V_{DC}
DIGITAL I/O (RESET_N, MISO, MOSI, SCK, CS, PG[0..3], ADD[0..3])						
Input Logic High Threshold	V_{IH}		2.2			V
Input Logic Low Threshold	V_{IL}				0.8	V
Input Hysteresis Voltage			0.4	0.6	0.8	V
Input High Current	I_{IH}		-10		10	uA
Input Low Current	I_{IL}		-10		10	uA
Output High Voltage	V_{OH}	For I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OH} = 1 mA			0.4	V
POE LOAD CURRENTS						
AF Limit Mode	AF_LIM		400	425	450	mA
AT Limit	AT_LIM		775	850	925	mA
AT Limit Dynamic Range	Configurable by communication	R_{SENSE} = 0.36 Ω 1% connected at Port_Sense pin	540		1200	mA
MAIN POWER SWITCHING FET						
On Resistance	R_{DSON}			0.3		Ω
Internal Thermal Protection Threshold				200		°C

Dynamic Characteristics

The PD69108 utilizes three current level thresholds (I_{min}, I_{cut}, I_{lim}) and three timers (T_{min}, T_{cut}, T_{lim}).

- Loads that consume I_{lim} current for more than T_{lim} are classified as being in 'short circuit state' and are shutdown.
- Loads that dissipate more than I_{cut} for longer than T_{cut} are classified as 'overloads' and are automatically shutdown.
- If output power is below I_{min} for more than T_{min}, the PD is classified as 'no-load' and is shutdown.

Automatic recovery from over-load condition is attempted every T_{OVLREC} periods (typically 1 second). Output power is limited to $I_{lim,}$ which is a maximum peak current allowed at the port.

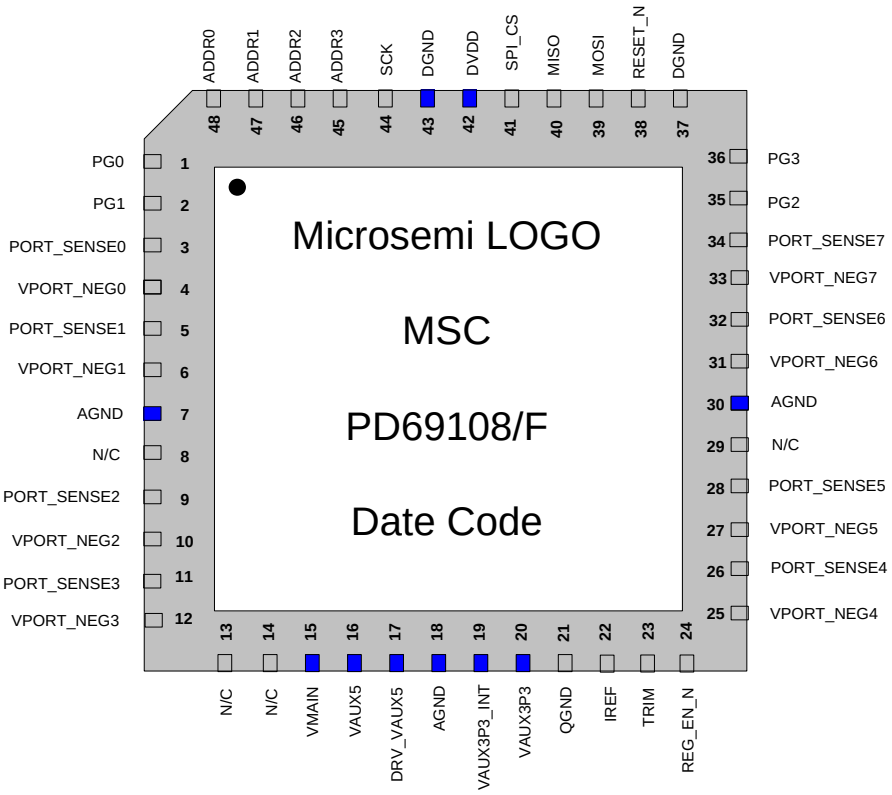
IEEE802.3 AF Mode Parameters

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic recovery from no-load shutdown	T_{UDLREC} value, measured from port shutdown point (can be modified through control port)			1		Sec
Cutoff timers accuracy	Typical accuracy of T_{cut}			2		ms
Inrush current	I_{Inrsh}	For t = 50 ms, C_{load}= 180 uF max.	400		450	mA
Output current operating range	I_{port}	Continuous operation after startup period.	10		350	mA
Output power available operating range	P_{port}	Continuous operation after startup period, at port output.	0.57		15.4	W
Off mode current	I_{min1}	Must disconnect for T greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect where T is greater than T_{UVL}	5	7.5	10	mA
PD power maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Over-load current detection range	I_{cut}	Time limited to T_{OVL}	350		400	mA
Over load time limit	T_{OVL}		50		75	ms
Turn on rise time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100 uF capacitor in parallel to 200 Ω).	15			us
Turn off time	T_{off}	From V_{port} to 2.8 VDC			500	ms
Time maintain power signature	T_{MPS}	DC modulation time for DC disconnect		49		ms

IEEE802.3 AT Mode Parameters

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic recovery from no-load shutdown	T_{UDLREC} value, measured from port shutdown point (can be modified through control port)			1		s
Cutoff timers accuracy	Typical accuracy of T_{cut}			2		ms
Inrush current	I_{Inrsh}	For t = 50 ms, Cload = 180 uF max.	400		450	mA
Output current operating range	I_{port}	Continuous operation after startup period	10		600	mA
Output power available, operating range	P_{port}	Continuous operation after startup period at port output	0.57		36	W
Off mode current	I_{min1}	Must disconnect where T is greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect where T is greater than T_{UVL}	5	7.5	10	mA
PD power maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Over-load current detection range	I_{cut}	Time limited to T_{OVL}	600		775	mA
Over-load time limit	T_{OVL}		50		75	ms
Turn on rise time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100 uF capacitor in parallel to 200 Ω).	15			us
Turn off time	Toff	From V_{port} to 2.8 VDC			500	ms
Time maintain power signature	TMPS	DC modulation time for DC disconnect		49		ms

Package Pinout



PD69108 for -10° to +85°C Operating Ambient Temperature Range
PD69108F for -40° to +85°C Operating Ambient Temperature Range

Detailed Pinout Description

PIN	PIN NAME	PIN TYPE	DESCRIPTION
0	Exposed PAD	Analog Gnd	Exposed PAD: Metal plate on the IC bottom side connected to analog ground. A decent ground plane (about 500 mil inch over 500 mil inch) should be deployed around this pin whenever possible
1	PG0	Digital Input	Power supply monitoring
2	PG1	Digital Input	Power supply monitoring
3	PORT_SENSE0	Analog Input	Sense resistor port input (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
4	VPORT_NEG0	Analog I/O	Negative port output
5	PORT_SENSE1	Analog Input	Sense resistor port input (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
6	VPORT_NEG1	Analog I/O	Negative port output

PIN	PIN NAME	PIN TYPE	DESCRIPTION
7	AGND	Power	Analog ground
8	N/C		Not Connected
9	PORT_SENSE2	Analog Input	Sense resistor port input (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
10	VPORT_NEG2	Analog I/O	Negative port output
11	PORT_SENSE3	Analog Input	Sense resistor port input (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
12	VPORT_NEG3	Analog I/O	Negative port output
13	N/C	Analog I/O	Test pin for production use only Keep open, not connected
14	N/C	Analog I/O	
15	VMAIN	Power	Supplies voltage for the internal analog circuitry. A low ESR 1 uF (or higher) bypass capacitor, connected to AGND should be placed as close as possible to this pin through low resistance traces.
16	VAUX5	Power	Regulated 5 VDC output voltage source; it needs to be connected to a filtering capacitor of 4.7 uF or higher. If an external NPN is used to regulate the voltage, connect this pin to the "Emitter" (the "collector" should be connected to Vmain)
17	DRV_VAUX5	Power	Driven outputs for 5 VDC external regulation; if internal regulation is used, connect to pin 16. If an external NPN is used to regulate the voltage, connect this pin to the "Base".
18	AGND	Power	Analog ground
19	VAUX3P3_INT	Power	Connected to VAX3P3 (pin 20) if internal 3.3 VDC regulator is used. Connect to VAUX5 (pin 16) if external 3.3 VDC regulator is used
20	VAUX3P3	Power	Regulated 3.3v output voltage source. A 4.7 µF or higher filtering capacitor should be connected between this pin and AGND. When an external 3.3 VDC regulator is used, connect it to this pin to supply the chip.
21	QGND	Power	Quiet analog ground.
22	IREF	Analog Input	Reference resistor pin. Connect a 30.1 kΩ 1% resistor to QGND.
23	TRIM	Analog Input	Trimming Input for IC production. Should be connected to VAUX3P3.
24	REG_EN_N	REG_EN_N	Enable/Disable the internal 3.3 VDC regulator in case an external 3.3 VDC is used to supply the chip. • GND: Internal regulator enabled • 3.3 VDC: Internal regulator disabled
25	VPORT_NEG4	Analog I/O	Negative port output.
26	PORT_SENSE4	Analog Input	Sense resistor port input (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
27	VPORT_NEG5	Analog I/O	Negative port output.
28	PORT_SENSE5	Analog Input	Sense resistor port input. (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
29	N/C		Not Connected
30	AGND	Power	Analog ground.
31	VPORT_NEG6	Analog I/O	Negative port output.

PIN	PIN NAME	PIN TYPE	DESCRIPTION
32	PORT_SENSE6	Analog Input	Sense resistor port input. (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
33	VPORT_NEG7	Analog I/O	Negative port output.
34	PORT_SENSE7	Analog Input	Sense resistor port input. (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
35	PG2	Digital Input	Power supply monitoring.
36	PG3	Digital Input	Power supply monitoring.
37	TST	Digital I/O	Test pin for production use only. Keep connected to DGND.
38	RESET_N	Digital Input	Reset input; active low ('0' = reset) An external 10K pull-up resistor should be connected between this pin and DVDD.
39	MOSI	Digital Input	SPI bus, Master Data out/slave in
40	MISO	Digital Output	SPI bus, Master Data in/slave out
41	SPI_CS	Digital Input	SPI bus, Chip Select
42	DVDD	Power	Digital 3.3 V input. It needs to be connected to filtering capacitor of 1 uF.
43	DGND	Digital I/O	Digital GND
44	SCK	Digital Input	SPI bus, Serial clock input
45	ADDR3	Digital Input	Address bus to set SPI address
46	ADDR2	Digital Input	Address bus to set SPI address
47	ADDR1	Digital Input	Address bus to set SPI address
48	ADDR0	Digital Input	Address bus to set SPI address

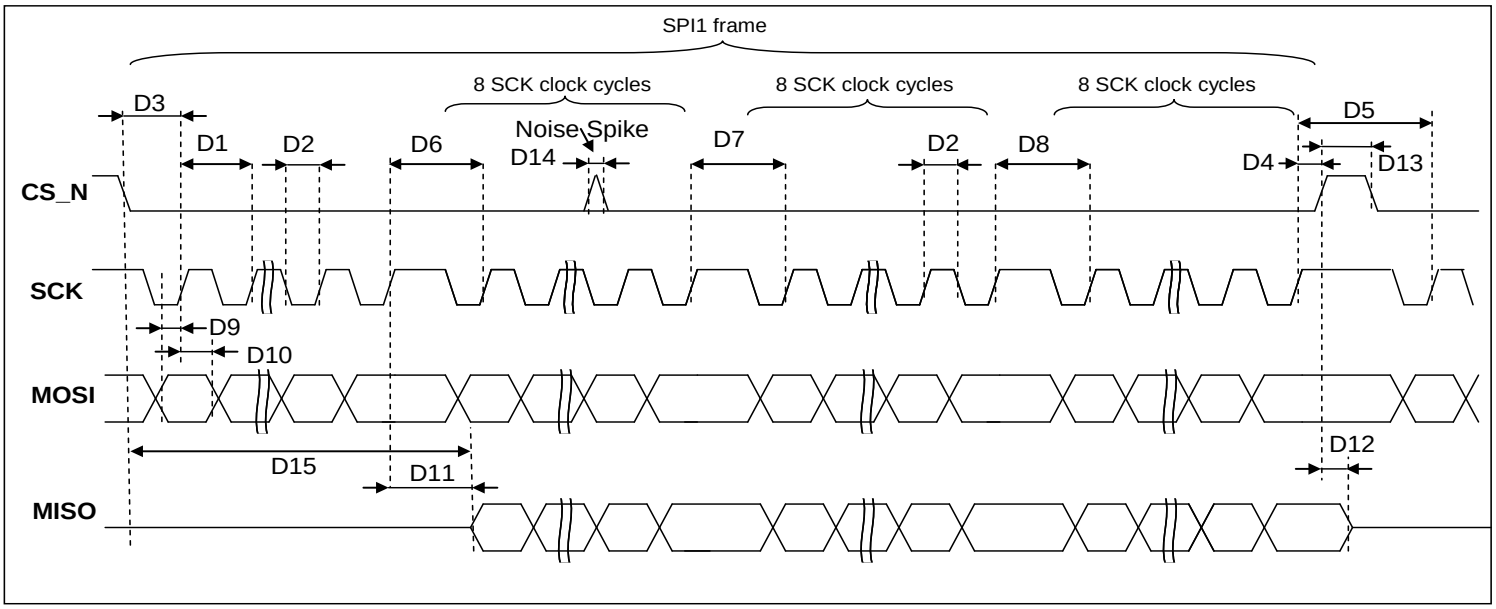
Address Pin Description (ADDR<3:0>)

ADDR3	ADDR2	ADDR1	ADDR0	SPI ADDRESS [HEX]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E – **Broadcast** (See note)
1	1	1	1	F

- '1' = DVDD (3.3 V)
- '0' = DGND (digital ground)

Note: This address is used for Broadcast. Do not set any PD69108s in the system to this address.

SPI Detailed Timing Information



Name	Min Delay	Max Delay	Description
D1		714ns	SPI clock period
D2	45	55	SPI duty cycle
D3	340 ns		SPI_CS setup to SPI clock Positive Edge (delay after SPI_CS active signal)
D4	340 ns		SPI_CS hold to SPI clock Positive Edge (delay before SPI_CS inactive Signal)
D5	2 spi clock cycles		Delay between last SCK in eSPI1 frame and first SCK at adjacent eSPI1 frame
D6	1 spi clock cycles		Between byte 0 (IC addr) and byte 1(addr)
D7	1 spi clock cycles		Between byte 1 (addr) and byte 2(data).
D8	1 SPI clock cycles		Between byte 2 (MS data byte) and byte 3(LS data byte).
D9	340 ns		MOSI setup time
D10	210 ns		MOSI hold time
D11		140ns	MISO tri-state to valid data from clock positive edge
D12		300ns	MISO valid data to tri-state from SPI_CS positive edge
D13	1 SPI clock cycles		SPI_CS width (Delay eSPI1 frame to adjacent eSPI1 frame)
D14		60ns	Filtered Glitch Width
D15	D3 + 15.5 SPI clock cycles	D3+23.75 SPI clock cycles	MISO tri-state from SPI_CS Negative Edge to valid data

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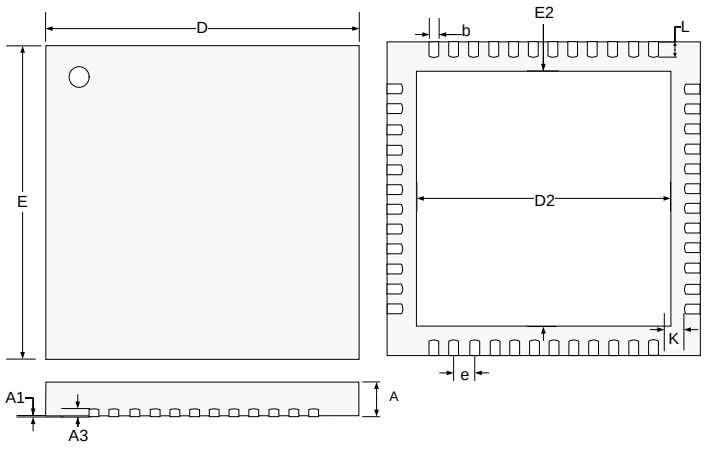
PACKAGE DESCRIPTION

48-Pin 8x8mm QFN



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.35	6.60	0.250	0.260
E2	6.35	6.60	0.250	0.260
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Note:
Dimensions do not include protrusions; these do not exceed 0.155 mm (.006") on any side. Lead dimension do not include solder coverage.

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PD69108 Internal Block Diagram

The PD69108 is based on two major sections:

- A Digital section which controls and monitors the logical PoE functions (state machines, timings etc.)
- An Analog section which performs the Front End analog PoE functionality.

Figure 1 illustrates both functions.

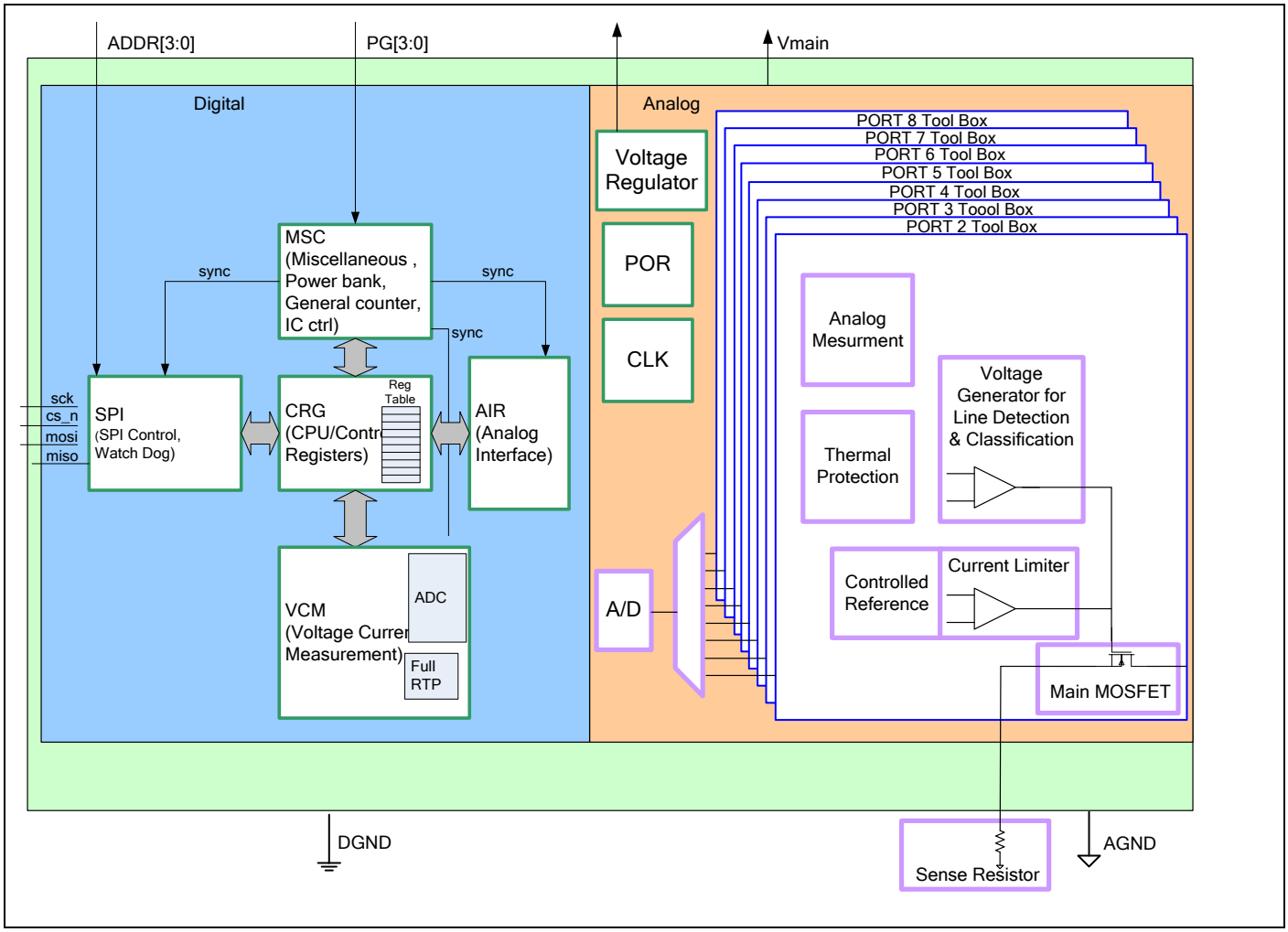


Figure 1: PD69108 Internal Block Diagram

Logic Main Control Module

The Logic Main Control Block includes the Digital Timing Mechanisms and State Machines synchronizing and activating PoE functions according to MCU control commands such as:

- Real Time Protection (RTP)
- Start Up Macro (DVDT)
- Load Signature Detection (RES DET)
- Classification Macro (CLASS)
- Voltage and Current Monitoring Registers (VMC)
- ADC Interfacing
- Direct Digital Signals with Analog Block

Line Detection Generator

Upon request from the MCU to the Main Control Module, four different voltage levels are generated by the Line Detection Generator to ensure a robust AF / AT Line Detection functionality.

Classification Generator

Upon request from the MCU to the Main Control Module, the State Machine applies a regulated Class Event and Mark Event voltage to the ports, as required by the IEEE standard.

Current Limiter

This circuit continuously monitors the current of powered ports and limits the current to a specific value, according to pre-defined limits as set by AF/AT and Current_Set pins. In cases where the current exceeds this specific level, the system starts measuring the elapsed time. If this time period is greater than a preset threshold, the port is disconnected.

Main MOSFET

Main power switching FET, used to control PoE current into the load.

ADC

A 10-Bit Analog to Digital converter, used to convert analog signals into digital registers for the Logic Control module.

Power on Reset (POR)

Monitors the internal 3.3 V voltage DC levels; if this voltage drops below specific thresholds, a reset signal is generated and the PD69108 is reset.

Voltage Regulator

The voltage regulator generates 3.3 VDC and 5 VDC for the internal circuitry. These voltages are derived from the Vmain supply.

To use the internal voltage regulator connect:

- VAUX5 to DRV_VAUX5
- VAUX3P3 to VAUX3P3_INT
- REG_EN_N to AGND.

There are two options to reduce the PD69108 power dissipation by regulating the voltage outside the chip:

- Use an external NPN transistor to regulate the 5 VDC.
  In this setup, the configuration of the regulators pins should be:
  - DRV_VAUX5 is connected to the NPN BASE
  - VAUX5 is connected to the NPN EMITTER

  (Connect the **Collector** to VMAIN)
  - VAUX3P3 is connected to VAUX3P3_INT
  - REG_EN_N is connected to AGND
- Supply the PD69108 with an external 3.3 V voltage regulator.
  In this setup, the configuration of the regulators pins should be:
  - VAUX5 is connected to DRV_VAUX5
  - VAUX3P3_INT is connected to VAUX5
  - VAUX3P3 is connected to the external 3.3 V
  - REG_EN_N is connected to VAUX3P3

The above two options can be implemented simultaneously.

CLK

CLK is an internal 8 MHz clock oscillator.

Theory of Operation

The PD69108 performs IEEE802.3af and IEEE802.3at functionality as well as legacy (capacitor) and Cisco's PDs detection and additional protections such as short circuit and dV/dT protection upon startup.

Line Detection

The Line Detection feature detects a valid AF or AT load, as specified in the AF / AT standard. The resistor value should go from 19 kΩ to 26.5 kΩ. Line detection is based on four different voltage levels generated over the PD (the load) as illustrated in Figure 2.

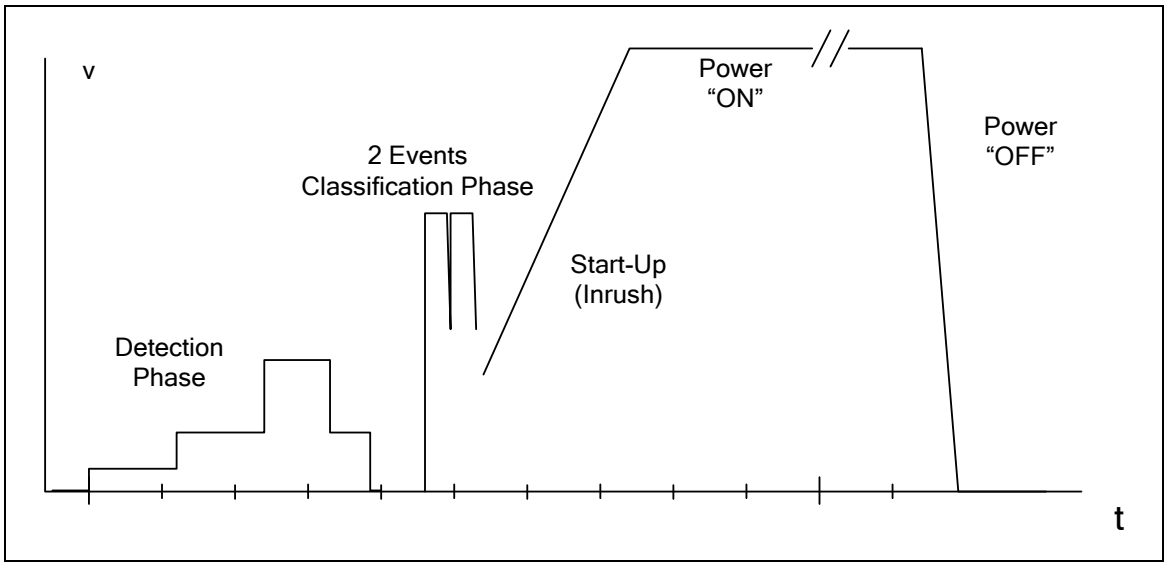


Figure 2: Typical PoE Voltage Time Diagram

Legacy (Cap) Detection

In cases where **legacy** is set, the PD69108's Detection mechanism detects and powers up legacy PDs as well as AF/AT compliant PDs.

This mechanism is designed to detect and power up CISCO legacy PDs as well.

Classification

The classification process takes place immediately after resistor detection has successfully completed. The goal of the classification process is to detect PD class, as specified in the IEEE802.3AF and AT standards.

In the AF mode, classification mechanism is based on a single voltage level (single finger).

In the AT mode, classification mechanism is based on two voltage levels (dual finger) as defined in IEEE802.3at-2009.

Port Start Up

Upon a successful detection and classification process, power is applied to the load via a controlled Start Up mechanism.

During this period current is limited to 425 mA for a typical duration of 65 mS, which allows the PD load to charge and allow steady state power condition.

Over-Load Detection and Port Shut Down

After power up, the PD69108 automatically initializes its internal protection mechanisms utilized to monitor and disconnect power from the load in cases where extreme conditions such as over-current or short ports terminals scenario occur, as specified in the IEEE802.3AF/AT standard.

Disconnect Detection

The PD69108 supports DC Disconnect Function as per the IEEE802.3AF/AT standard.

This mechanism continuously monitors load current and disconnects power in cases where load current is below 7.5 mA (typical) for more than 322 mS.

Over-Temperature Protection

The PD69108 has internal temperature sensors that continuously monitor the main MOSFET junction temperature and disconnect load power in cases where

junction temperature exceeds 200° C. This mechanism protects the device from extreme events, such as high ambient temperature or other thermo-mechanical failures that could damage the PD69108.

V_{MAIN} Out of Range Protection

The PD69108 automatically disconnects port power in cases where Vmain exceeds 60 VDC. This valuable mechanism protects the load in cases where main power source is faulty or damaged.

TYPICAL APPLICATION

This typical application illustrates a simple Power Over Ethernet system Solution for an 8 Ethernet Ports Switch or Hub.

"POS" and "NEG" Signals should be connected to the Switch RJ45 Jack

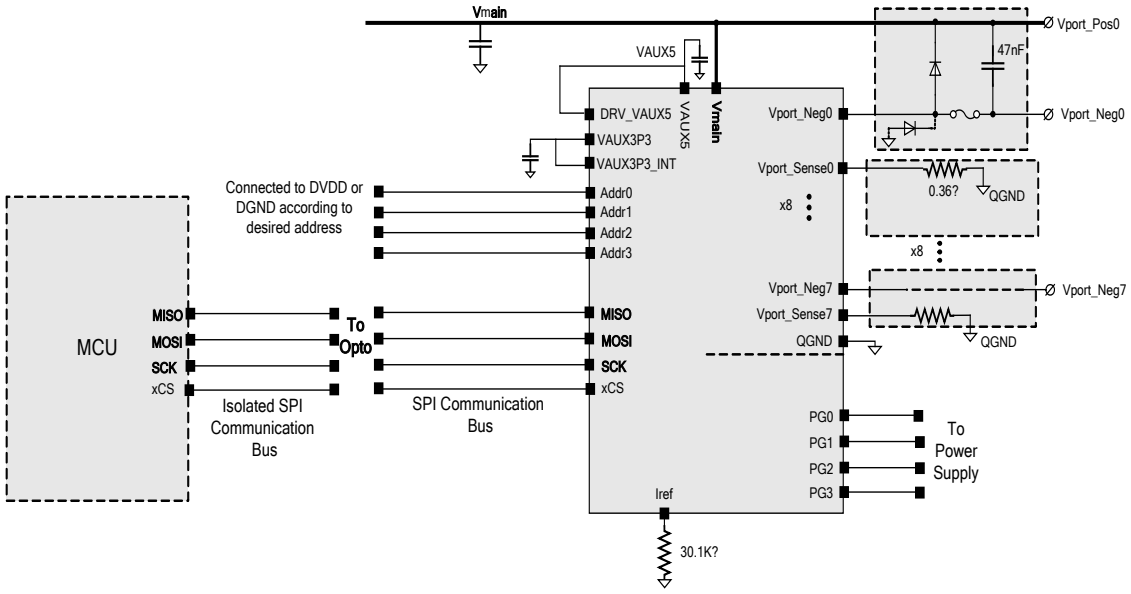
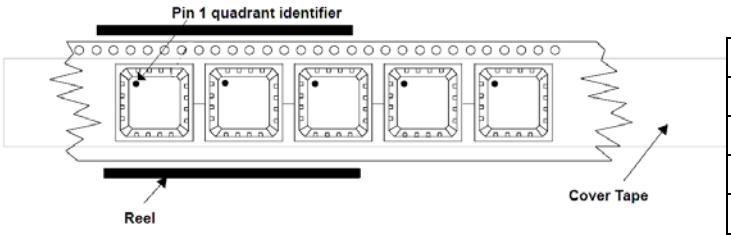


Figure 3: Typical Application

* For detailed application's schematics and layout recommendations, contact: sales_AMSG@microsemi.com

Tape and Reel – Packaging Information

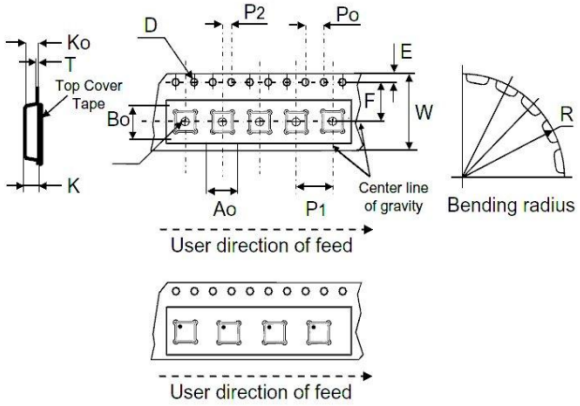


Pin-1 Orientation of QFN Packages

REEL MECHANICAL DATA		
	mm.	inch
Tape size	16.00 ±0.3	0.630 ±0.012
A max.	330	13”
B max.	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D min.	20.2	0.795
N min.	50	1.968
G	16.4+2.0/-0.0	0.645+0.079/-0.0
T max.	29	1.142
BASE QUANTITY	2000 pcs.	

TAPE & REEL SHIPMENT INFORMATION

TAPE SPECIFICATIONS



TAPE & REEL SHIPMENT INFORMATION

REEL SPECIFICATIONS