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Kind regards,

Team Nexperia

PNP resistor-equipped transistors; R1 = 2.2 k Ω , R2 = open

Rev. 02 — 3 September 2009

Product data sheet

1. Product profile

1.1 General description

PNP Resistor-Equipped Transistors (RET) family.

Table 1.Product overview

Type number	Package	NPN complement		
	NXP	JEITA	JEDEC	
PDTA123TE	SOT416	SC-75	-	PDTC123TE
PDTA123TK	SOT346	SC-59A	TO-236	PDTC123TK
PDTA123TM	SOT883	SC-101	-	PDTC123TM
PDTA123TS ^[1]	SOT54	SC-43A	TO-92	PDTC123TS
PDTA123TT	SOT23	-	TO-236AB	PDTC123TT
PDTA123TU	SOT323	SC-70	-	PDTC123TU

[1] Also available in SOT54A and SOT54 variant packages (see Section 2)

1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- 100 mA output current capability

1.3 Applications

- Digital applications
- Controlling IC inputs

1.4 Quick reference data

Table 2. Quick reference data

	Reduces	component	count
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- Reduces pick and place costs
- Cost-saving alternative for BC857 series in digital applications
- Switching loads

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	-50	V
lo	output current		-	-	-100	mA
R1	bias resistor 1 (input)		1.54	2.2	2.86	kΩ



PNP resistor-equipped transistors; R1 = 2.2 kΩ, R2 = open

2. Pinning information

Pin	Description	Simplified outline	Symbol
SOT54			
1	input (base)		
2	output (collector)		
3	GND (emitter)	001aab347	1 R1
SOT54A			
1	input (base)		
2	output (collector)		
3	GND (emitter)	001aab348	1 R1 006aaa217
SOT54 va	ariant		
1	input (base)		
2	output (collector)		
3	GND (emitter)	Cm Cm Cm Cm Cm Cm Cm Cm Cm Cm Cm Cm Cm C	1 R1 006aaa217
SOT23; S	OT323; SOT346; SOT416		
1	input (base)		
2	GND (emitter)	3	
3	output (collector)	1 2 006aaa144	1 R1 Sym009
SOT883			
1	input (base)		
2	GND (emitter)		
3	output (collector)	2 Transparent top view	

PDTA123T_SER_2
Product data sheet

PNP resistor-equipped transistors; R1 = 2.2 kΩ, R2 = open

3. Ordering information

Table 4. Ordering information						
Type number	Package	Package				
	Name	Description	Version			
PDTA123TE	SC-75	plastic surface mounted package; 3 leads	SOT416			
PDTA123TK	SC-59A	plastic surface mounted package; 3 leads	SOT346			
PDTA123TM	SC-101	leadless ultra small plastic package; 3 solder lands; body $1.0\times0.6\times0.5$ mm	SOT883			
PDTA123TS ^[1]	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54			
PDTA123TT	-	plastic surface mounted package; 3 leads	SOT23			
PDTA123TU	SC-70	plastic surface mounted package; 3 leads	SOT323			

[1] Also available in SOT54A and SOT54 variant packages (see Section 2 and Section 9)

4. Marking

Type numberMarking code[1]PDTA123TE2APDTA123TKGAPDTA123TMFAPDTA123TSTA123T	
PDTA123TK GA PDTA123TM FA	
PDTA123TM FA	
PDTA123TS TA123T	
PDTA123TT ZL*	
PDTA123TU *1S	

[1] * = -: made in Hong Kong

* = p: made in Hong Kong

* = t: made in Malaysia

* = W: made in China

PNP resistor-equipped transistors; $R1 = 2.2 \text{ k}\Omega$, R2 = open

5. Limiting values

Table 6. In accordar	Limiting values nce with the Absolute Maximu	um Rating System	(IEC 60134	<i>ı</i>).	
Symbol	Parameter	Conditions	Mir	n Max	Unit
V _{CBO}	collector-base voltage	open emitter	-	-50	V
V _{CEO}	collector-emitter voltage	open base	-	-50	V
V _{EBO}	emitter-base voltage	open collector	-	-5	V
lo	output current		-	-100	mA
I _{CM}	peak collector current	single pulse; $t_p \leq 1 \text{ ms}$	-	-100	mA
P _{tot}	total power dissipation	$T_{amb} \le 25 \ ^{\circ}C$			
	SOT416		<u>[1]</u> _	150	mW
	SOT346		<u>[1]</u> _	250	mW
	SOT883		[2][3]	250	mW
	SOT54		<u>[1]</u> _	500	mW
	SOT23		<u>[1]</u> -	250	mW
	SOT323		<u>[1]</u> _	200	mW
T _{stg}	storage temperature		-65	5 +150	°C
Tj	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	5 +150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

[3] Device mounted on an FR4 PCB with 60 µm copper strip line, standard footprint.

6. Thermal characteristics

Table 7.	Thermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air				
	SOT416		<u>[1]</u> _	-	833	K/W
	SOT346		<u>[1]</u> _	-	500	K/W
	SOT883		[2][3] _	-	500	K/W
	SOT54		<u>[1]</u> _	-	250	K/W
	SOT23		<u>[1]</u> _	-	500	K/W
	SOT323		<u>[1]</u> _	-	625	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

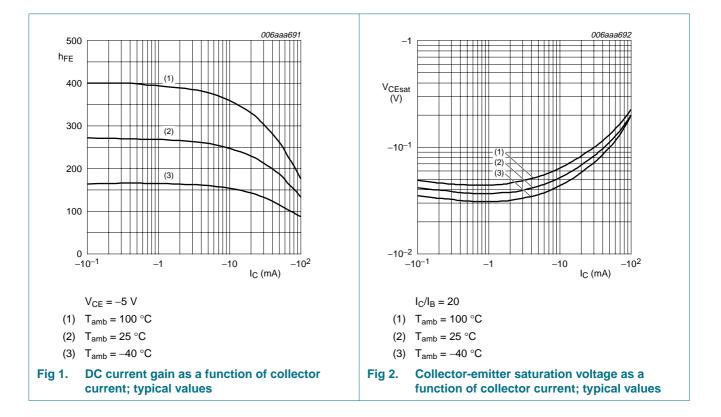
[2] Reflow soldering is the only recommended soldering method.

[3] Device mounted on an FR4 PCB with 60 μ m copper strip line, standard footprint.

PNP resistor-equipped transistors; R1 = 2.2 k Ω , R2 = open

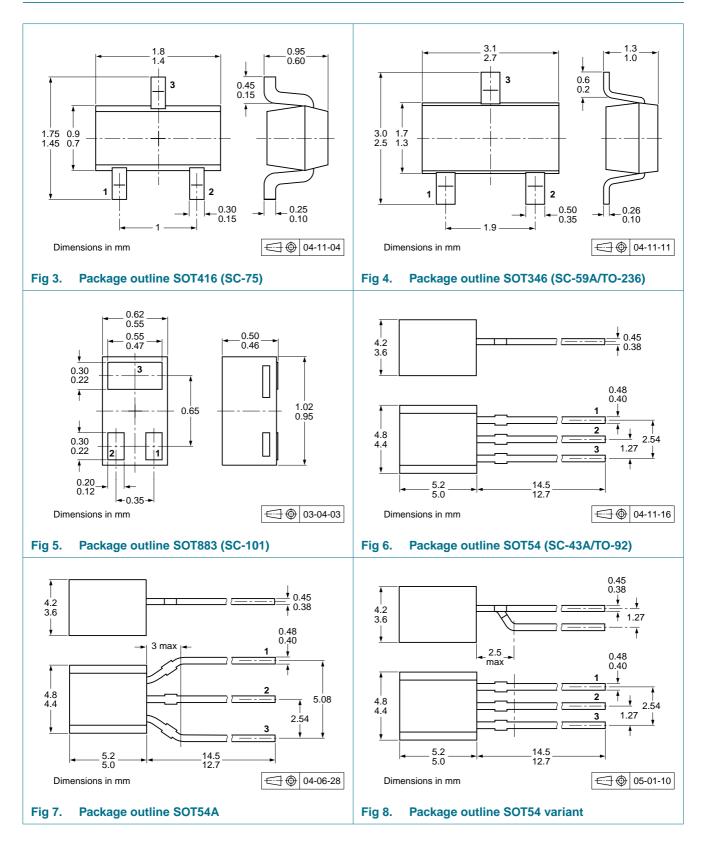
7. Characteristics

Characteristics °C unless otherwise spec	ified				
Parameter	Conditions	Min	Тур	Max	Unit
collector-base cut-off current	$V_{CB} = -50 \text{ V}; I_E = 0 \text{ A}$	-	-	-100	nA
collector-emitter cut-off	$V_{CE} = -30$ V; $I_B = 0$ A	-	-	-1	μΑ
current	$V_{CE} = -30 \text{ V}; \text{ I}_{B} = 0 \text{ A};$ T _j = 150 °C	-	-	-50	μA
emitter-base cut-off current	$V_{EB} = -5 \text{ V}; \text{ I}_{C} = 0 \text{ A}$	-	-	-100	nA
DC current gain	V_{CE} = -5 V; I_C = -20 mA	30	-	-	
collector-emitter saturation voltage	$I_{C} = -10$ mA; $I_{B} = -0.5$ mA	-	-	-150	mV
bias resistor 1 (input)		1.54	2.2	2.86	kΩ
collector capacitance	$V_{CB} = -10 \text{ V}; \text{ I}_{E} = \text{i}_{e} = 0 \text{ A};$ f = 1 MHz	-	-	3	pF
	 C unless otherwise spect Parameter collector-base cut-off current collector-emitter cut-off current emitter-base cut-off current DC current gain collector-emitter saturation voltage bias resistor 1 (input) 	$^{\circ}C$ unless otherwise specifiedParameterConditionscollector-base cut-off current $V_{CB} = -50 \text{ V}; I_E = 0 \text{ A}$ collector-emitter cut-off current $V_{CE} = -30 \text{ V}; I_B = 0 \text{ A}$ collector-emitter cut-off current $V_{CE} = -30 \text{ V}; I_B = 0 \text{ A};$ rj = 150 °C $V_{EB} = -5 \text{ V}; I_C = 0 \text{ A}$ emitter-base cut-off current $V_{CE} = -5 \text{ V}; I_C = 0 \text{ A}$ DC current gain $V_{CE} = -5 \text{ V}; I_C = -20 \text{ mA}$ collector-emitter saturation voltage $I_C = -10 \text{ mA}; I_B = -0.5 \text{ mA}$ bias resistor 1 (input) $V_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A};$	$^{\circ}C$ unless otherwise specifiedMinParameterConditionsMincollector-base cut-off current $V_{CB} = -50 \text{ V}; I_E = 0 \text{ A}$ -collector-emitter cut-off current $V_{CE} = -30 \text{ V}; I_B = 0 \text{ A}$ - $V_{CE} = -30 \text{ V}; I_B = 0 \text{ A};$ $T_j = 150 ^{\circ}\text{C}$ -emitter-base cut-off current $V_{EB} = -5 \text{ V}; I_C = 0 \text{ A};$ $T_j = 150 ^{\circ}\text{C}$ -DC current gain $V_{CE} = -5 \text{ V}; I_C = -20 \text{ mA}$ 30collector-emitter saturation voltageI_C = -10 \text{ mA}; I_B = -0.5 \text{ mA};-bias resistor 1 (input)1.54collector capacitance $V_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A};$ -	$^{\circ}C$ unless otherwise specifiedMinTypParameterConditionsMinTypcollector-base cut-off current $V_{CB} = -50 \text{ V}; I_E = 0 \text{ A}$ collector-emitter cut-off current $V_{CE} = -30 \text{ V}; I_B = 0 \text{ A}$ $V_{CE} = -30 \text{ V}; I_B = 0 \text{ A};$ $T_j = 150 ^{\circ}\text{C}$ emitter-base cut-off current $V_{EB} = -5 \text{ V}; I_C = 0 \text{ A};$ $T_j = 150 ^{\circ}\text{C}$ DC current gain $V_{CE} = -5 \text{ V}; I_C = -20 \text{ mA}$ 30-collector-emitter saturation voltage $I_C = -10 \text{ mA}; I_B = -0.5 \text{ mA}$ $I_C = -10 \text{ V}; I_E = i_e = 0 \text{ A};$ bias resistor 1 (input) $V_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A};$	°C unless otherwise specifiedParameterConditionsMinTypMaxcollector-base cut-off current $V_{CB} = -50 \text{ V}; I_E = 0 \text{ A}$ 100collector-emitter cut-off current $V_{CE} = -30 \text{ V}; I_B = 0 \text{ A}$ 1 $C_{CE} = -30 \text{ V}; I_B = 0 \text{ A};$ $T_j = 150 °C50emitter-base cut-offcurrentV_{EB} = -5 \text{ V}; I_C = 0 \text{ A}DC current gainV_{CE} = -5 \text{ V}; I_C = -20 \text{ mA}30DC current gainV_{CE} = -10 \text{ mA}; I_B = -0.5 \text{ mA}150bias resistor 1 (input)I_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A};3$

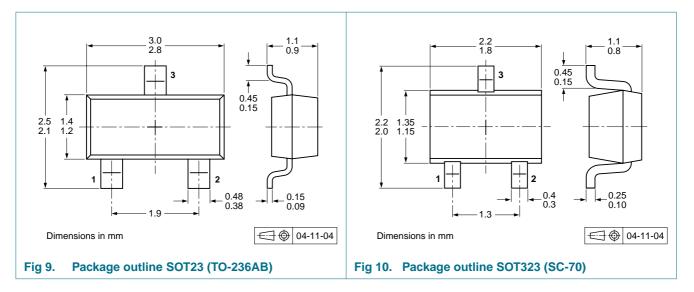


PNP resistor-equipped transistors; R1 = 2.2 k Ω , R2 = open

8. Package outline



PNP resistor-equipped transistors; R1 = 2.2 k Ω , R2 = open



9. Packing information

Table 9.Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packin	Packing quantity		
			3000	5000	10000	
PDTA123TE	SOT416	4 mm pitch, 8 mm tape and reel	-115	-	-135	
PDTA123TK	SOT346	4 mm pitch, 8 mm tape and reel	-115	-	-135	
PDTA123TM	SOT883	2 mm pitch, 8 mm tape and reel	-	-	-315	
PDTA123TS	SOT54	bulk, straight leads	-	-412	-	
	SOT54A	tape and reel, wide pitch	-	-	-116	
		tape ammopack, wide pitch	-	-	-126	
	SOT54 variant	bulk, delta pinning	-	-112	-	
PDTA123TT	SOT23	4 mm pitch, 8 mm tape and reel	-215		-235	
PDTA123TU	SOT323	4 mm pitch, 8 mm tape and reel	-115		-135	

[1] For further information and the availability of packing methods, see Section 12.

PNP resistor-equipped transistors; R1 = 2.2 kΩ, R2 = open

10. Revision history

Table 10. Revision hi	story			
Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTA123T_SER_2	20090903	Product data sheet	-	PDTA123T_SER_1
Modifications:		eet was changed to reflect w legal definitions and disc		
PDTA123T_SER_1	20060307	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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