

PDTC114ET

50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 10 k Ω

1 July 2022

Product data sheet

1. General description

NPN Resistor-Equipped Transistor (RET) in a small SOT23 Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA114ET

2. Features and benefits

- 100 mA output current capability
- · Built-in bias resistors
- · Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

3. Applications

- · Digital application in automotive and industrial segments
- Cost-saving alternative for BC847 series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{CEO}	collector-emitter voltage	open base		-	-	50	V
Io	output current			-	-	100	mA
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	

[1] See "Section 11: Test information" for resistor calculation and test conditions.



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)]3	
2	GND	ground (emitter)		R1
3	0	output (collector)	SOT23	GND R2

6. Ordering information

Table 3. Ordering information

Type number	Package						
	Name	Description	Version				
PDTC114ET	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23				

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PDTC114ET	%16

[1] % = placeholder for manufacturing site code

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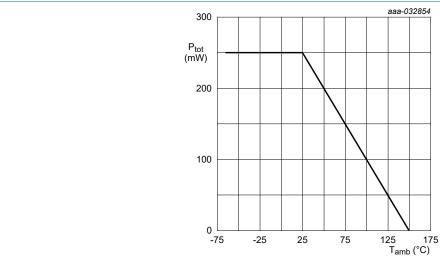
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
VI	input voltage	positive		-	40	V
		negative		-	-10	V
Io	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	250	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

Fig. 1. Power derating curve

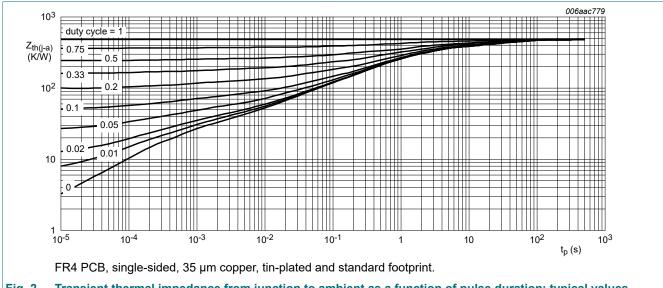
50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 10 k Ω

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.



Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

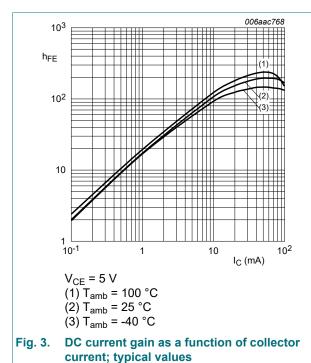
50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 10 k Ω

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{(BR)CBO}	collector-base breakdown voltage	I _C = 100 μA; I _E = 0 A; T _{amb} = 25 °C		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		50	-	-	V
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C		-	-	100	nA
I _{CEO}	collector-emitter cut-off	V _{CE} = 30 V; I _B = 0 A; T _{amb} = 25 °C		-	-	100	nA
	current	V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C		-	-	5	μΑ
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C		-	-	400	μΑ
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA; T _{amb} = 25 °C		30	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		-	-	100	mV
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA; T _{amb} = 25 °C		-	1.1	0.8	V
V _{I(on)}	on-state input voltage	V _{CE} = 0.3 V; I _C = 10 mA; T _{amb} = 25 °C		2.5	1.8	-	V
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C _c	collector capacitance	V_{CB} = 10 V; I_{E} = 0 A; i_{e} = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	2.5	pF
f _T	transition frequency	V_{CE} = 5 V; I_{C} = 10 mA; f = 100 MHz; T_{amb} = 25 °C	[2]	-	230	-	MHz

- [1] See "Section 11: Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor.



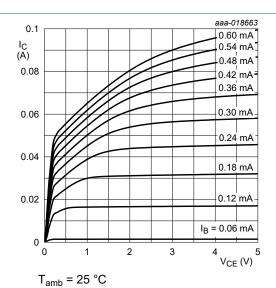
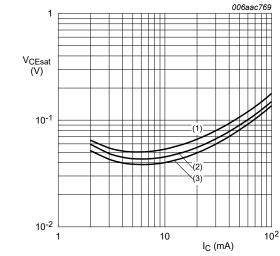


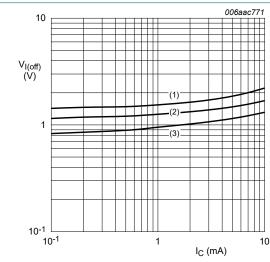
Fig. 4. Collector current as a function of collectoremitter voltage; typical values

50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 10 k Ω



I_C/I_B = 20 (1) T_{amb} = 100 °C (2) T_{amb} = 25 °C (3) T_{amb} = -40 °C

Fig. 5. Collector-emitter saturation voltage as a function of collector current; typical values



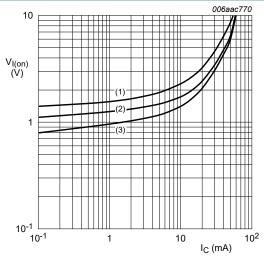
 $V_{CE} = 5 V$

(1) $T_{amb} = -40 \, ^{\circ}C$

(2) T_{amb} = 25 °C

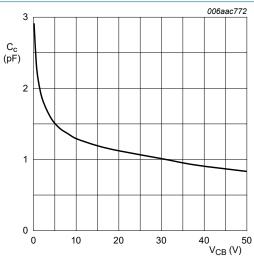
(3) $T_{amb} = 100 \, ^{\circ}C$

Fig. 7. Off-state input voltage as a function of collector current; typical values



V_{CE} = 0.3 V (1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C

Fig. 6. On-state input voltage as a function of collector current; typical values

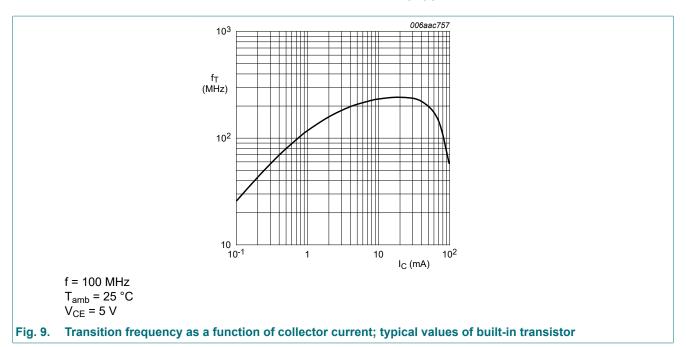


f = 1 MHz

T_{amb} = 25 °C

Fig. 8. Collector capacitance as a function of collectorbase voltage; typical values

50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 10 k Ω



50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 10 k Ω

11. Test information

Resistor calculation

• Calculation of bias resistor 1 (R1)

$$RI = \frac{V(I_{12}) - V(I_{11})}{I_{12} - I_{11}}$$

· Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$

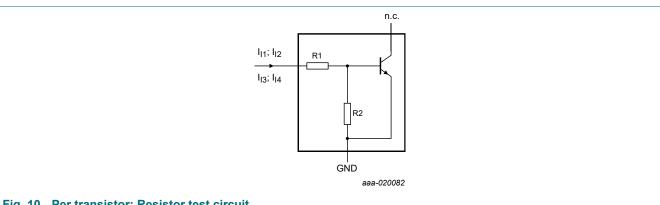


Fig. 10. Per transistor: Resistor test circuit

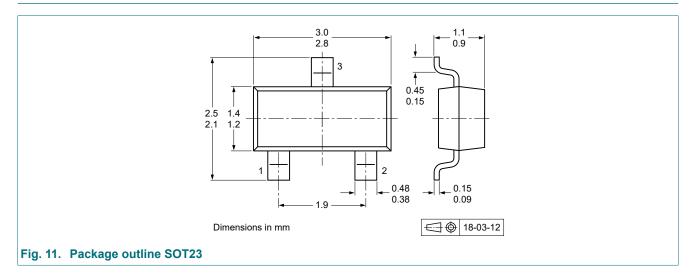
Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions				
			I ₁₁	I _{I2}	I ₁₃	I ₁₄	
PDTC114ET	10	10	350 μΑ	450 μΑ	-350 μA	-450 μA	

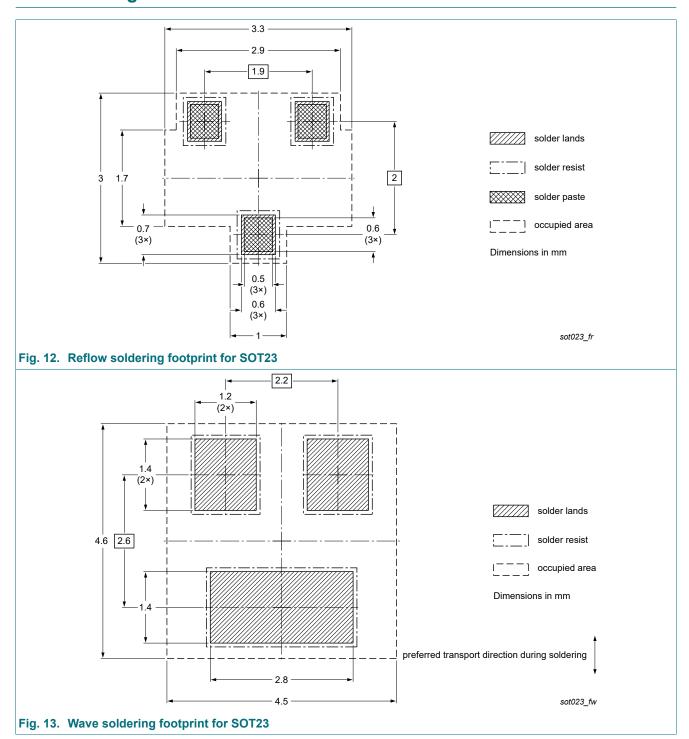
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12. Package outline



50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 10 k Ω

13. Soldering



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14. Revision history

Table 9. Revision history

Table 5. Revision history							
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PDTC114ET v.13	20220701	Product data sheet	-	PDTC114E_SER v.12			
Modification:	 Family data sheet reduced to single type data sheet. Product(s) changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s). Packing information removed. 						
PDTC114E_SER v.12	20111221	Product data sheet	-	PDTC114E_SER v.11			
PDTC114E_SER v.11	20111121	Product data sheet	-	PDTC114E_SERIES v.10			
PDTC114E_SERIES v.10	20040805	Product specification	-	PDTC114E_SERIES v.9			
PDTC114E_SERIES v.9	20030410	Product specification	-	-			

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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