PE35400

Document Category: Product Specification

UltraCMOS® Divide-by-4 Prescaler, 3–13.5 GHz

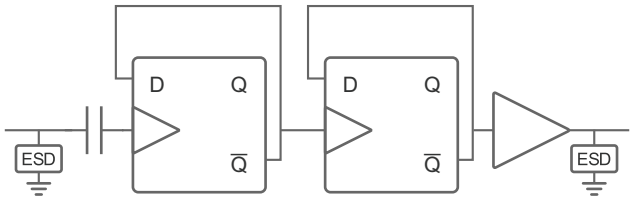
Features

- High frequency support up to 13.5 GHz
- Low SSB phase noise of –135 dBc/Hz @ 3.025 GHz output frequency
- Low supply current of 16 mA
- Bare die

Applications

- Wireless communication
- Test and measurement
- Phased array radar

Figure 1 • *PE35400 Functional Diagram*



Product Description

The PE35400 is a high-performance UltraCMOS® prescaler with a fixed divide ratio of 4. It supports an operating frequency range from 3–13.5 GHz. It operates on a single voltage supply with a frequency-selecting bias resistor and draws a low current of 16 mA. The PE35400 is available in bare die.

The PE35400 is manufactured on Peregrine's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE35400*

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	3.3	V
Input power, 50Ω		+14	dBm
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins(*)		250	V
Note: * Human body model (MIL-STD 883 Method 3015).			

Recommended Operating Conditions

Table 2 lists the recommending operating conditions for the PE35400. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Conditions for PE35400*

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	2.65	2.8	2.95	V
Input power, 50Ω, based on optimal R_{BIAS} (see **Figure 3**), P_{IN}			+7	dBm
Operating temperature range	–40		+85	°C

Electrical Specifications

Table 3 provides the PE35400 key electrical specifications @ +25 °C, V_{DD} = 2.8V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3 • *PE35400 Electrical Specifications*(*)

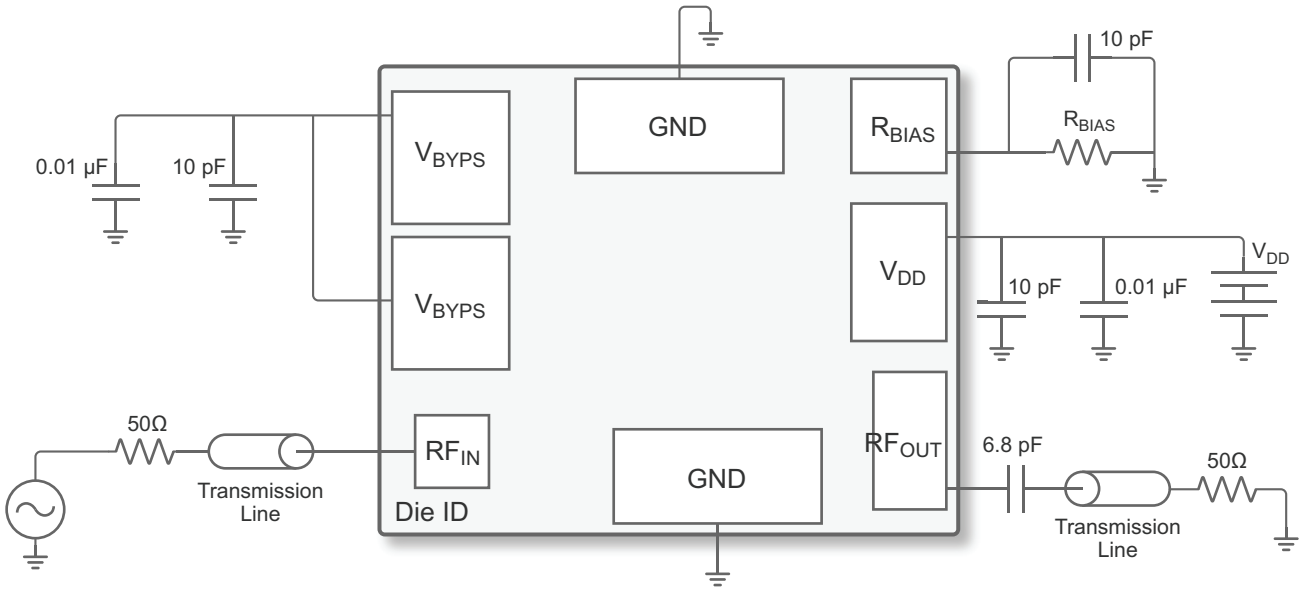
Parameter	Condition	Min	Typ	Max	Unit
Operating frequency, F_{IN}		3.0 GHz		13.5 GHz	As shown
Input power sensitivity	F_{IN} = 3–4.5 GHz	–5	> –7		dBm
	F_{IN} = >4.5–11.5 GHz	–15	> –20		dBm
	F_{IN} = >11.5–13.5 GHz	–1	> –7		dBm
Output power	0.75–3.375 GHz output frequency range	0	5		dBm
Reverse leakage	F_{IN} = 3–13.5 GHz, P_{IN} = 0 dBm		–45		dBm
SSB phase noise	3.025 GHz output frequency @ 100 kHz offset, P_{IN} = 0 dBm		–135		dBc/Hz
Supply current, I_{DD}	F_{IN} = 8 GHz		16		mA

Note: * All values in Min/Max columns are guaranteed by design characterization.

Device Functional Considerations

The PE35400 divides a 3.0–13.5 GHz input signal by four, producing a 750 MHz to 3.375 GHz output signal. In order for the prescaler to work properly, several conditions need to be adhered to. It is crucial that V_{BYPS} and V_{DD} are supplied with bypass capacitors to ground. In addition, the output signal RF_{OUT} needs to be AC coupled via an external capacitor, as shown in **Figure 2**. The input frequency range is selected by the value of R_{BIAS} according to **Figure 3**. The ground pattern on the board should be made as wide as possible to minimize ground impedance.

Figure 2 • ***Circuit Block Diagram for PE35400***(*)



Note: * For optimal performance, the following bond wire configuration is recommended. V_{BYPS}: 2 bond wires per pad. RF_{IN}: 1 bond wire. GND: 3 bond wires per pad. RF_{OUT}: 2 bond wires. V_{DD}: 2 bond wires. R_{BIAS}: 1 bond wire.

Typical Performance Data

Figure 3 through **Figure 11** show the typical performance data @ +25 °C, V_{DD} = 2.8V (Z_S = Z_L = 50Ω), based on optimal R_{BIAS} as shown in **Figure 3**, unless otherwise specified.

Figure 3 • *Frequency vs R_{BIAS}*

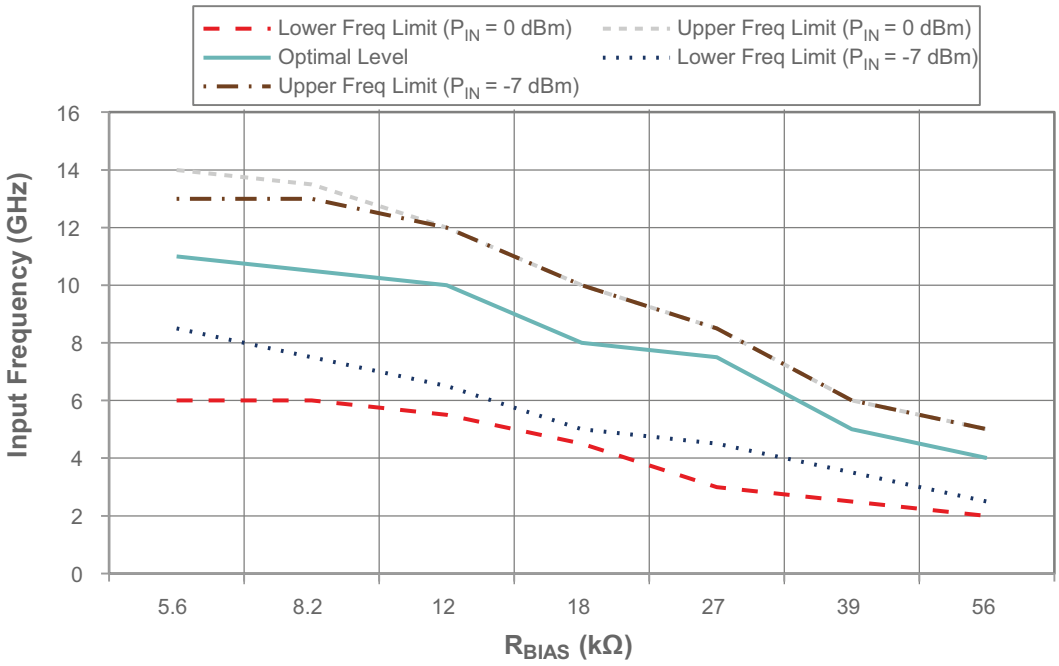


Figure 4 • *Input Power Sensitivity*

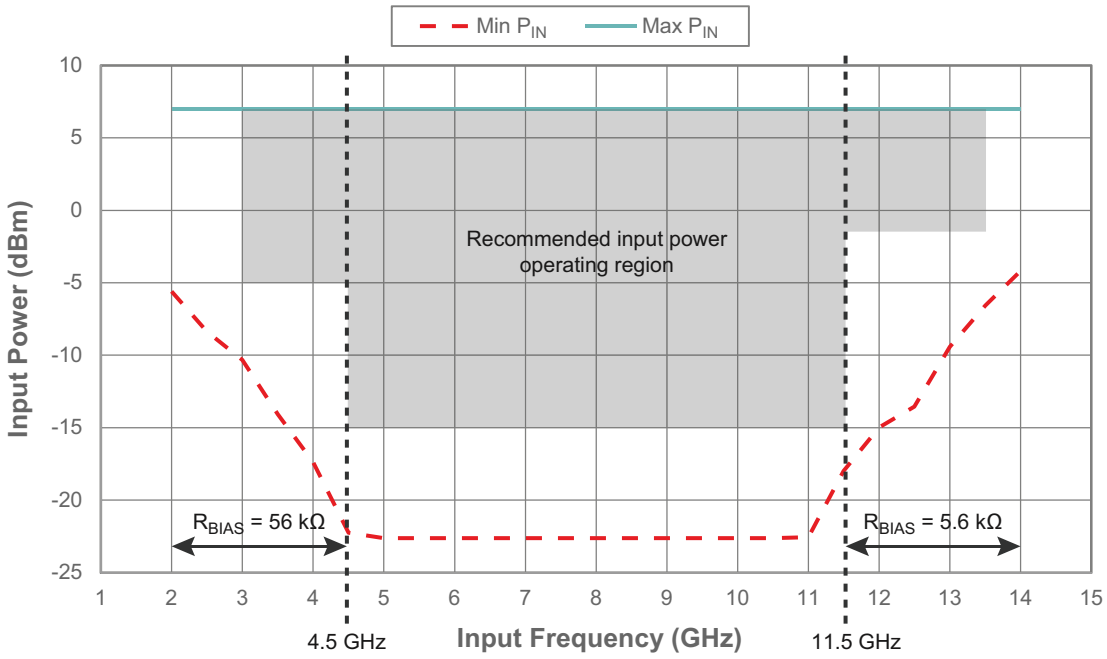


Figure 5 • *Input Power Sensitivity vs Temperature*

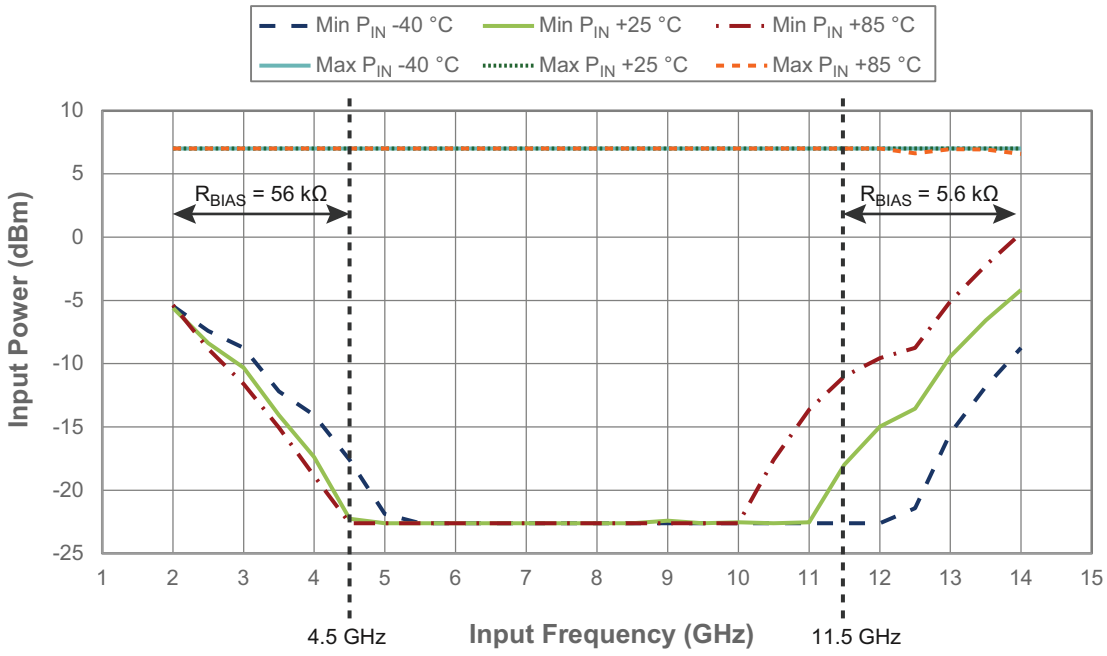


Figure 6 • *Output Power vs V_{DD}*

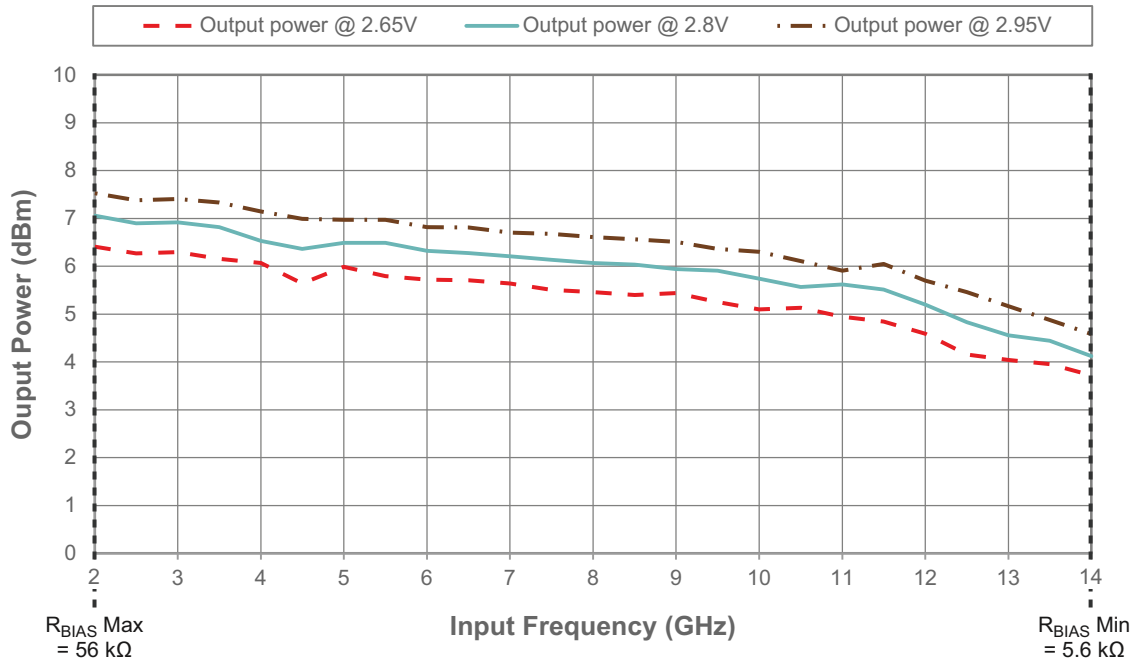


Figure 7 • *Output Power vs Temperature*

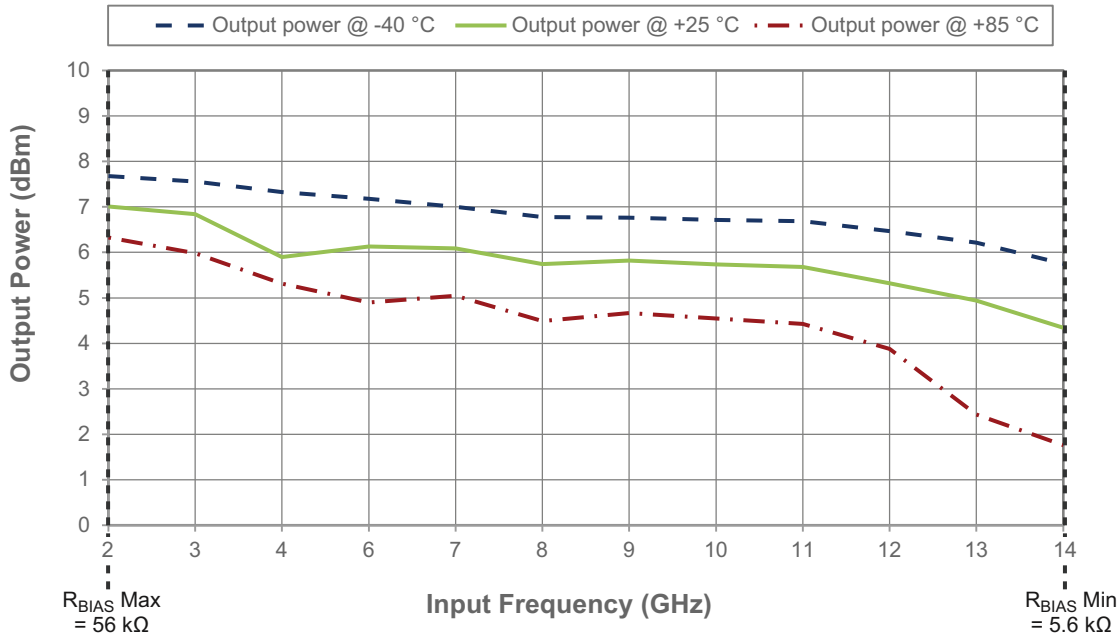


Figure 8 • *SSB Phase Noise @ 3.025 GHz Output Frequency, P_{IN} = 0 dBm*

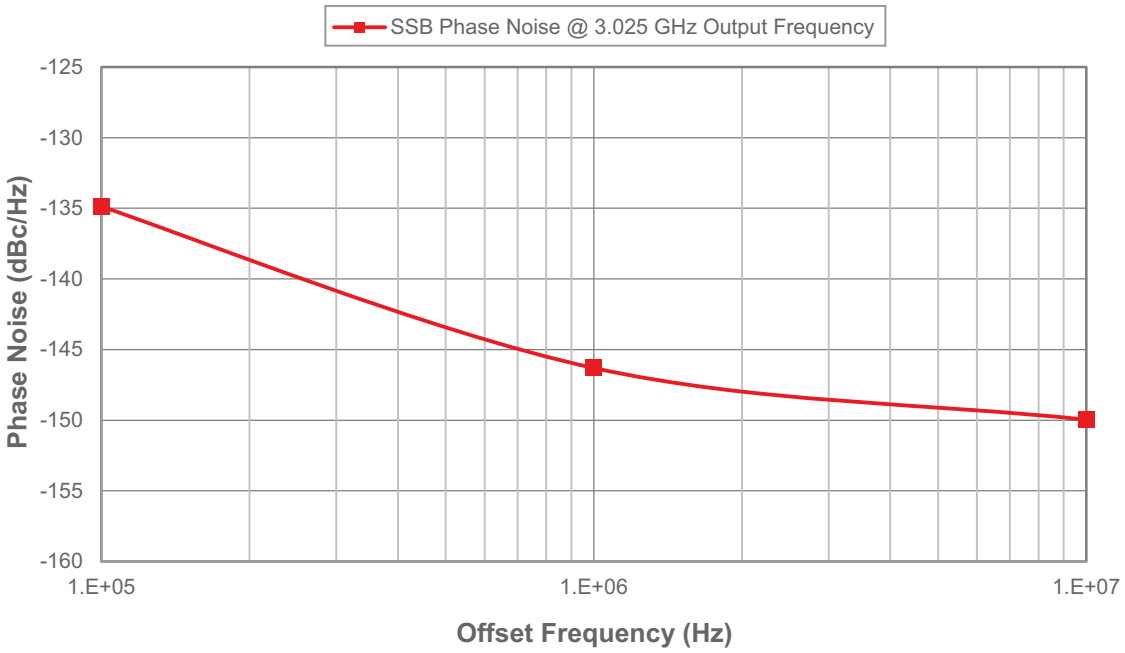


Figure 9 • *Output Harmonics, P_{IN} = 0 dBm*

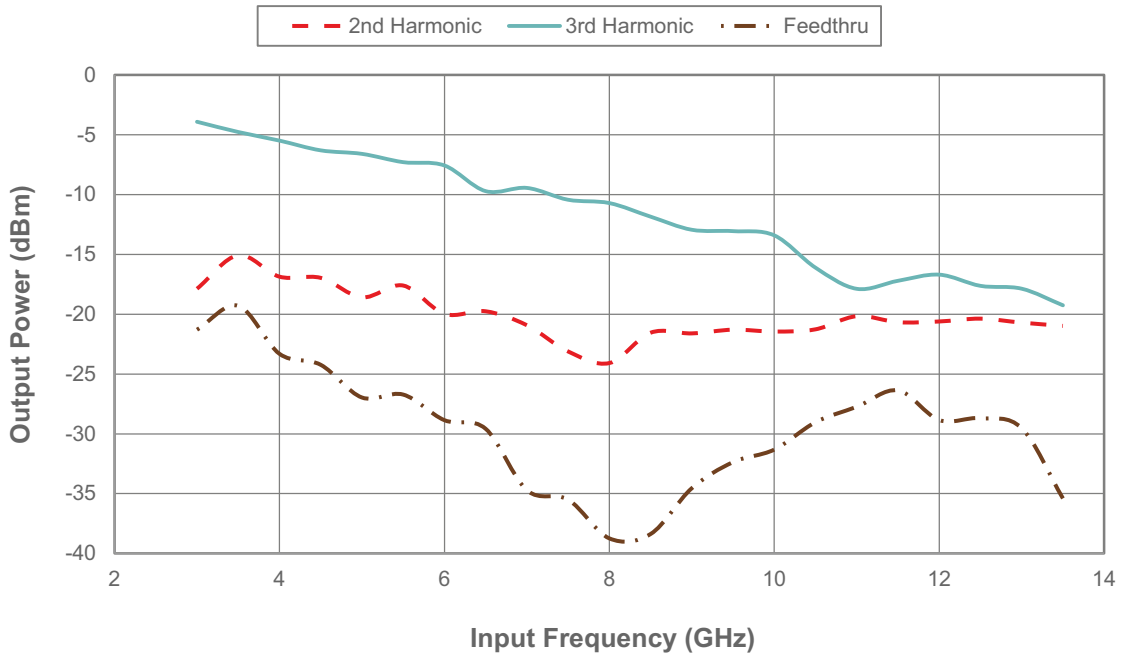


Figure 10 • I_{DD} vs R_{BIAS}

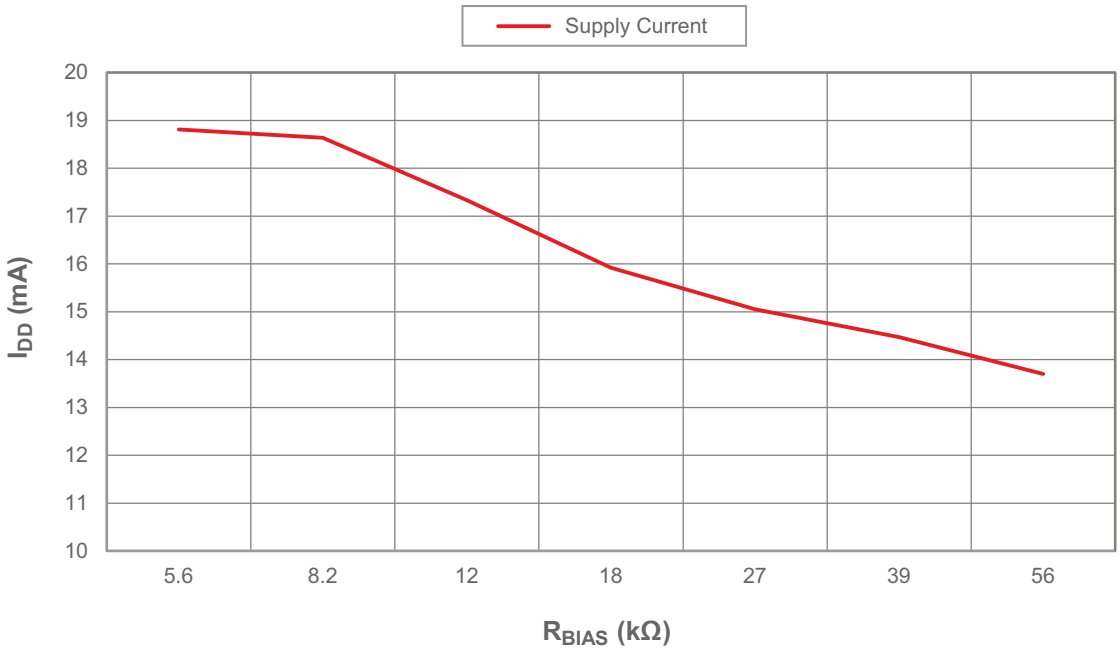
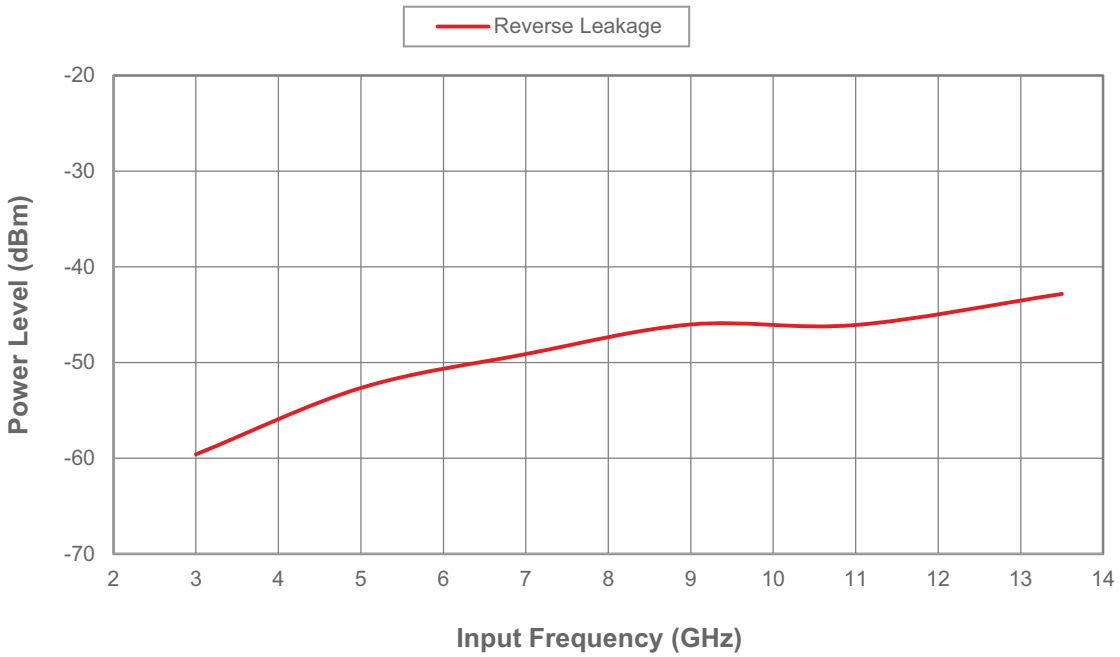


Figure 11 • *Reverse Leakage, P_{IN} = 0 dBm*



Pad Configuration

This section provides pad information for the PE35400. **Figure 12** shows the pad configuration of this device. **Table 4** provides a description for each pad.

Figure 12 • *Pad Configuration (Top View)*

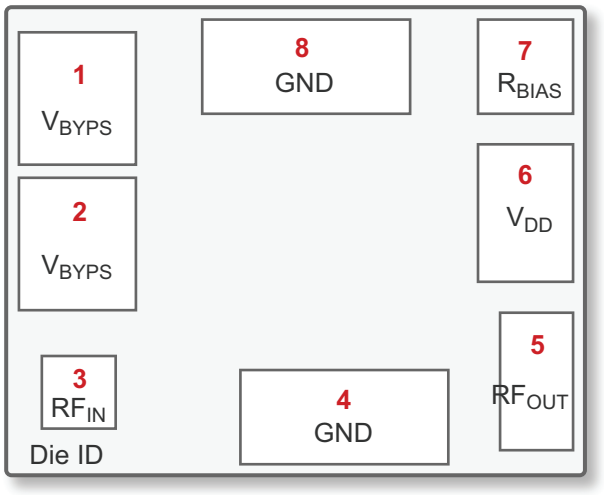


Table 4 • *Pad Descriptions for PE35400*

Pad No.	Pad Name	Description
1	V_{BYPS}	Prescaler supply bypass
2	V_{BYPS}	Prescaler supply bypass
3	RF_{IN}	RF input
4	GND	Ground
5	RF_{OUT}	RF output
6	V_{DD}	Supply voltage
7	R_{BIAS}	Frequency selecting bias resistor
8	GND	Ground

Die Mechanical Specifications

This section provides the die mechanical specifications for the PE35400.

Table 5 • *Mechanical Specifications for PE35400*

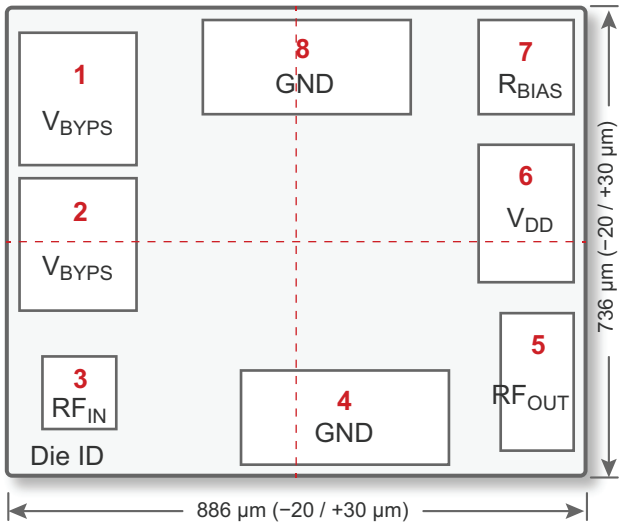
Parameter	Min	Typ	Max	Unit	Condition
Die size, singulated (x,y)	866 × 716	886 × 736	916 × 766	µm	Including excess sapphire, max tolerance = –20/+30 µm
Wafer thickness	180	200	220	µm	
Wafer size		150		mm	

Table 6 • *Pad Coordinates for PE35400*(*)

Pad No.	Pad Name	Pad Center (µm)		Pad Opening Size (µm)	
		X	Y	X	Y
1	V_{BYPS}	–303	198	160	180
2	V_{BPYS}	–303	–3	160	180
3	RF_{IN}	–303	–208	100	100
4	GND	68	–243	290	130
5	RF_{OUT}	333	–193	100	190
6	V_{DD}	318	40	130	190
7	R_{BIAS}	318	243	130	130
8	GND	14	243	290	130

Note: * All pad locations originate from the die center and refer to the center of the pad.

Figure 13 • *Pad Layout for PE35400*(1)(2)



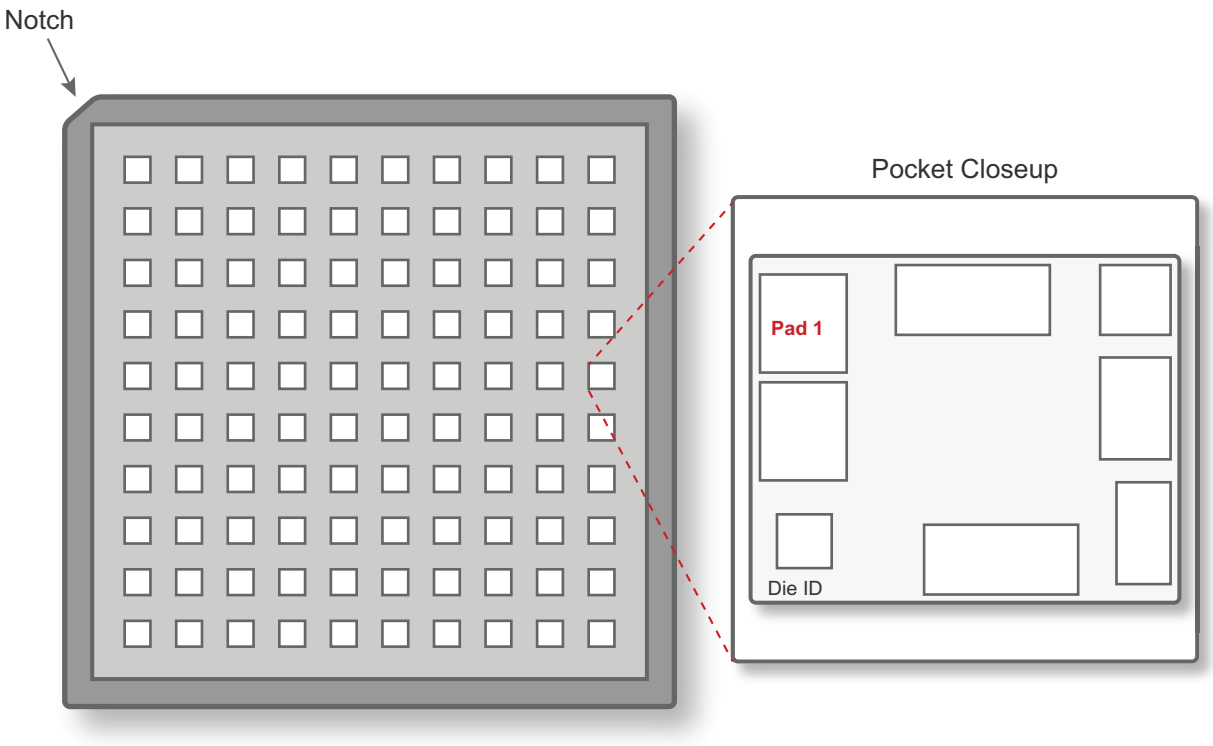
Notes:

1) Drawings are not drawn to scale.
2) Singulated die size shown, pad side up.

Waffle Pack Information

Figure 14 provides the waffle pack information for the PE35400.

Figure 14 • *2 × 2 Inch Waffle Pack for PE35400*[(1)(2)(3)]



Notes:

1) Drawings are not drawn to scale.
2) Die in pocket shown pad side up.
3) Die will be oriented in the same direction in and within all waffle packs. Unless otherwise stated, die will be oriented such that the top left corner of die will be in-line with the "notched" corner of the die plate base and corner. The die base cover label will be affixed on the die base cover such that the top of the label indicates the top of the die within the waffle pack.