Product Specification

PE42423

UltraCMOS® SPDT RF Switch
100 MHz - 6 GHz

Features

- 802.11 a/b/g/n/ac support
- Wide supply range of 2.3V to 5.5V
- +1.8V control logic compatible
- Exceptional isolation
  - 47 dB @ 2.4 GHz
  - 43 dB @ 6.0 GHz
- High linearity across supply range
  - IIP3 of 65 dBm
  - IIP2 of 120 dBm
- High power handling
  - 38.5 dBm @ 2.4 GHz
  - 37.0 dBm @ 6.0 GHz
- Fast switching time of 500 ns
- ESD performance
  - 3kV HBM on RF pins to GND
  - 1.5kV HBM on all pins
  - 1kV CDM on all pins

Product Description

The PE42423 is a HaRP™ technology-enhanced absorptive 50Ω SPDT RF switch designed for use in high power and high performance WLAN 802.11 a/b/g/n/ac applications such as carrier and enterprise Wi-Fi Products, supporting bandwidths up to 6 GHz.

This switch features high linearity which remains invariant across the full supply range. PE42423 also features exceptional isolation, high power handling and is offered in a 16-lead 3x3 mm QFN package. In addition, no external blocking capacitors are required if 0V DC is present on the RF ports.

The PE42423 is manufactured on PSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

PSemi's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

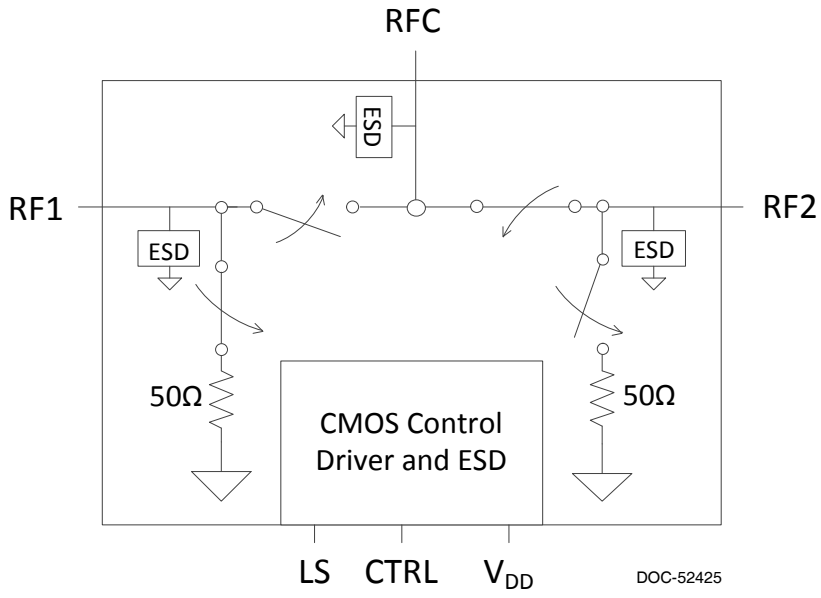


Figure 2. Package Type

16-lead 3x3 mm QFN

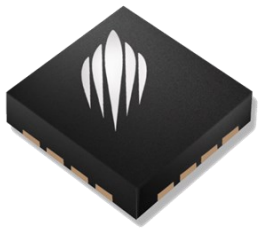


Table 1. Electrical Specifications Temp = 25°C, V_{DD} = 3.3V

Parameter	Path	Condition	Min	Typ	Max	Unit
Operational frequency			0.1		6	GHz
Insertion loss	RFC–RFX	0.1–2.4 GHz 2.4–5.8 GHz 5.8–6.0 GHz		0.80 0.95 0.95	1.0 1.1 1.1	dB dB dB
Isolation	RFX–RFX	0.1–2.4 GHz 2.4–5.8 GHz 5.8–6.0 GHz	49 39 39	51 41 41		dB dB dB
Isolation	RFC–RFX	0.1–2.4 GHz 2.4–5.8 GHz 5.8–6.0 GHz	44 39 40	47 41 43		dB dB dB
Return loss (common and active port)	RFX	0.1–2.4 GHz 2.4–5.8 GHz 5.8–6.0 GHz		19 16 16		dB dB dB
Return loss (terminated port)	RFX	0.1–2.4 GHz 2.4–5.8 GHz 5.8–6.0 GHz		23 23 24		dB dB dB
Input 0.1 dB compression point[1]	RFC–RFX	0.6–4.0 GHz		39.5		dBm
Input IP3[2]	RFC–RFX	0.8–2.7 GHz		65		dBm
Input IP2[2]	RFC–RFX	0.8–2.7 GHz		120		dBm
Switching time		50% CTRL to 90% or 10% of final value		500	700	ns

Notes: 1. The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 3* for the operating RF input power (50)
2. The input intercept point remains invariant over the full supply range as defined in *Table 3*

Figure 3. Pin Configuration (Top View)

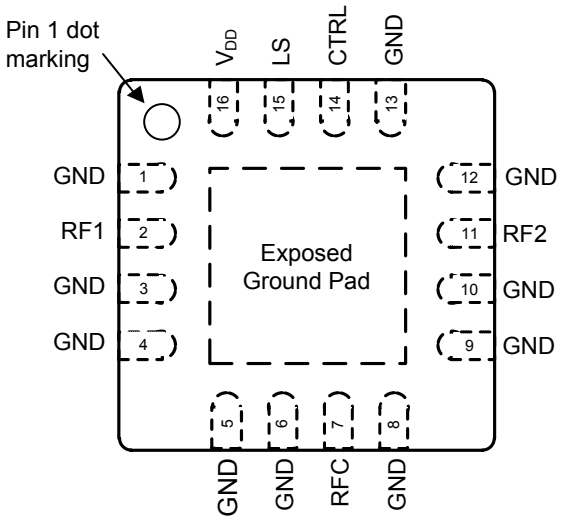


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1, 3, 4, 5, 6, 8, 9, 10, 12, 13	GND	Ground
2	RF1[1]	RF port 1
7	RFC[1]	RF common
11	RF2[1]	RF port 2
14	CTRL	Digital control logic input
15	LS	Logic Select - used to determine the definition for the CTRL pin (see *Table 5*)
16	V_{DD}	Supply voltage (nominal 3.3V)
Pad	GND	Exposed pad: ground for proper operation

Note 1: RF pins 2, 7 and 11 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.3		5.5	V
Supply current	I_{DD}		120	200	µA
Digital input high (CTRL)	V_{IH}	1.17		3.6	V
Digital input low (CTRL)	V_{IL}	-0.3		0.6	V
RF input power, CW 0.1–0.6 GHz 0.6–4.0 GHz 4.0–6.0 GHz	$P_{MAX,CW}$			 27 *Fig. 4* *Fig. 4*	 dBm dBm dBm
RF input power, pulsed[1] 0.1–0.6 GHz 0.6–4.0 GHz 4.0–6.0 GHz	$P_{MAX,PULSED}$			 27 *Fig. 4* *Fig. 4*	 dBm dBm dBm
RF input power into terminated ports, CW	$P_{MAX,TERM}$			22	dBm
Operating temperature range	T_{OP}	-40	+25	+125	°C

Note 1: Pulsed, 5% duty cycle of 4620 µs period, 50Ω

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage (CTRL)	V_{CTRL}	-0.3	3.6	V
LS input voltage	V_{LS}	-0.3	3.6	V
Maximum input power 0.1–0.6 GHz 0.6–4.0 GHz 4.0–6.0 GHz	$P_{MAX,ABS}$		 *30* *39* *37.5*	 dBm dBm dBm
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM[1] RF pins to GND All pins	$V_{ESD,HBM}$		 3000 1500	 V V
ESD voltage MM[2], all pins	$V_{ESD,MM}$		200	V
ESD voltage CDM[3], all pins	$V_{ESD,CDM}$		1000	V

Notes: 1. Human Body Model (MIL-STD 883 Method 3015)
2. Machine Model (JEDEC JESD22-A115)
3. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Switching Frequency

The PE42423 has a maximum 25 kHz switching rate. Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Table 5. Control Logic Truth Table

LS	CTRL	RFC-RF1	RFC-RF2
0	0	off	on
0	1	on	off
1	0	on	off
1	1	off	on

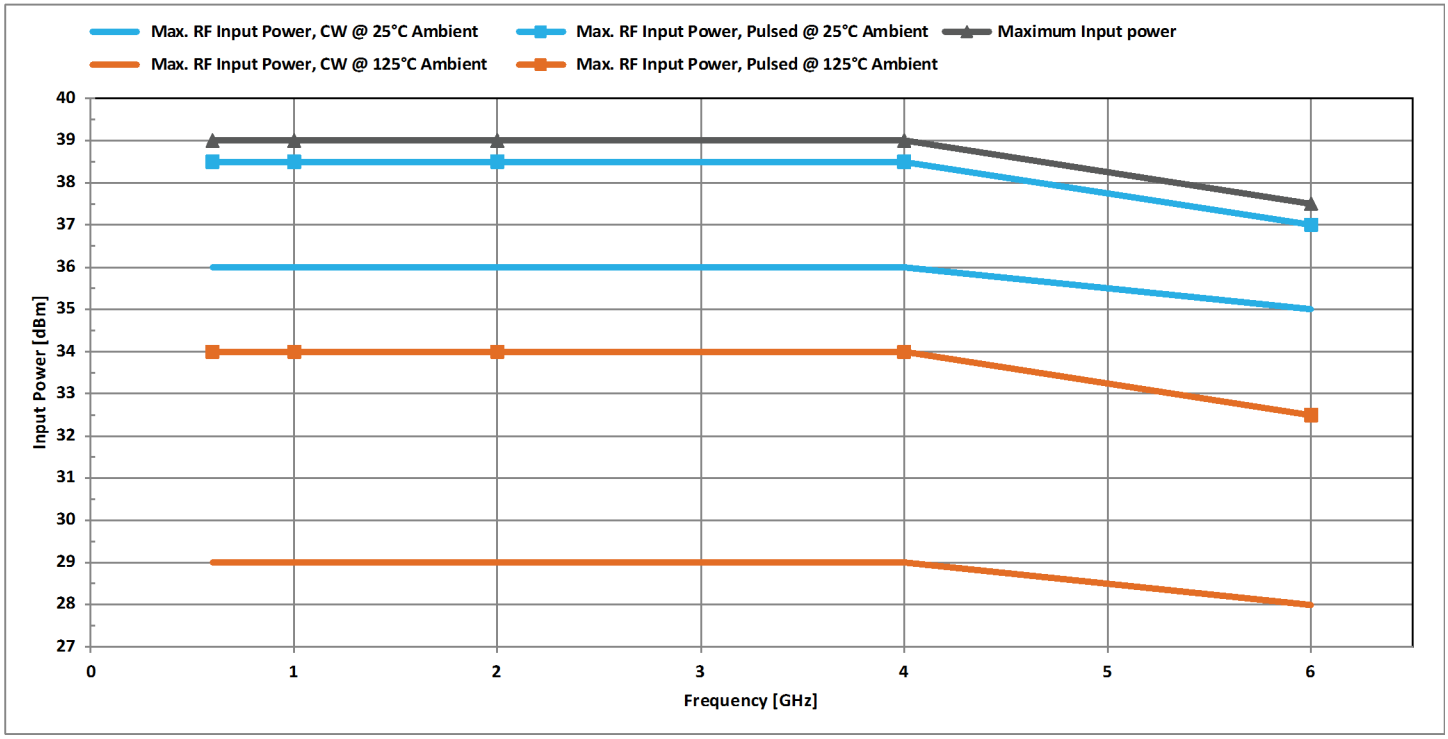
Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42423 in the 16-lead 3x3 mm QFN package is MSL3.

Logic Select (LS)

The Logic Select feature is used to determine the definition for the CTRL pin.

Figure 4. Power De-rating Curve for 600 MHz – 6 GHz



Typical Performance Data @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 5. Insertion Loss vs. Temp (RFC–RFX)

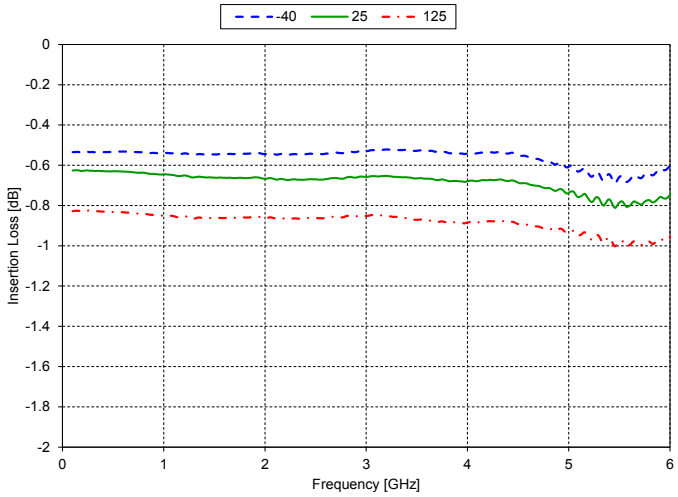


Figure 6. Insertion Loss vs. V_{DD} (RFC–RFX)

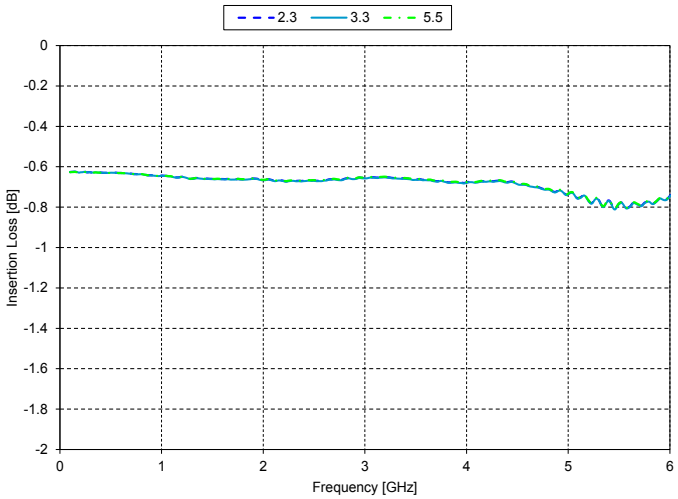


Figure 7. RFX Port Return Loss vs. Temp

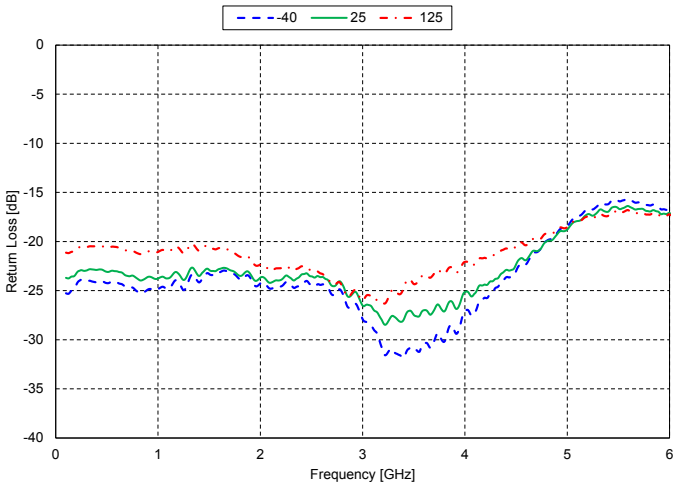
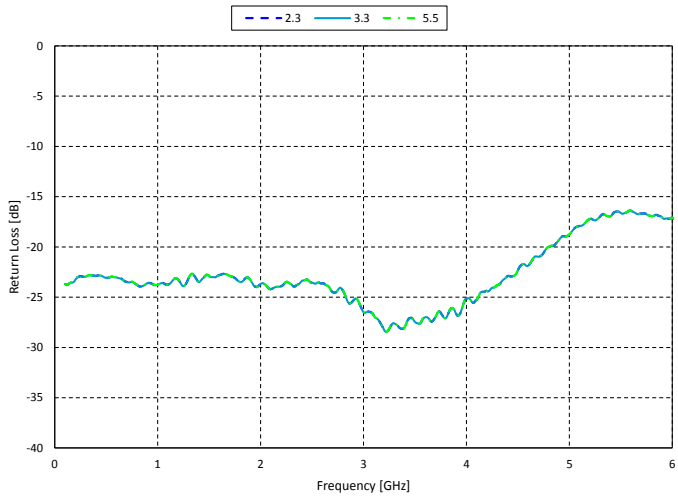


Figure 8. RFX Port Return Loss vs. V_{DD}



Typical Performance Data @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 9. Terminated Port Return Loss vs. Temp (RFX Active)

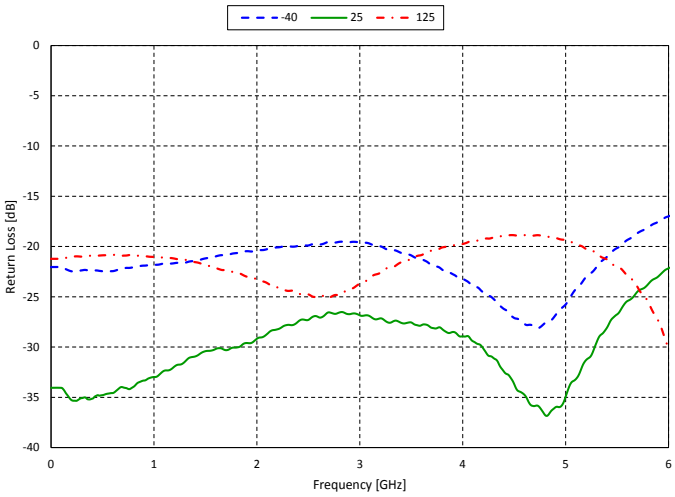


Figure 10. Terminated Port Return Loss vs. V_{DD} (RFX Active)

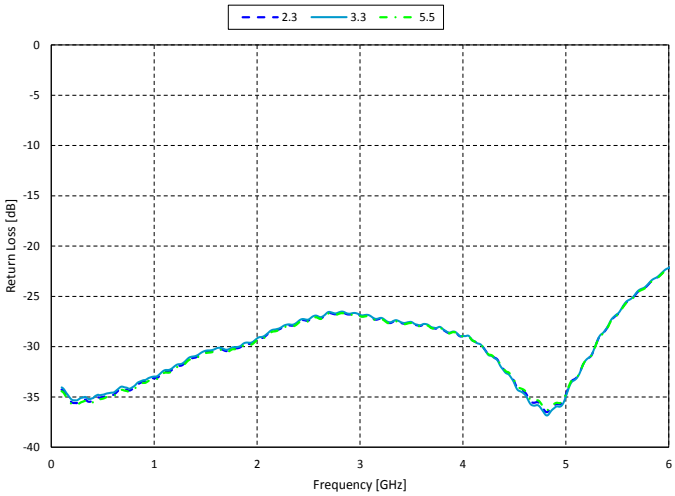


Figure 11. Isolation vs. Temp (RFX–RFX, RFX Active)

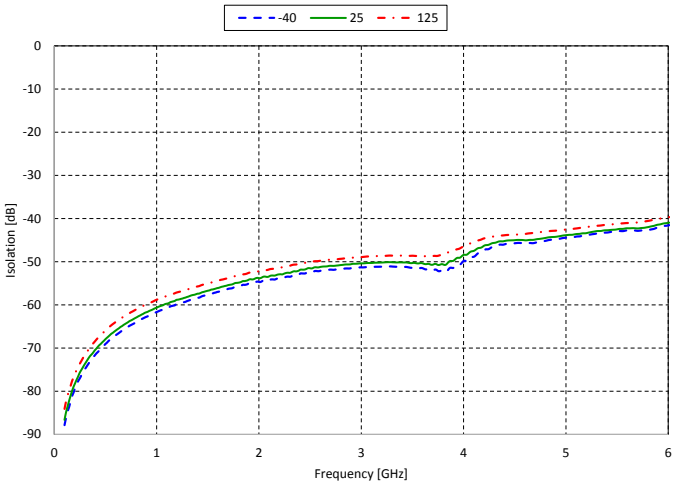
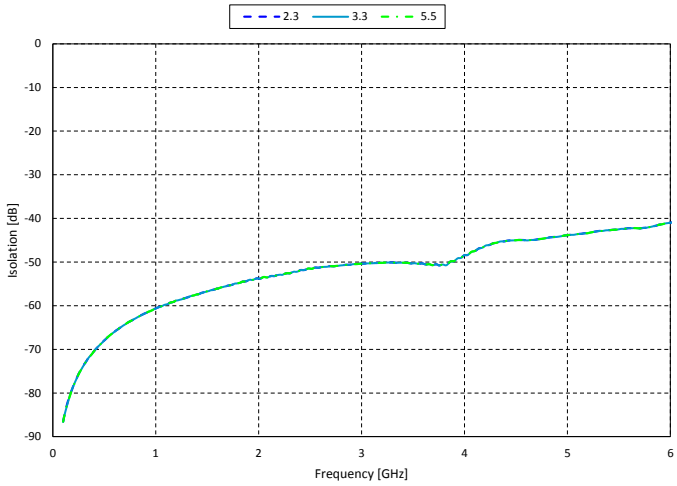


Figure 12. Isolation vs. V_{DD} (RFX–RFX, RFX Active)



Typical Performance Data @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 13. Isolation vs. Temp (RFC–RFX, RFX Active)

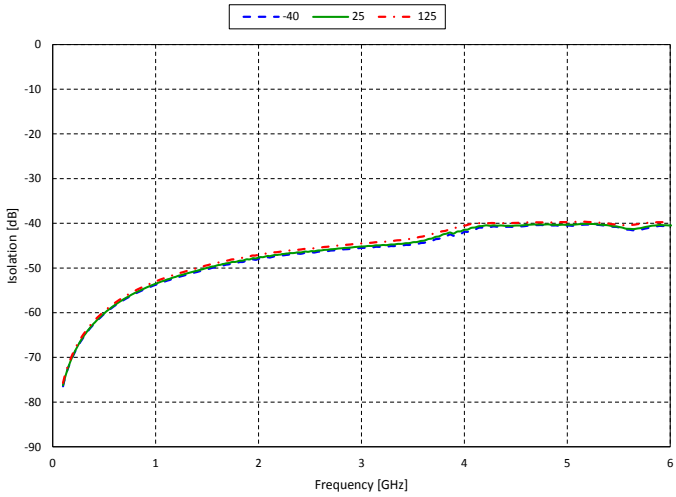
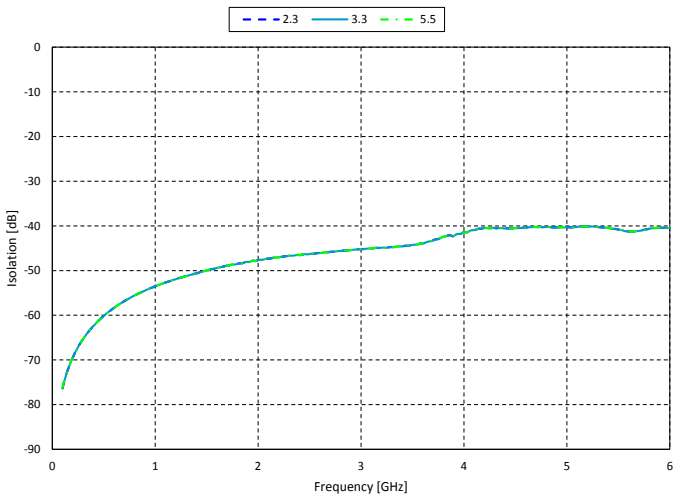


Figure 14. Isolation vs. V_{DD} (RFC–RFX, RFX Active)

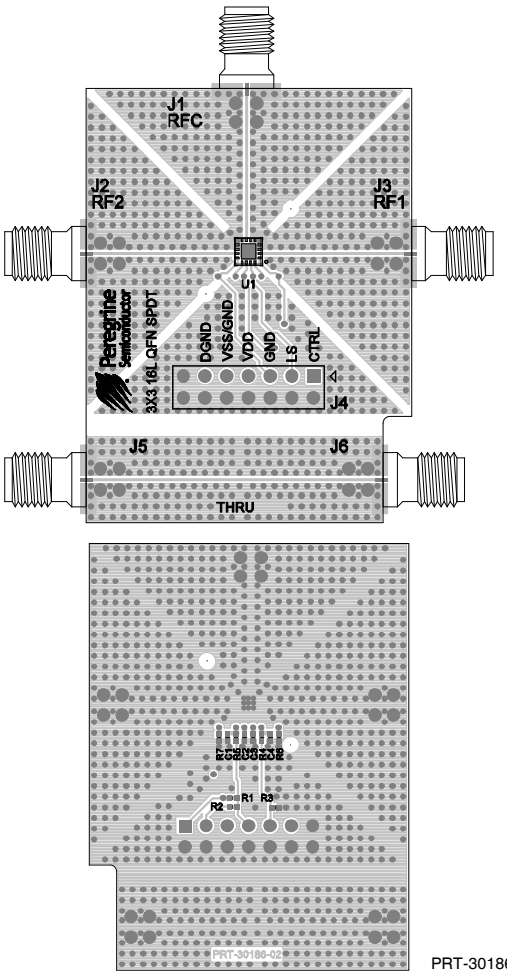


Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of PSemi's PE42423. The RF common port is connected through a 50Ω transmission line via the SMA connector, J1. RF1 and RF2 ports are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A 50Ω through transmission line is available via SMA connectors J5 and J6, which can be used to de-embed the loss of the PCB. J4 provides DC and digital inputs to the device.

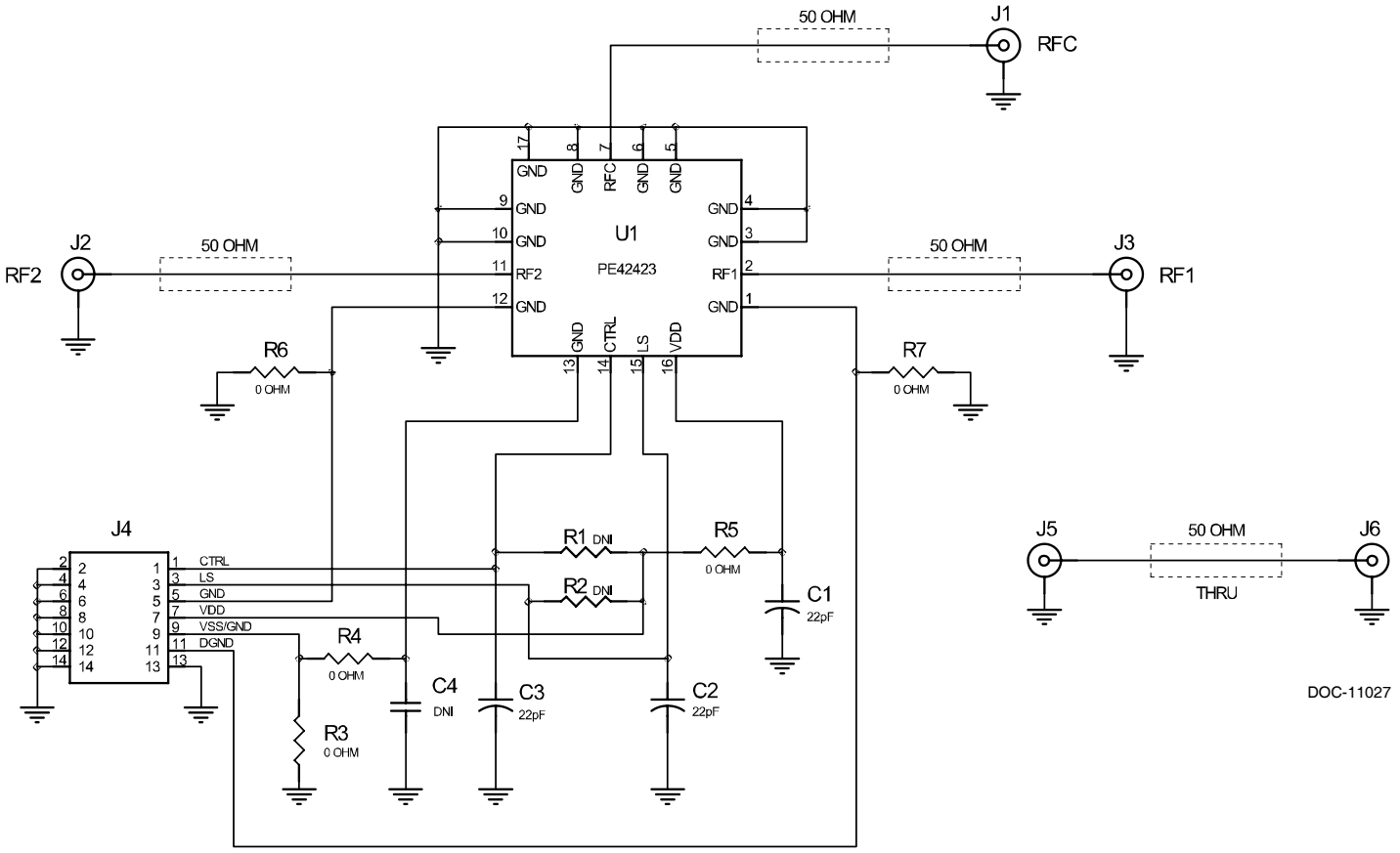
For the true performance of the PE42423 to be realized, the PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

Figure 15. Evaluation Kit Layout



PRT-30186

Figure 16. Evaluation Board Schematic



Notes: 1. Use PRT-30186-2 PCB
2. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD)

Figure 17. Package Drawing
16-lead 3x3 mm QFN

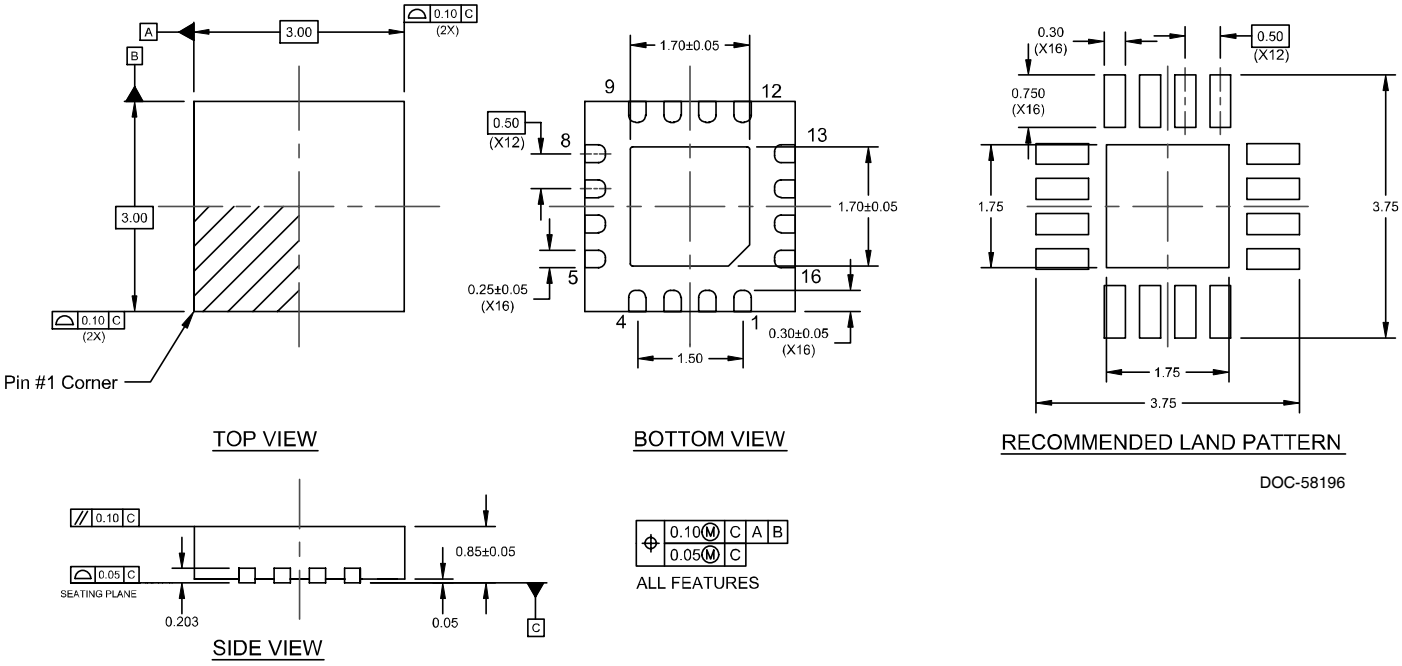
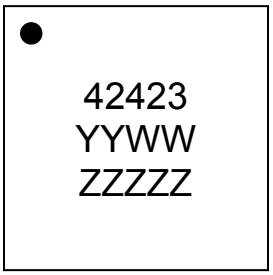


Figure 18. Top Marking Specifications



17-0009

● = Pin 1 designator
YYWW = Date code
ZZZZZ = Last five digits of lot number