PE42426

Document Category: Product Specification

UltraCMOS® SPDT RF Switch, 5–6000 MHz

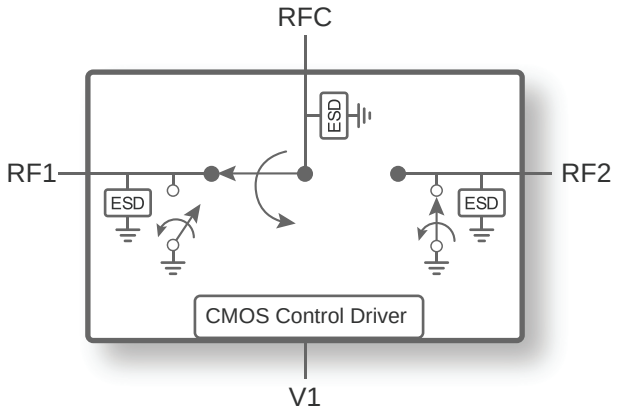
Features

- Best in class linearity across frequency band
- Exceptional harmonics
  - 2fo of –121 dBc @ 900 MHz
  - 3fo of –135 dBc @ 900 MHz
- Low insertion loss and high isolation performance
  - Insertion loss of 0.3 dB @ 2000 MHz
- High ESD performance of 3 kV HBM
- Packaging – 12-lead 3 × 3 × 0.75 mm QFN

Applications

- Land mobile radio (LMR)
- General switching applications

Figure 1 • *PE42426 Functional Diagram*



Product Description

The PE42426 is a HaRP™ technology-enhanced reflective SPDT RF switch designed for use in land mobile radio (LMR) and general switching applications. It delivers high linearity and excellent harmonics performance across the entire operational band. It also features low insertion loss and high isolation performance making the PE42426 ideal for general switching applications.

The PE42426 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE42426*

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	5.5	V
Digital input voltage, V1	–0.3	3.6	V
RF input power		39	dBm
Maximum junction temperature		+150	°C
Storage temperature range	–65	+150	°C
ESD voltage HBM(1), all pins		3000	V
ESD voltage CDM(2), all pins		500	V

Notes:
1) Human body model (MIL-STD 883 Method 3015).
2) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE42426. Devices should not be operated outside the operating conditions listed below.

Table 2 • *Recommended Operating Conditions for PE42426*

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	2.3	3.3	5.5	V
Supply current, I_{DD}		130	200	µA
Digital input high, V1	1.17		3.6(1)	V
Digital input low, V1	–0.3		0.6	V
RF input power, CW(2)			33	dBm
RF input power, pulse(3)			38	dBm
Operating temperature range	–40	+25	+105	°C

Notes:

1) Maximum digital input voltage is limited to V_{DD} and cannot exceed 3.6V.
2) 100% duty cycle.
3) Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Electrical Specifications

Table 3 provides the PE42426 key electrical specifications @ +25 °C, V_{DD} = 3.3V, Z_S = Z_L = 50Ω, unless otherwise specified.

Table 3 • *PE42426 Electrical Specifications*

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			5		6000	MHz
Insertion loss[1]	RFC–RFX	5–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz		0.30 0.35 0.40 0.40 0.75	0.55 0.65 0.75 0.75 1.30	dB dB dB dB dB
Isolation	All paths	5–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz	31 27 23.5 20 17	33 29 25 22 20		dB dB dB dB dB
Return loss[1]	RFC, RFX	5–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz		33 22 20 25 12		dB dB dB dB dB
2nd harmonic, 2fo	RFX	P_{IN} = 18 dBm @ 900 MHz, fo		–121		dBc
3rd harmonic, 3fo	RFX	P_{IN} = 18 dBm @ 900 MHz, fo		–135		dBc
Input IP2		P_{IN} = 18 dBm @ 900 MHz		130		dBm
Input IP3		P_{IN} = 18 dBm @ 900 MHz		83		dBm
Input 0.1dB compression point[2]		5–6000 MHz		40		dBm
Switching time		50% CTRL to 90% or 10% RF		35		µs

Notes:
1) High frequency performance can be improved by external matching.
2) The input 0.1dB compression point is a linearity figure of merit. Refer to **Table 2** for the operating RF input power (50Ω).

Switching Frequency

The PE42426 has a maximum 10 kHz switching frequency. Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reached 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spurious Performance

The PE42426 spur fundamental occurs around 10 MHz. Its typical performance is –154 dBm/Hz (V1 = H) and –165 dBm/Hz (V1 = L), with 100 kHz bandwidth.

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$\Psi_{JT} = (T_J - T_T)/P$

where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 4 • *Thermal Data for PE42426*

Parameter	Typ	Unit
Ψ_{JT}	21	°C/W

Control Logic

Table 5 provides the control logic truth table for the PE42426.

Table 5 • *Truth Table for PE42426*

State	V1
RFC–RF1	H
RFC–RF2	L

Typical Performance Data

Figure 2–Figure 11 show the typical performance data @ +25 °C, V_{DD} = 3.3V, Z_S = Z_L = 50Ω, unless otherwise specified.

Figure 2 • *Insertion Loss vs Temperature (RFC–RFX)*

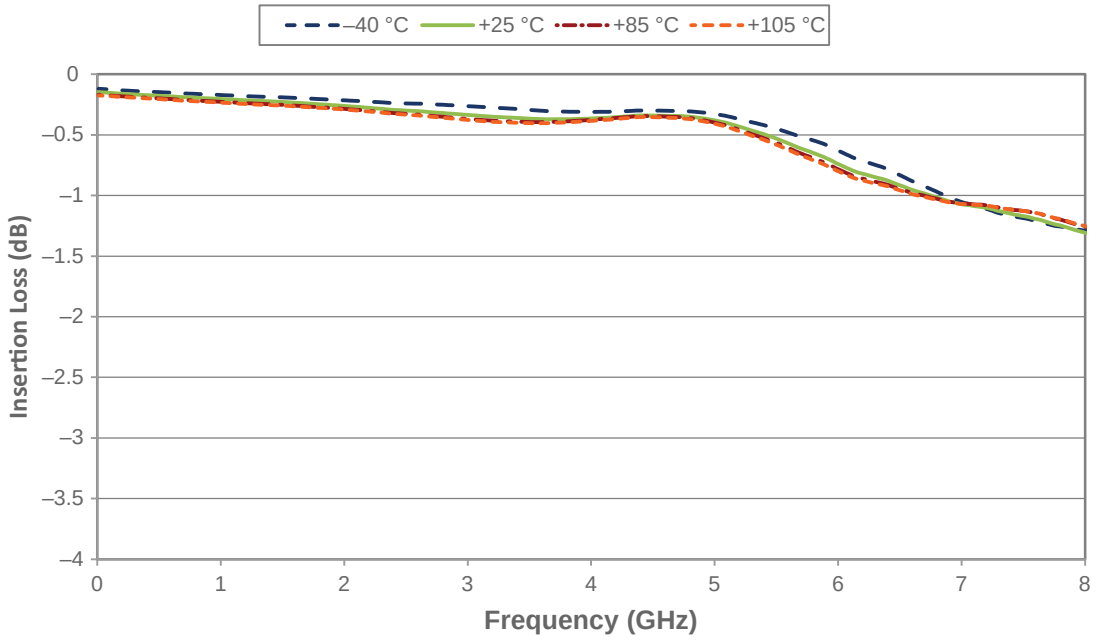


Figure 3 • *Insertion Loss vs V_{DD} (RFC–RFX)*

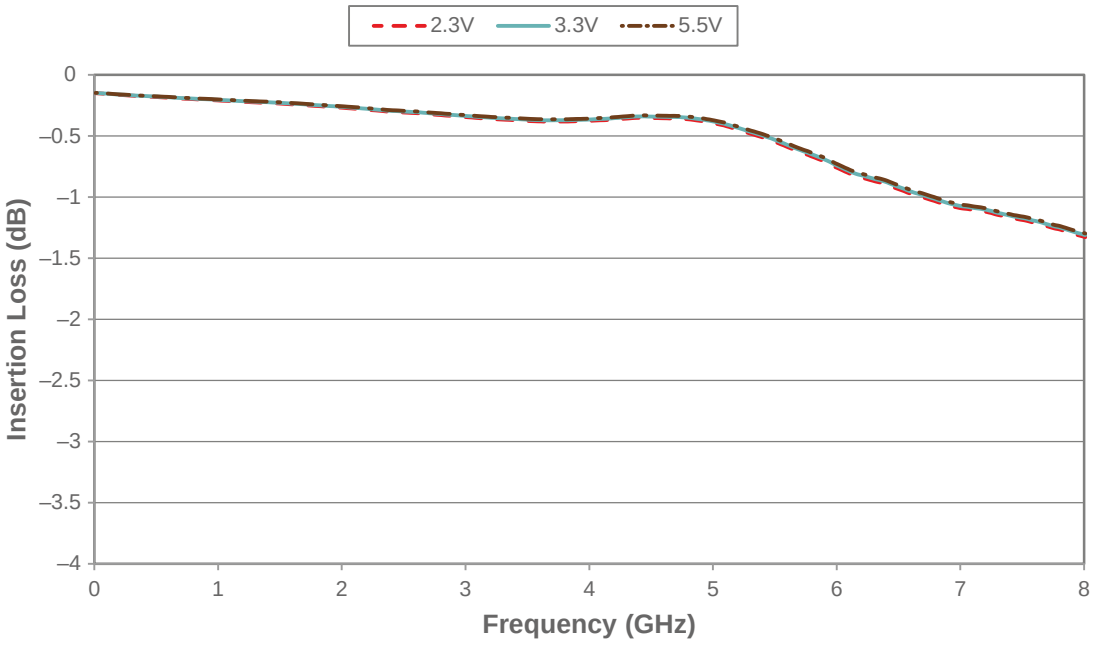


Figure 4 • *RFC Port Return Loss vs Temperature*

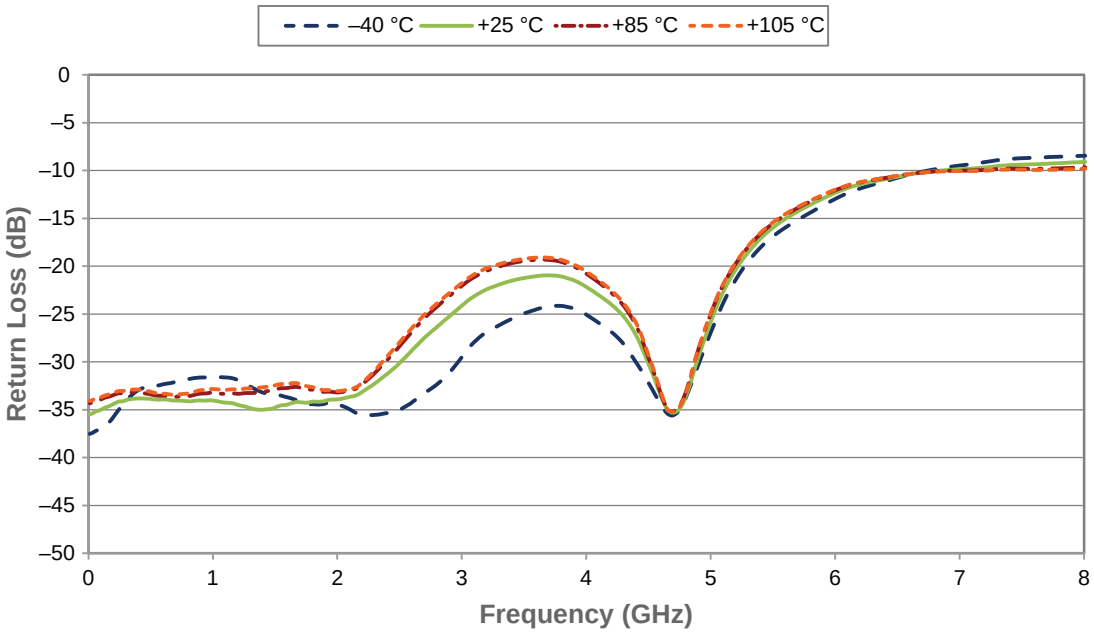


Figure 5 • *RFC Port Return Loss vs V_{DD}*

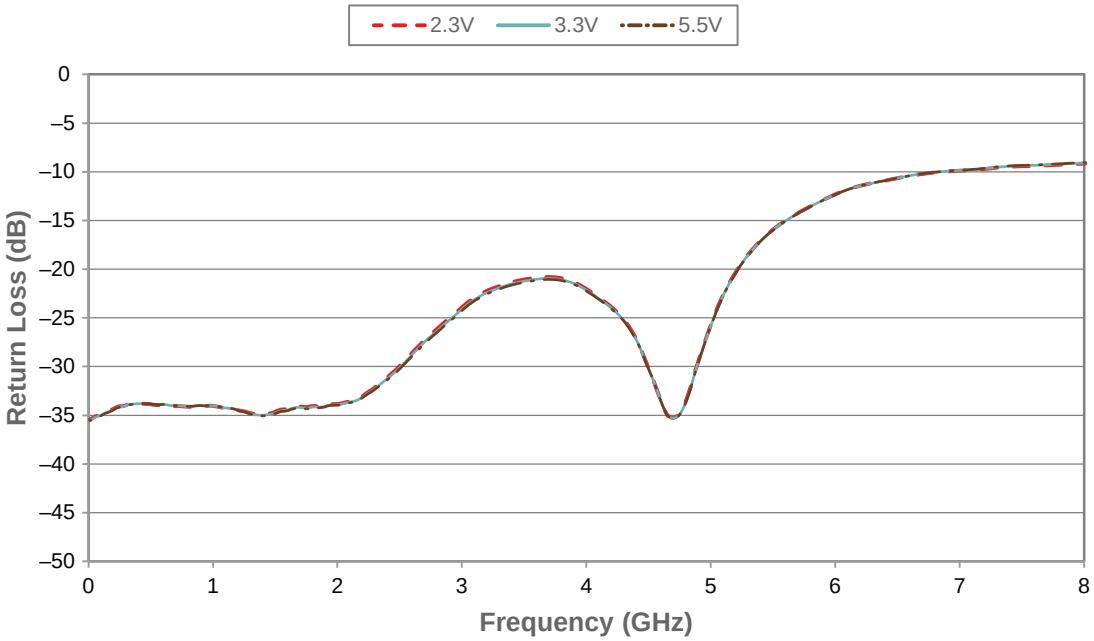


Figure 6 • *Active Port Return Loss vs Temperature*

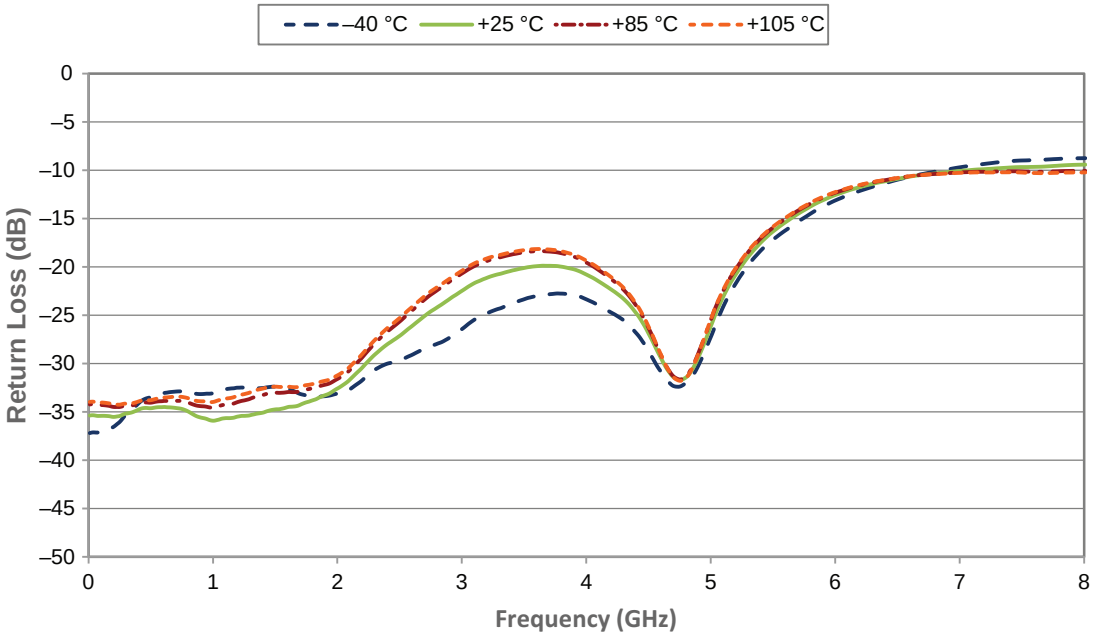


Figure 7 • *Active Port Return Loss vs V_{DD}*

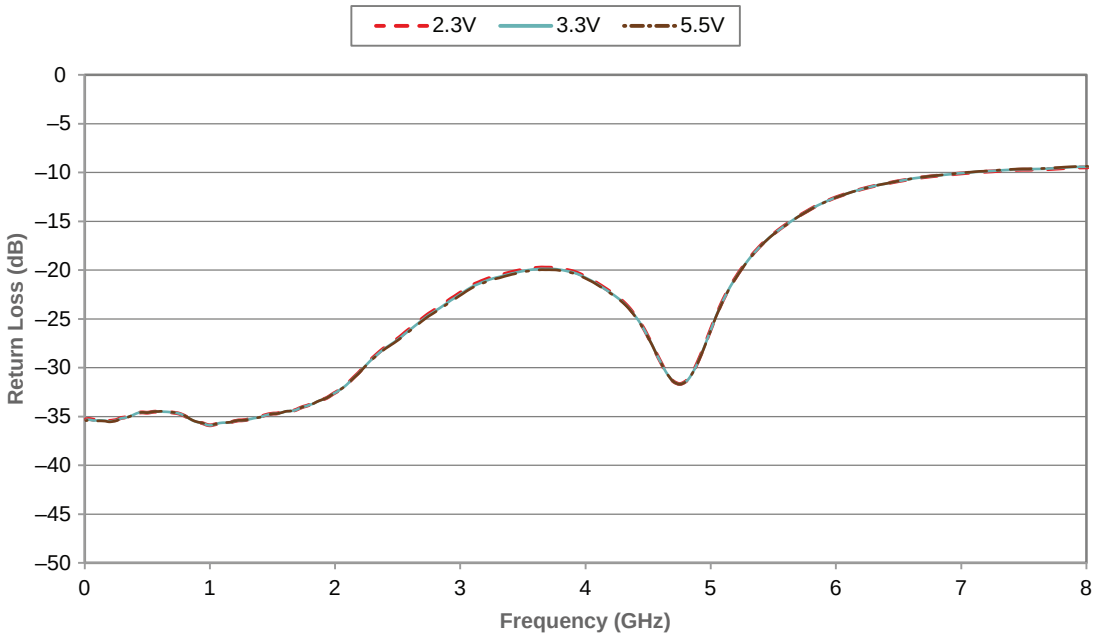


Figure 8 • *Isolation vs Temperature (RFX–RFX)*

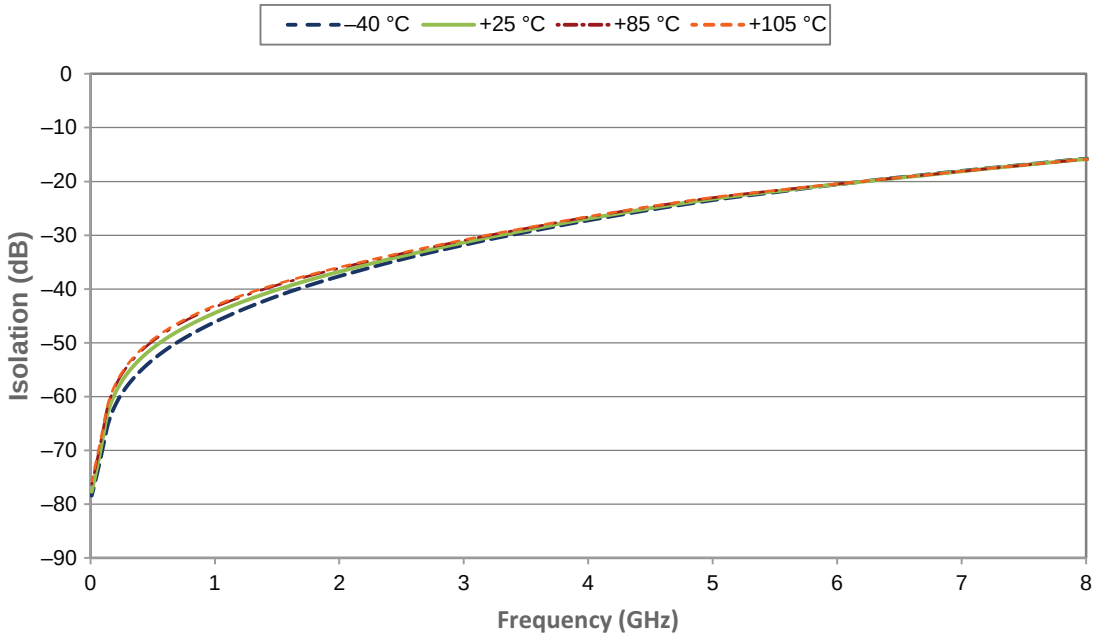


Figure 9 • *Isolation vs V_{DD} (RFX–RFX)*

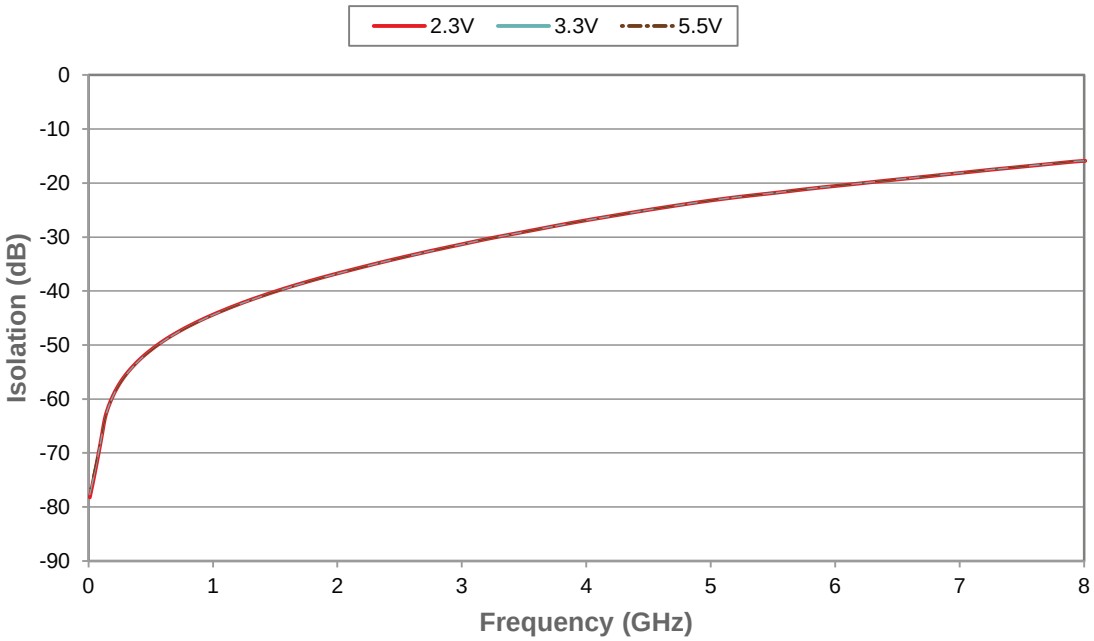


Figure 10 • *Isolation vs Temperature (RFC–RFX)*

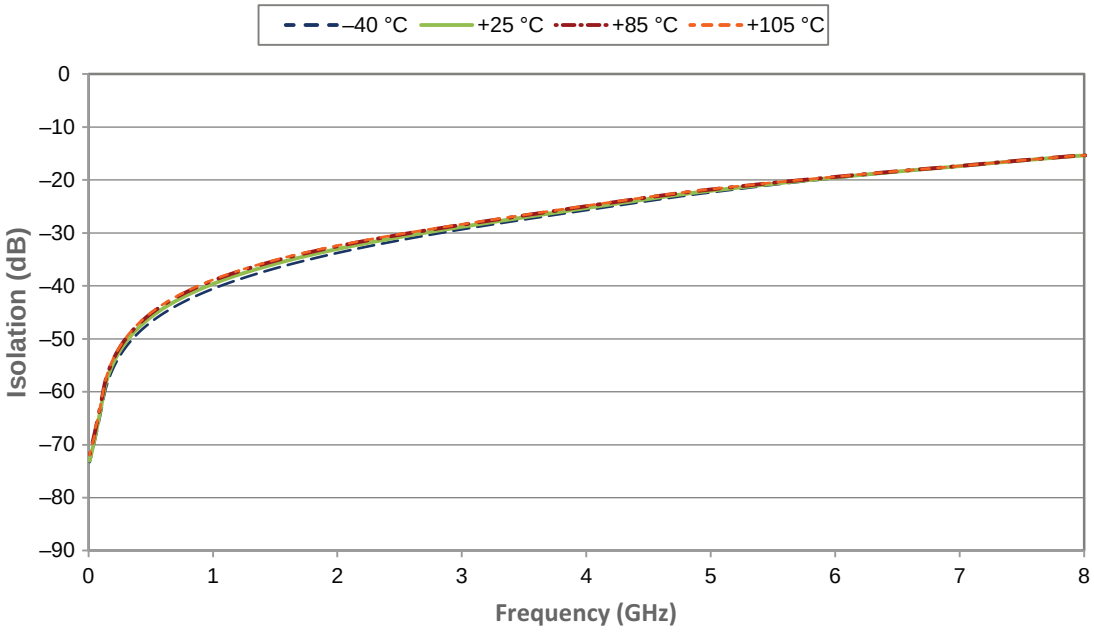


Figure 11 • *Isolation vs V_{DD} (RFC–RFX)*

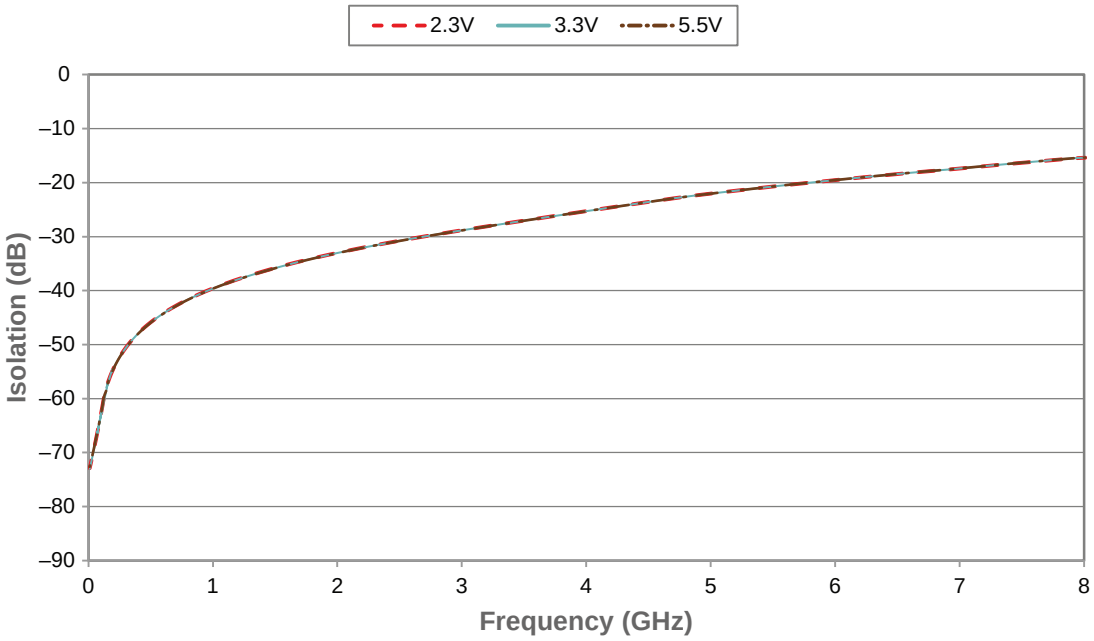


Figure 12 • *IIP2 vs Frequency*

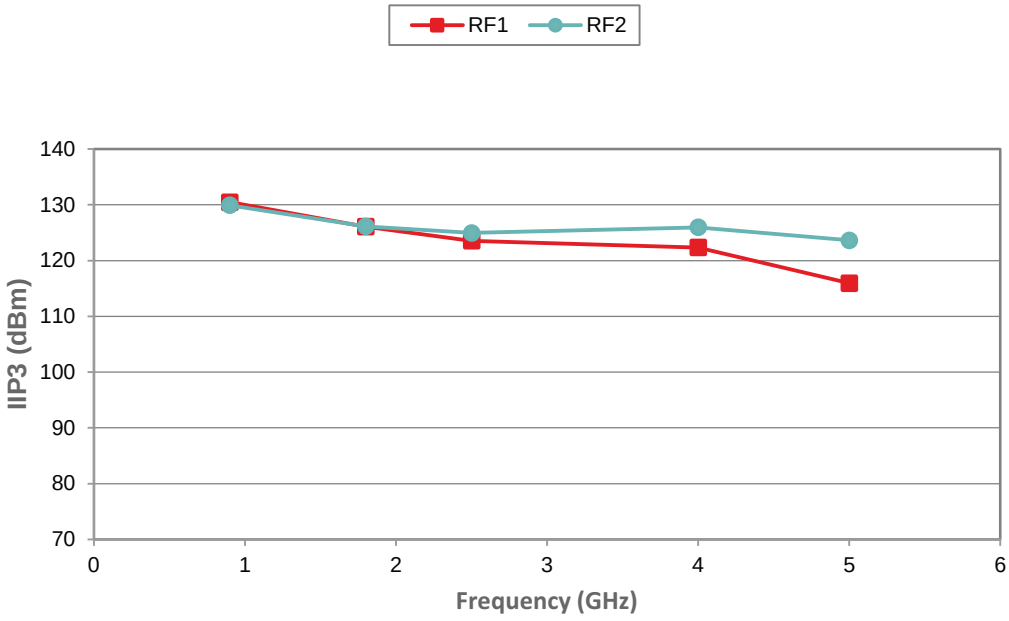
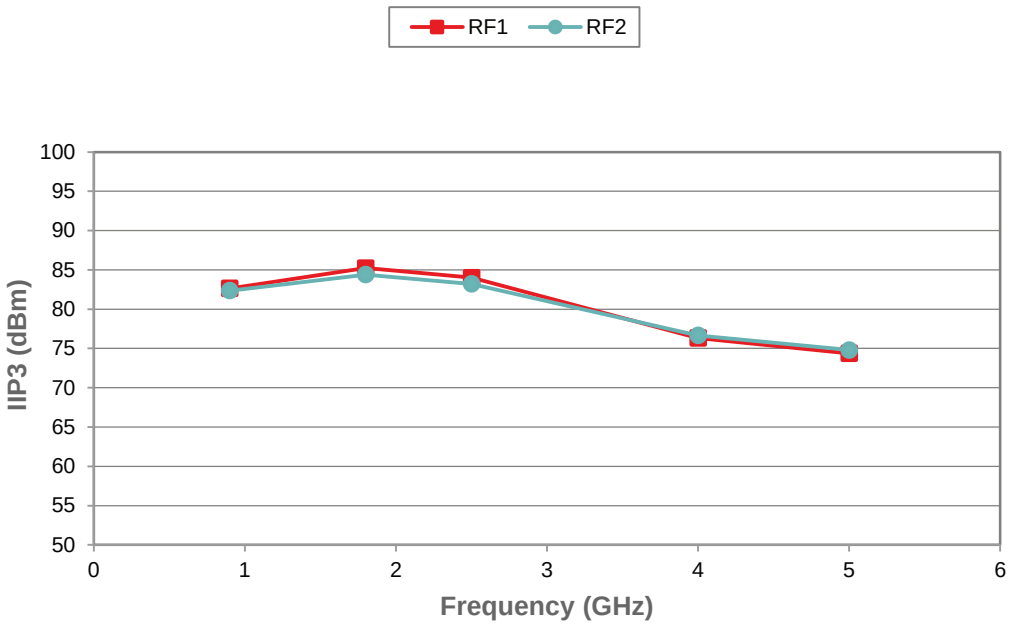


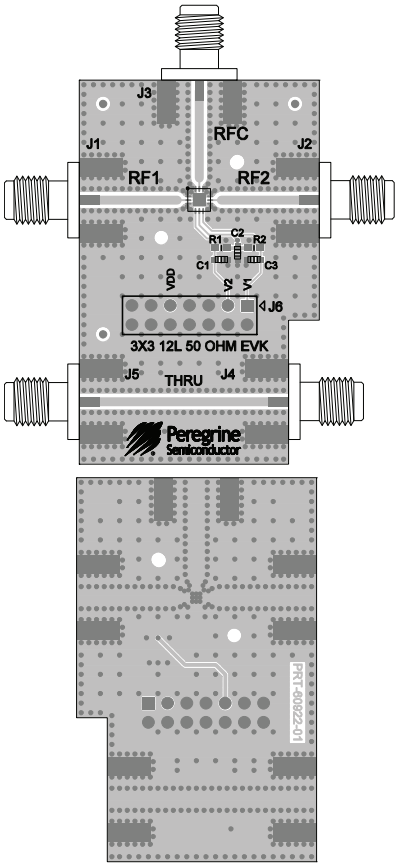
Figure 13 • *IIP3 vs Frequency*



Evaluation Kit

The PE42426 evaluation board was designed to ease customer evaluation of the PE42426 RF switch. The RF common port is connected through a 50Ω transmission line via J3. RF1 and RF2 ports are connected through 50Ω transmission lines via J1 and J2, respectively. A 50Ω through transmission line is available via J4 (THRU left) and J5 (THRU right), which can be used to de-embed the loss of the PCB. J6 provides DC and digital inputs to the device.

Figure 14 • ***Evaluation Kit Layout for PE42426***



Pin Information

This section provides pinout information for the PE42426. **Figure 15** shows the pin map of this device for the available package. **Table 6** provides a description for each pin.

Figure 15 • *Pin Configuration (Top View)*

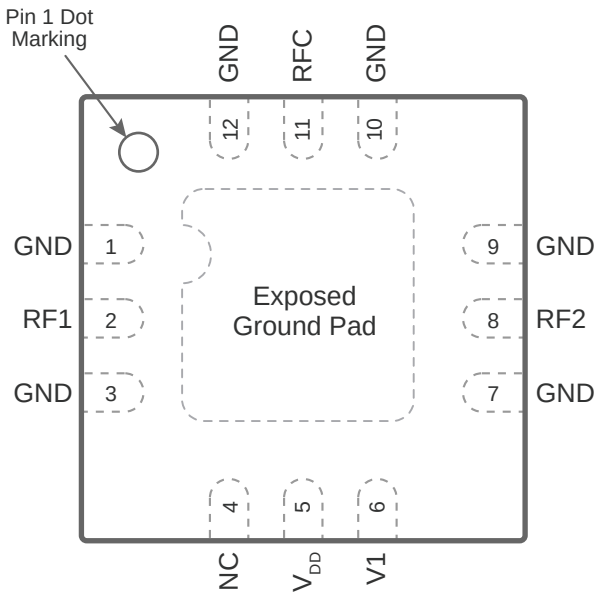


Table 6 • *Pin Descriptions for PE42426*

Pin No.	Pin Name	Description
1, 3, 7, 9, 10, 12	GND	Ground
2	RF1(*)	RF port 1
4	NC	Do not connect
5	V_{DD}	Supply voltage (nominal 3.3V)
6	V1	Digital control logic input 1
8	RF2(*)	RF port 2
11	RFC(*)	RF common
Pad	GND	Exposed pad: ground for proper operation

Note: * RF pins 2, 8 and 11 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Packaging Information

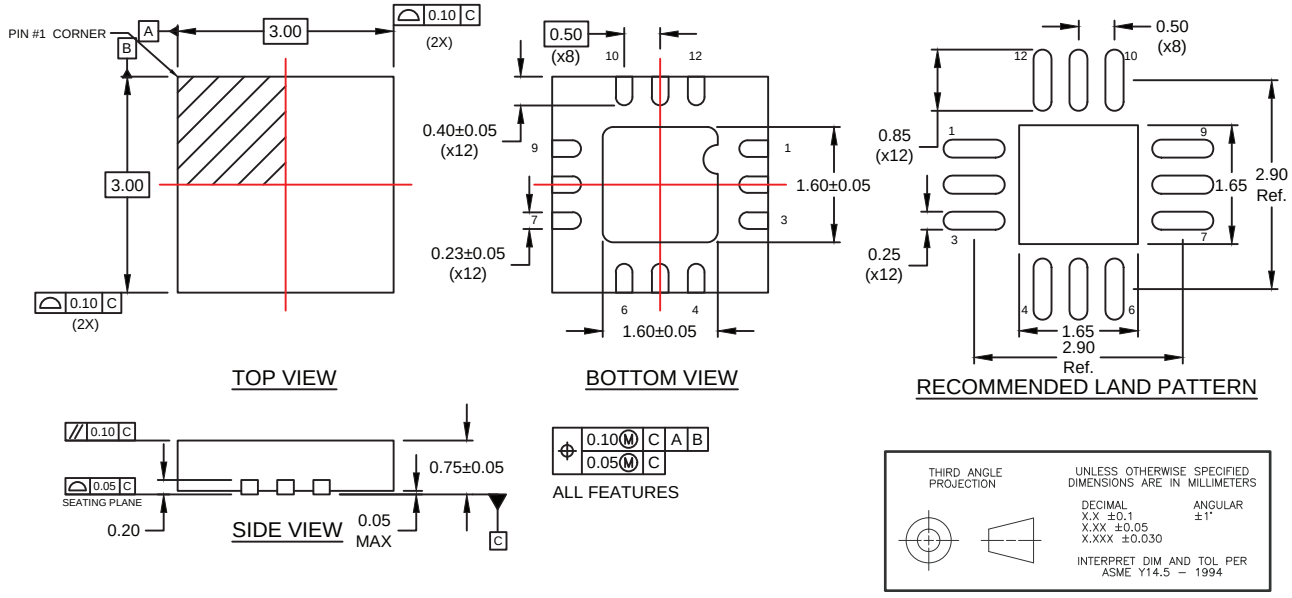
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE42426 in the 12-lead 3 × 3 × 0.75 mm QFN package is MSL1.

Package Drawing

Figure 16 • ***Package Mechanical Drawing for 12-lead 3 × 3 × 0.75 mm QFN***



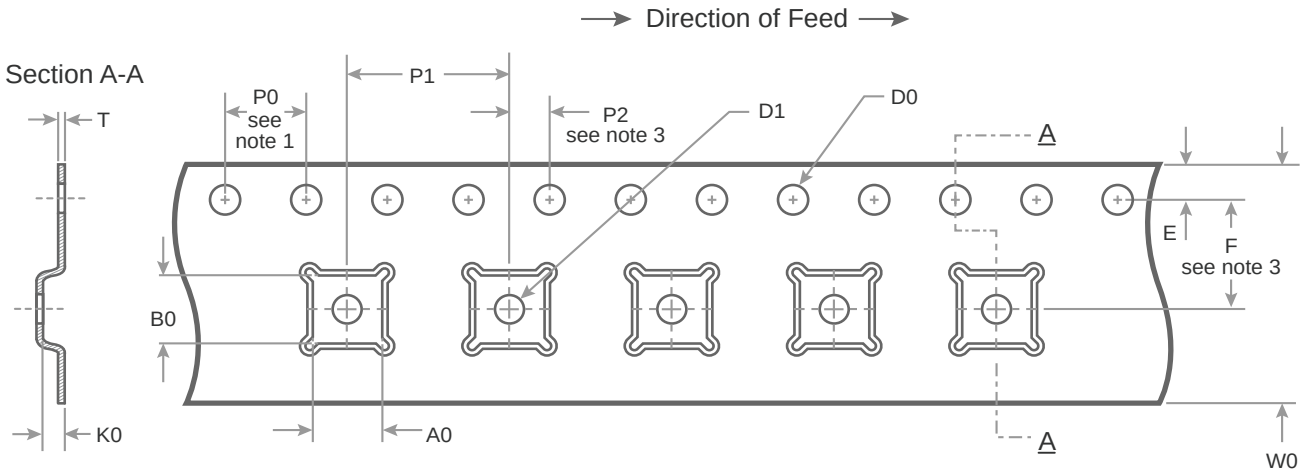
Top-Marking Specification

Figure 17 • ***Package Marking Specifications for PE42426***

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum six characters)

Tape and Reel Specification

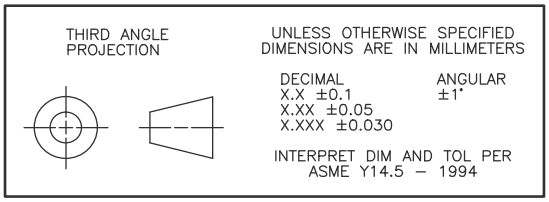
Figure 18 • ***Tape and Reel Specifications for 12-lead 3 × 3 × 0.75 mm QFN***

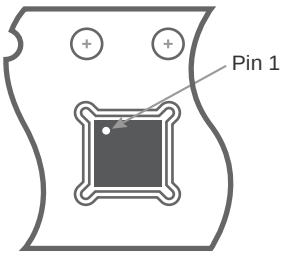


A0	3.30
B0	3.30
K0	1.10
D0	1.50 + 0.1/ -0.0
D1	1.5 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.3

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole





Device Orientation in Tape