Product Specification

PE42440

SP4T UltraCMOS® RF Switch
50 – 3000 MHz

Product Description

The PE42440 is a HaRP™-enhanced SP4T RF switch developed on the UltraCMOS® process technology. This general-purpose switch contains 4 identical RF ports and can be used in a multitude of applications up to 3000 MHz. It integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface and requires no DC blocking capacitors. This RoHS-compliant part is available in a standard 3 x 3 x 0.75 mm QFN package.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS® process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Features

- HaRP™ - Enhanced Technology for Unparalleled Linearity
- Very Low Insertion Loss: 0.45 dB @ 1000 MHz, 0.5 dB @ 2000 MHz
- Very High Isolation: 34 dB @ 1000 MHz, 28 dB @ 2000 MHz
- Exceptionally High ESD tolerance:
  - Class 3 (4.0 kV HBM) on RFC pin
  - Class 2 (2.0 kV HBM) on all pins
- Integrated Decoder for 2-pin control
  - Accepts 1.8V and 2.75V Control Logic Levels
- Low 4.5Ω Series ON Resistance
- No Blocking Capacitors Required

Figure 1. Functional Diagram

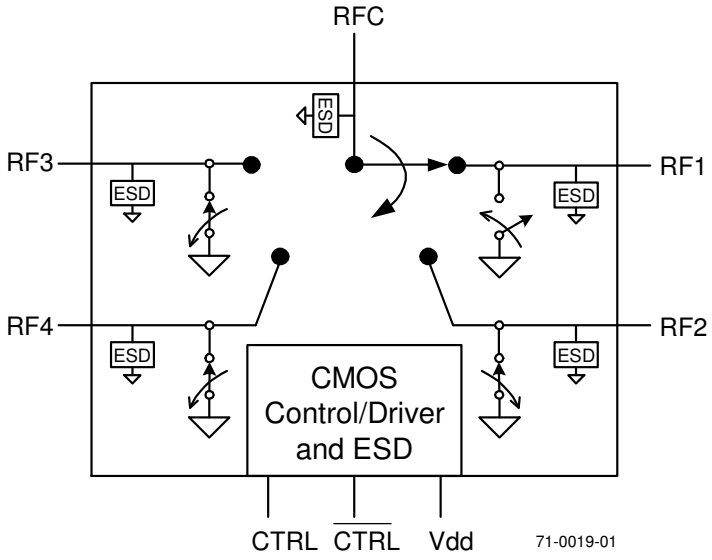


Figure 2. Package Type
16L 3 x 3 x 0.75 mm QFN

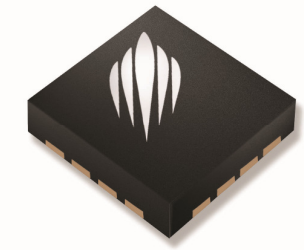


Table 1. Electrical Specifications: Temp = 25°C, V_{DD} = 2.75V (Z_S = Z_L = 50Ω)

Parameter	Condition	Min	Typ	Max	Units
Operational Frequency		50		3000	MHz
Insertion Loss (RFC - RFX)	50 - 1000 MHz	-	0.45	0.65	dB
	1000 - 2000 MHz	-	0.5	0.7	dB
	2000 - 3000 MHz	-	0.85	1.15	dB
Return Loss (RFC - RFX, Active Ports)	50 - 1000 MHz	-	22	-	dB
	1000 - 2000 MHz	-	15	-	dB
	2000 - 3000 MHz	-	11	-	dB
Isolation (RFC - RFX)	50 - 1000 MHz	31	34	-	dB
	1000 - 2000 MHz	25	28	-	dB
	2000 - 3000 MHz	20	22	-	dB
Input IP2	50 - 3000 MHz, +18 dBm per tone, 1 MHz spacing		96		dBm
Input IP3	50 - 3000 MHz, +18 dBm per tone, 1 MHz spacing		67		dBm
P1dB[1]	50 - 3000 MHz		41.5		dBm
Switching time	50% CNTL to 10/90% of RF		2		µs

Note: 1. Please refer to Maximum Operating Pin (50Ω) in *Table 4*

Table 2. Electrical Specifications, Worst Case Conditions: Temp = 85°C, V_{DD} = 2.65V (Z_S = Z_L = 50Ω)

Parameter	Condition	Min	Typ	Max	Units
Operational Frequency		50		3000	MHz
Insertion Loss (RFC - RFX)	50 - 1000 MHz	-	0.5	0.65	dB
	1000 - 2000 MHz	-	0.65	0.75	dB
	2000 - 3000 MHz	-	1.0	1.25	dB
Return Loss (RFC - RFX, Active Ports)	50 - 1000 MHz	-	21	-	dB
	1000 - 2000 MHz	-	15	-	dB
	2000 - 3000 MHz	-	10	-	dB
Isolation (RFC - RFX)	50 - 1000 MHz	30	32	-	dB
	1000 - 2000 MHz	24	26	-	dB
	2000 - 3000 MHz	20	22	-	dB
Input IP2	50 - 3000 MHz, +18 dBm per tone, 1 MHz spacing		95		dBm
Input IP3	50 - 3000 MHz, +18 dBm per tone, 1 MHz spacing		66		dBm
P1dB[1]	50 - 3000 MHz		41		dBm
Switching time	50% CNTL to 10/90% of RF		2		µs

Note: 1. Please refer to Maximum Operating Pin (50Ω) in *Table 4*

Figure 3. Pin Configuration (Top View)

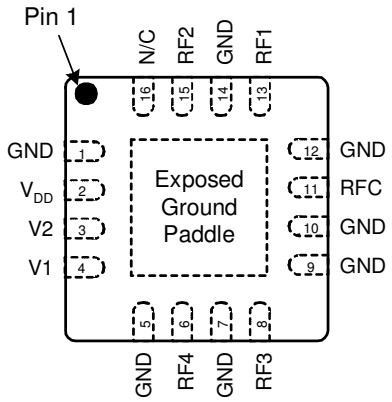


Table 3. Pin Descriptions

Pin No.	Pin Name	Description
1	GND	Ground
2	V_{DD}	Supply
3	V2	Switch control input, CMOS logic level
4	V1	Switch control input, CMOS logic level
5	GND	Ground
6	RF4[1]	RF Port 4
7	GND	Ground
8	RF3[1]	RF Port 3
9	GND	Ground
10	GND	Ground
11	RFC[1]	RF Common
12	GND	Ground
13	RF1[1]	RF Port 1
14	GND	Ground
15	RF2[1]	RF Port 2
16	N/C	No Connect
Paddle	GND	Exposed ground paddle

Notes: 1. All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}

Table 4. Operating Ranges[4]

Parameter	Symbol	Min	Typ	Max	Units
V_{DD} Supply Voltage	V_{DD}	2.65	2.75	3.3	V
I_{DD} Power Supply Current (V_{DD} = 2.75V)	I_{DD}		13	50	µA
RF input power (50Ω) (50 - 500 MHz) (500 - 3000 MHz)	P_{IN}			 +28 +33	 dBm dBm
Control Voltage High	V_{IH}	1.4			V
Control Voltage Low	V_{IL}			0.4	V
Temperature Range	T_{OP}	-40	+25	+85	℃
Storage Temperature Range	T_{ST}	-65	+25	+160	℃

Note: 1. Operation should be restricted to the limits in the Operating Ranges table

Table 5. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any DC input	-0.3	V_{DD}+ 0.3	V
P_{IN} (50Ω)[1]	RF input power (50 - 500 MHz) (500 - 3000 MHz)		 +28 +33	 dBm dBm
V_{ESD}	HBM[2] ESD Voltage, RFC pin		4000	V
	HBM[2] ESD Voltage, all pins		2000	V
	MM ESD Voltage, RFC pin		300	V
	MM ESD Voltage, all pins		100	V

Notes: 1. V_{DD} within operating range specified in *Table 4*
2. ESD Voltage (HBM, MIL-STD-883 Method 3015.7)

Exceeding absolute maximum ratings may cause permanent damage. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 6. Truth Table

Path	V2	V1
RFC – RF1	0	0
RFC – RF2	1	0
RFC – RF3	0	1
RFC – RF4	1	1

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42440 in the 16-lead 3 x 3 x 0.75 mm QFN package is MSL1.

Switching Frequency

The PE42440 has a maximum 25 kHz switching rate.

Evaluation Kit

The SP4T switch EK Board was designed to ease customer evaluation of Peregrine's PE42440. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1, RF2, RF3 and RF4 are connected through 50Ω transmission lines via SMA connectors J3, J5, J2 and J4, respectively. A through 50Ω transmission is available via SMA connectors J6 and J7. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a four metal layer FR4 material with a total thickness of 62 mils. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 32 mils, trace gaps of 25 mils, and metal thickness of 2.1 mils.

Figure 4. Evaluation Board Layouts
Peregrine Specification 101-0287-03

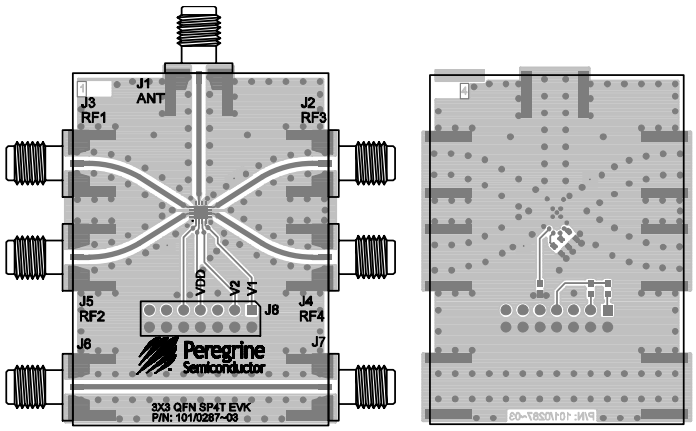
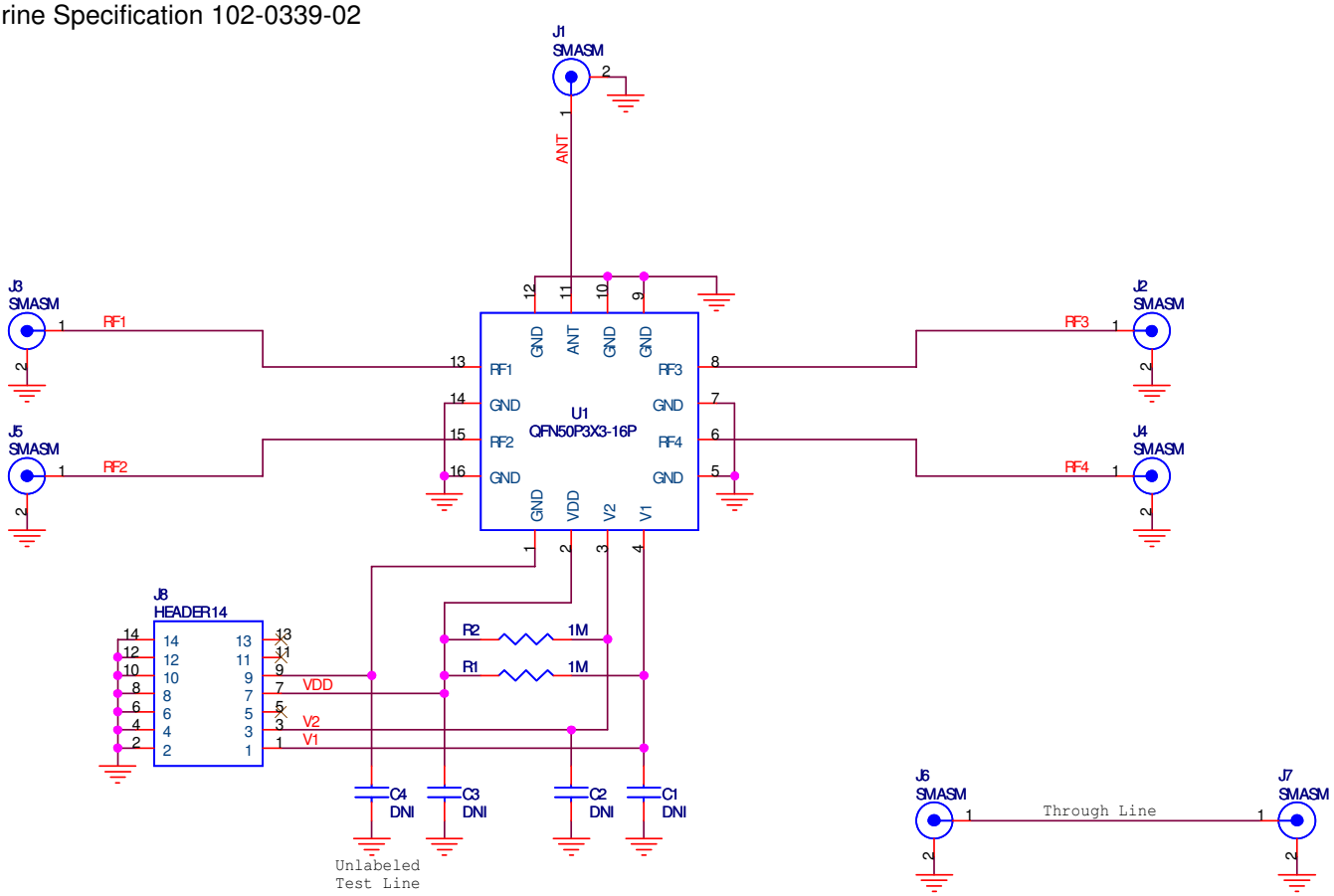


Figure 5. Evaluation Board Schematic
Peregrine Specification 102-0339-02



Typical Performance Data

Figure 6. Insertion Loss: RFC-RF @ 25°C

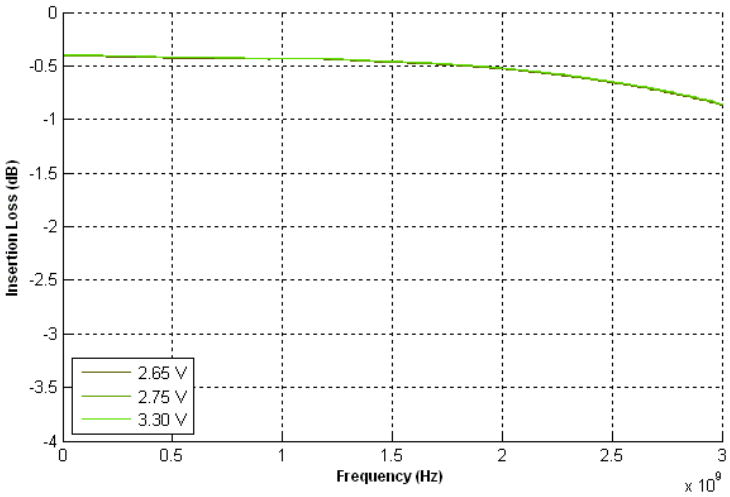


Figure 7. Insertion Loss: RFC-RF @ 2.75V

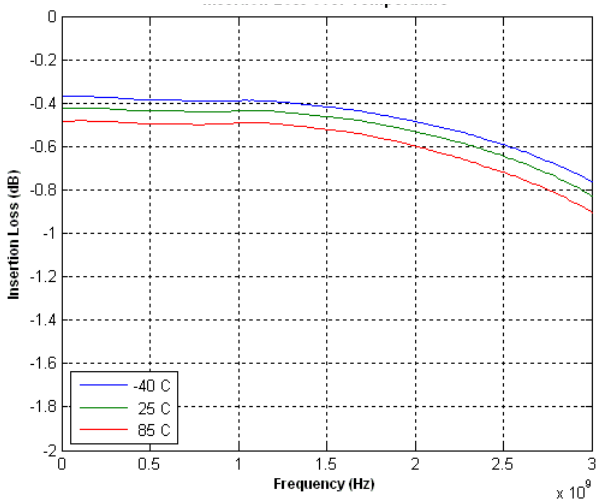


Figure 8. Isolation: RFC-RF @ 25°C

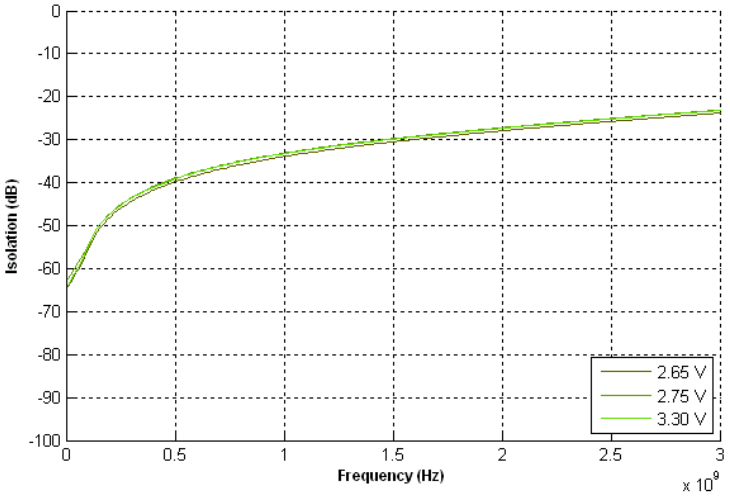


Figure 9. Isolation: RFC-RF @ 2.75V

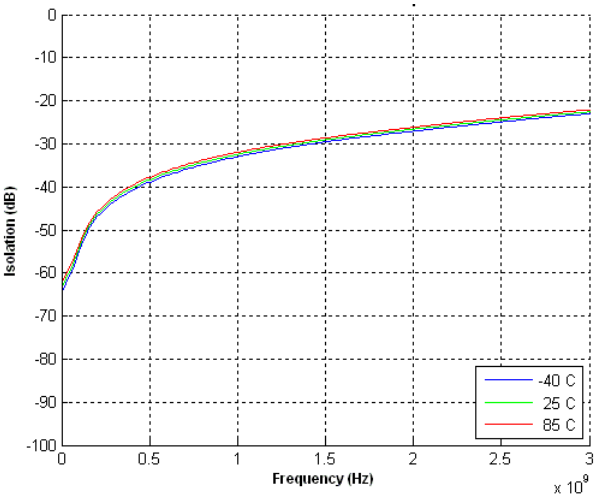


Figure 10. Return Loss at Active Port @ 25 °C

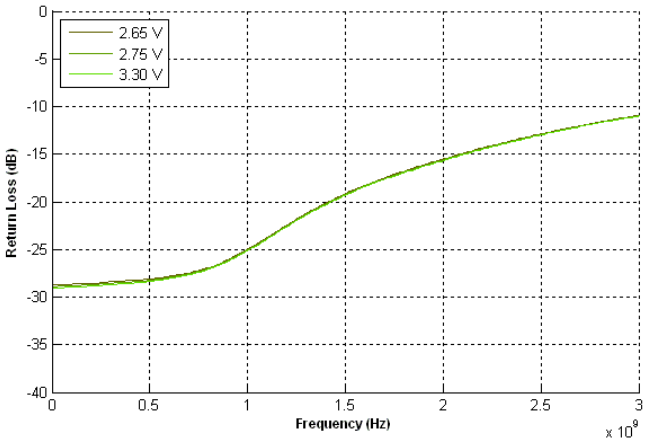


Figure 11. Return Loss at Active Port @ 2.75 V

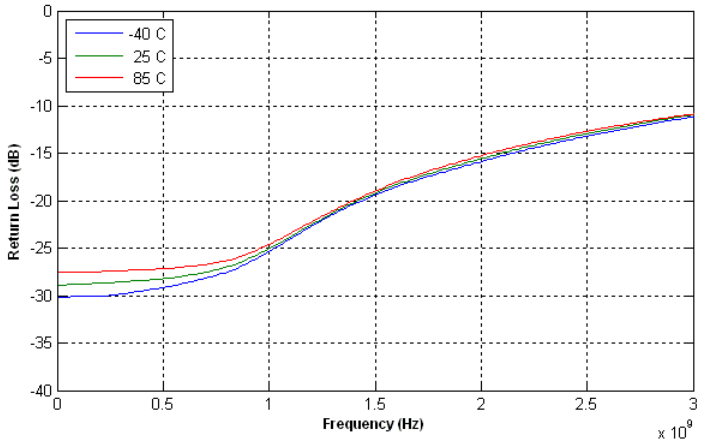


Figure 12. Maximum Operating Power vs. Frequency

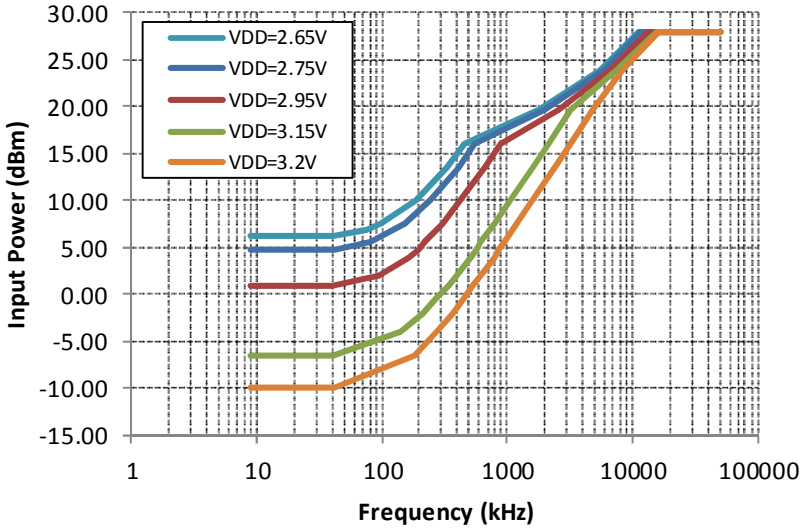


Figure 13. Package Drawing

16-lead 3 x 3 x 0.75 mm QFN

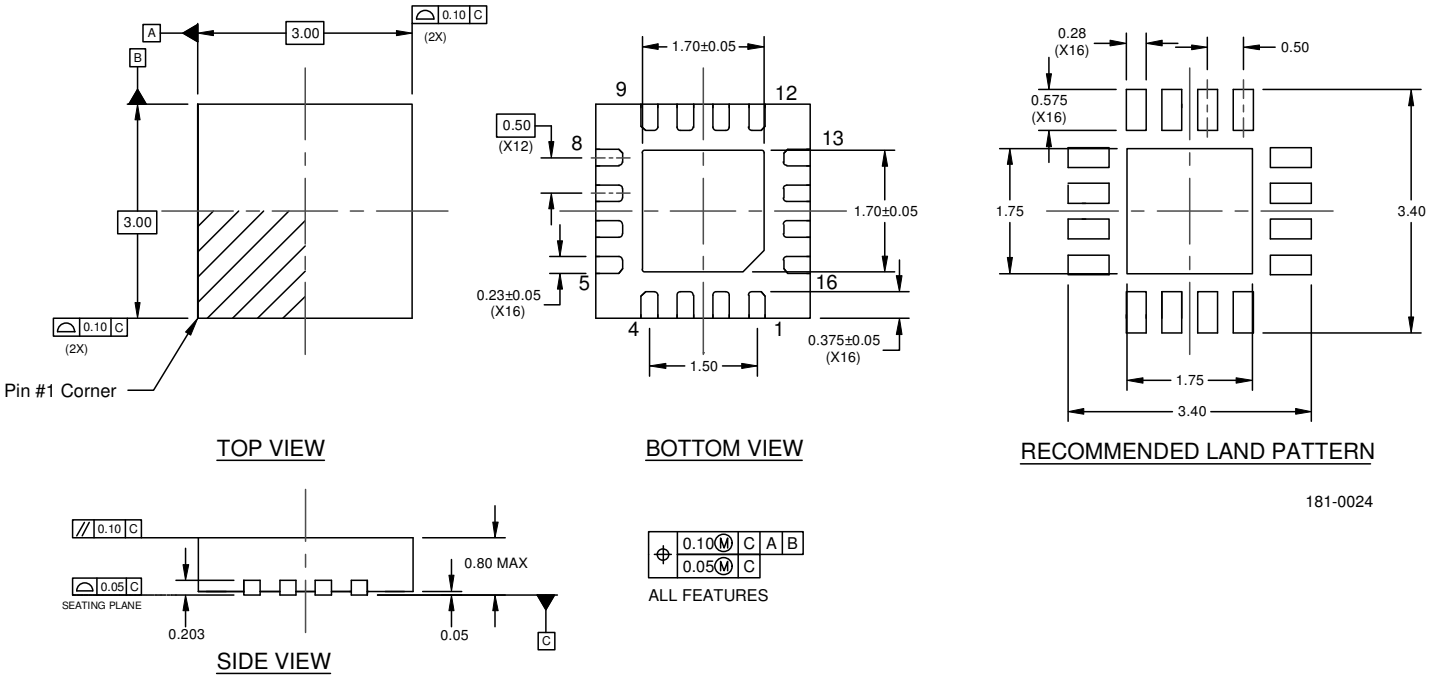


Figure 14. Marking Specifications

YYWW = Date Code
ZZZZZ = Last five digits of Lot Number

17-0009