Product Specification

PE42442

UltraCMOS® SP4T RF Switch
30 MHz–6 GHz

Product Description

The PE42442 is a HaRP™ technology-enhanced absorptive SP4T RF switch designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

This switch is a pin-compatible four throw version of the PE42451 with a wider frequency and power supply range. It is comprised of four symmetric RF ports with very high isolation up to 6 GHz. An integrated CMOS decoder facilitates a two- or three-pin 1.8V CMOS control interface. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE42442 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- Four symmetric, absorptive RF ports
- High isolation
  - 61 dB @ 900 MHz
  - 55 dB @ 2100 MHz
  - 52 dB @ 2700 MHz
  - 43 dB @ 4000 MHz
  - 32 dB @ 6000 MHz
- High linearity
  - IIP2 of 97 dBm
  - IIP3 of 58 dBm
- 1.8V control logic compatible
- 125 °C operating temperature
- Fast switching time of 255 ns
- Two- or three-pin CMOS logic control
- External negative supply option
- ESD performance
  - 4 kV HBM on RF pins to GND
  - 2 kV HBM on all pins

Figure 1. Functional Diagram

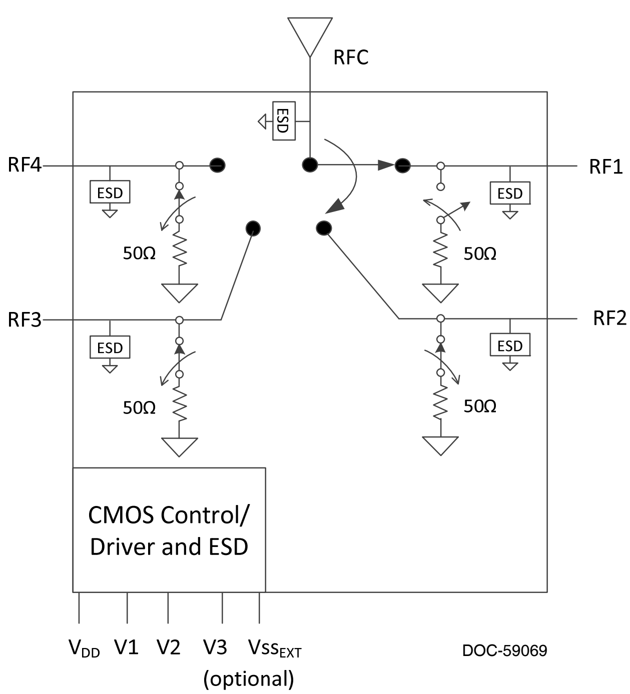


Figure 2. Package Type
24-lead 4 × 4 mm QFN

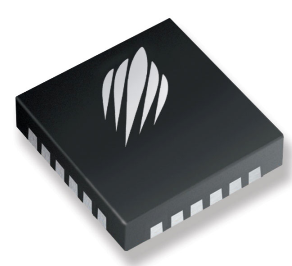


Table 1. Electrical Specifications @ +25 °C ($Z_S = Z_L = 50\Omega$) unless otherwise noted Normal mode[1]: V_{DD} = 3.3V, V_{SS_EXT} = 0V or Bypass mode[2]: V_{DD} = 3.3V, V_{SS_EXT} = –3.3V

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			30		6000	MHz
Insertion loss	RFC–RFX	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz		0.85 0.90 1.10 1.15 1.25 1.90	1.00 1.05 1.35 1.40 1.50 2.35	dB dB dB dB dB
Isolation	RFC–RFX	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz	62 55 52 50 42 27	67 61 55 52 43 32		dB dB dB dB dB
Isolation	RFX–RFX	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz	61 56 51 50 41 29	65 61 54 52 44 32		dB dB dB dB dB
Return loss (active port)	RFX	30–4000 MHz 4000–6000 MHz		17 12		dB dB
Return loss (terminated port)	RFX	30–4000 MHz 4000–6000 MHz		22 19		dB dB
Input 0.1 dB compression point[3]	RFC–RFX	900 MHz		35		dBm
Input IP2	RFC–RFX	1900 MHz		97		dBm
Input IP3	RFC–RFX	1900 MHz		58		dBm
Switching time		50% control to 90% or 10% RF		255	330	ns

Notes: 1. Normal mode: single external positive supply used.
2. Bypass mode: both external positive supply and external negative supply used.
3. The input 0.1 dB compression point is a linearity figure of merit. Refer to *Table 4* for the operating RF input power (50Ω).

Table 2. Electrical Specifications @ +125 °C ($Z_S = Z_L = 50\Omega$) unless otherwise noted Normal mode[1]: V_{DD} = 3.3V, V_{SS_EXT} = 0V or Bypass mode[2]: V_{DD} = 3.3V, V_{SS_EXT} = –3.3V

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			30		6000	MHz
Insertion loss	RFC–RFX	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz		1.11 1.18 1.43 1.50 1.59 2.28	1.38 1.45 1.79 1.95 2.04 2.91	dB dB dB dB dB dB
Isolation	RFC–RFX	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz	56 54 49 46 33 23	66 60 55 52 43 32		dB dB dB dB dB dB
Isolation	RFX–RFX	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz	59 54 50 49 39 26	65 61 53 52 43 32		dB dB dB dB dB dB
Return loss (active port)	RFX	30–4000 MHz 4000–6000 MHz		16 13		dB dB
Return loss (terminated port)	RFX	30–4000 MHz 4000–6000 MHz		17 15		dB dB
Input 0.1 dB compression point[3]	RFC–RFX	900 MHz		35		dBm
Input IP2	RFC–RFX	1900 MHz		91		dBm
Input IP3	RFC–RFX	1900 MHz		56		dBm
Switching time		50% control to 90% or 10% RF		355	439	ns

Notes: 1. Normal mode: single external positive supply used.
2. Bypass mode: both external positive supply and external negative supply used.
3. The input 0.1 dB compression point is a linearity figure of merit. Refer to *Table 4* for the operating RF input power (50Ω).

Figure 3. Pin Configuration (Top View)

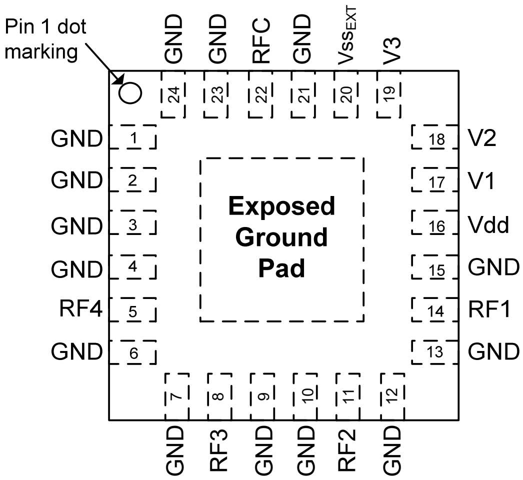


Table 3. Pin Descriptions

Pin #	Name	Description
1-3, 4, 6, 7, 9, 10, 12, 13, 15, 21, 23, 24	GND	Ground
5	RF4[1]	RF port 4
8	RF3[1]	RF port 3
11	RF2[1]	RF port 2
14	RF1[1]	RF port 1
16	V_{DD}	Supply voltage
17	V1	Digital control logic input 1
18	V2	Digital control logic input 2
19	V3[2]	Digital control logic input 3
20	V_{SS_EXT}[3]	External Vss negative voltage control/ ground
22	RFC[1]	RF common
Pad	GND	Exposed pad: Ground for proper operation

Notes: 1. RF pins 5, 8, 11, 14 and 22 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Pin 19 must be grounded for 2-pin control, refer to *Table 5A*.
3. Use V_{SS_EXT} (pin 20, refer to *Table 3*) to bypass and disable internal

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Normal mode[1]					
Supply voltage	V_{DD}	2.3		5.5	V
Supply current	I_{DD}		110		µA
Bypass mode[2]					
Supply voltage	V_{DD}	2.7		5.5	V
Supply current	I_{DD}		50		µA
Negative supply voltage	V_{SS_EXT}	–3.6		–3.2	V
Normal or Bypass mode					
Digital input high (V1, V2, V3)	V_{IH}	1.17		3.6	V
Digital input low (V1, V2, V3)	V_{IL}	–0.3		0.6	V
Digital input current[3]	I_{CTRL}			1	µA
RF input power, CW	$P_{MAX,CW}$ +105 °C			33	dBm
RF input power, CW	$P_{MAX,CW}$ +125 °C			28	dBm
RF input power into terminated ports, CW	$P_{MAX,TERM}$ +105 °C			24	dBm
RF input power into terminated ports, CW	$P_{MAX,TERM}$ +125 °C			20	dBm
Operating temperature range	T_{OP}	–40		+125	°C

Notes: 1. Normal mode: connect pin 20 to GND to enable internal negative voltage generator.
2. Bypass mode: apply a negative voltage to V_{SS_EXT} (pin 20) to bypass and disable internal negative voltage generator.
3. The pull-down resistor in the EVK schematic may increase control current.

Table 5. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	5.5	V
Voltage on any DC input	V_I	–0.3	3.6	V
Maximum input power	P_{MAX_ABS} +105 °C		34	dBm
Maximum input power	P_{MAX_ABS} +125 °C		28	dBm
Storage temperature range	T_{ST}	–65	+150	°C
ESD voltage HBM[1] All pins RF pins to ground	V_{ESD_HBM}		2.0 4.0	kV kV
ESD voltage MM[2], all pins	V_{ESD_MM}		150	V
ESD voltage CDM[3], all pins	V_{ESD_CDM}		250	V

Notes: 1. Human Body Model (MIL_STD 883 Method 3015)
2. Machine Model (JEDEC JESD22-A115)

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Switching Frequency

The PE42442 has a maximum 25 kHz switching rate in normal mode (pin 20 = GND). A faster switching rate is available in bypass mode (pin 20 = V_{SS_EXT}). The rate at which the PE42442 can be switched is then limited to the switching time as specified in *Table 1*.

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42442 in the 24-lead 4 × 4 mm QFN package is MSL1.

Table 6. Truth Table (3-pin control)*

Mode	V3	V2	V1
Unsupported	0	0	0
RF1 on	0	0	1
RF2 on	0	1	0
RF3 on	0	1	1
RF4 on	1	0	0
All off	1	0	1
All off	1	1	0
Unsupported	1	1	1

Note: * 3-pin control intended for legacy product support to PE42450 and PE42451 or if All Off mode is required. Logic States 000 and 111 are unsupported and should not be used under any operating conditions.

Table 6A. Truth Table (2-pin control[1])[2]

Mode	V2	V1
RF4 on	0	0
RF1 on	0	1
RF2 on	1	0
RF3 on	1	1

Notes: 1. Pin 19 = V3 must be grounded.
2. 2-pin control is recommended for new product designs if All Off mode is not required.

Optional External V_{SS} Control (V_{SS_EXT})

For applications the require a faster switching rate or spur-free performance, this part can be operated in bypass mode. Bypass mode requires an external negative voltage in addition to an external V_{DD} supply voltage.

As specified in *Table 3*, the external negative voltage (V_{SS_EXT}) when applied to pin 20 will disable and bypass the internal negative voltage

Spurious Performance

The typical low-frequency spurious performance of the PE42442 in normal mode is –120 dBm (pin 20 = GND). If spur-free performance is desired, the internal negative voltage generator can be disabled by applying a negative voltage to V_{SS_EXT} (pin 20).

Typical Performance Data @ 25 °C and V_{DD} = 3.3V unless otherwise noted

Figure 4. Insertion Loss (All Paths)

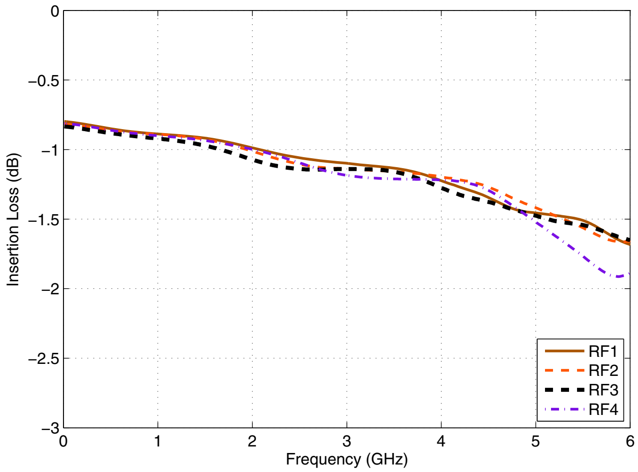


Figure 5. Insertion Loss vs Temp (RFC–RFX)

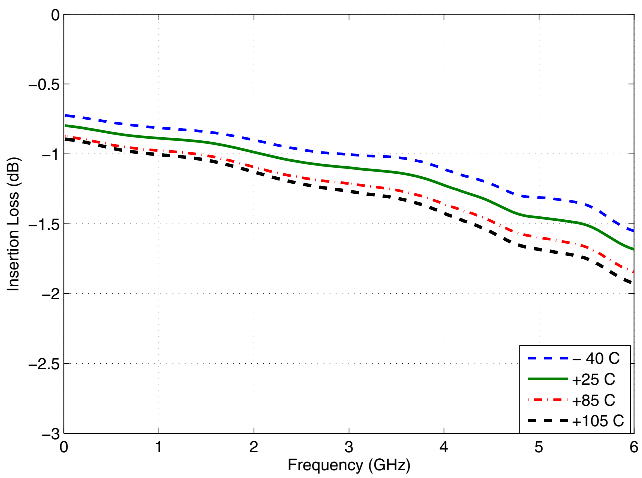
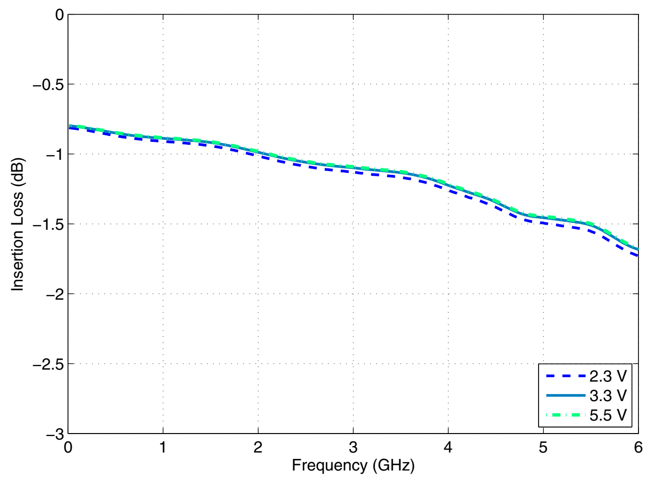


Figure 6. Insertion Loss vs V_{DD} (RFC–RFX)



Typical Performance Data @ 25 °C and V_{DD} = 3.3V unless otherwise noted

Figure 7. Isolation vs Temp (RFC–RFX)

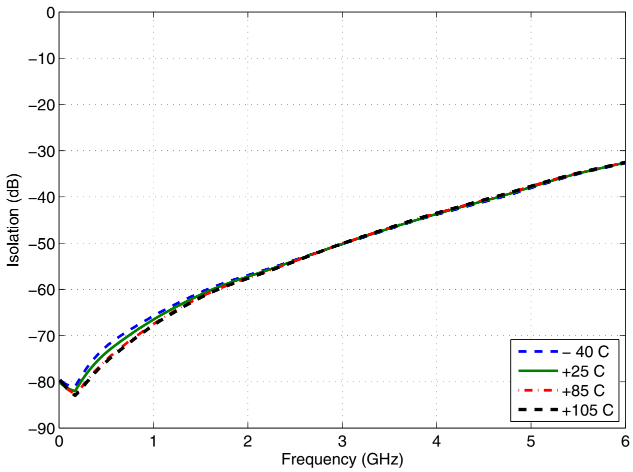


Figure 8. Isolation vs V_{DD} (RFC–RFX)

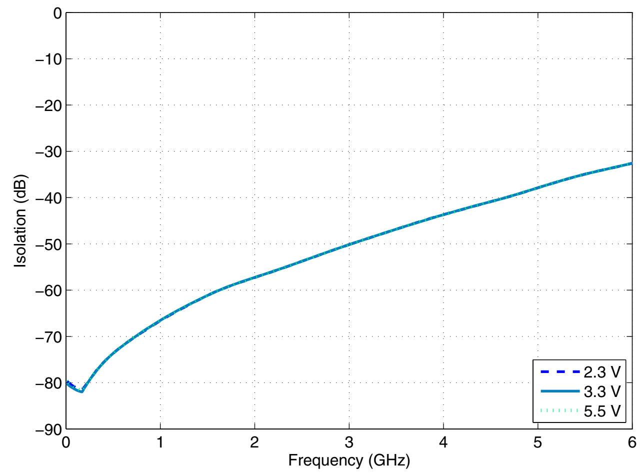


Figure 9. Isolation vs Temp (RFX–RFX)

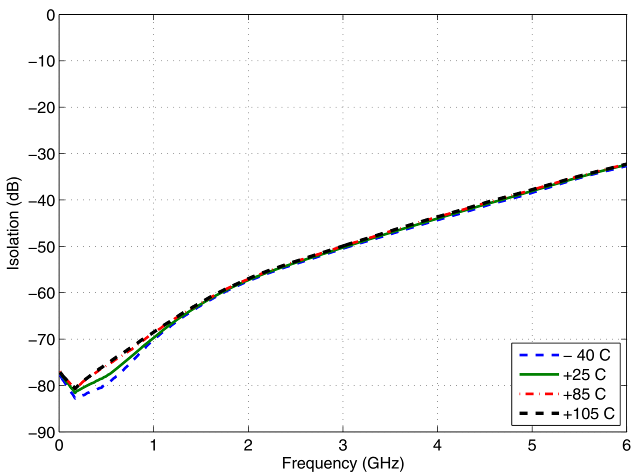
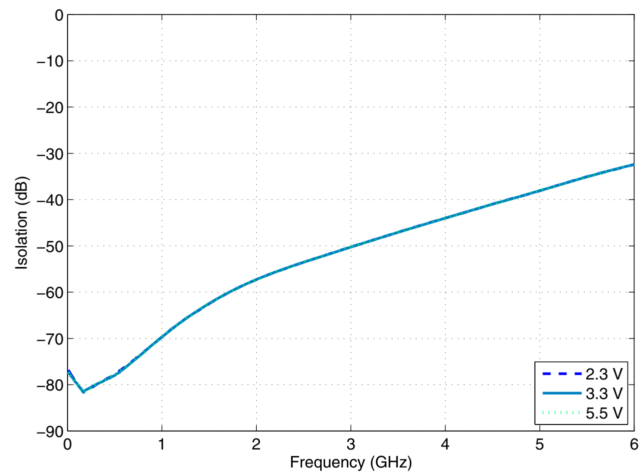


Figure 10. Isolation vs V_{DD} (RFX–RFX)



Typical Performance Data @ 25 °C and V_{DD} = 3.3V unless otherwise noted

Figure 11. Active Port Return Loss vs Temp

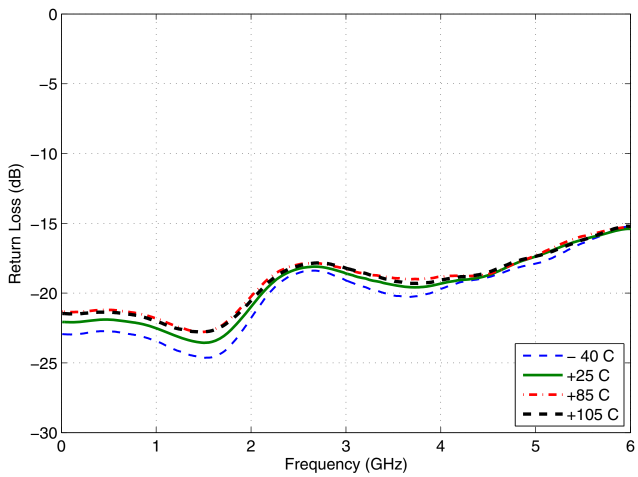


Figure 12. Active Port Return Loss vs V_{DD}

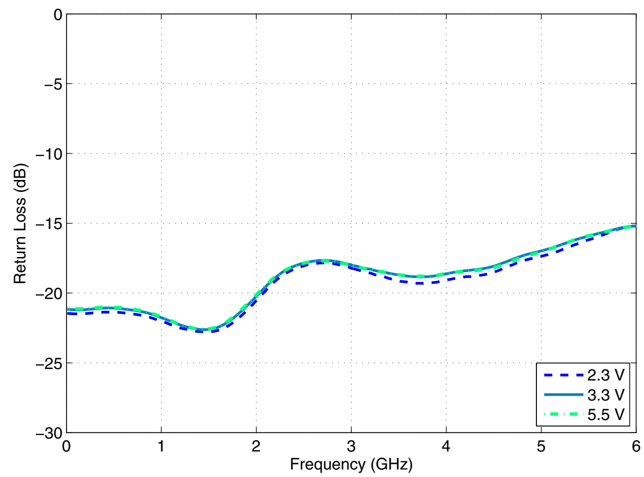


Figure 13. RFC Port Return Loss vs Temp

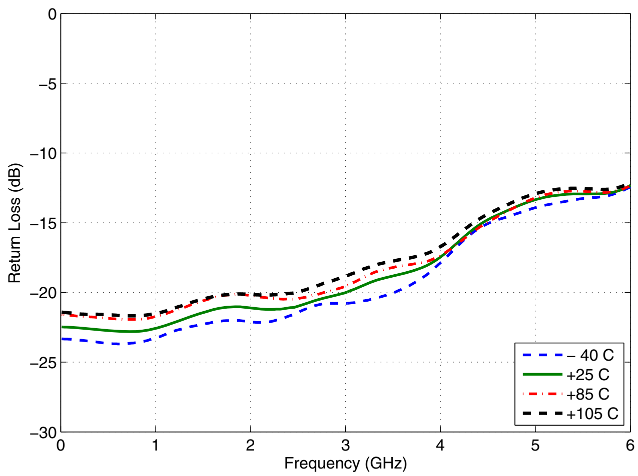


Figure 14. RFC Port Return Loss vs V_{DD}

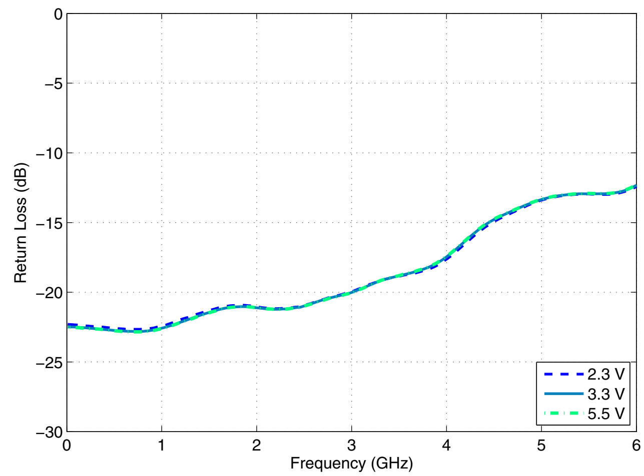


Figure 15. Return Loss (All Ports Terminated)

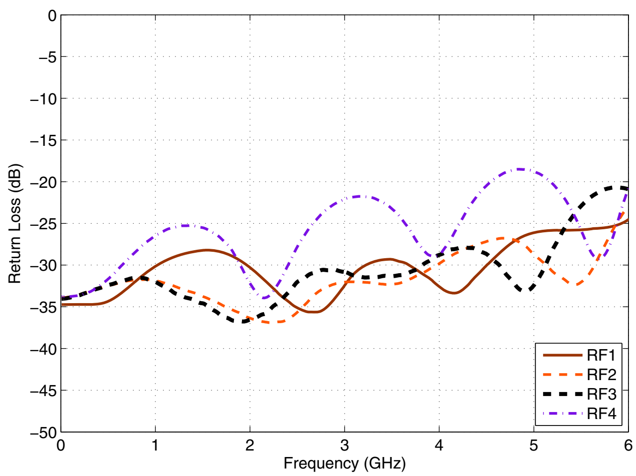
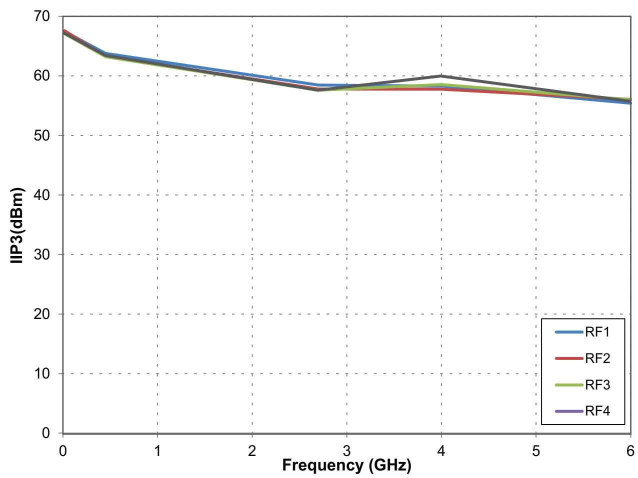


Figure 16. IIP3 vs Frequency



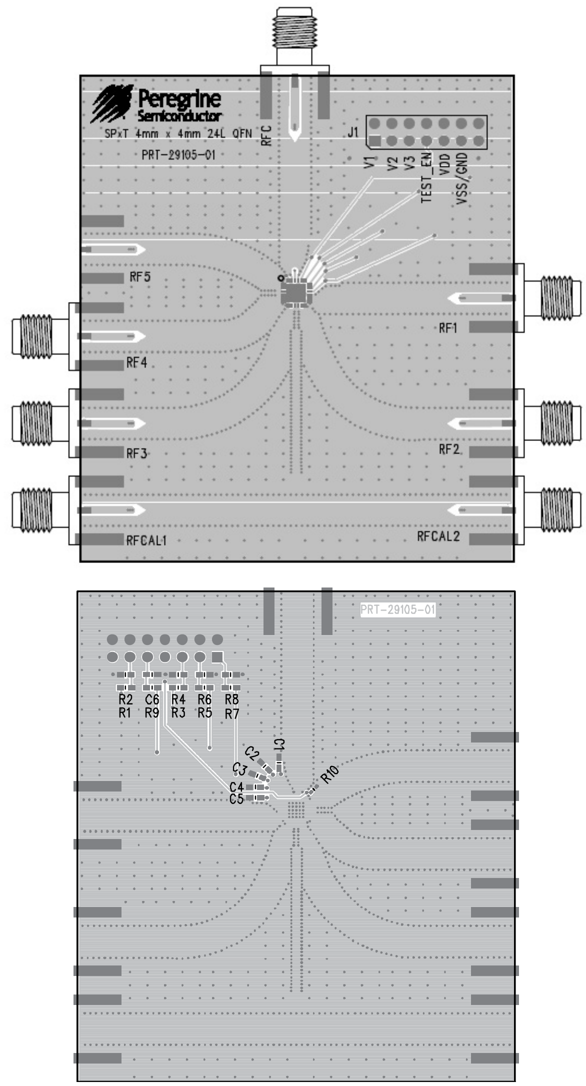
Evaluation Kit

The SP4T switch Evaluation Board was designed to ease customer evaluation of pSemi's PE42442. The RF common port is connected through a 50Ω transmission line via the top SMA connector. RF1, RF2, RF3, and RF4 are connected through 50Ω transmission lines via side SMA connectors. A through 50Ω transmission is available via SMA connectors RFCAL1 and RFCAL2. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The EVK board is constructed with four metal layers on dielectric materials of Rogers 4003C and 4450 with a total thickness of 32 mils. Layer 1 and layer 3 provide ground for the 50Ω transmission lines. The 50Ω transmission lines are designed in layer 2 for high isolation purpose and use a stripline waveguide design with a trace width of 9.4 mils and trace metal thickness of 1.8 mils. The board stack up for 50Ω transmission lines has 8 mil thickness of Rogers 4003C between layer 1 and layer 2, and 10 mil thickness of Rogers 4450 between layer 2 and layer 3.

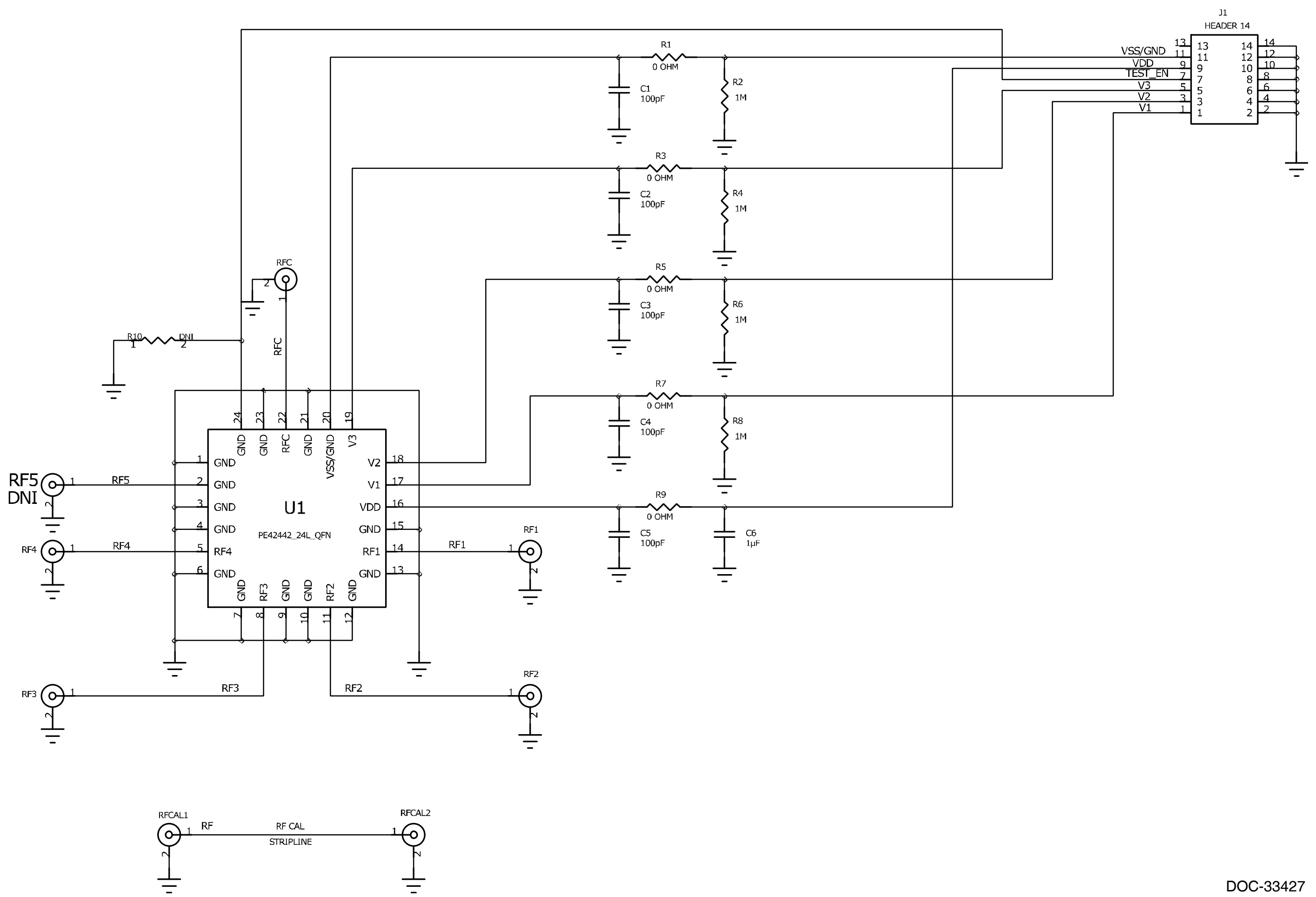
Please consult manufacturer's guidelines for proper board material properties in your application. The PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces such as V_{SS_EXT} are heavily isolated from one another, otherwise the true performance of the PE42442 will not be yielded.

Figure 17. Evaluation Board Layout



DOC-59282

Figure 18. Evaluation Board Schematic



DOC-33427

Figure 19. Package Drawing
24-lead 4 × 4 mm QFN

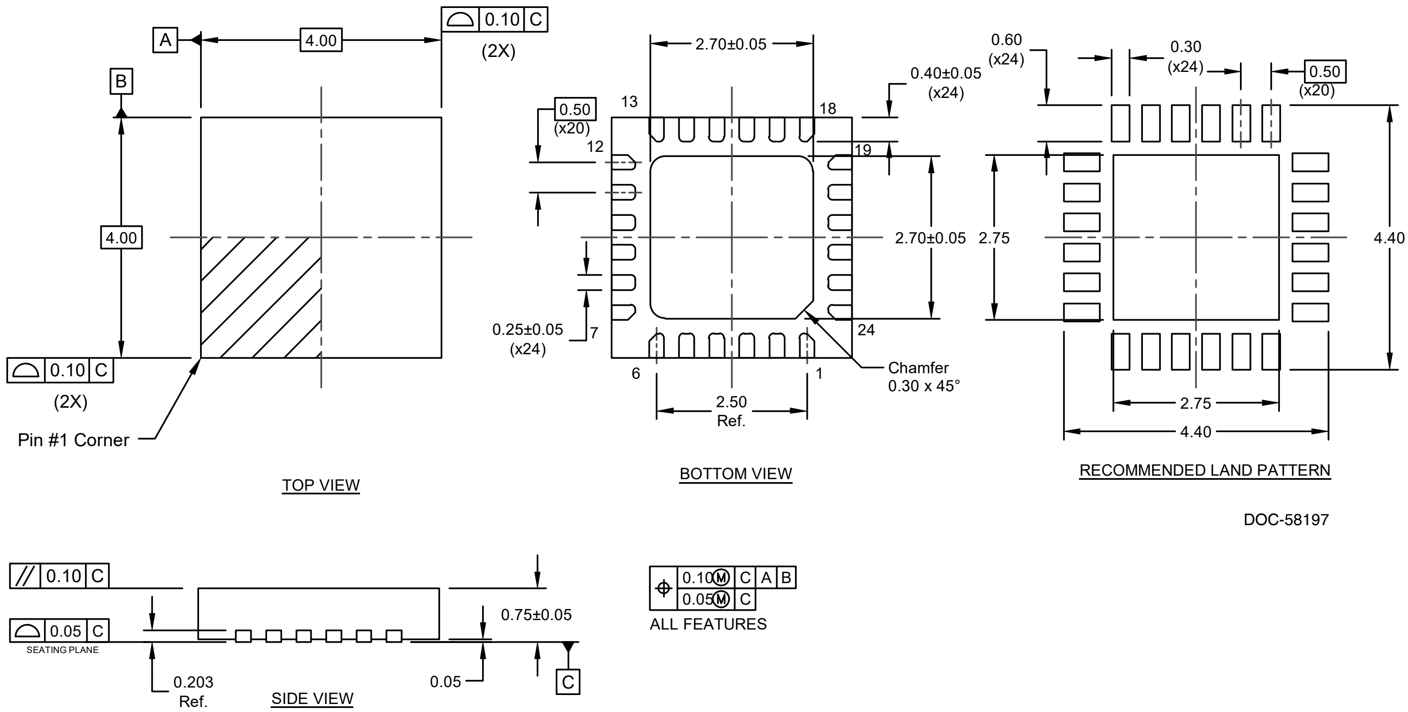
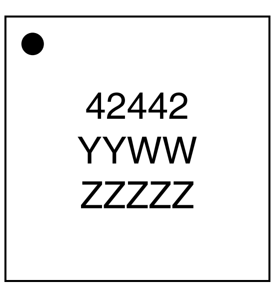


Figure 20. Marking Specifications



DOC-51207

● = Pin 1 designator
YYWW = Date code
ZZZZZ = Las five digits of the lot number