Product Specification

PE4256

75 Ω SPDT CATV UltraCMOS® Switch
5 MHz–3 GHz

Features

- 75Ω characteristic impedance
- Integrated 75Ω terminations
- CTB performance of –90 dBc
- High isolation 65 dB at 1000 MHz
- Low insertion loss: typically 0.5 dB at 5 MHz, 0.9 dB at 1000 MHz
- High input IP3: >50 dBm
- CMOS two-pin control
- Single +3 volt supply operation
- Low current consumption: 8 µA
- Unique all off terminated mode
- 4 x 4 mm QFN package

Product Description

The PE4256 is an UltraCMOS® Switch designed for CATV applications, covering a broad frequency range from 5 MHz up to 3 GHz. This single-supply SPDT switch integrates a two-pin CMOS control interface. It also provides low insertion loss with extremely low bias requirements while operating on a single 3-volt supply. In a typical CATV application, the PE4256 provides for a cost effective and manufacturable solution when compared to mechanical relays.

The PE4256 is manufactured on Peregrine's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

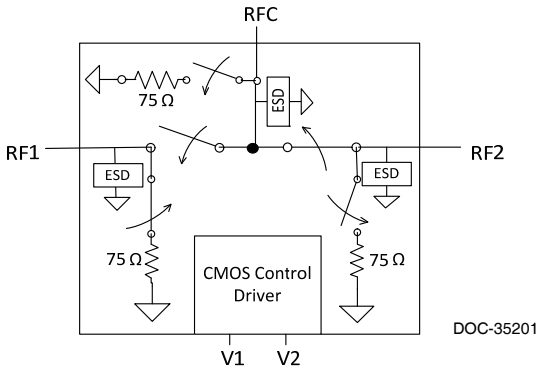


Figure 2. Package Type

20-lead 4 x 4 mm QFN

Table 1. Electrical Specifications @ +25 °C, V_{DD} = +3V (Z_S = Z_L = 75Ω)

Parameter	Condition	Minimum	Typical	Maximum	Units
Operating Frequency[1]		5		3000	MHz
Insertion Loss	5–250 MHz 250–750 MHz 750–1000 MHz 1000–2200 MHz		0.5 0.8 0.9 1.1	0.6 0.95 1.1 1.3	dB
Isolation	5–250 MHz 250–750 MHz 750–1000 MHz 1000–2200 MHz	75 65 62 49	80 70 65 52		dB
Input IP2[2]	5–1000 MHz		80		dBm
Input IP3[2]	5–1000 MHz	50	55		dBm
Input 1dB Compression[2]	1000 MHz	29	31		dBm
CTB / CSO	77 & 110 channels; Power Out = 44 dBm V		–90		dBc
Switching Time	50% CTRL to 10/90% RF		2		µs
Video Feedthrough[3]	51000 MHz			15	mV_{pp}

Notes: 1. Device linearity will begin to degrade below 5 MHz.
2. Measured in a 50Ω system.
3. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth.

Figure 3. Pin Configuration (Top View)

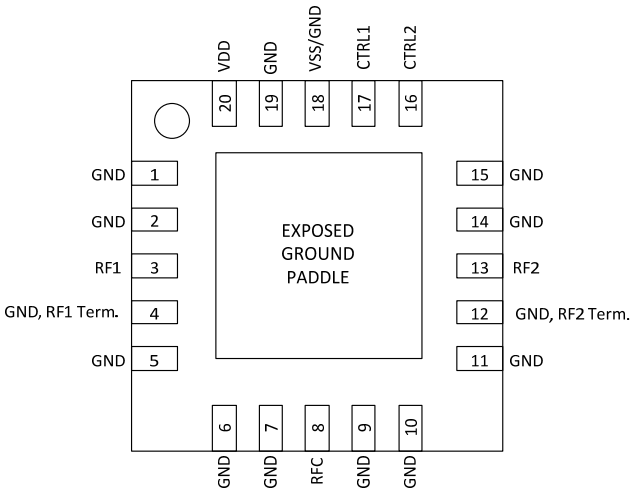


Table 2. Pin Descriptions

No.	Name	Description
1	GND	Ground
2	GND	Ground
3[1]	RF1	RF I/O
4[4]	GND	Ground
5	GND	Ground
6	GND	Ground
7[4]	GND	Ground
8[1]	RFC	Common
9[4]	GND	Ground
10	GND	Ground
11	GND	Ground
12[4]	GND	Ground
13[1]	RF2	RF I/O
14	GND	Ground
15	GND	Ground
16[2]	C2	Control 2
17[2]	C1	Control 1
18[3]	VSS/GND	Negative Supply Option
19	GND	Ground
20	VDD	Supply
Paddle	GND	Exposed Ground Paddle

Notes: 1. RF pins 3, 8, and 13 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Pins 16 and 17 are the CMOS controls that set the three operating states.
3. Connect pin 18 to GND to enable the on-chip negative voltage generator. Connect pin 18 to V_{SS} (–3V) to bypass and disable internal -3V supply generator.
4. Customer can add external resistance to ground to change or modify termination resistance.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on CTRL input	-0.3	V_{DD} + 0.3	V
P_{RF}	RF CW power		24	dBm
T_{ST}	Storage temperature	–65	150	° C
T_{OP}	Operating temperature	–40	85	° C
V_{ESD}	ESD voltage (Human Body Model)		1000	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. DC Electrical Specifications @ 25 °C

Parameter	Min	Typ	Max	Unit
V_{DD} Power Supply	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CNTL} = 3V)		8	20	µA
Control Voltage High	70% V_{DD}			V
Control Voltage Low			30% V_{DD}	V

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE4256 in the 20-lead 4 x 4 mm QFN package is MSL1.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Switching Frequency

The PE4256 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 18 = GND).

Table 5. RF Path Truth Table

C1	C2	RFC – RF1	RFC – RF2
Low	Low	OFF	OFF
Low	High	OFF	ON
High	Low	ON	OFF
High	High	N/A[1]	N/A[1]

Table 6. Termination Truth Table

C1	C2	RFC – 75 Ω	RF1 – 75 Ω	RF2 – 75 Ω
Low	Low	X[2]	X[2]	X[2]
Low	High		X[2]	
High	Low			X[2]
High	High	N/A[1]	N/A[1]	N/A[1]

Notes: 1. The operation of the PE4256 is not supported or characterized in the C1 = V_{DD} and C2 = V_{DD} state.
2. "X" denotes termination enabled.

Evaluation Kit

The SPDT Switch Evaluation Kit was designed to ease customer evaluation of the PE4256 SPDT switch. The RF common port (RFC) is connected through a 75 Ω transmission line to J2. Port 1 and Port 2 are connected through 75 Ω transmission lines to J1 and J3. A through transmission line connects F connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed with four metal layers in FR4 material with a total thickness of 0.062". The transmission lines were designed using a coplanar waveguide with ground plane (28 mil core, 21 mil width, 30 mil gap).

J6 provides a means for controlling DC and digital inputs to the device. The provided jumpers short the package pin to ground for logic low. When the jumper is removed, the pin is pulled up to V_{DD} for logic high.

When the jumper is in place, 3 µA of current will flow through the 1 MΩ pull-up resistor. This extra current should not be attributed to the device.

Proper PCB design is essential for full isolation performance. This evaluation board demonstrates good trace and ground management for minimum coupling and radiation.

Figure 4. Evaluation Board Layouts

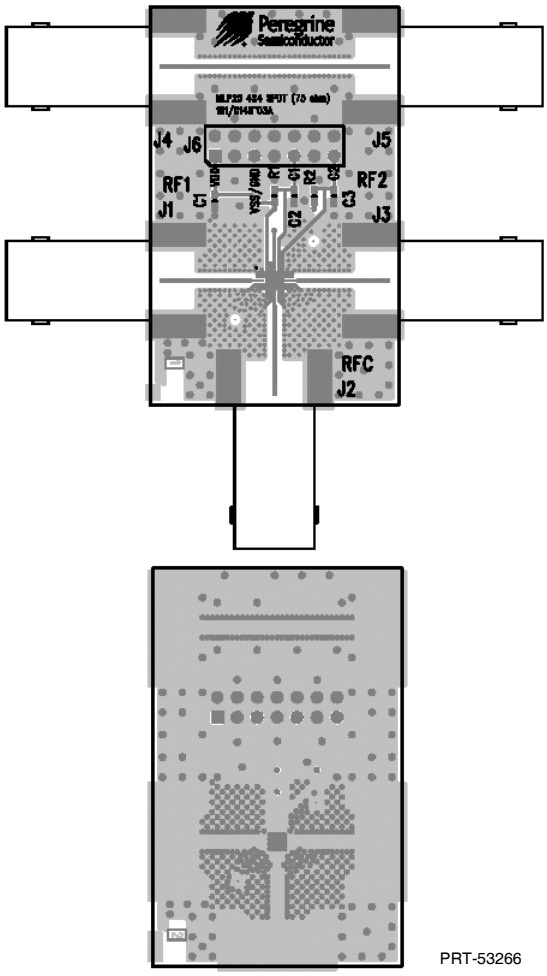
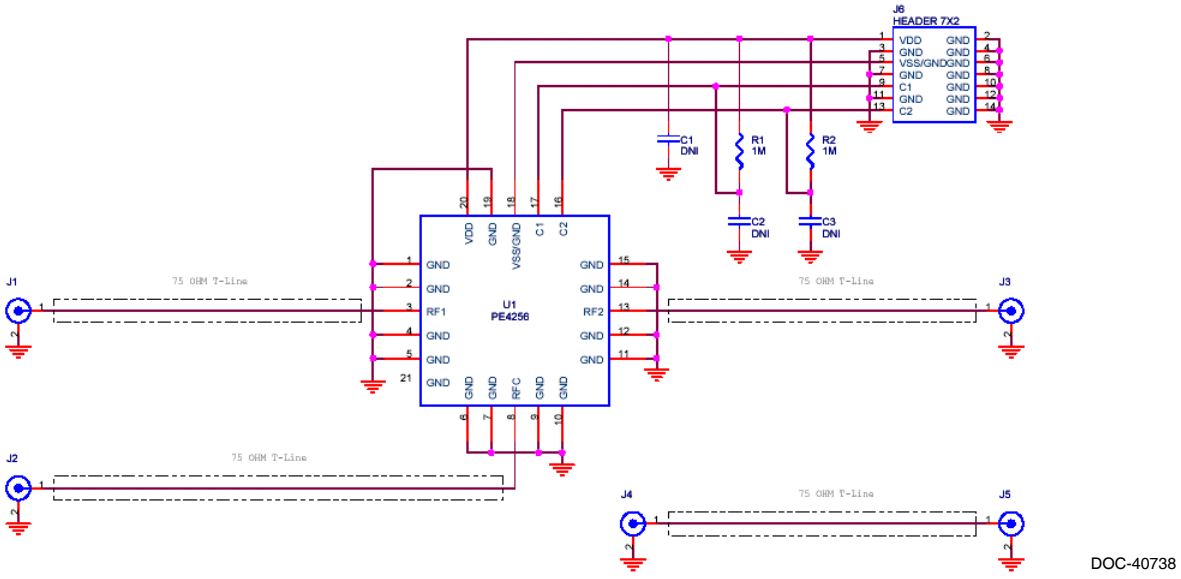


Figure 5. Evaluation Board Schematic



Typical Performance Data from –40 °C to +85 °C, 75Ω Impedance

Figure 6. Insertion Loss (RFC to RF1 or RF2)

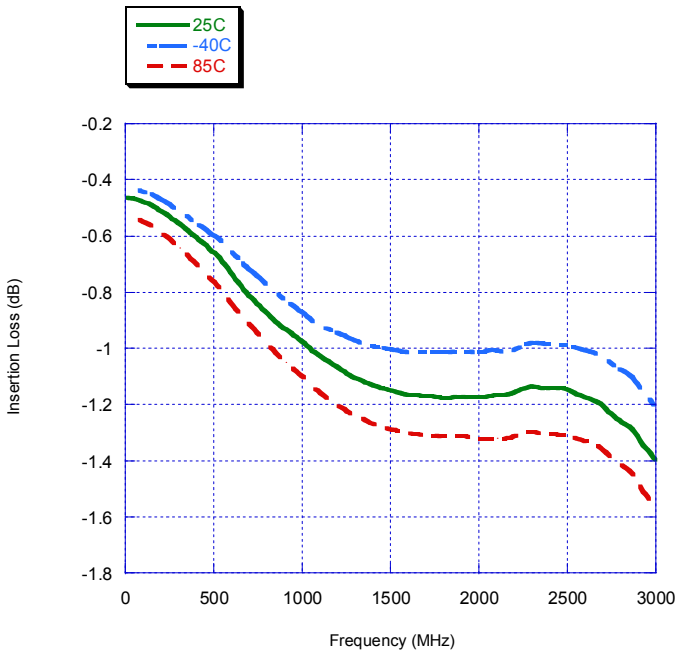


Figure 7. Input to Output Isolation (Closed)

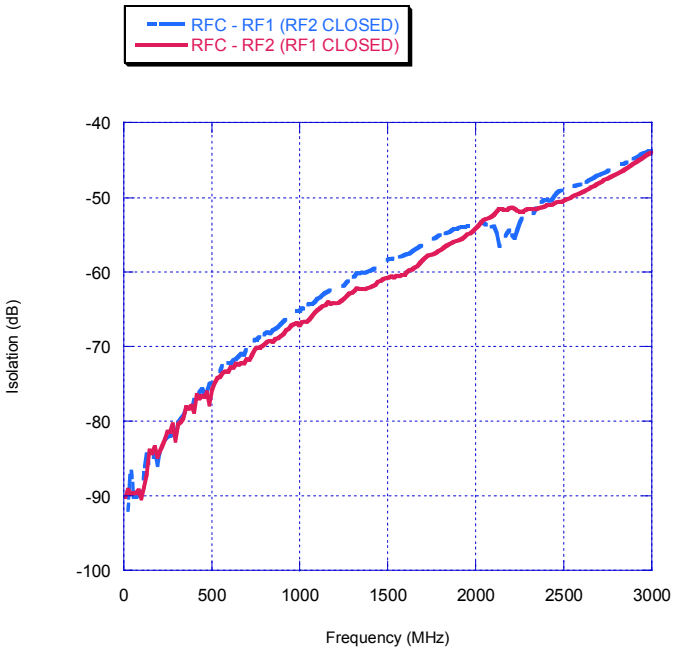


Figure 8. Input to Output Isolation (Open)

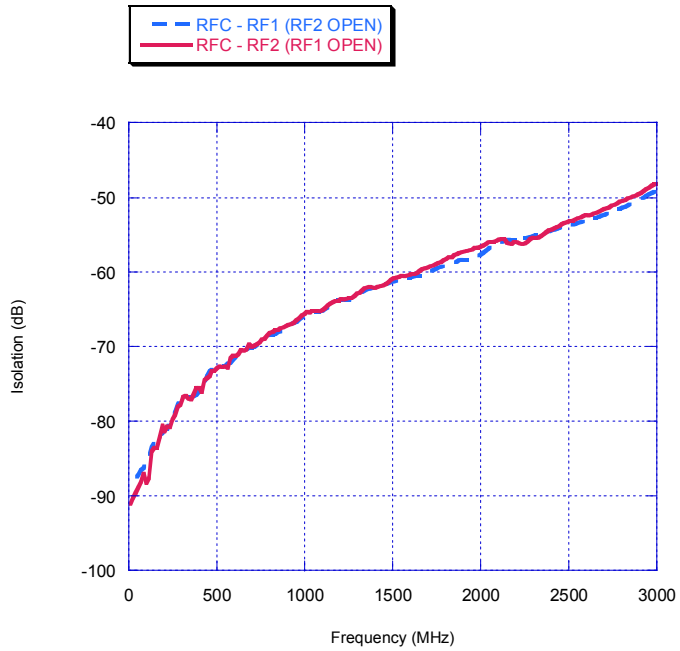
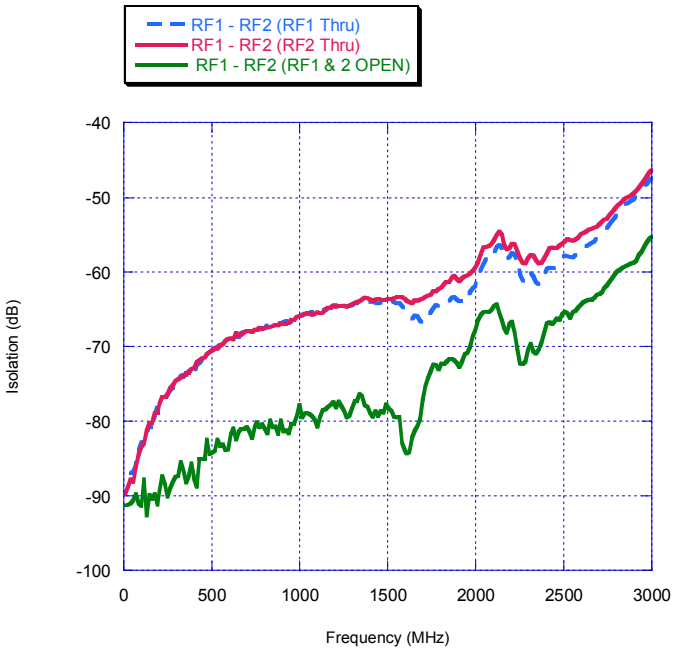


Figure 9. Isolation – RF1 To RF2



Typical Performance Data @ +25 °C, 75Ω Impedance (unless otherwise noted)

Figure 10. RFC Return Loss

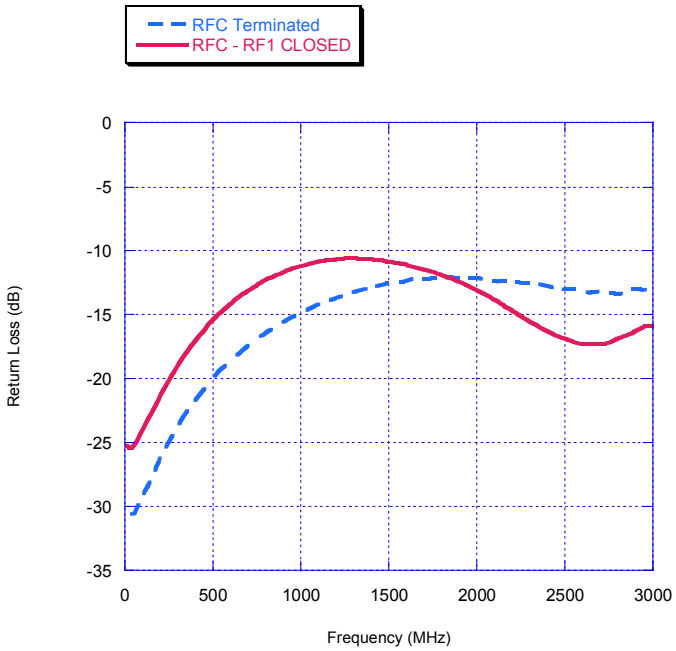


Figure 11. RF1 Return Loss

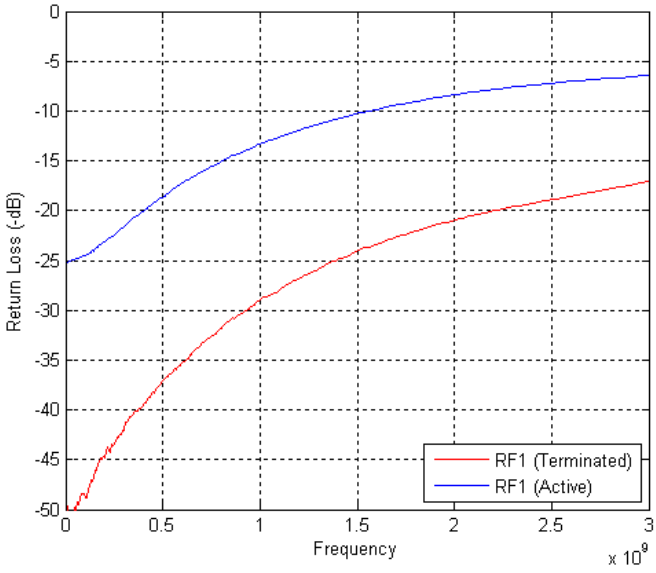


Figure 12. RF2 Return Loss

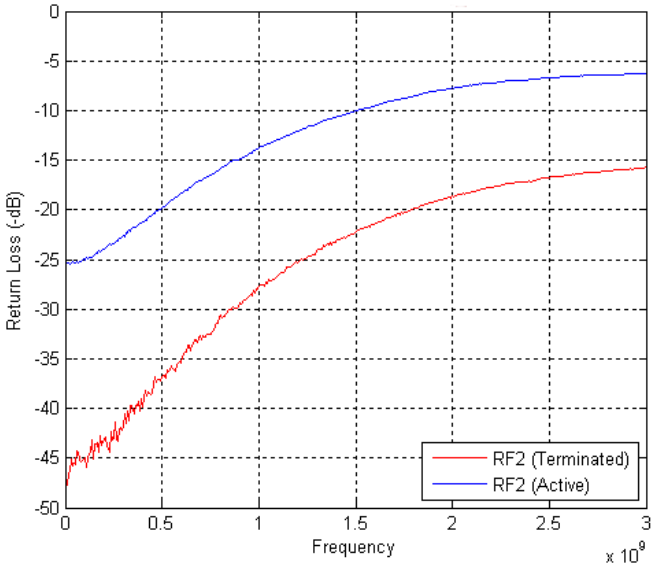


Figure 13. Linearity (50Ω System Impedance)

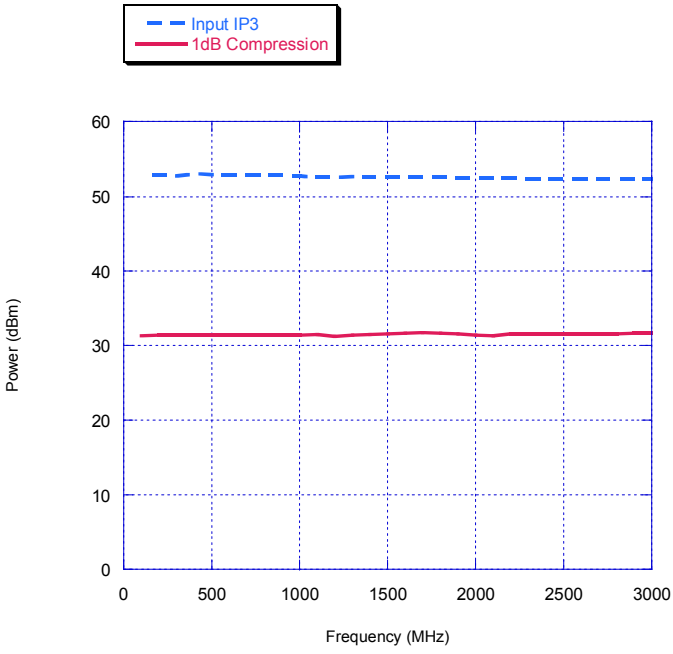


Figure 14. Package Drawing (mm)

20-lead 4 x 4 mm QFN

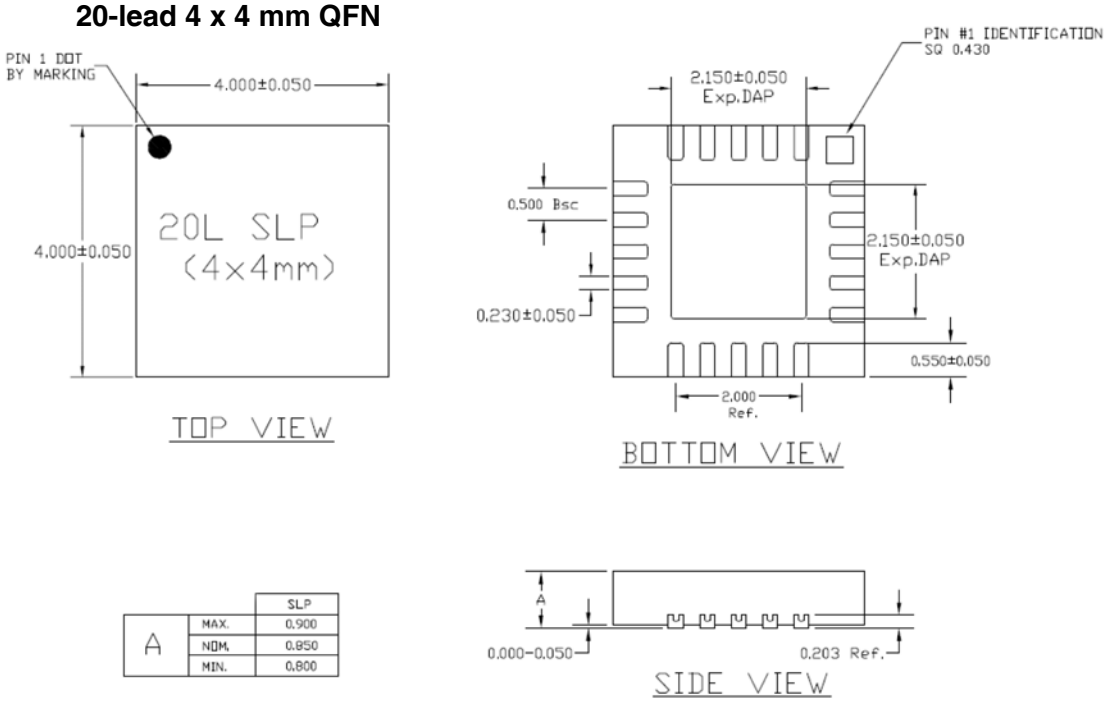
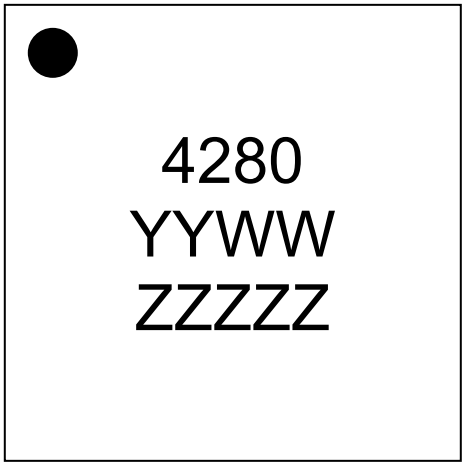


Figure 15. Marking Specifications



YYWW = Date Code
ZZZZZ = Last five digits of PSC Lot Number