Product Specification

PE42851

UltraCMOS® SP5T RF Switch 100–1000 MHz

Features

- Dual mode operation: SP5T or SP3T
- HaRP™ technology enhanced
  - Fast settling time
  - No gate and phase lag
  - No drift in insertion loss and phase
- Up to 45 dBm instantaneous power in 50Ω
- Up to 40 dBm instantaneous power < 8:1 VSWR
- 36 dB TX to RX isolation
- Low harmonics of $2f_o$ and $3f_o$ = –80 dBc (1.15:1 VSWR)
- ESD performance
  - 1.5 kV HBM on all pins

Product Description

The PE42851 is a HaRP™ technology-enhanced SP5T high power RF switch supporting wireless applications up to 1 GHz. It offers maximum power handling of 42.5 dBm continuous wave (CW). It delivers high linearity and excellent harmonics performance. It has both a standard and attenuated RX mode. No blocking capacitors are required if DC voltage is not present on the RF ports.

The PE42851 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Package Type

32-lead 5 × 5 mm QFN

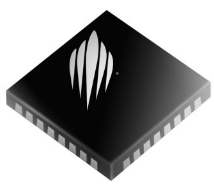
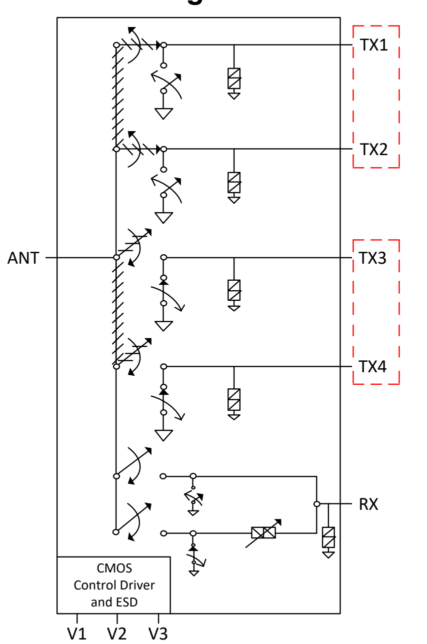
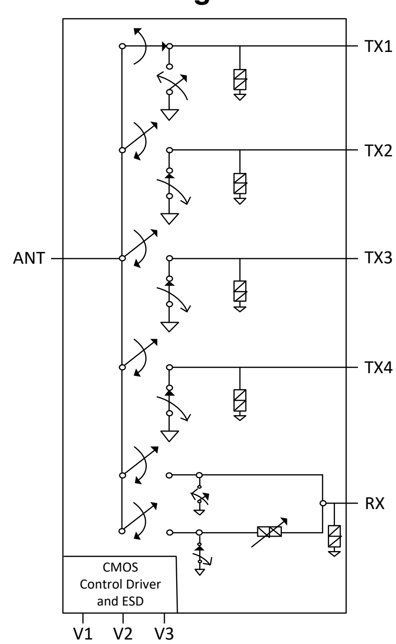


Figure 2. Functional Diagram of SP3T Configuration



ANT can be tied to TX1 and TX2 or TX3 and TX4

Figure 3. Functional Diagram of SP5T Configuration



SP5T, standard configuration

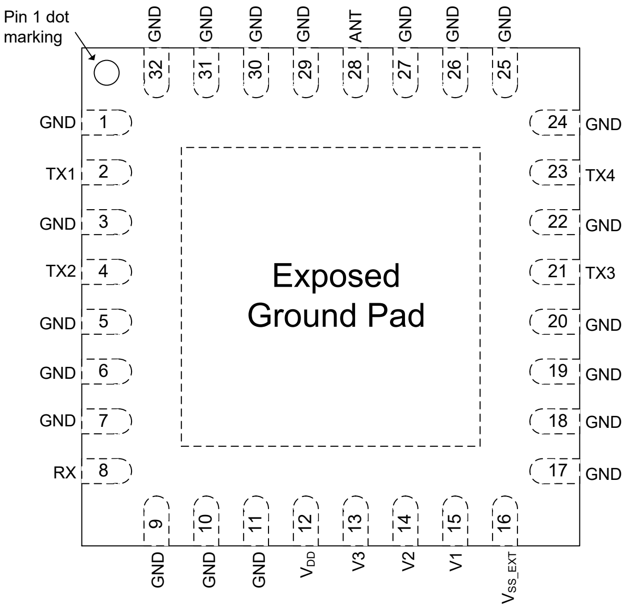
DOC-02178

Table 1. Electrical Specifications @ –40 to +85 °C, V_{DD} = 2.3–5.5V, V_{SS_EXT} = 0V or V_{DD} = 3.4–5.5V, V_{SS_EXT} = –3.4V (Z_S = Z_L = 50Ω), unless otherwise noted[1]

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			100		1000	MHz
Insertion loss[2]	ANT–TX	Active TX port 1, 2, 3 or 4 @ rated power (–40 °C, +25 °C) 100–520 MHz 520–1000 MHz		 0.25 0.40	 0.35 0.55	 dB dB
		Active TX port 1, 2, 3 or 4 @ rated power (+85 °C) 100–520 MHz 520–1000 MHz		 0.30 0.50	 0.40 0.60	 dB dB
Insertion loss[2] (un-attenuated state)	ANT–RX	Active RX port (–40 °C, +25 °C) 100–520 MHz 520–1000 MHz		 0.60 0.70	 0.70 0.90	 dB dB
		Active RX port (+85 °C) 100–520 MHz 520–1000 MHz		 0.70 0.80	 0.80 1.00	 dB dB
		1575 MHz for GPS RX, < –10 dBm, +25 °C		1.2	1.3	dB
Insertion loss[2] (attenuated state)	ANT–RX	Active RX port 100–1000 MHz	15.2	16	16.8	dB
Isolation (supply biased)	TX–TX	100–520 MHz 520–1000 MHz	33 29	36 30		dB dB
Isolation (supply biased)	TX–RX	100–520 MHz 520–1000 MHz	34 29	36 30		dB dB
Unbiased isolation V_{DD}, V1, V2, V3 = 0V	ANT–TX	+27 dBm	6			dB
Unbiased isolation V_{DD}, V1, V2, V3 = 0V	ANT–RX	+27 dBm	14			dB
Return loss[2]	ANT–RX	Un-attenuated state 100–520 MHz 520–1000 MHz	 22 18	 27 22		 dB dB
		Un-attenuated state, 1575 MHz for GPS RX, < –10 dBm, +25 °C	10	14		dB
		Attenuated state, optimized without attenuator engaged 100–520 MHz 520–1000 MHz	 16 13	 21 18		 dB dB
Return loss[2]	ANT–TX	100–520 MHz 520–1000 MHz	21 15	28 17		dB dB
2nd and 3rd harmonic (< 1.15:1 VSWR)	TX	100–520 MHz @ +40.0 dBm 521–870 MHz @ +38.5 dBm 871–1000 MHz @ +37.5 dBm		–80	–78	dBc
2nd and 3rd harmonic (< 8:1 VSWR)	TX	100–520 MHz @ +40.0 dBm (pulsed signal, at 10% duty cycle[3]) 521–870 MHz @ +38.5 dBm (pulsed signal, at 10% duty cycle[3]) 871–1000 MHz @ +37.5 dBm (pulsed signal, at 10% duty cycle[3])		–76	–70	dBc
2nd and 3rd harmonic (50Ω source/load impedance)	TX	100–1000 MHz @ +45.0 dBm (pulsed signal, at 10% duty cycle[3])		–76	–70	dBc
2nd and 3rd harmonic (50Ω source/load impedance)	TX	100–1000 MHz @ +42.5 dBm (CW)		–78	–74	dBc
Input 0.1dB compression point[5]	ANT–TX	1000 MHz		45.5		dBm
IIP3	RX	Un-attenuated state Attenuated state	42 38			dBm dBm
Settling time		From 50% control until harmonics within specifications		15		µs
Switching time in normal mode[4] (V_{SS_EXT} = 0V)		50% CTRL to 90% or 10% of RF		6		µs
Switching time in bypass mode[4] (V_{SS_EXT} = –3.4V)		50% CTRL to 90% or 10% of RF		4		µs

Notes: 1. In a 2TX–1RX SP3T configuration, TX1 and TX2 are tied and TX3 and TX4 are tied respectively. Refer to Application Note AN35 for SP3T performance data.
2. Narrow trace widths are used near each port to improve impedance matching. Refer to evaluation board layouts (*Figure 23*) and schematic (*Figure 24*) for details.
3. 10% of 4620 µs period.
4. Normal mode: connect V_{SS_EXT} (pin 16) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator. Bypass mode: use V_{SS_EXT} (pin 16) to bypass and disable internal negative voltage generator.
5. The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 3* for the RF input power P_{IN}.

Figure 4. Pin Configuration (Top View)*



Note: * Pins 1, 3, 5, 7, 9, 10, 17, 19, 20, 22, 24, 26, 27, 29, 30 and 31 can be N/C if deemed necessary by the customer

Table 2. Pin Descriptions

Pin #	Pin Name	Description
1, 3, 5–7, 9–11, 17–20, 22, 24–27, 29–32	GND	Ground
2	TX1[2]	Transmit pin 1
4	TX2[1,2]	Transmit pin 2
8	RX[2]	Receive pin
12	V_{DD}	Supply voltage (nominal 3.3V)
13	V3	Digital control logic input 3
14	V2	Digital control logic input 2
15	V1	Digital control logic input 1
16	V_{SS_EXT}[3]	External V_{SS} negative voltage control
21	TX3[2]	Transmit pin 3
23	TX4[1,2]	Transmit pin 4
28	ANT[2]	Antenna pin
Pad	GND	Exposed pad: ground for proper operation

Notes: 1. To operate the part as a 2TX–1RX SP3T, tie TX1 to TX2 and TX3 to TX4 respectively. Refer to Application Note AN35 for SP3T performance data.
2. RF pins 2, 4, 8, 21, 23 and 28 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
3. Use V_{SS_EXT} (pin 16) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 16) to GND (V_{SS_EXT} = 0V) to enable

Table 3. Operating Ranges[1]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage (normal mode, V_{SS_EXT} = 0V)	V_{DD}	2.3		5.5	V
Supply voltage (bypass mode, V_{SS_EXT} = –3.4V, $V_{DD} \geq$ 3.4V for full spec. compliance)	V_{DD}	2.7	3.4	5.5	V
Negative supply voltage (bypass mode)	V_{SS_EXT}	–3.6		–3.2	V
Supply current (normal mode, V_{SS_EXT} = 0V)	I_{DD}		130	200	µA
Supply current (bypass mode, V_{SS_EXT} = –3.4V)	I_{DD}		50	80	µA
Negative supply current (bypass mode, V_{SS_EXT} = –3.4V)	I_{SS}	–40	–16		µA
Digital input high (V1, V2, V3)	V_{IH}	1.17		3.6	V
Digital input low (V1, V2, V3)	V_{IL}	–0.3		0.6	V
TX RF input power[2,3]	P_{IN-TX}			40	dBm
TX RF input power[2,3] (50Ω source/load	P_{IN-TX}			45	dBm
TX RF input power[2] (50Ω source/load	P_{IN-TX}			42.5	dBm
ANT RF input power,	P_{IN-ANT}			27	dBm
RX RF input power[2]	P_{IN-RX}			27	dBm
Operating temperature range (case)	T_{OP}	–40		85	°C
Operating junction temperature	T_j			135	°C

Notes: 1. In a 2TX–1RX SP3T configuration, TX1 and TX2 are tied and TX3 and TX4 are tied respectively. Refer to Application Note AN35 for SP3T performance data.
2. Supply biased.
3. Pulsed, 10% duty cycle of 4620 µs period.

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	5.5	V
Digital input voltage (V1, V2, V3)	V_{CTRL}	–0.3	3.6	V
TX RF input power[1](50Ω	$P_{IN–TX}$		45	dBm
TX RF input power[1]	$P_{IN–TX}$		40	dBm
ANT RF input power, unbiased	$P_{IN–ANT}$		27	dBm
RX RF input power[1]	$P_{IN–RX}$		27	dBm
Storage temperature range	T_{ST}	–65	150	°C
Maximum case temperature	T_{CASE}		85	°C
Peak maximum junction temperature (10 seconds max)	T_j		200	°C
ESD voltage HBM[2], all pins	$V_{ESD,HBM}$		1500	V
ESD voltage MM[3], all pins	$V_{ESD,MM}$		200	V
ESD voltage CDM[4], all pins	$V_{ESD,CDM}$		1000	V

Notes: 1. Supply biased
2. Human Body Model (MIL-STD 883 Method 3015)
3. Machine Model (JEDEC JESD22-A115)
4. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the 5x5 mm QFN package is MSL3.

Switching Frequency

The PE42851 has a maximum 10 kHz switching rate when the internal negative voltage generator is used (pin 16 = GND). The rate at which the PE42851 can be switched is only limited to the switching time (*Table 1*) if an external negative supply is provided (pin 16 = V_{SS_EXT}).

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its

Optional External V_{SS} Control (V_{SS_EXT})

For proper operation, the V_{SS_EXT} control pin must be grounded or tied to the Vss voltage specified in *Table 3*. When the V_{SS_EXT} control pin is grounded, FETs in the switch are biased with an internal voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative

Spurious Performance

The typical spurious performance of the PE42851 is –130 dBm when V_{SS_EXT} = 0V (pin 16 = GND). If further improvement is desired, the internal negative voltage generator can be disabled by setting V_{SS_EXT} = –3.4V.

Table 5. Truth Table

Path	V3	V2	V1
ANT – RX Attenuated	L	L	L
ANT – TX1	L	L	H
ANT – TX2	L	H	L
ANT – TX1 and TX2*	L	H	H
ANT – RX	H	L	L
ANT – TX3	H	L	H
ANT – TX4	H	H	L
ANT – TX3 and TX4*	H	H	H

Note: * In a 2TX–1RX SP3T configuration, TX1 and TX2 are tied and TX3 and TX4 are tied respectively. Refer to Application Note AN35 for SP3T

Typical Performance Data @ +25 °C and V_{DD} = 3.4V, unless otherwise specified

Figure 5. Insertion Loss vs. Temp (TX)

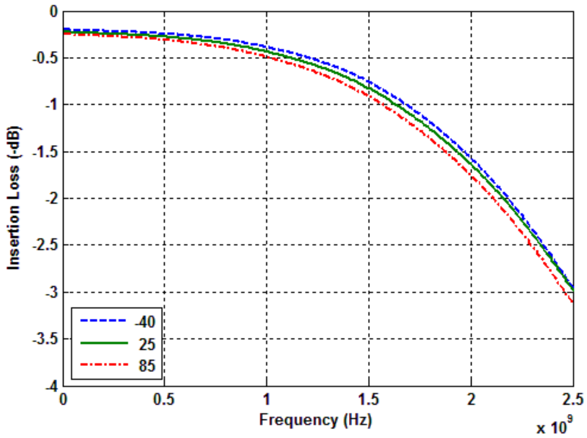


Figure 6. Insertion Loss vs. V_{DD} (TX)

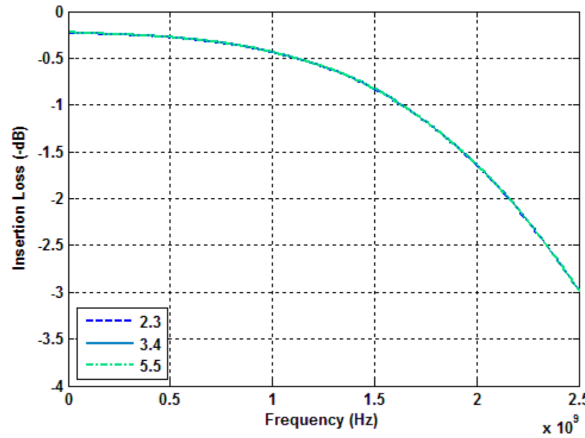


Figure 7. Insertion Loss vs. Temp (RX, Un-Attenuated)

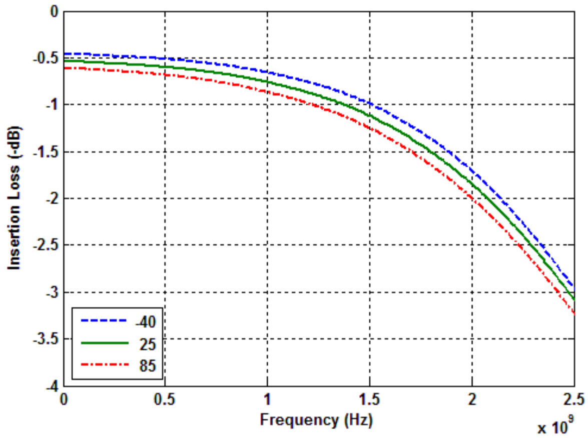


Figure 8. Insertion Loss vs. V_{DD} (RX, Un-Attenuated)

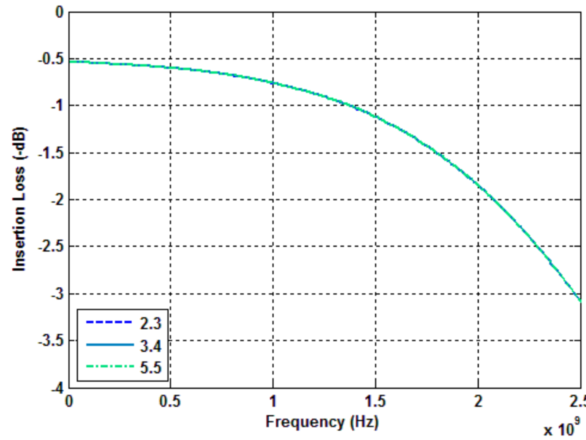


Figure 9. Insertion Loss vs. Temp (RX, Attenuated)

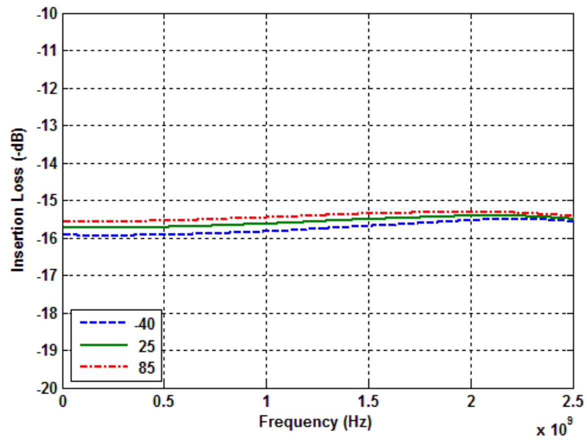
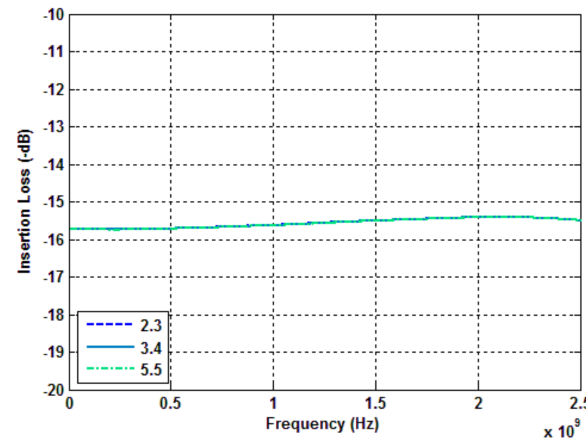


Figure 10. Insertion Loss vs. V_{DD} (RX, Attenuated)



Typical Performance Data @ +25 °C and V_{DD} = 3.4V, unless otherwise specified

Figure 11. Return Loss vs. Temp (ANT)

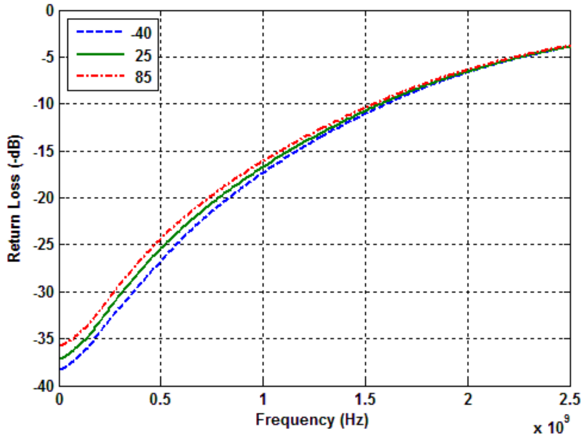


Figure 12. Return Loss vs. V_{DD} (ANT)

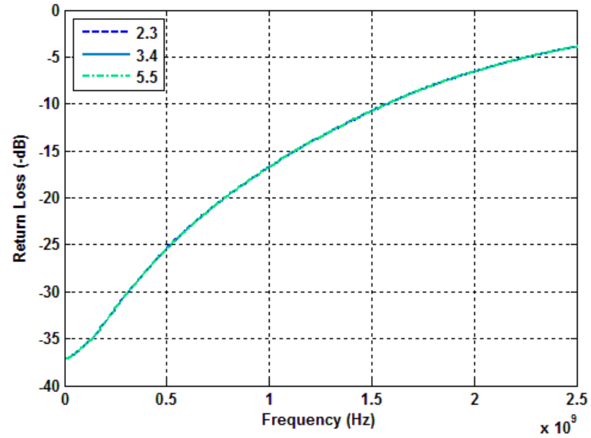


Figure 13. Return Loss vs. Temp (TX)

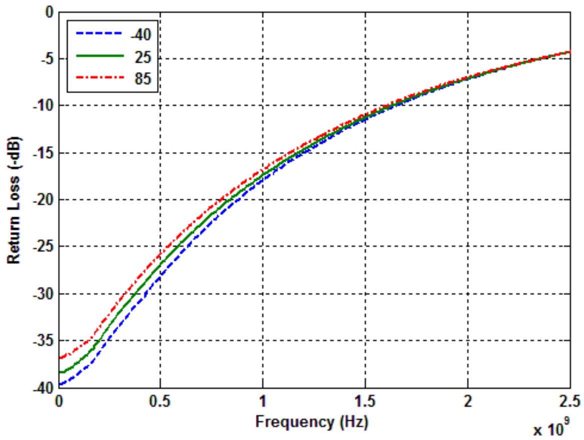


Figure 14. Return Loss vs. V_{DD} (TX)

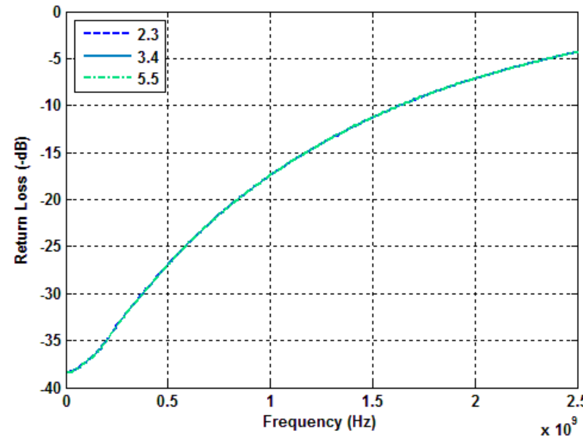


Figure 15. Return Loss vs. Temp (RX, Attenuated)

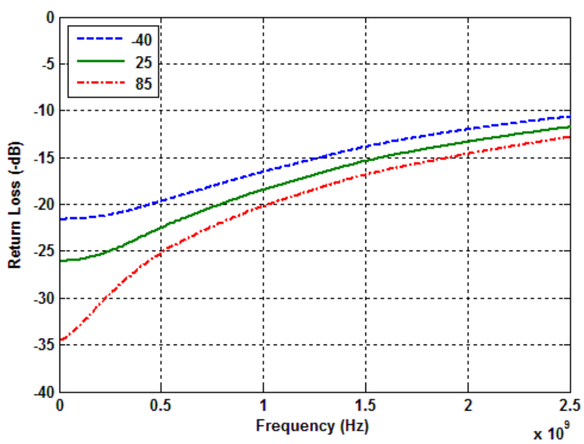
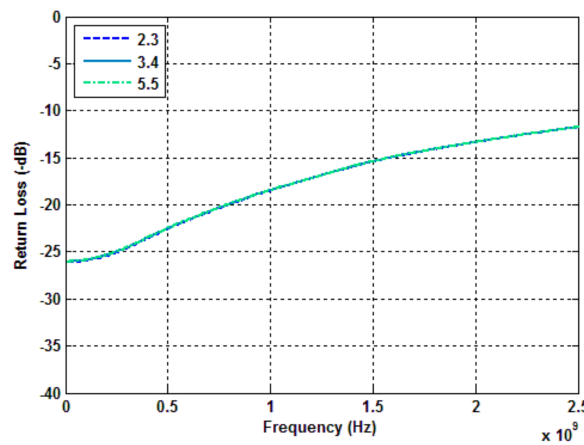


Figure 16. Return Loss vs. V_{DD} (RX, Attenuated)



Typical Performance Data @ +25 °C and V_{DD} = 3.4V, unless otherwise specified

Figure 17. Return Loss vs. Temp (RX, Un-Attenuated)

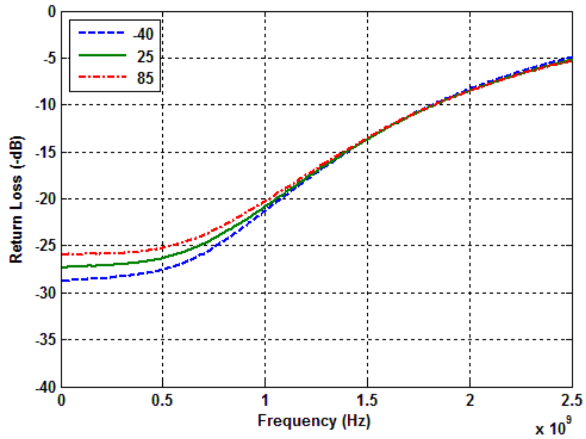


Figure 18. Return Loss vs. V_{DD} (RX, Un-Attenuated)

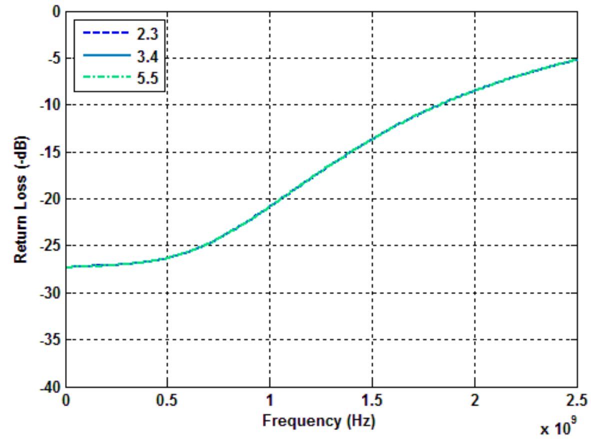


Figure 19. Isolation vs. Temp (TX–TX)

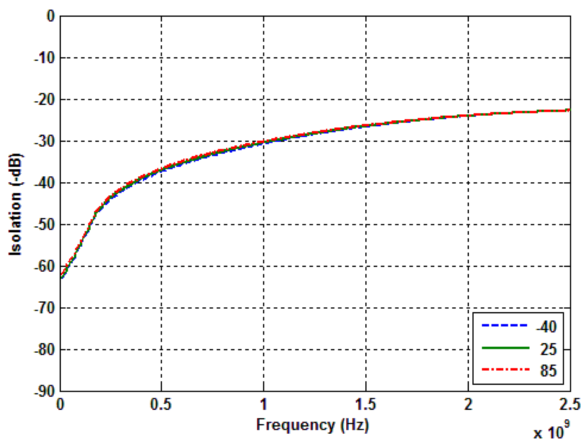


Figure 20. Isolation vs. V_{DD} (TX–TX)

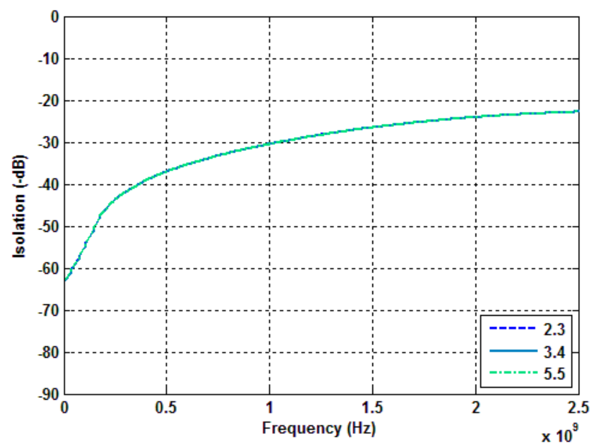


Figure 21. Isolation vs. Temp (TX–RX)

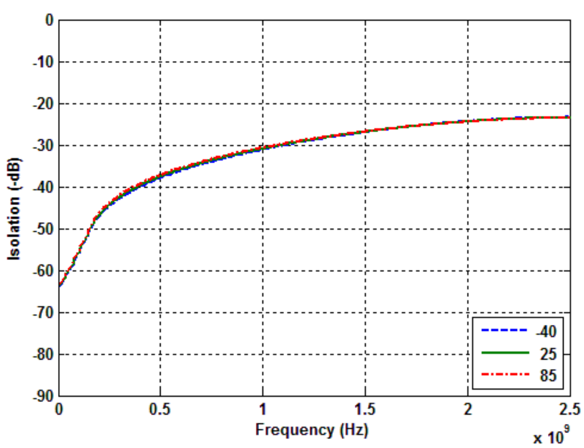
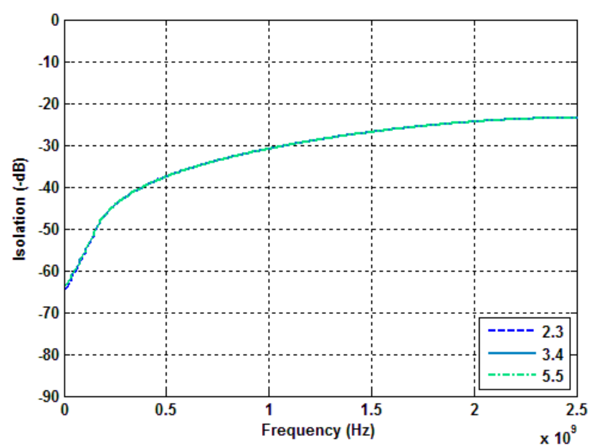


Figure 22. Isolation vs. V_{DD} (TX–RX)



Thermal Data

Though the insertion loss for this part is very low, when handling high power RF signals, the junction temperature rises significantly.

VSWR conditions that present short circuit loads to the part can cause significantly more power dissipation than with proper matching.

Special consideration needs to be made in the design of the PCB to properly dissipate the heat away from the part and maintain the +85 °C maximum case temperature. It is recommended to use best design practices for high power QFN packages: multi-layer PCBs with thermal vias in a thermal pad soldered to the slug of the package. Special care also needs to be made to alleviate solder voiding under the part.

Table 6. Theta JC

Parameter	Min	Typ	Max	Unit
Theta JC (+85 °C)		20		°C/W

Evaluation Kit

The PE42851 Evaluation Kit board was designed to ease customer evaluation of the PE42851 RF switch.

The evaluation board in Figure 23 was designed to test the part in the 5T configuration. DC power is supplied through J10, with V_{DD} on pin 9, and GND on the entire lower row of even numbered pins. To evaluate a switch path, add or remove jumpers on V1 (pin 3), V2 (pin 5), and V3 (pin 7) using *Table 5* (adding a jumper pulls the CMOS control pin low and removing it allows the on-board pull-up resistor to set the CMOS control pin high). Pins 11 and 13 of J10 are N/C.

The ANT port is connected through a 50Ω transmission line via the top SMA connector, J1. RX and TX paths are also connected through 50Ω transmission lines via SMA connectors. A 50Ω through transmission line is available via SMA connectors J8 and J9. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. An open-ended 50Ω transmission line is also provided at J7 for calibration if needed.

Narrow trace widths are used near each part to improve impedance matching.

Figure 23. Evaluation Board Layouts

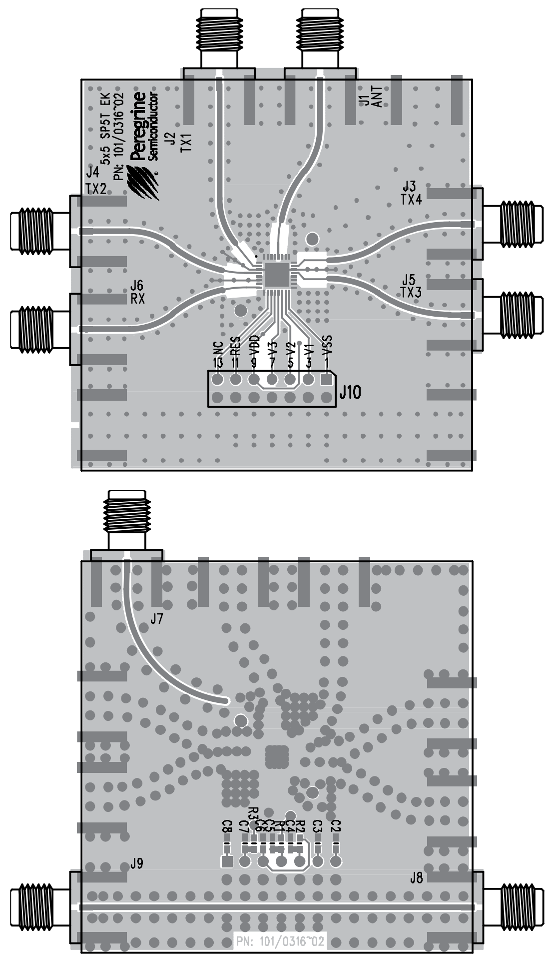


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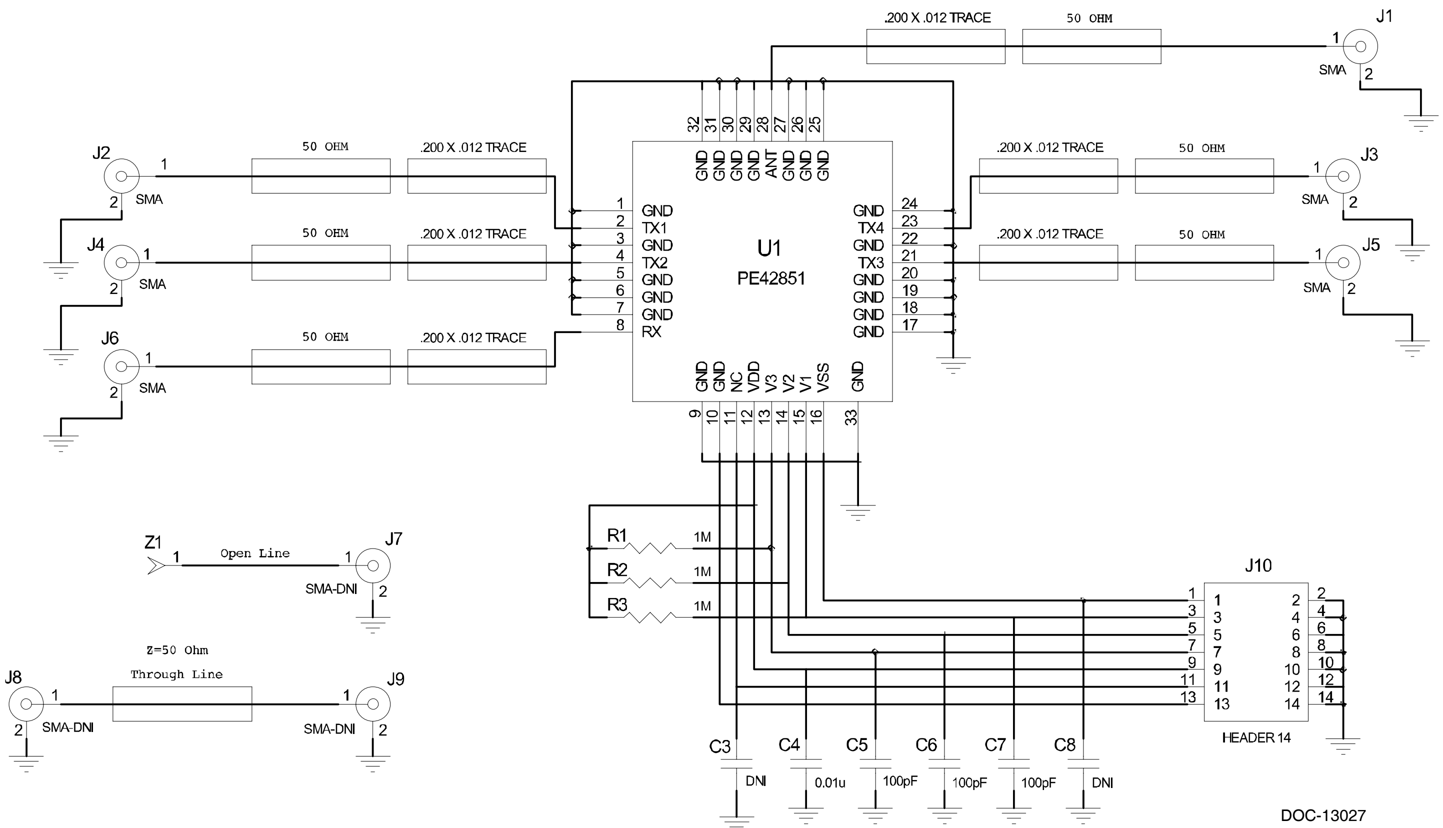
Figure 24. Evaluation Board Schematic



Notes: 1. Use 101-0316-02 PCB
2. 32 mil Width, 10 mil Gaps, 28 mil Core, 4.3 Er, and 2.1 mil Cu

Figure 25. Package Drawing
32-lead 5x5 mm QFN

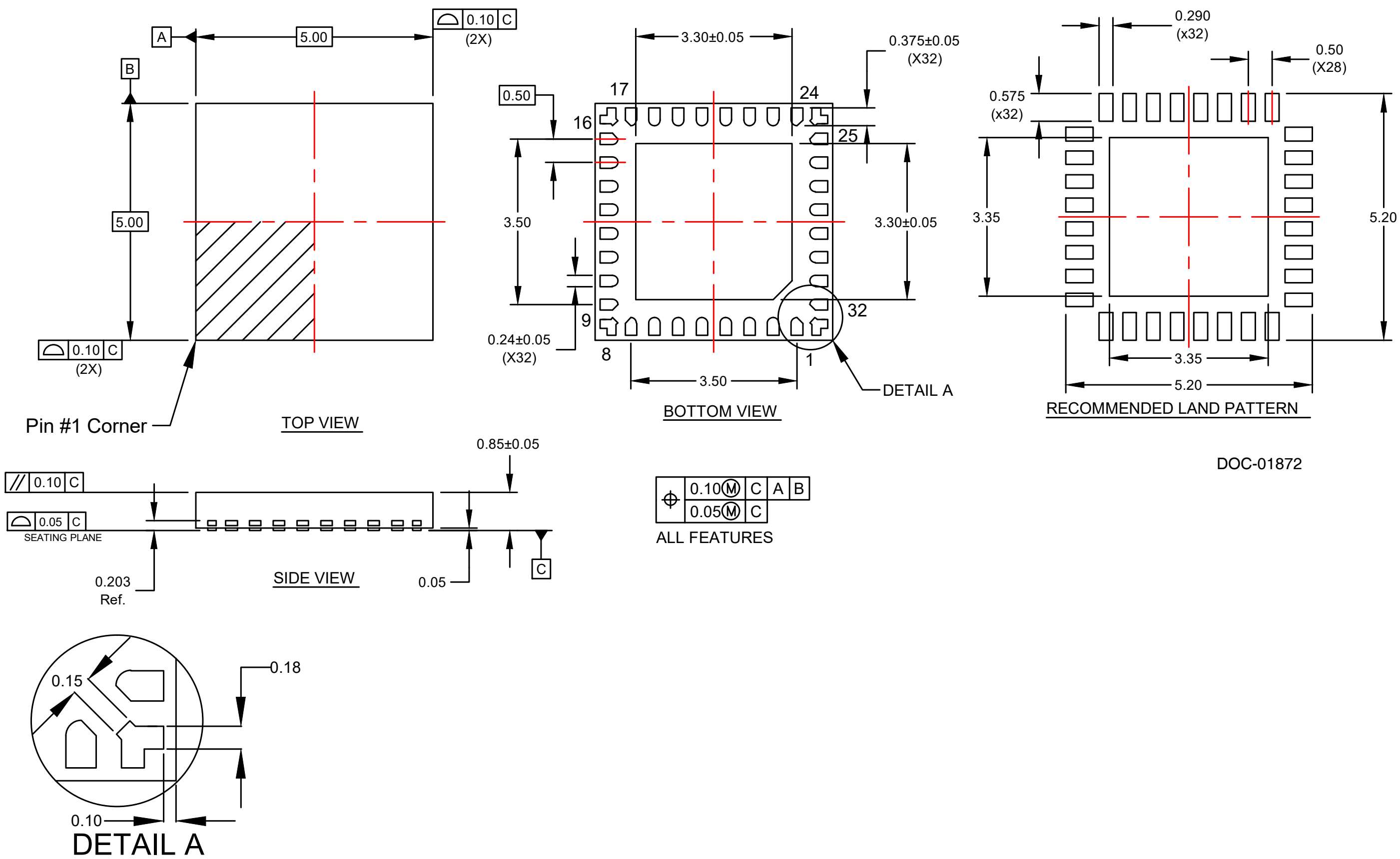


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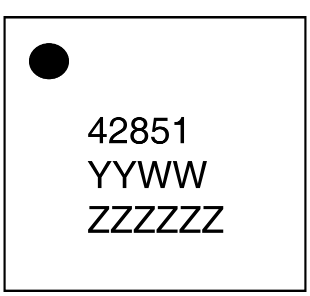
Figure 26. Top Marking Specification



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● = Pin 1 designator

YYWW = Date code, last two digits of the year and work week

ZZZZZZ = Six digits of the lot number