Product Specification

PE4312

UltraCMOS® RF Digital Step Attenuator
6-bit, 31.5 dB, 1 MHz–4 GHz

Features

- Attenuation: 0.5 dB steps to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- High attenuation accuracy
  - ±(0.10 + 1% x Atten) @ 1 GHz
  - ±(0.15 + 2% x Atten) @ 2.2 GHz
  - ±(0.15 + 8% x Atten) @ 4 GHz
- High linearity: +59 dBm IIP3
- Wide power supply range of 2.3–5.5V
- 1.8V control logic compatible
- 105 °C operating temperature
- Programming modes
  - Direct parallel
  - Latched parallel
  - Serial
- Unique power-up state selection
- Pin compatible to PE4302, PE4305 and PE4306

Product Description

The PE4312 is a 50Ω, HaRP™ technology-enhanced 6-bit RF Digital Step Attenuator (DSA) designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

This DSA is a pin-compatible upgraded version of the PE4302 with higher linearity, improved attenuation accuracy and faster switching speed. An integrated digital control interface supports both serial and parallel programming of the attenuation, including the capability to program an initial attenuation state at power-up.

Covering a 31.5 dB attenuation range in 0.5 dB steps, it maintains high linearity and low power consumption from 1 MHz through 4 GHz. PE4312 also features an external negative supply option, and is offered in a 20-lead 4 × 4 mm QFN package. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE4312 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

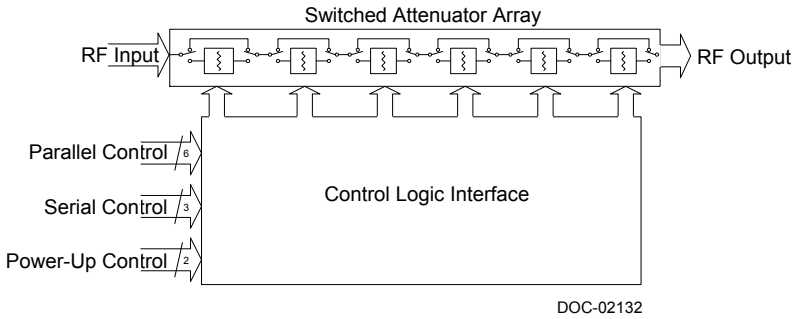


Figure 2. Package Type
20-lead 4 × 4 mm QFN

Table 1. Electrical Specifications @ 25 °C (Z_S= Z_L = 50Ω), unless otherwise noted
Normal Mode[1]: V_{DD} = 3.3V, V_{SS_EXT} = 0V or Bypass Mode[2]: V_{DD} = 3.3V, V_{SS_EXT} = –3.3V

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operation frequency			1		4000	MHz
Attenuation range	0.5 dB step			0–31.5		dB
Insertion loss		1 MHz–<1 GHz 1–2.2 GHz 2.2–4 GHz		1.3 1.5 2.1	1.5 1.8 2.3	dB dB dB
Attenuation error	Any bit or bit combination	1 MHz–1 GHz 1–<2.2 GHz 2.2–4 GHz			±(0.10 + 1% of atten setting) ±(0.15 + 2% of atten setting) ±(0.15 + 8% of atten setting)	dB dB dB
Return loss (input or output port)		1–2.2 GHz 2.2–4 GHz	14 10	18 17		dB
Input 0.1dB compression point[3]		1 MHz–4 GHz		30		dBm
Input IP3	Two tones at +18 dBm, 10 kHz spacing	1950 MHz		59		dBm
Switching time	50% CTRL to 90% or 10% RF			500	800	ns

Notes: 1. Normal mode: single external positive supply used.
2. Bypass mode: both external positive supply and external negative supply used.
3. The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 5* for the operating RF input power (50Ω).

Figure 3. Pin Configuration (Top View)

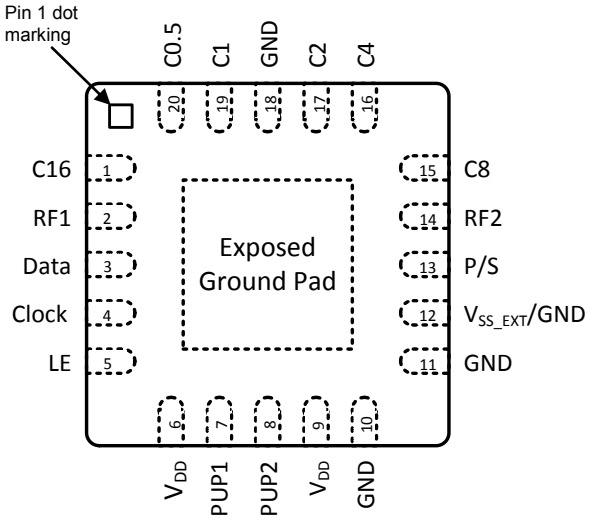


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	C16[3,5]	Attenuation control bit, 16 dB
2	RF1[1]	RF1 port (RF input)
3	Data[3]	Serial interface data input
4	Clock	Serial interface clock input
5	LE[4]	Latch Enable input
6	V_{DD}	Supply voltage (nominal 3.3V)
7	PUP1[5]	Power-up selection bit 1
8	PUP2	Power-up selection bit 2
9	V_{DD}	Supply voltage (nominal 3.3V)
10, 11, 18	GND	Ground
12	V_{SS_EXT}/ GND[2]	External V_{SS} negative voltage control or ground
13	P/S	Parallel/Serial mode select
14	RF2[1]	RF2 port (RF output)
15	C8	Attenuation control bit, 8 dB
16	C4	Attenuation control bit, 4 dB
17	C2	Attenuation control bit, 2 dB
19	C1	Attenuation control bit, 1 dB
20	C0.5[5]	Attenuation control bit, 0.5 dB
Pad	GND	Exposed pad: ground for proper operation

Notes: 1. RF pins 2 and 14 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Use V_{SS_EXT} (pin 12, refer to *Table 3*) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 12, V_{SS_EXT} = GND) to enable internal negative voltage generator.
3. Place a 10 kΩ resistor in series, as close to pin as possible to avoid frequency resonance.
4. This pin has an internal 2 MΩ resistor to internal positive digital supply.
5. This pin has an internal 200 kΩ resistor to GND.

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Normal mode[1]					
Supply voltage	V_{DD}	2.3		5.5	V
Supply current	I_{DD}		130	200	µA
Bypass mode[2]					
Supply voltage	V_{DD}	2.7		5.5	V
Supply current	I_{DD}		50	80	µA
Negative supply voltage	V_{SS_EXT}	-3.6		-3.2	V
Negative supply current	I_{SS}	-40	-16		µA
Normal or Bypass mode					
Digital input high		1.17		3.6	V
Digital input low		-0.3		0.6	V
Digital input leakage[3]				20	µA
RF input power, CW 1–50 MHz >50 MHz–4 GHz	P_{MAX_CW}			*Fig. 4* +24	dBm dBm
RF input power, pulsed[4] 1–50 MHz >50 MHz–4 GHz	P_{MAX_PULSED}			*Fig. 4* +27	dBm dBm
Operating temperature range	T_{OP}	-55		+105	°C

Notes: 1. Normal mode: connect pin 12 to GND to enable internal negative voltage generator.
2. Bypass mode: apply a negative voltage to V_{SS_EXT} (pin 12) to bypass and disable internal negative voltage generator.
3. Applies to all pins except pins 1, 5, 7 and 20. Pins 1, 7 and 20 have an internal pull-down resistor and pin 5 has an internal pull-up resistor.
4. Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage	V_{CTRL}	-0.3	3.6	V
Maximum input power	P_{MAX_ABS}		+30	dBm
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM*, all pins	V_{ESD}		1500	V

Note: * Human Body Model (MIL-STD-883 Method 3015)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Switching Frequency

The PE4312 has a maximum 25 kHz switching rate in normal mode (pin 12 = GND). A faster switching rate is available in bypass mode (pin 12 = V_{SS_EXT}). The rate at which the PE4312 can be switched is then limited to the switching time as specified in *Table 1*.

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Safe Attenuation State Transitions

The PE4312 features a novel architecture to provide safe transition behavior when changing attenuation states. When RF input power is applied, positive output power spikes are prevented during attenuation state changes by optimized internal timing control.

Resistor on Pin 1 & 3

A 10 kΩ resistor on the inputs to pin 1 and 3 (see *Figure 26*) will eliminate package resonance between the RF input pin and the two digital inputs. Specified attenuation error versus frequency performance is dependent upon this condition.

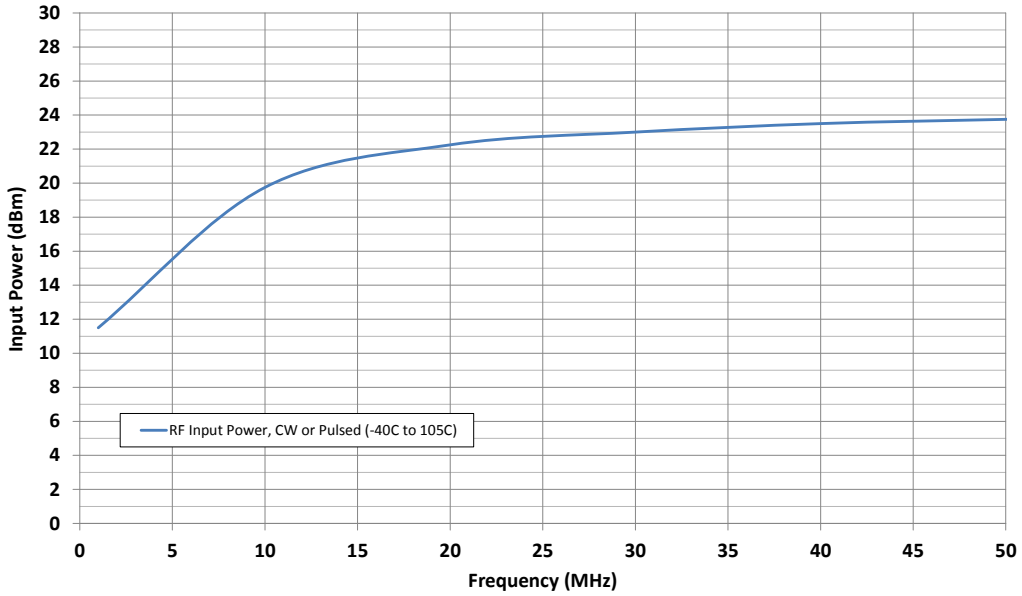
Moisture Sensitivity Level

The moisture sensitivity level rating for the PE4312 in the 4 × 4 mm QFN package is MSL1.

Spurious Performance

The typical low-frequency spurious performance of the PE4312 in normal mode is –140 dBm (pin 12 = GND). If spur-free performance is desired, the internal negative voltage generator can be disabled by applying a negative voltage to V_{SS_EXT} (pin 12).

Figure 4. Power Derating Curve for 1–50 MHz



Programming Options

Parallel/Serial Selection

Either a parallel or serial interface can be used to control the PE4312. The P/S bit provides this selection, with P/S = LOW selecting the parallel interface and P/S = HIGH selecting the serial interface.

Parallel Mode Interface

The parallel interface consists of six CMOS-compatible control lines that select the desired attenuation state, as shown in *Table 5*.

The parallel interface timing requirements are defined by *Figure 5* (Parallel Interface Timing Diagram), *Table 9* (Parallel Interface AC Characteristics), and switching speed (*Table 1*).

For *latched* parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per *Figure 5*) to latch the new attenuation state into the device.

For *direct* parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Table 5. Truth Table*

P/S	C16	C8	C4	C2	C1	C0.5	Attenuation State
0	0	0	0	0	0	0	Reference Loss
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB

Note: * Not all 64 possible combinations of C0.5–C16 are shown in table.

Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by *Figure 5* (Serial Interface Timing Diagram) and *Table 8* (Serial Interface AC Characteristics).

Power-up Control Settings

The PE4312 always assumes a specifiable attenuation setting on power-up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in Serial mode (P/S = 1), the six control bits are set to whatever data is present on the six parallel data inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode (P/S = 0) with LE = 0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in *Table 6* (Power-Up Truth Table, Parallel Mode).

Table 6. Parallel PUP Truth Table*

P/S	LE	PUP2	PUP1	Attenuation State
0	0	0	0	Reference Loss
0	0	1	0	8 dB
0	0	0	1	16 dB
0	0	1	1	31.5 dB
0	1	X	X	Defined by C0.5-C16

Note: * Power up with LE = 1 provides normal parallel operation with C0.5-C16, and PUP1 and PUP2 are not active.

Figure 5. Serial Interface Timing Diagram

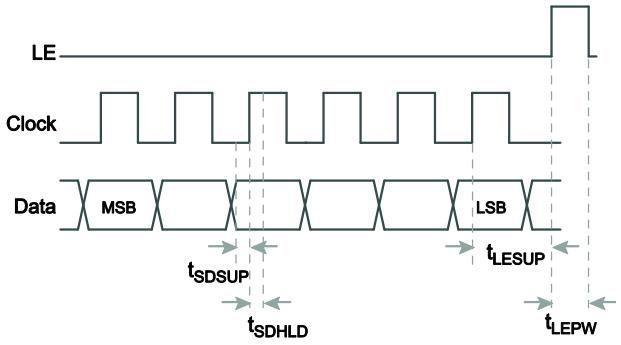


Figure 6. Parallel Interface Timing Diagram

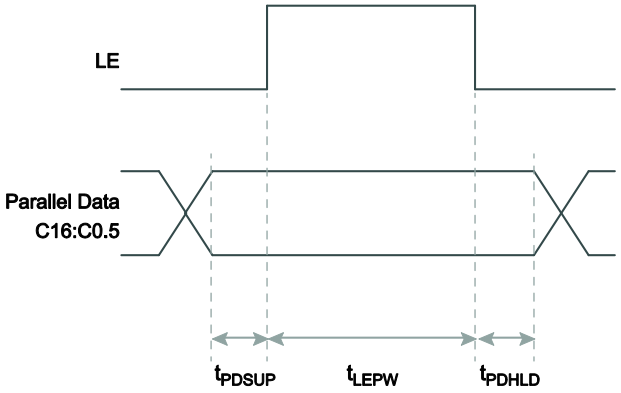


Table 7. 6-Bit Attenuator Serial Programming Register Map

B5	B4	B3	B3	B1	B0
C16	C8	C4	C2	C1	C0.5

MSB (first in) — LSB (last in)

Table 8. Serial Interface AC Characteristics

V_{DD} = 3.3V, –55 °C < T_A < 105 °C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
f_{Clk}	Serial data clock frequency*		10	MHz
t_{ClkH}	Serial clock HIGH time	30		ns
t_{ClkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock rising edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock rising edge	10		ns

Note: * f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{clk} specification

Table 9. Parallel Interface AC Characteristics

V_{DD} = 3.3V, –55 °C < T_A < 105 °C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
t_{LEPW}	LE minimum pulse width	10		ns
t_{PDSUP}	Data set-up time before rising edge of LE	10		ns
t_{PDHLD}	Data hold time after falling edge of LE	10		ns

Typical Performance Data @ 25 °C and V_{DD} = 3.3V, unless otherwise noted

Figure 7. Insertion Loss vs Frequency @ Major Attenuation Steps

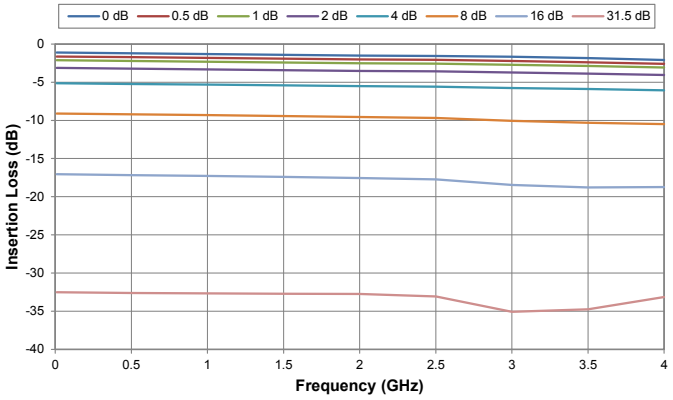


Figure 8. Insertion Loss vs Temperature

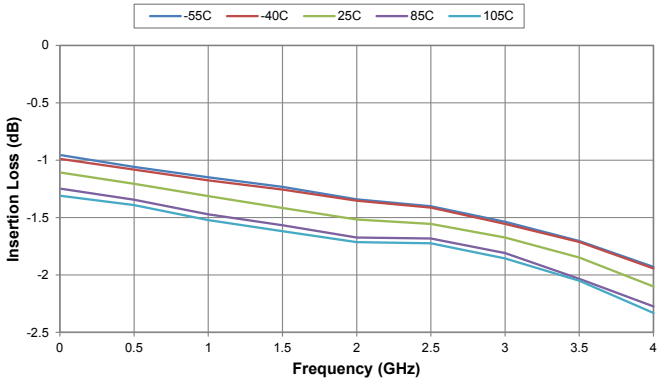


Figure 9. Input Return Loss vs Frequency @ Major Attenuation Steps

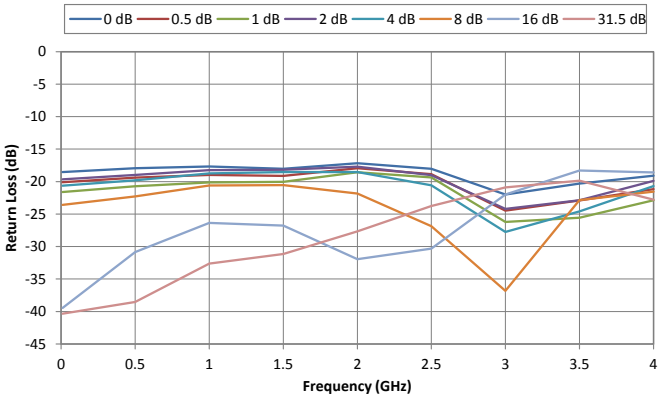


Figure 10. Input Return Loss vs Temperature

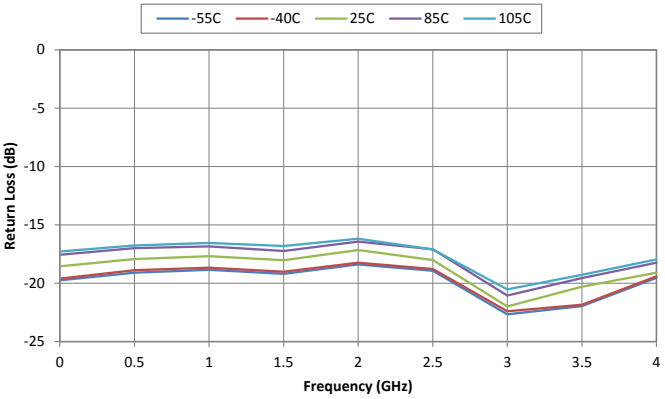


Figure 11. Output Return Loss vs Frequency @ Major Attenuation Steps

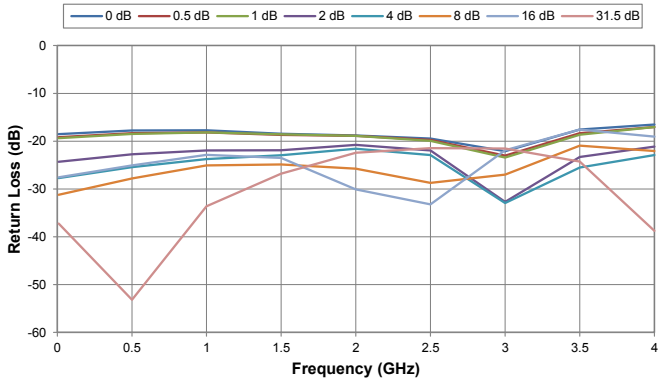
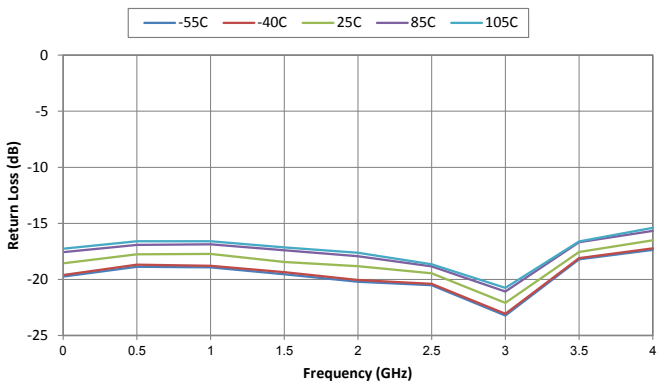


Figure 12. Output Return Loss vs Temperature



Typical Performance Data @ 25 °C and V_{DD} = 3.3V, unless otherwise noted

Figure 13. Attenuation Error vs Frequency @ Major Attenuation Steps

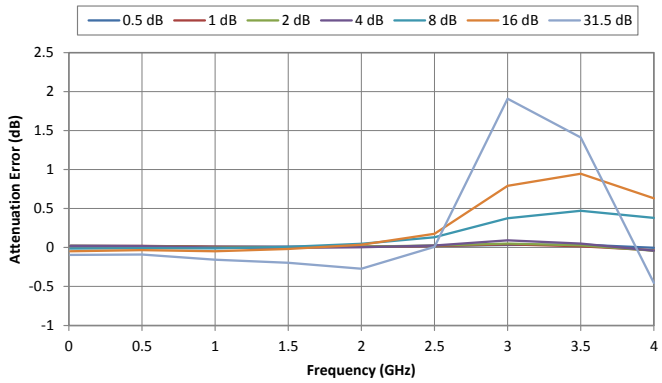


Figure 14. Attenuation Error vs Attenuation Setting

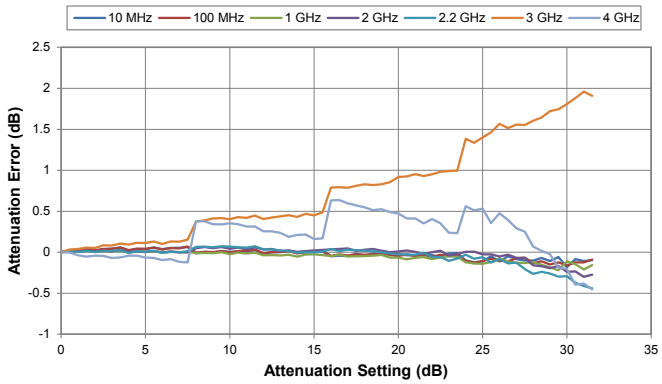


Figure 15. Actual Attenuation vs Ideal Attenuation

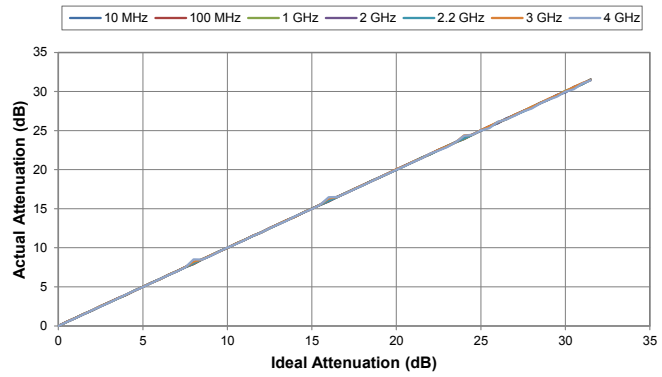
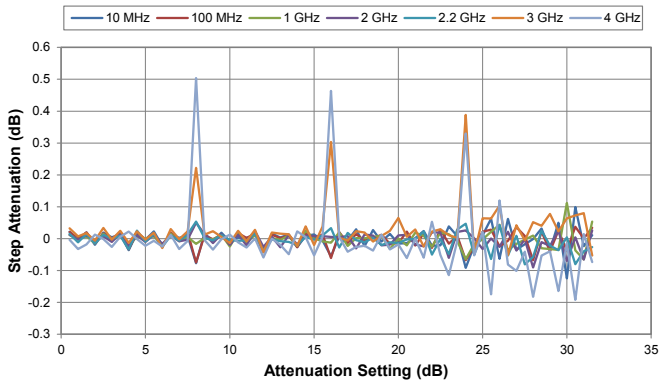


Figure 16. 0.5 dB Step Attenuation vs Attenuation Setting*



Note: * Monotonicity is held as long as step attenuation does not cross below –0.5 dB.

Figure 17. Relative Phase Error vs Frequency @ Major Attenuation Steps

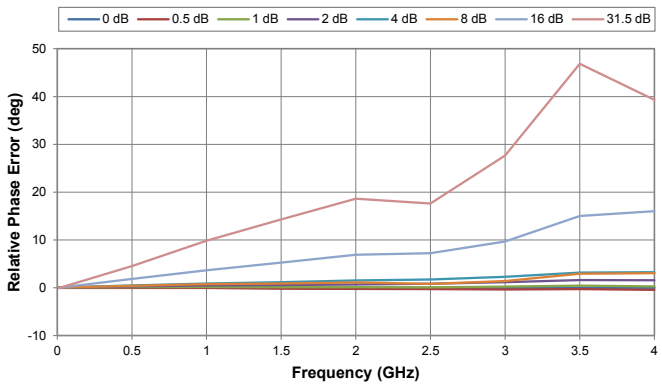
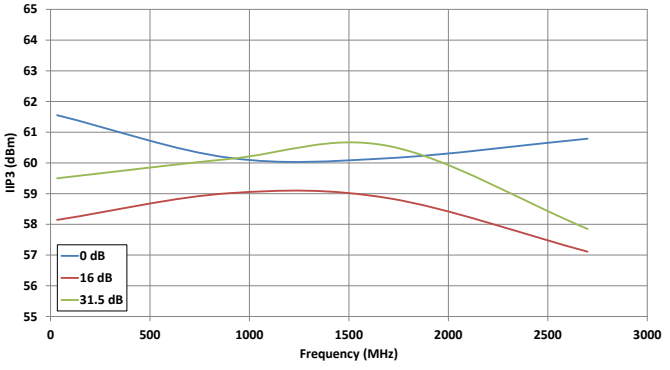


Figure 18. IIP3 vs Frequency



Typical Performance Data @ 25 °C and V_{DD} = 3.3V, unless otherwise noted

Figure 19. Attenuation Error @ 10 MHz vs Temperature

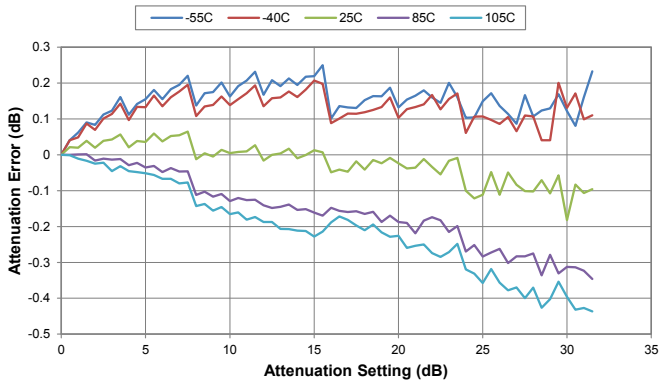


Figure 20. Attenuation Error @ 100 MHz vs Temperature

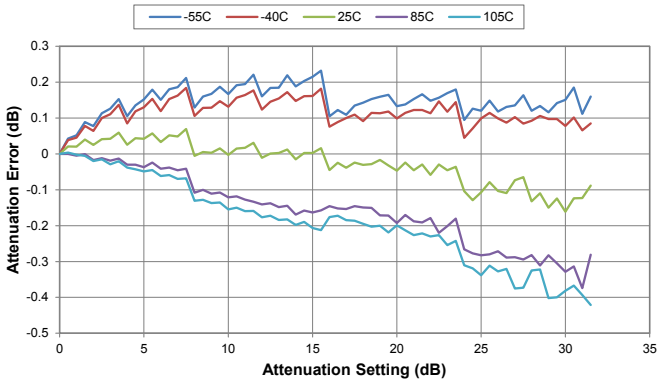


Figure 21. Attenuation Error @ 1 GHz vs Temperature

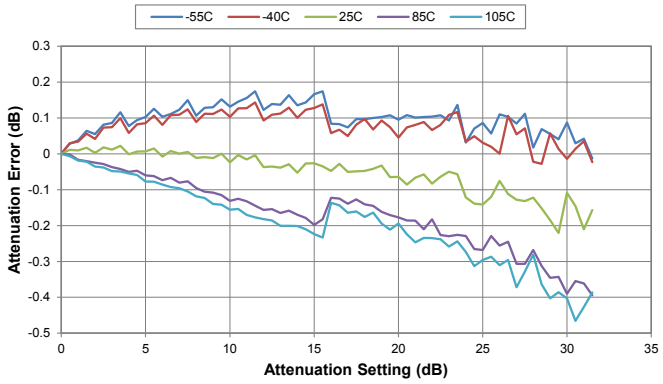


Figure 22. Attenuation Error @ 2.2 GHz vs Temperature

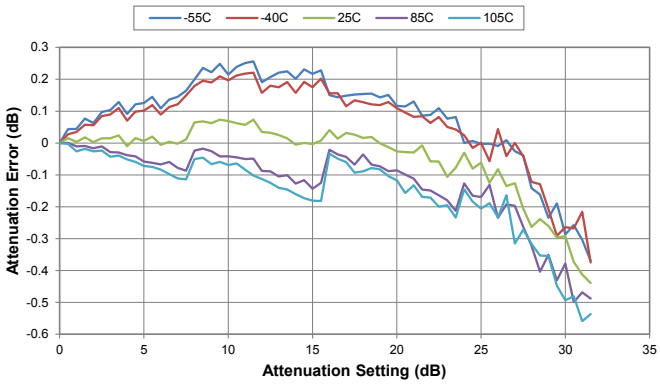
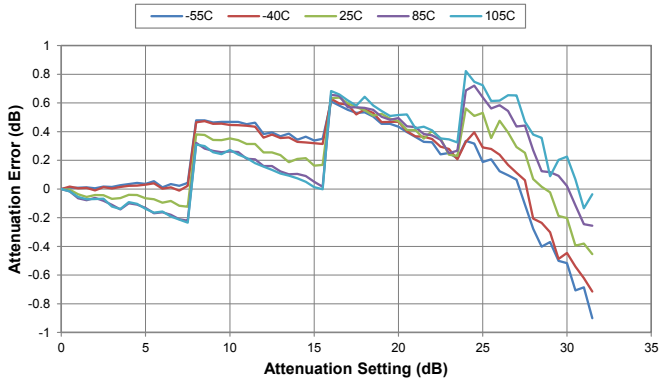


Figure 23. Attenuation Error @ 4 GHz vs Temperature



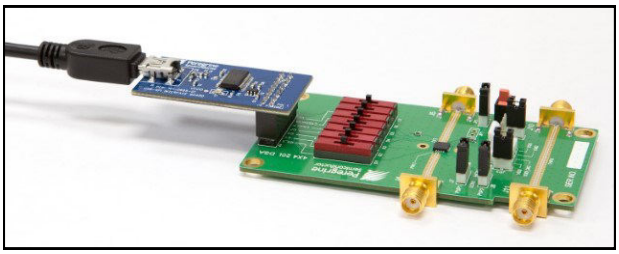
Evaluation Kit

The Digital Step Attenuator Evaluation Board (EVB) was designed to ease customer evaluation of the PE4312 Digital Step Attenuator. PE4312 EVB supports Direct Parallel, Latched Parallel, and Serial programming modes.

Evaluation Kit Setup

Connect the EVB with the USB dongle board and USB cable as shown in *Figure 24*.

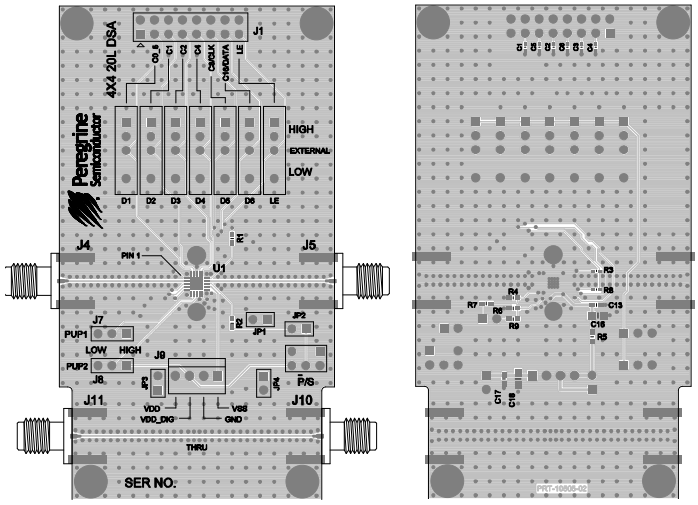
Figure 24. Evaluation Kit



Direct Parallel Programming Procedure

Direct Parallel programming is suitable for manual operation without software programming. For manual Direct Parallel programming, position the Parallel/Serial (P/S) select switch to the Parallel (or left) position. The LE mechanical programming switch must be set to the HIGH position. Switches D1–D6 are SP3T switches that enable the user to manually program the parallel bits. When D1–D6 are toggled to the HIGH position, logic high is presented to the parallel input. When toggled to the LOW position, logic low is presented to the parallel input. Setting D1–D6 to the EXTERNAL position presents as OPEN, which is set for software programming of Latched Parallel and Serial mode. *Table 5* depicts the parallel programming truth table.

Figure 25. Evaluation Board Layout



PRT-10505

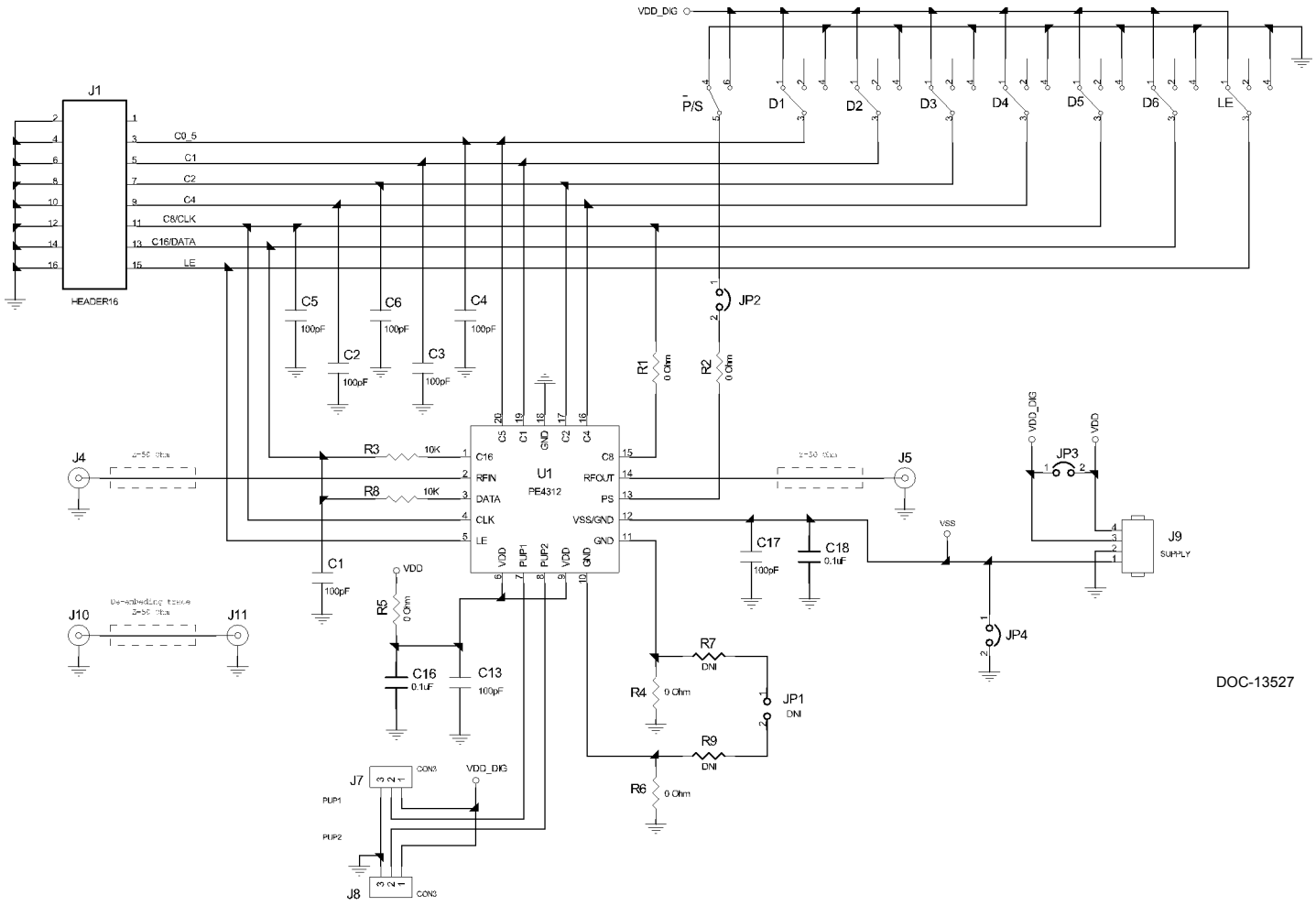
Latched Parallel Programming Procedure

For automated Latched Parallel programming, connect the USB dongle board and cable that is provided with the Evaluation Kit (EVK) from the USB port of the PC to the J1 header of the PE4312 EVB, and set the D1–D6 SP3T switches to the EXTERNAL position. Position the Parallel/Serial (P/S) select switch to the Parallel (or left) position. The evaluation software is written to operate the DSA in Parallel mode. Ensure that the software GUI is set to Latched Parallel mode. Use the software GUI to enable the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

Serial Programming Procedure

For automated Serial programming, connect the USB dongle board and cable that is provided with the Evaluation Kit (EVK) from the USB port of the PC to the J1 header of the PE4312 EVB, and set the D1–D6 SP3T switches to the EXTERNAL position. Position the Parallel/Serial (P/S) select switch to the Serial (or right) position. The evaluation software is written to operate the DSA in Serial mode. Ensure that the software GUI is set to Serial mode. Use the software GUI to enable the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

Figure 26. Evaluation Board Schematic



Notes: 1. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).
2. Install shunt connector on JP2, JP3 and JP4.

Figure 27. Package Drawing
20-lead 4 × 4 mm QFN

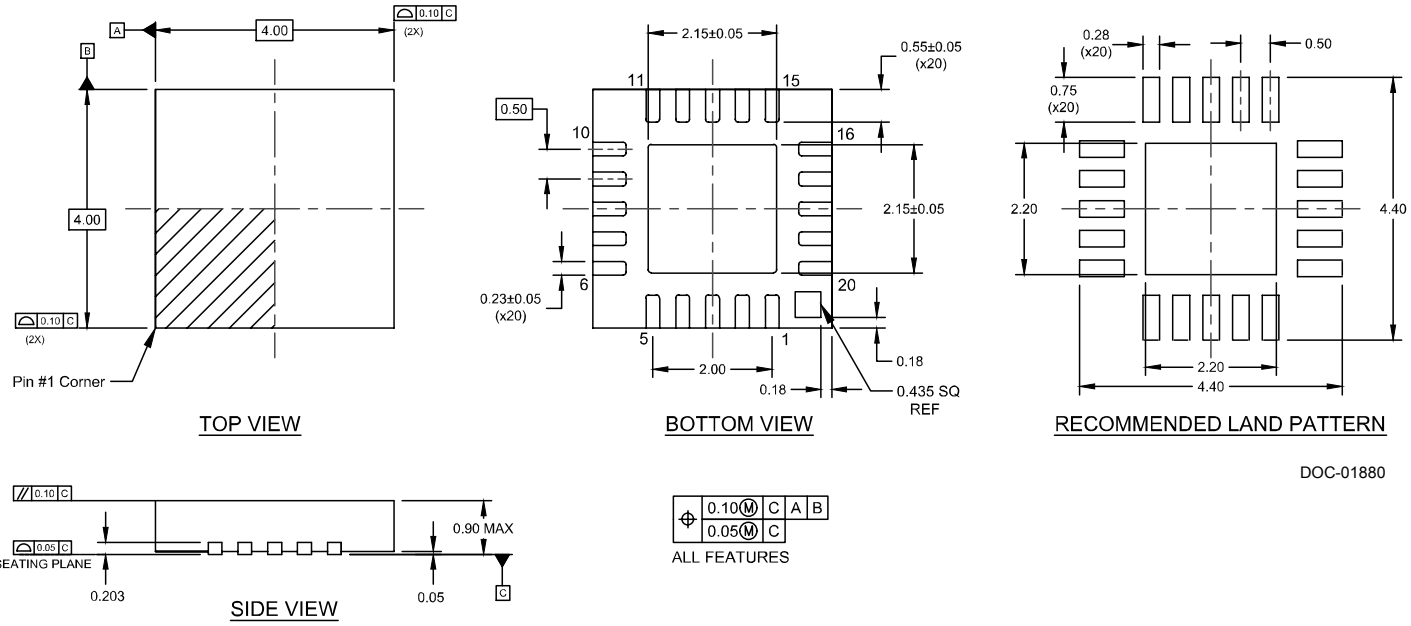


Figure 28. Top Marking Specifications

DOC-65736

● = Pin 1 designator
YYWW = Date code, last two digits of the year and work week
ZZZZZZ = Assembly lot code (max 6 characters)