PE43670

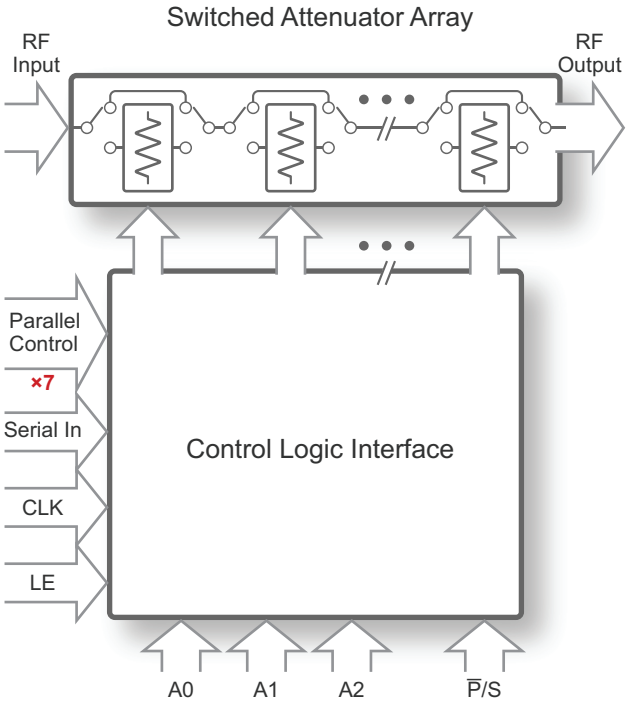
Document Category: Product Specification

50 Ω RF Digital Attenuator 7-bit, 31.75 dB, 9 kHz-4.0 GHz

Features

- Attenuation: 0.25 dB steps to 31.75 dB
- High linearity: Typical +59 dBm IIP3
  - Excellent low-frequency performance
- Fast switch settling time
- Programming modes:
  - Direct parallel
  - Latched parallel
  - Serial-addressable: Program up to eight addresses 000 - 111
- CMOS-compatible
- No DC blocking capacitors required
- Packaged in a 32-lead 5x5x0.85 mm QFN

Figure 1 • *PE43670 Functional Diagram*



Product Description

The PE43670 is a high linearity, 7-bit RF Digital Step Attenuator (DSA). This highly versatile DSA covers a 31.75 dB attenuation range in 0.25 dB steps. The Peregrine 50Ω RF DSA provides a parallel or serial-addressable CMOS control interface. It maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss and low power consumption. Performance does not change with V_{DD} due to on-board regulator. This Peregrine DSA is available in a 5x5 mm 32-lead QFN footprint.

The PE43670 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE43670*

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Power supply voltage	-0.3	6.0	V
V_I	Voltage on any digital input	-0.3	5.8	V
P_{IN}	Input power (50Ω) 1 Hz ≤ 20 MHz 20 MHz ≤ 4 GHz		See **Fig. 2** +23	dBm dBm
T_{ST}	Storage temperature range	-65	150	°C
V_{ESD}	ESD voltage (HBM)[1] ESD voltage (machine model)		500 100	V V

Notes:
1) Human body model (HBM, MIL-STD 883 Method 3015.7).

Recommended Operating Conditions

Table 2 lists the recommending operating conditions for the PE43670. Devices should not be operated outside the operating conditions listed below.

Table 2 • *Recommended Operating Conditions for PE43670*

Parameter	Min	Typ	Max	Unit
V_{DD} Power Supply Voltage	3.0	3.3		V
V_{DD} Power Supply Voltage		5.0	5.5	V
I_{DD} Power Supply Current		70	350	µA
Digital Input High	2.6		5.5	V
P_{IN} Input power (50Ω): 1 Hz ≤ 20 MHz 20 MHz ≤ 4 GHz			See **Fig. 2** +23	dBm dBm

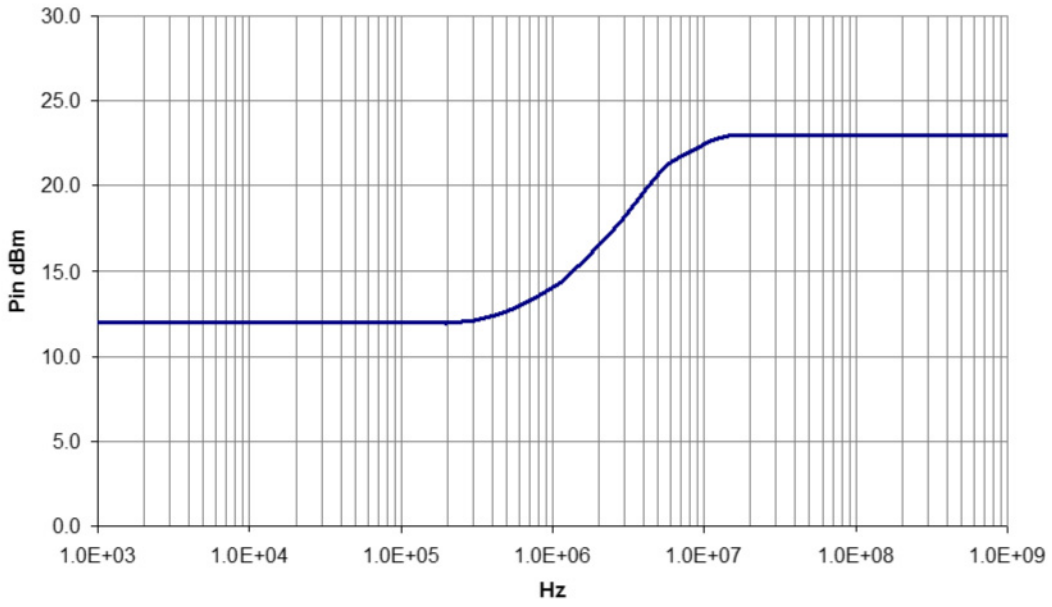
Table 2 • *Recommended Operating Conditions for PE43670 (Cont.)*

Parameter	Min	Typ	Max	Unit
T_{OP} Operating temperature range	-40	25	85	°C
Digital Input Low	0		1	V
Digital Input Leakage[1]			15	µA
Note: * 1. Input leakage current per control pin.				

Maximum Power Handling Capability

Figure 2 shows the maximum power handling capability for the PE43670.

Figure 2 • *Maximum Power Handling Capability: Z0 = 50 Ω*



Electrical Specifications

Table 3 provides the PE43670 key electrical specifications @ +25°C, V_{DD} = 3.3 V or 5.0 V, unless otherwise specified.

Table 3 • *PE43670 Electrical Specifications*

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Frequency Range			9 kHz		4.0	GHz
Attenuation Range	0.25 dB Step			0 – 31.75		dB
Insertion Loss		9 kHz ≤ 4 GHz		1.9	2.4	dB
Attenuation Error	0 dB - 7.75 dB Attenuation settings 8 dB - 31.75 dB Attenuation settings 0 dB - 31.75 dB Attenuation settings	9 kHz < 3 GHz 9 kHz < 3 GHz 3 GHz ≤ 4 GHz			±(0.2+1.5%) ±(0.15+4%) ±(0.25+4.5%)	dB dB dB
Return Loss		9 kHz - 4 GHz		18		dB
Relative Phase	All States	9 kHz - 4 GHz		44		deg
P1dB (Note 1)	Input	20 MHz - 4 GHz	30	32		dBm
IIP3	Two tones at +18 dBm, 20 MHz spacing	20 MHz - 4 GHz		59		dBm
Typical Spurious Value		1 MHz		-110		dBm
Video Feed Through				10		mVpp
Switching Time	50% DC CTRL to 10% / 90% RF			650		ns
RF Trise/Tfall	10% / 90% RF			400		ns
Settling Time	RF settled to within 0.05 dB of final value RBW = 5 MHz, Averaging ON.			4	25	µs

Notes:
1) Please note Maximum Operating Pin (50Ω) of +23dBm as shown in **Table 2**.

Switching Frequency

The PE43670 has a maximum 25 kHz switching frequency. Switching frequency is defined to be the speed at which the DSA can be toggled across attenuation states. Switching time is the time duration between the point the control signal reached 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Control Voltage

Table 4 provides the control voltage table for the PE43670.

Table 4 • *Control Voltage Table for PE43670*

State	Bias Condition
Low	0 to +1.0 Vdc at 2 µA (typ)
High	+2.6 to +5 Vdc at 10 µA (typ)

Latch and Clock Specifications

Table 5 provides the latch and clock specifications table for the PE43670.

Table 5 • *Latch and Clock Specifications for PE43670*

Latch Enable	Shift Clock	Function
0	↑	Shift Register Clocked
↑	X	Contents of shift register transferred to attenuator core

Truth Tables

Table 6, Table 7, and Table 8 provide the truth tables for the PE43670.

Table 6 • *Parallel Truth Table*

Parallel Control Setting							Attenuation Setting RF1-RF2
D6 (MSB)	D5	D4	D3	D2	D1	D0	
L	L	L	L	L	L	L	Reference I.L.
L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	H	L	0.5 dB
L	L	L	L	H	L	L	1 dB
L	L	L	H	L	L	L	2 dB
L	L	H	L	L	L	L	4 dB
L	H	L	L	L	L	L	8 dB
H	L	L	L	L	L	L	16 dB

Table 6 • *Parallel Truth Table (Cont.)*

Parallel Control Setting							Attenuation Setting RF1-RF2
D6 (MSB)	D5	D4	D3	D2	D1	D0	
H	H	H	H	H	H	H	31.75 dB

Table 7 • *Address Word Truth Table*

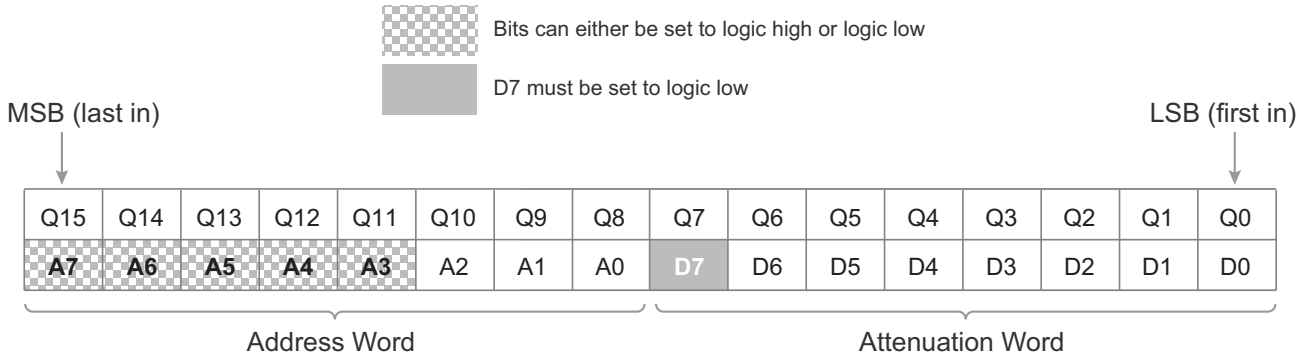
Address Word								Address Setting
A7 (MSB)	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	L	L	L	000
X	X	X	X	X	L	L	H	001
X	X	X	X	X	L	H	L	010
X	X	X	X	X	L	H	H	011
X	X	X	X	X	H	L	L	100
X	X	X	X	X	H	L	H	101
X	X	X	X	X	H	H	L	110
X	X	X	X	X	H	H	H	111

Table 8 • *Attenuation Word Truth Table*

Attenuation Word								Attenuation Setting RF1-RF2
D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Reference I.L.
L	L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	H	31.75 dB

Serial-Addressable Register Map

Figure 3 • *Serial-Addressable Register Map*



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.

For example, to program the 18.25 dB state at address 3:

$$4 \times 18.25 = 73$$
$$73 \rightarrow 01001001$$

Address Word: XXXXX011
Attenuation Word: 01001001
Serial Input: XXXXX01101001001

Programming Options

Parallel/Serial-Addressable Selection

Either a parallel or serial-addressable interface can be used to control the PE43670. The $\overline{P}$/S bit provides this selection, with $\overline{P}$/S=LOW selecting the parallel interface and $\overline{P}$/S=HIGH selecting the serial interface.

Parallel Mode Interface

The parallel interface consists of seven CMOS-compatible control lines that select the desired attenuation state, as shown in **Table 6**.

The parallel interface timing requirements are defined by **Figure 5** (Parallel Interface Timing Diagram), **Table 10** (Parallel Interface AC Characteristics), and switching speed (**Table 3**).

For *latched*-parallel programming the latch enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (**Figure 5**) to latch new attenuation state into device.

For *direct* parallel programming, the latch enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Serial-Addressable Interface

The serial-addressable interface is a 16-bit serial-in, parallel-out shift register buffered by a transparent latch. The 16-bits make up two words comprised of 8-bits each. The first word is the attenuation word, which controls the state of the DSA. The second word is the address word, which is compared to the static (or programmed) logical states of the A0, A1 and A2 digital inputs. If there is an address match, the DSA changes state; otherwise its current state will remain unchanged. **Figure 4** illustrates a example timing diagram for programming a state. It is recommended that all parallel control inputs be grounded when the DSA is used in serial mode.

The serial-addressable interface is controlled using three CMOS-compatible signals: serial-in (SI), clock (CLK), and latch enable (LE). The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first, beginning with the attenuation word.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. Address word and attenuation word truth tables are listed in **Table 7** and **Table 8**, respectively. A programming example of the serial-addressable register is illustrated in **Figure 3**. The serial-addressable timing diagram is illustrated in **Figure 4**.

Power-up Control Settings

The PE43670 will always initialize to the maximum attenuation setting (31.75 dB) on power-up for both the serial-addressable and latched-parallel modes of operation and will remain in this setting until the user latches in the next programming word. In direct-parallel mode, the DSA can be preset to any state within the 31.75 dB range by pre-setting the parallel control pins prior to power-up. In this mode, there is a 400-µs delay between the time the DSA is powered-up to the time the desired state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (31.75 dB) before defaulting to the user defined state. If the control pins are left floating in this mode during power-up, the device will default to the minimum attenuation setting (insertion loss state).

Dynamic operation between serial-addressable and parallel programming modes is possible.

If the DSA powers up in serial-addressable mode ($\overline{P}$/S = HIGH), all the parallel control inputs DI[6:0] must be set to logic low. Prior to toggling to parallel mode, the DSA must be programmed serially to ensure D[7] is set to logic low.

If the DSA powers up in either latched or direct-parallel mode, all parallel pins DI[6:0] must be set to logic low prior to toggling to serial-addressable mode ($\overline{P}$/S = HIGH), and held low until the DSA has been programmed serially to ensure bit D[7] is set to logic low.

The sequencing is only required once on power-up. Once completed, the DSA may be toggled between serial-addressable and parallel programming modes at will.

Figure 4 • *Serial-Addressable Timing Diagram*

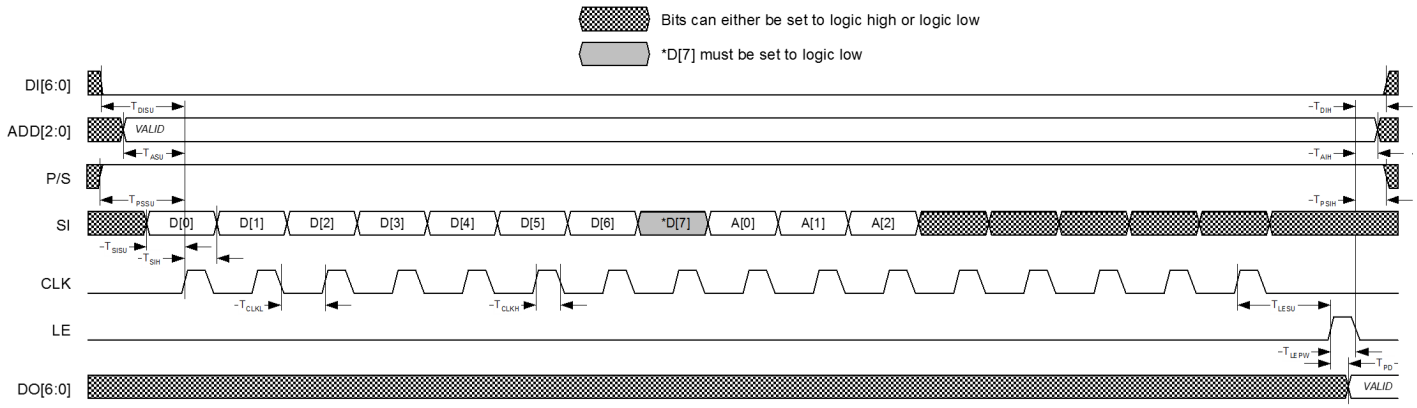


Figure 5 • *Latched-Parallel/Direct-Parallel Timing Diagram*

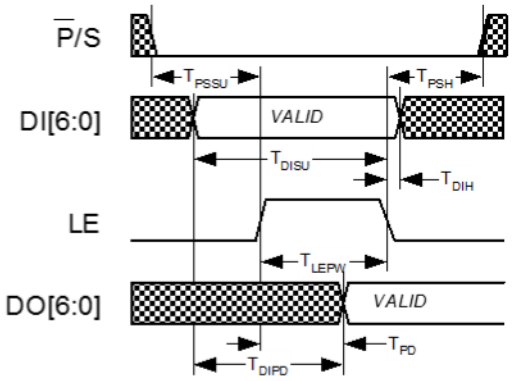


Table 9 • *Serial-Addressable Interface AC Characteristics*

Symbol	Parameter	Min	Max	Unit
F_{CLK}	Serial clock frequency	-	10	MHz
T_{CLKH}	Serial clock HIGH time	30	-	ns
T_{CLKL}	Serial clock LOW time	30	-	ns
T_{LESU}	Last serial clock rising edge setup time to Latch Enable rising edge	10	-	ns
T_{LEPW}	Latch Enable minimum pulse width	30	-	ns
T_{SISU}	Serial data setup time	10	-	ns
T_{SIH}	Serial data hold time	10	-	ns
T_{DISU}	Parallel data setup time	100	-	ns
T_{DIH}	Parallel data hold time	100	-	ns

Table 9 • *Serial-Addressable Interface AC Characteristics*

Symbol	Parameter	Min	Max	Unit
T_{ASU}	Address setup time	100	-	ns
T_{AH}	Address hold time	100	-	ns
T_{PSSU}	Parallel/serial setup time	100	-	ns
T_{PSH}	Parallel/serial hold time	100	-	ns
T_{PD}	Digital register delay (internal)	-	10	ns

Notes:
1. V_{DD} = 3.3V or 5.0V, –40 °C < T_A < +85 °C, unless otherwise specified.

Table 10 • *Parallel and Direct Interface AC Characteristics*

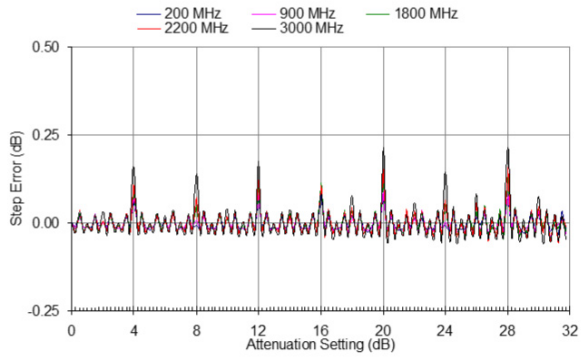
Symbol	Parameter	Min	Max	Unit
T_{LEPW}	Latch Enable minimum pulse width	30	-	ns
T_{DISU}	Parallel data setup time	100	-	ns
T_{DIH}	Parallel data hold time	100	-	ns
T_{PSSU}	Parallel/serial setup time	100	-	ns
T_{PSH}	Parallel/serial hold time	100	-	ns
T_{PD}	Digital register delay (internal)	-	10	ns
T_{DIPD}	Digital register delay (internal, direct mode only)	-	5	ns

Notes:
V_{DD} = 3.3V or 5.0V, –40 °C < T_A < +85 °C, unless otherwise specified.

Typical Performance Data

Figure 6 through **Figure 20** show the typical performance data at T = +25C, unless otherwise specified.

Figure 6 • *0.25 dB Step Error vs. Frequency**



*Monotonicity is held so long as Step-Error does not cross below -0.25

Figure 7 • *0.25 dB Attenuation vs. Attenuation State*

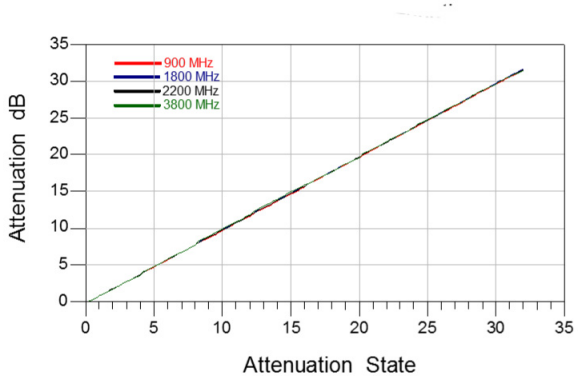


Figure 8 • *0.25 dB Major State Bit Error*

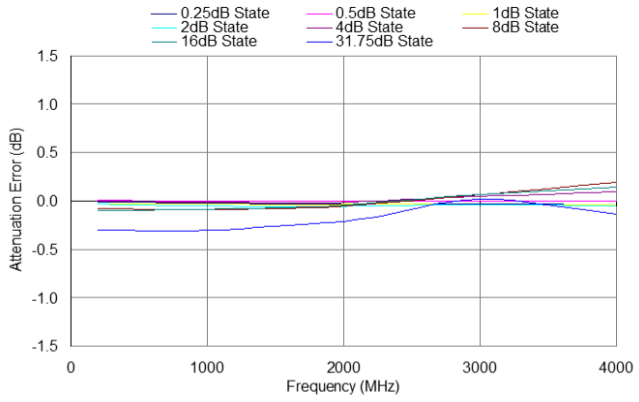


Figure 9 • *0.25 dB Attenuation Error vs. Frequency*

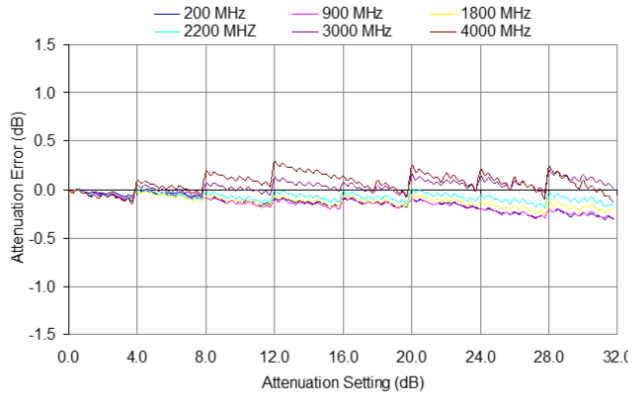


Figure 10 • *Insertion Loss vs. Temperature*

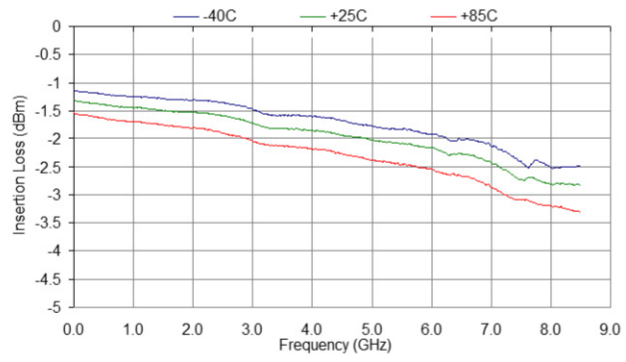


Figure 11 • *Input Return Loss vs. Attenuation: T = +25C*

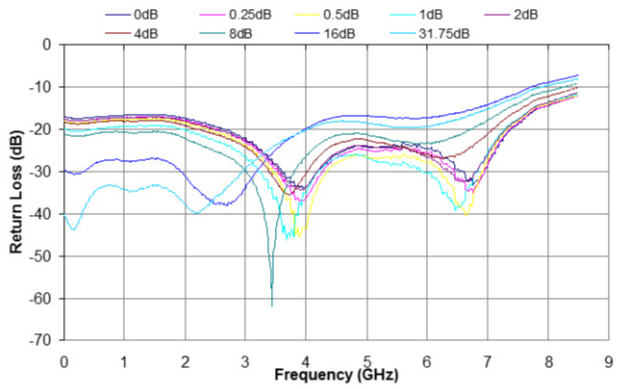


Figure 12 • *Output Return Loss vs. Attenuation: T = +25C*

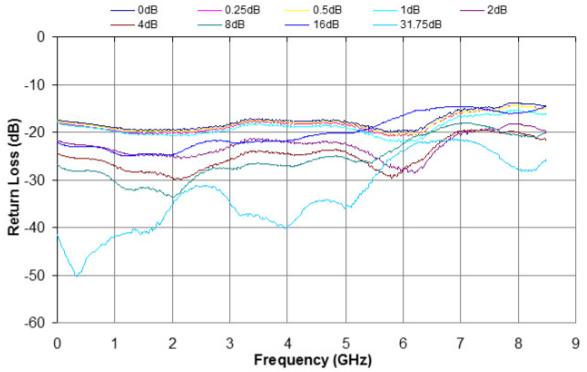


Figure 13 • *Input Return Loss vs. Temperature: 16 dB State*

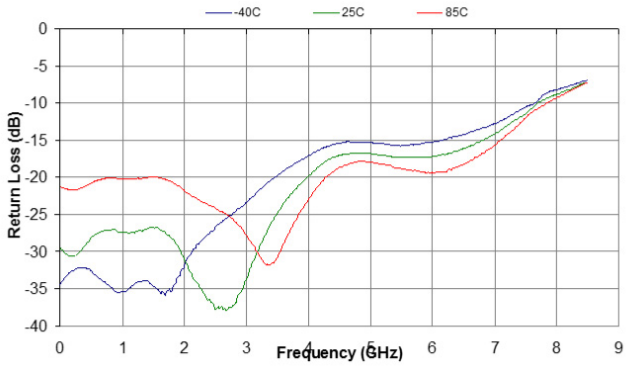


Figure 14 • *Output Return Loss vs. Temperature: 16 dB State*

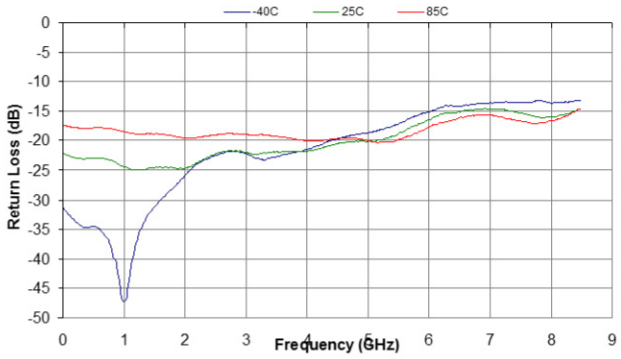


Figure 15 • *Relative Phase vs. Frequency*

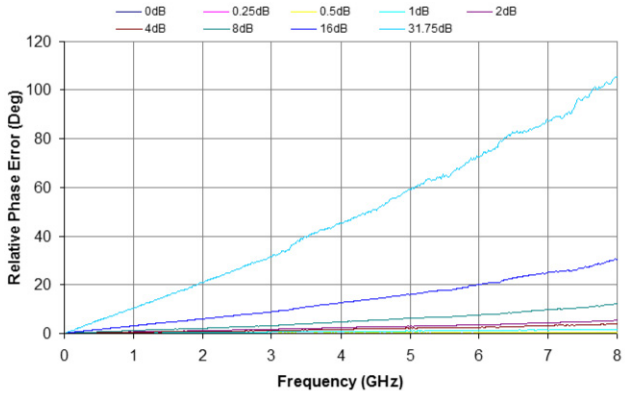


Figure 16 • *Relative Phase vs. Temperature: 31.75 dB State*

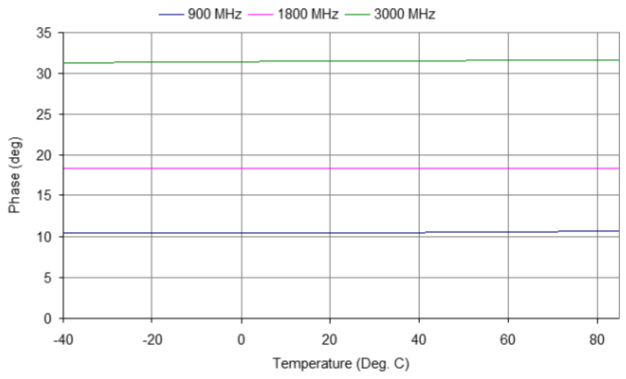


Figure 17 • *Attenuation Error vs. Attenuation*

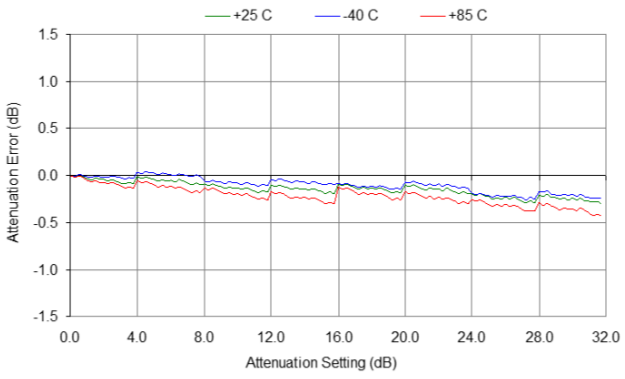


Figure 18 • *Attenuation Error vs. Attenuation Setting: 1800 MHz*

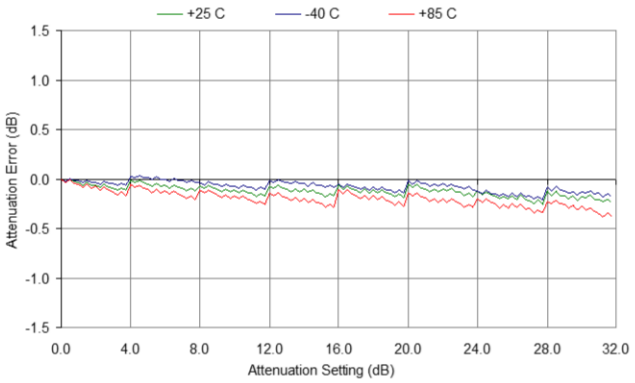


Figure 19 • *Attenuation Error vs. Attenuation Setting: 3000 MHz*

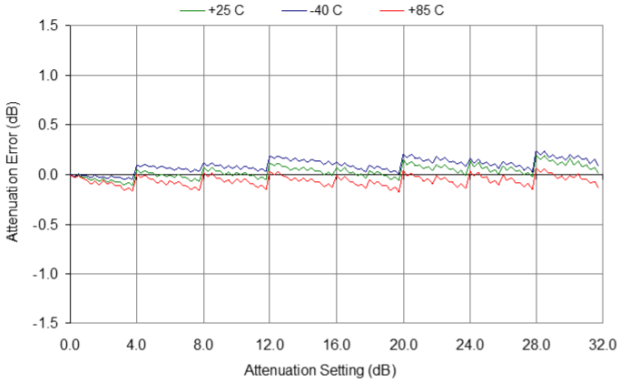
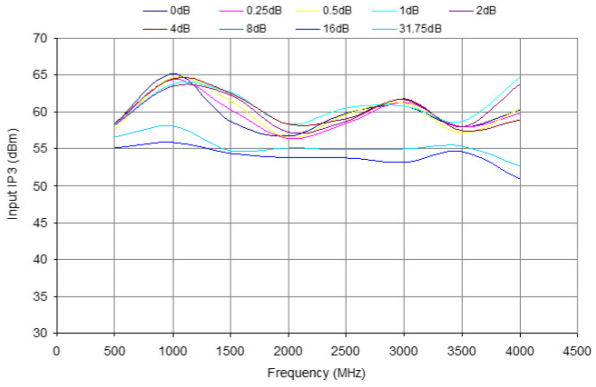


Figure 20 • *Input IP3 vs. Frequency*



Evaluation Kit

The Digital Attenuator Evaluation Kit board was designed to ease customer evaluation of the PE43670 DSA.

Direct-Parallel Programming Procedure

For automated direct-parallel programming, connect the test harness provided with the EVK from the parallel port of the PC to the J1 and serial header pin and set the D0-D6 SP3T switches to the 'MIDDLE' toggle position. Position the parallel/serial ($\overline{P}$/S) select switch to the parallel (or left) position. The evaluation software is written to operate the DSA in either parallel or serial-addressable mode. Ensure that the software is set to program in direct-parallel mode. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

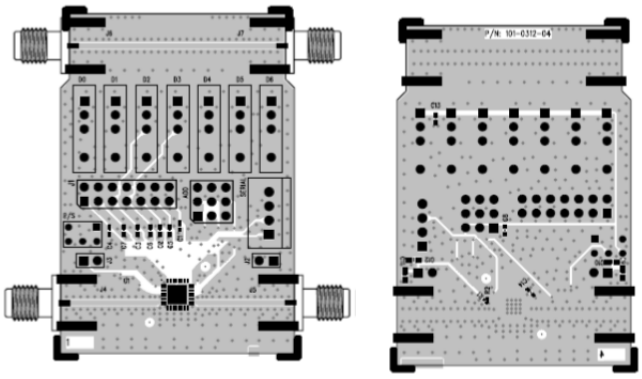
For manual direct-parallel programming, disconnect the test harness provided with the EVK from the J1 and serial header pins. Position the parallel/serial ($\overline{P}$/S) select switch to the parallel (or left) position. The LE pin on the serial header must be tied to VDD. Switches D0-D6 are SP3T switches which enable the user to manually program the parallel bits. When any input D0-D6 is toggled 'UP', logic high is presented to the parallel input. When toggled 'DOWN', logic low is presented to the parallel input. Setting D0-D6 to the 'MIDDLE' toggle position presents an OPEN, which forces an on-chip logic low. **Table 6** depicts the parallel programming truth table and **Figure 5** illustrates the parallel programming timing diagram.

Latched-Parallel Programming Procedure

For automated latched-parallel programming, the procedure is identical to the direct-parallel method. The user only must ensure that Latched-parallel is selected in the software.

For manual latched-parallel programming, the procedure is identical to direct-parallel except now the LE pin on the serial header must be logic low as the parallel bits are applied. The user must then pulse LE from 0V to V_{DD} and back to 0V to latch the programming word into the DSA. LE must be logic low prior to programming the next word.

Figure 21 • ***Evaluation Kit Layout for PE43670***



Serial-Addressable Programming Procedure

Position the parallel/serial ($\overline{P}$/S) select switch to the serial (or right) position. Prior to programming, the user must define an address setting using the ADD header pin. Jump the middle pins on the ADD header A0-A2 (or lower) row of pins to set logic high, or jump the middle pins to the upper row of pins to set logic low. If the ADD pins are left open, then 000 become the default address. The evaluation software is written to operate the DSA in either parallel or serial-addressable mode. Ensure that the software is set to program in serial-addressable mode. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

Pin Information

This section provides pinout information for the PE43670. Figure 22 shows the pin map of this device for the available package. Table 11 provides a description for each pin.

Figure 22 • *Pin Configuration (Top View)*

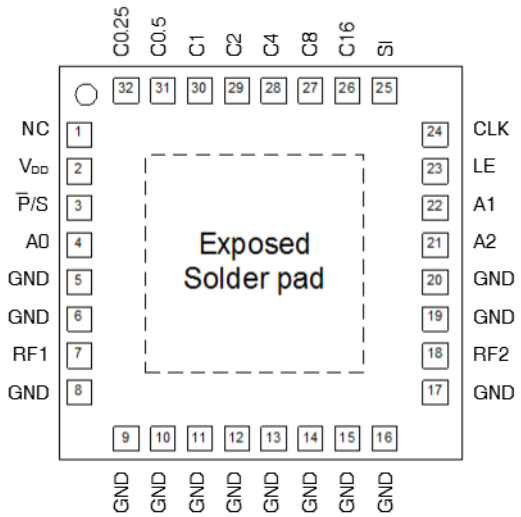


Table 11 • *Pin Descriptions for PE43670*

Pin No.	Pin Name	Description
1	N/C	No connect
2	V_{DD}	Power supply pin
3	$\overline{P}$/S	Serial/parallel mode select
4	A0	Address bit A0 (LSB)
5, 6, 8-17, 19, 20	GND	Ground
7	RF1	RF1 port
18	RF2	RF2 port
21	A2	Address bit A2
22	A1	Address bit A1
23	LE	Latch Enable input
24	CLK	Serial interface clock input
25	SI	Serial Interface input
26	C16	Attenuation control bit, 16 dB
27	C8	Attenuation control bit, 8dB
28	C4	Attenuation control bit, 4 dB
29	C2	Attenuation control bit, 2 dB
30	C1	Attenuation control bit, 1 dB
31	C0.5	Attenuation control bit, 0.5 dB
32	C0.25	Attenuation control bit, 0.25 dB (LSB)
Paddle	GND	Ground for proper operation
Note: Ground C0.25, C0.5, C1, C2, C4, C8, C16 if not in use.		

Packaging Information

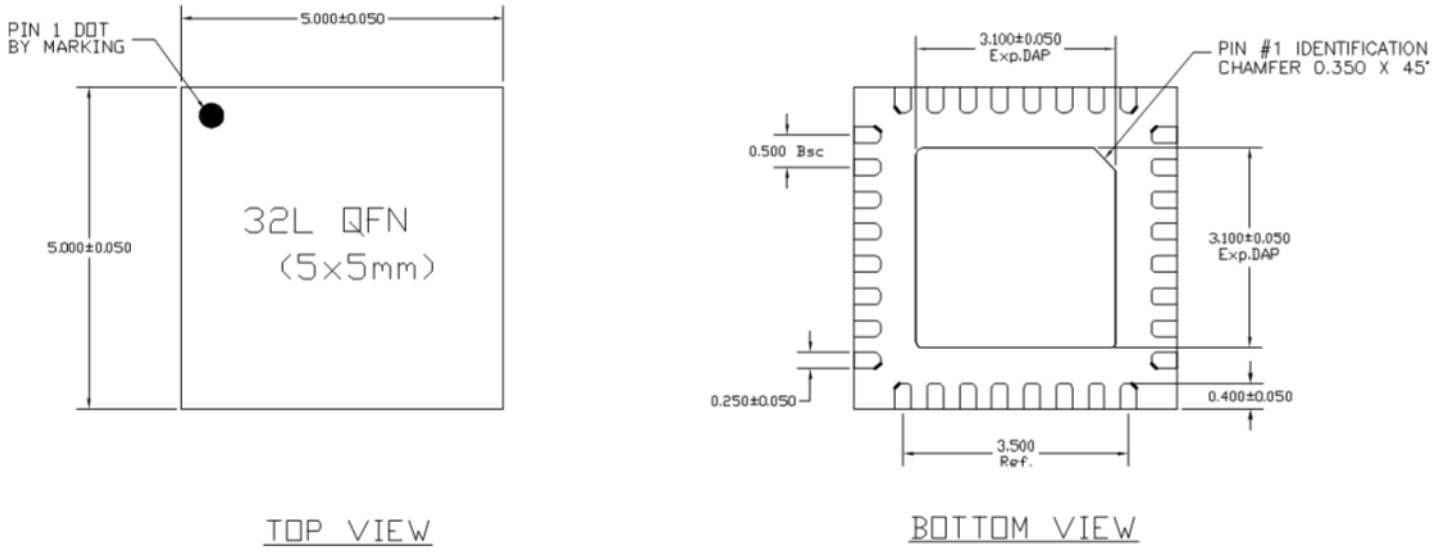
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

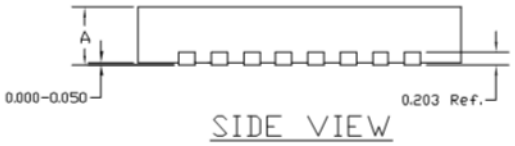
The moisture sensitivity level rating for the PE43670 in the 5x5 QFN package is MSL 1.

Package Drawing

Figure 23 • *Package Mechanical Drawing for 5x5 QFN*



		QFN 5x5 mm
A	MAX	0.900
	NOM	0.850
	MIN	0.800



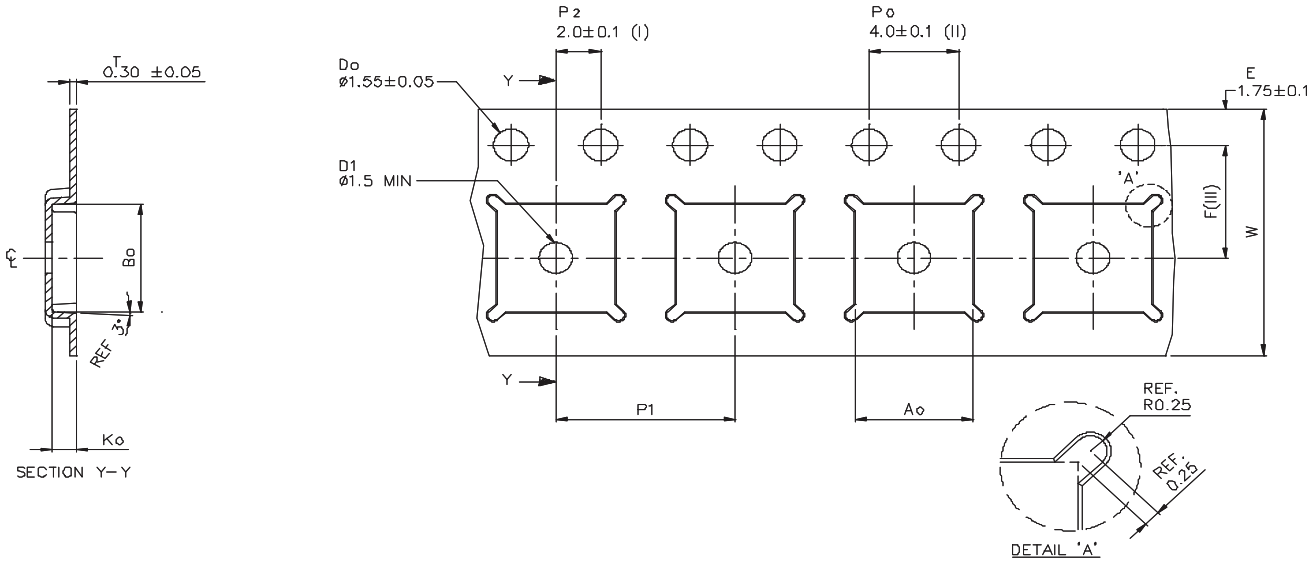
Top-Marking Specification

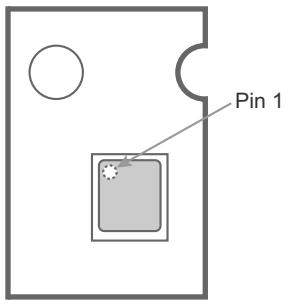
Figure 24 • *Package Marking Specifications for PE43670*

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum seven characters)

Tape and Reel Specification

Figure 25 • *Tape and Reel Specifications for 5x5 QFN*





Device Orientation in Tape

Ao	5.25 +/– 0.1
Bo	5.25 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.